FIRENZE2-R

CPU : Intel Yonah/Merom (533/667MHz)
Chip Set : RS600ME & SB600
Remarks : Mobility Platform

Model Name : FIRENZE II R
PBA Name : MAIN
PCB Code : TPT : BA41-00714A
GCE : BA41-00715A
Dev. Step : MP (6-Layer)
Revision : 1.0
T.R. Date : 2006.01.11

DRAW	CHECK	APPROVAL
TERMI	HJ KIM	SJ PARK

■ ***Owner : SEC Mobile R & D*** ***Signature :*** ***X***

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R COVER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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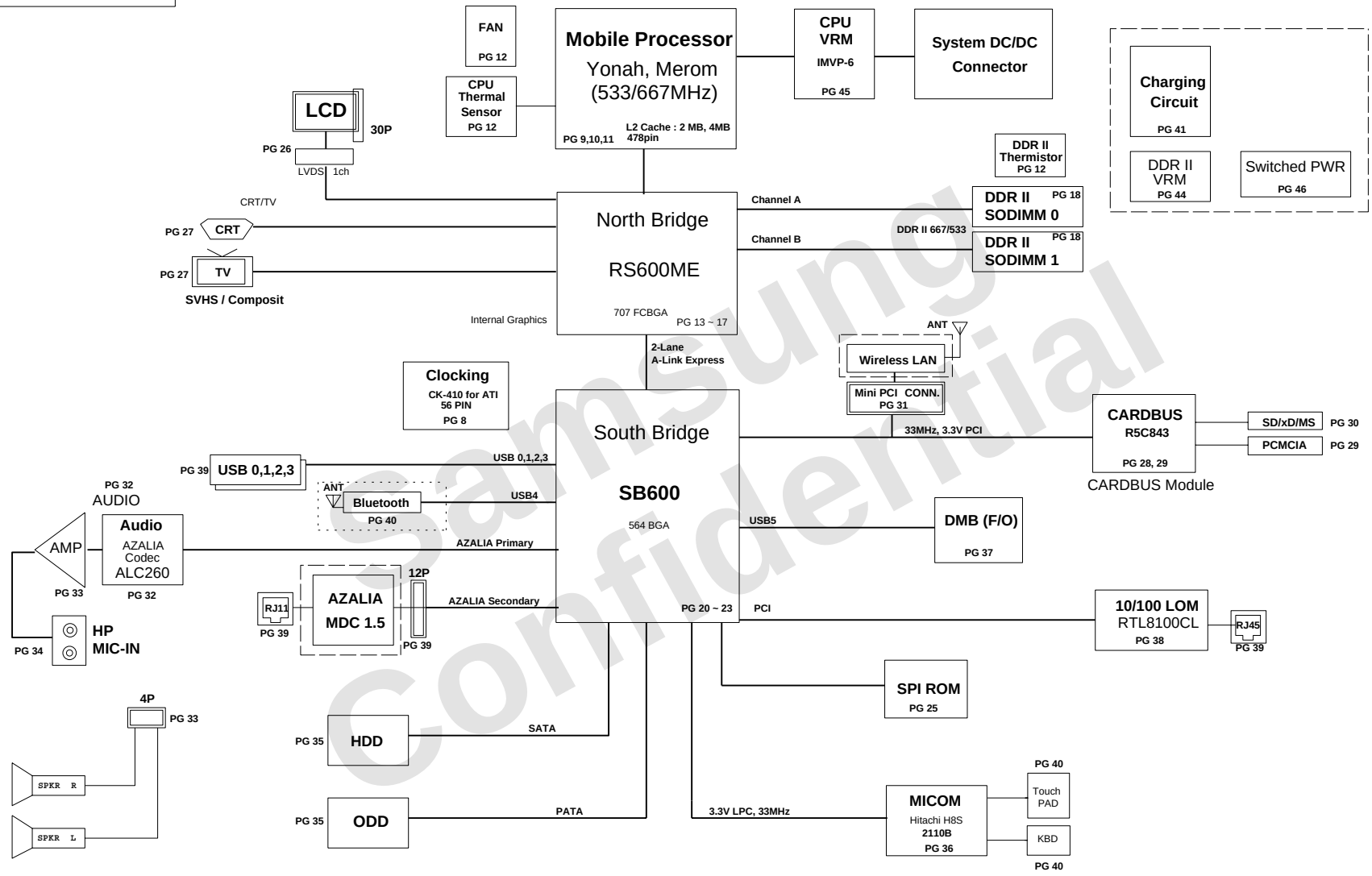

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN OPERATION BLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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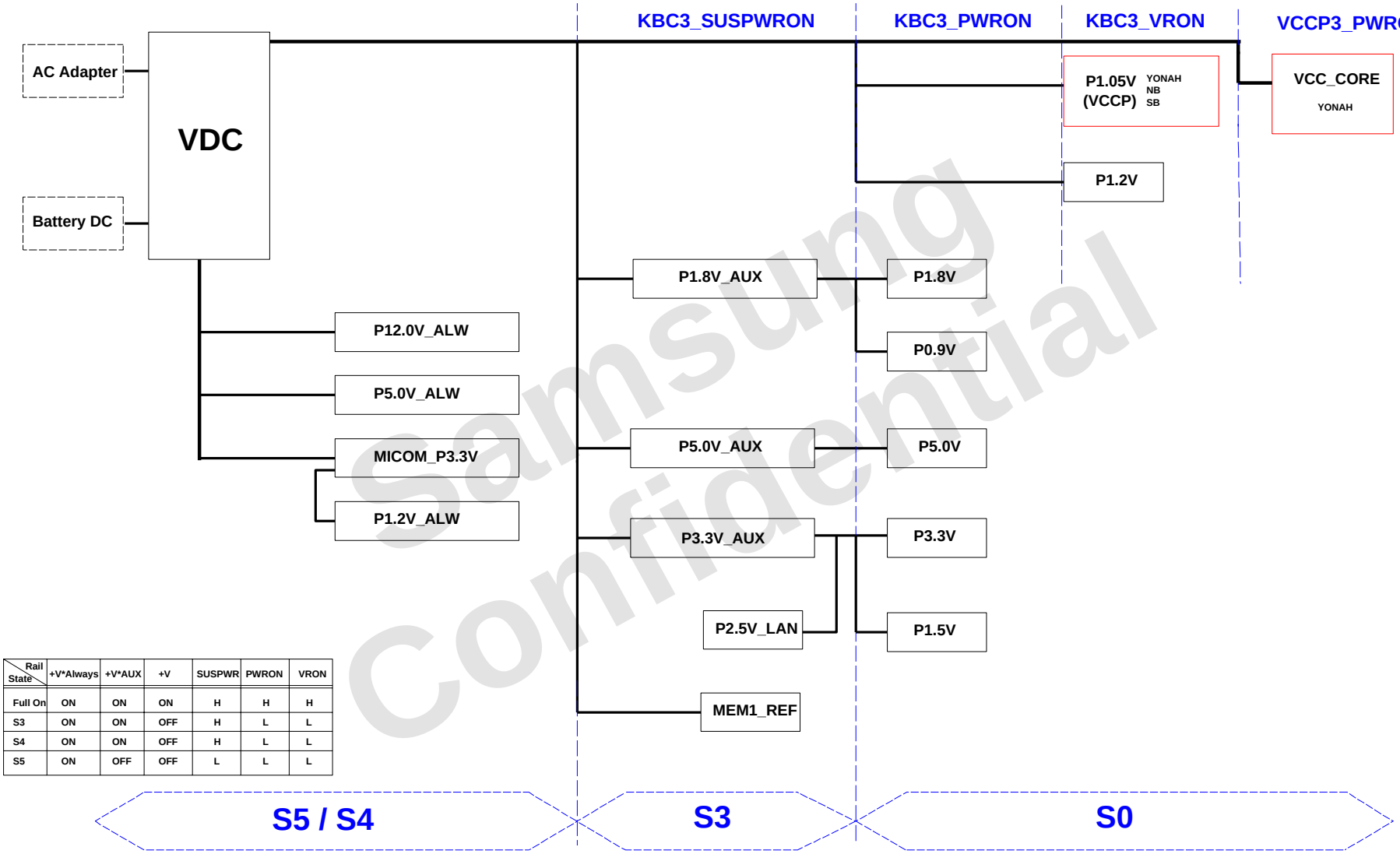
Power Diagram



Rail / State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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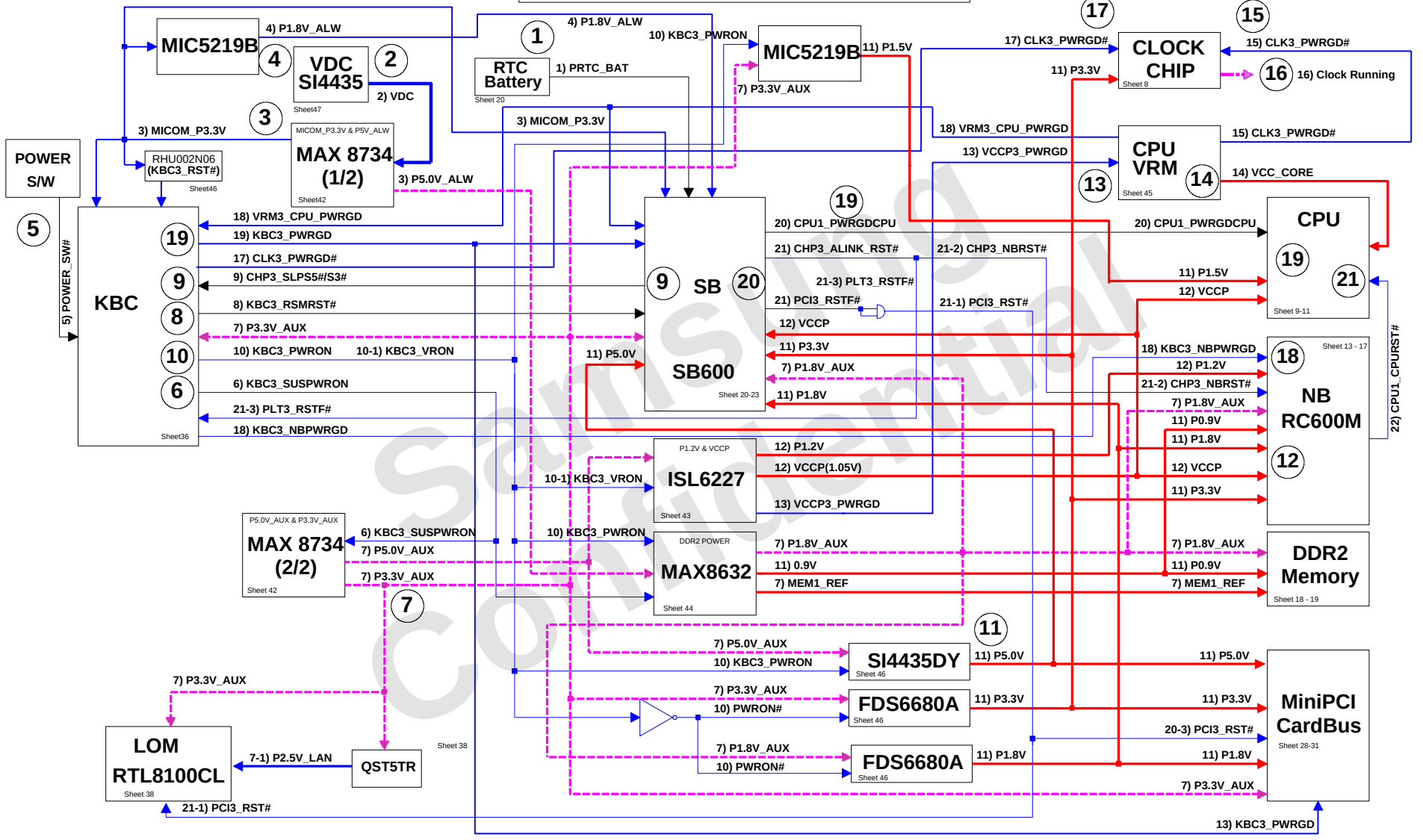
POWER SEQUENCE Rev. 0.1



DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0	POWER SEQUENCE	PART NO.: BA41-00714A
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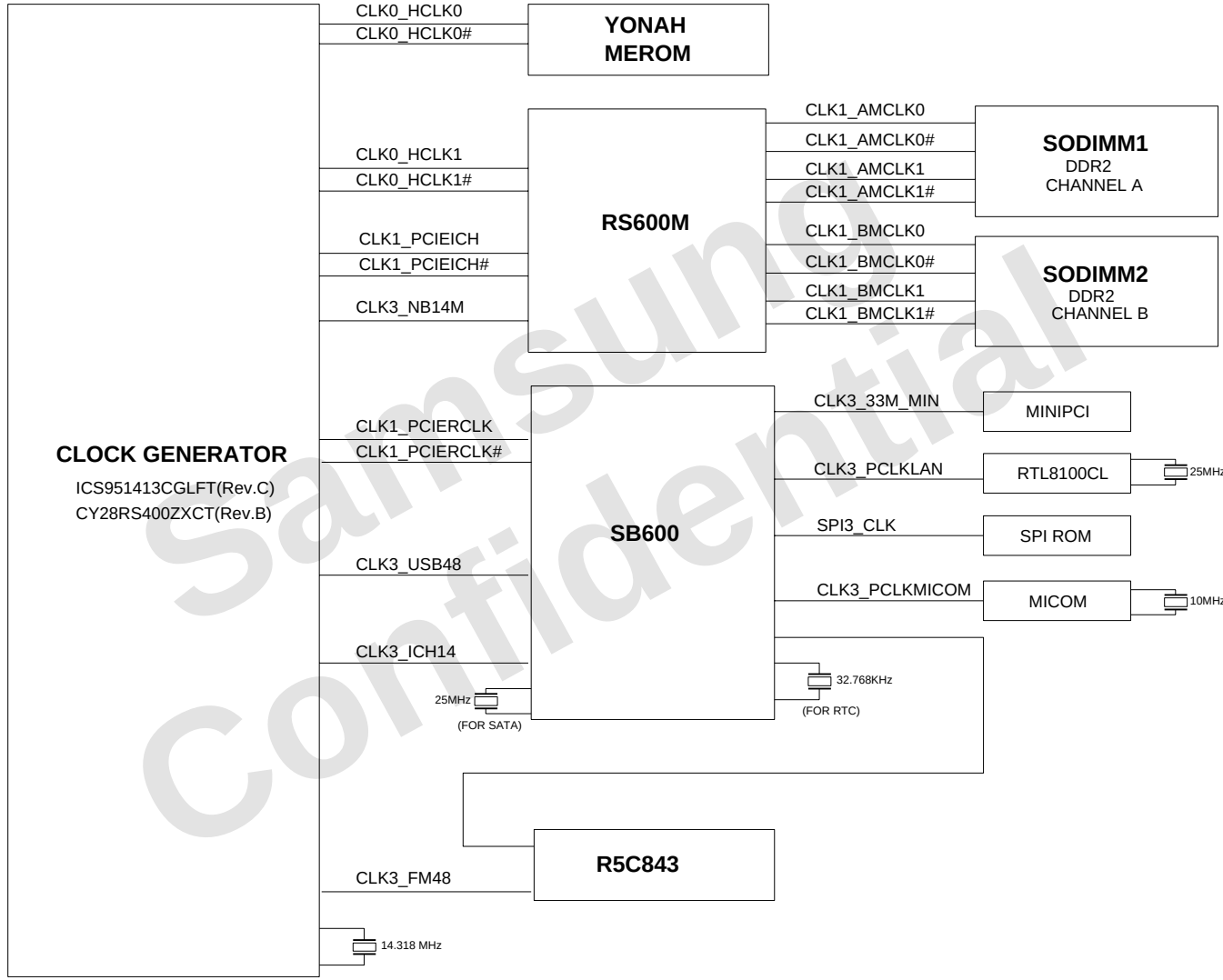

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R CLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	A, B, C
LAN	AD21	1	D
MINIPCI	AD23	2	A,B
USB	AD30(internal)	-	-
			-
			-
Hub to PCI	AD31(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	--
Internal MAC	AD31(internal)	-	-
AC Link	-	-	-

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for YONAH (0~1.5V)
VCCP	YONAH Processor System Bus(PSB) Termination (1.05V)
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P1.8V_ALWS	1.8V power rail (Always On)
P2.5V_LAN	2.5V power rail (off in S4-S5)
MICOM_P3.3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P5.0V_ALWS	5.0V power rail (Always On)
P12V_ALWS	12V power rail (Always On)

I2C / SMB Address

Devices	Address	Hex	Bus
SB600	Master	-	SMBUS Master
SODIMM0	1010 0100	A4h	-
SODIMM1	1010 0110	A6h	-
CK-410 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0, 1	SYSTEM PORT A
2, 3	SYSTEM PORT B
4	BLUETOOTH
5	DMB

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB600	Real Time Clock
Crystal	25MHz	SB600	SATA
Crystal	10MHz	MICOM	H8S-2110B
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	25MHz	LAN	LOM

CPU Core Voltage Table

IMVP-6

Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 **1** **1**	1.4125 V	0 1 0 1 1 **1** **1**	0.9125 V	1 0 1 1 0 **0** 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 **1**	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 **1** 0 1 **1** **1**	1.2125 V	0 1 **1** 1 1 **1** **1**	0.7125 V	1 1 **0** 1 0 0 **0**	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 **1** 0 0 **1** **1** 1	1.0125 V	1 **0** 0 1 **1** **1** 1	0.5125 V	1 **1** 1 1 0 **0** 0	0.0000 V
		1 **0** 1 0 **0** **0** 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

*"1111111" : 0V power good asserted.

Active	
DPRSLPVR	0
DPRSTP*	1
PSI2*	0 or 1

Deeper Slp	
DPRSLPVR	1
DPRSTP*	0
PSI2*	0 or 1

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other criticial subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.

CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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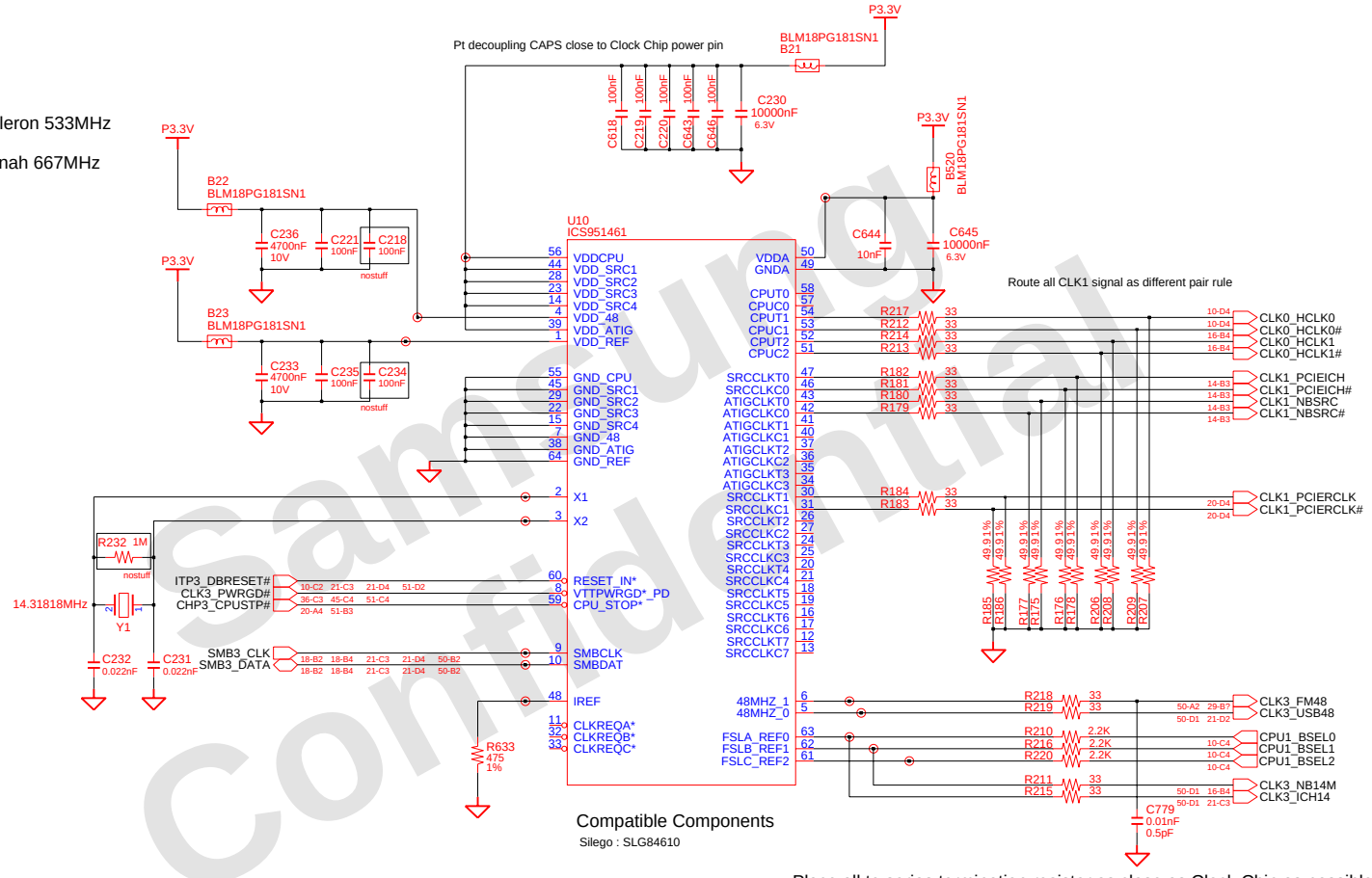
CPU FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK	
0	0	0	266 MHz	
0	0	1	333 MHz	
0	1	0	200 MHz	
0	1	1	400 MHz	
1	0	0	133 MHz	Celeron 533MHz
1	0	1	100 MHz	
1	1	0	166 MHz	Yonah 667MHz
1	1	1	RSVD	



FSA, FSB, FSC of Clock chip are low thershold inputs
Vih_fs_min = 0.7V
Vil_fs_max - 0.35V

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
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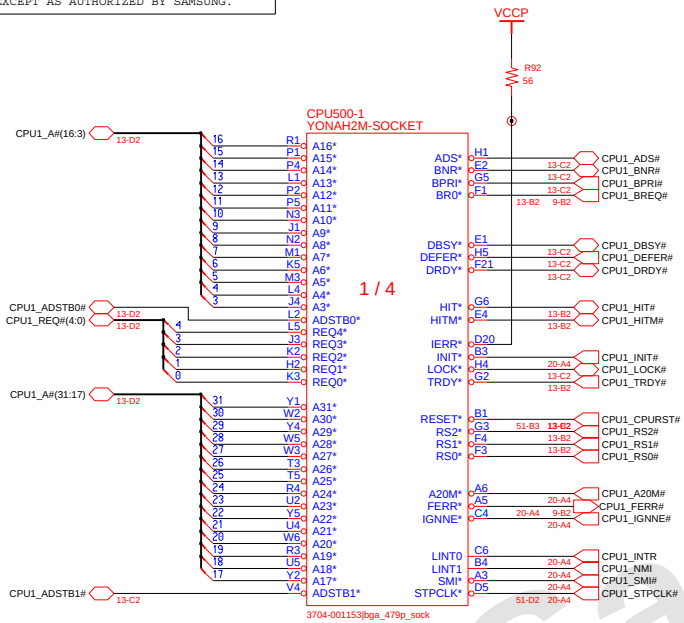
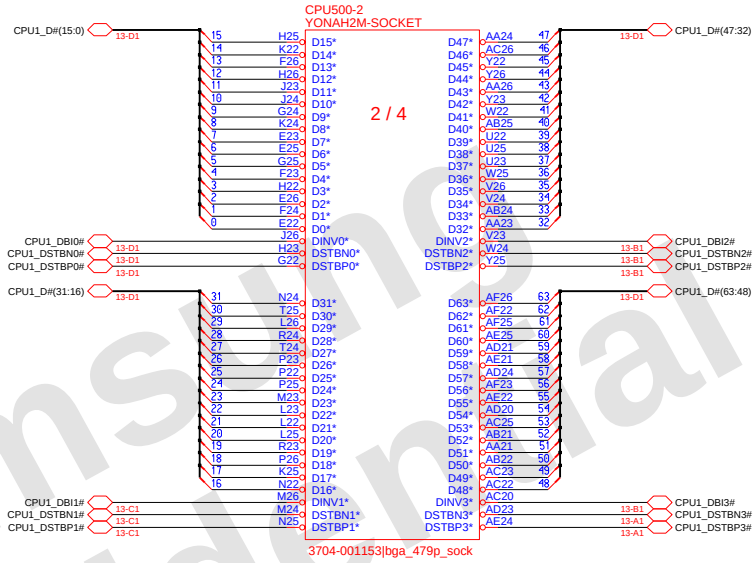




**NOTE

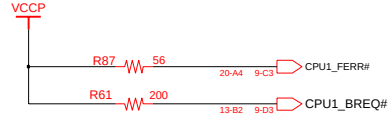
RHE SUPPORTER

MT5 RMNT-38-70-1P

MT9 RMNT-38-70-1P

MT6 RMNT-38-70-1P

MT8 RMNT-38-70-1P



DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN YONAH CPU (1/3)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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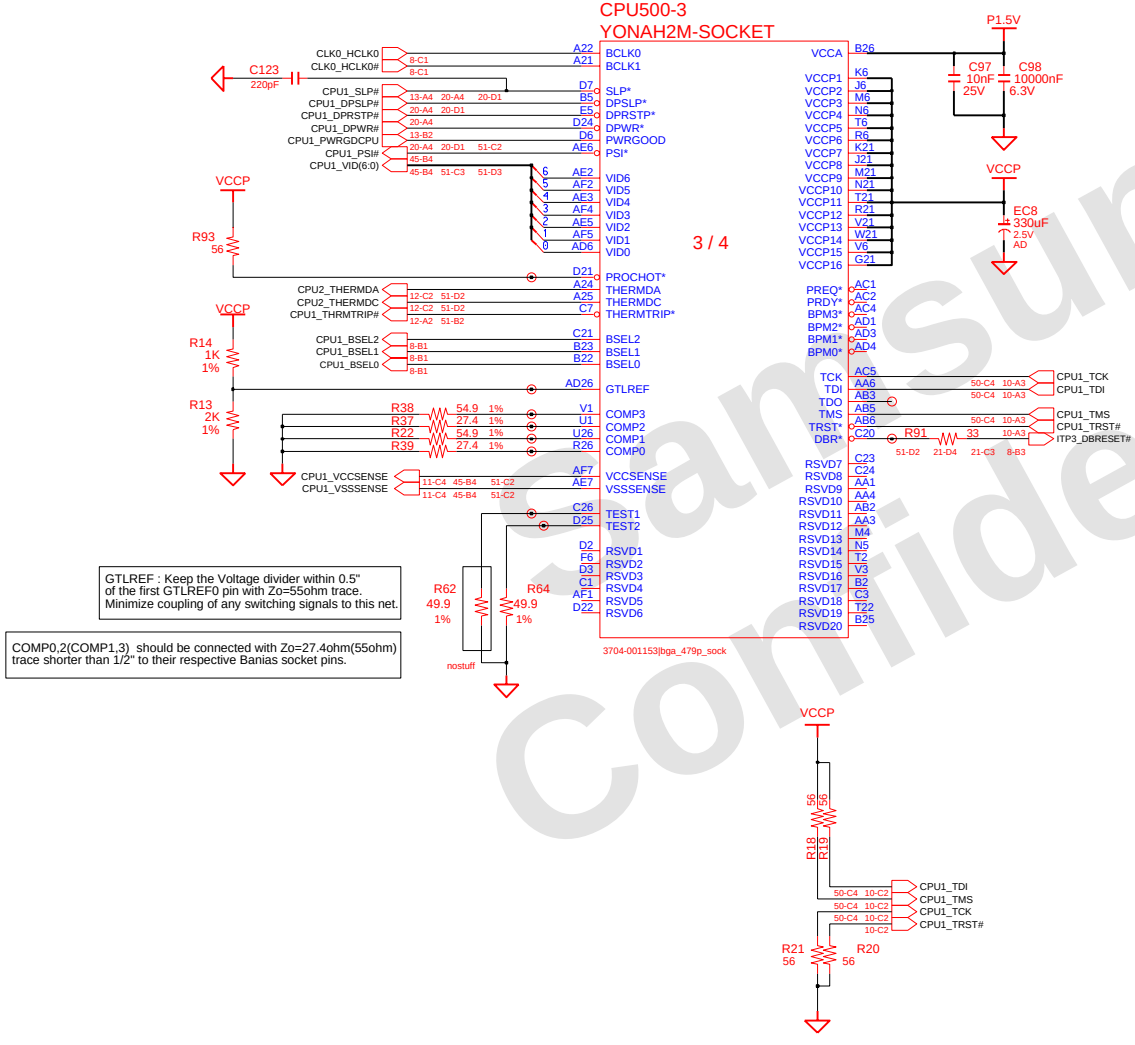


GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

CPU Core Voltage Table

IMVP-6

Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 0 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 0 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 0 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 0 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 0 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 0 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 0 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 0 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 0 1 1 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 0 1 1 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 0 1 1 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 0 1 1 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 0 1 1 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 0 1 1 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 0 1 1 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 0 1 1 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 0 1 1 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 0 1 1 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 0 1 1 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 0 1 1 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 0 1 1 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 0 1 1 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 0 1 1 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 0 1 1 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 0 1 0 0 0	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 0 1 0 0 1	0.0000 V
				1 1 1 0 1 0 1 0	0.0000 V
				1 1 1 0 1 0 1 1	0.0000 V
				1 1 1 0 1 1 0 0	0.0000 V
				1 1 1 0 1 1 0 1	0.0000 V
				1 1 1 0 1 1 1 0	0.0000 V
				1 1 1 0 1 1 1 1	0.0000 V

Active

DPRSLPVR	0
DPRSTP*	1
PSI2*	0 or 1

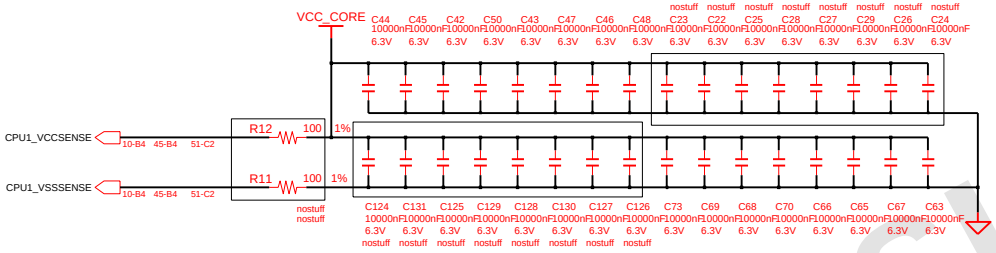
Deeper Slp

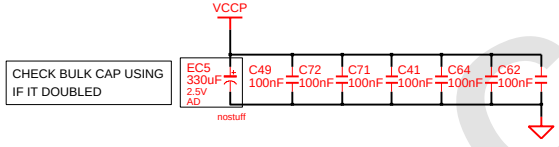
DPRSLPVR	1
DPRSTP*	0
PSI2*	0 or 1

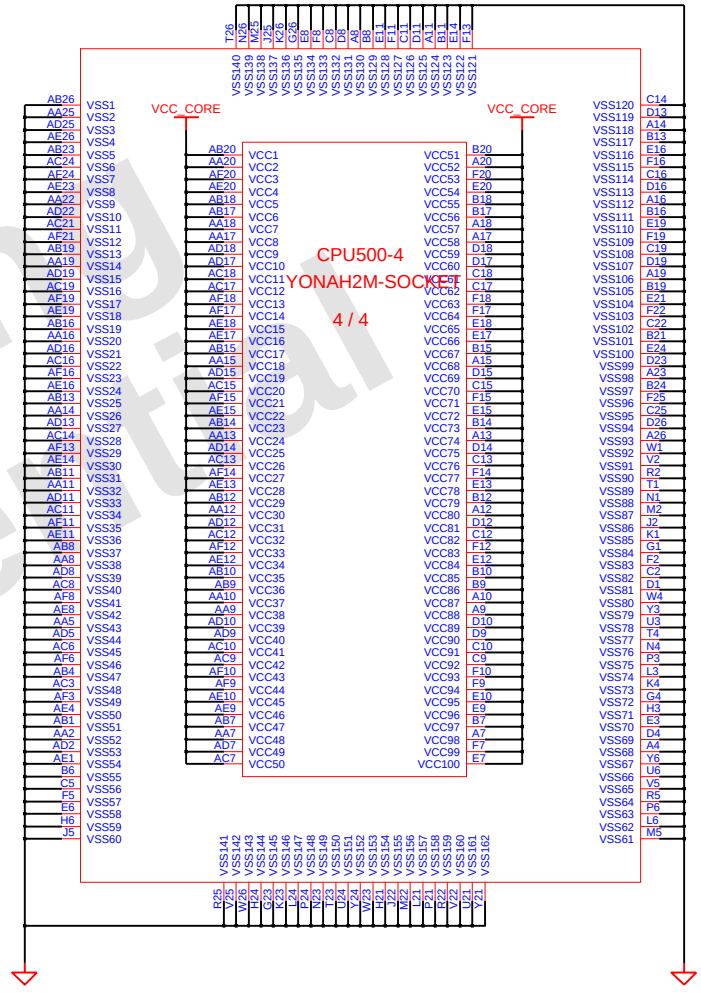
*"1111111" : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN YONAH CPU(2/3)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 10 OF 52	





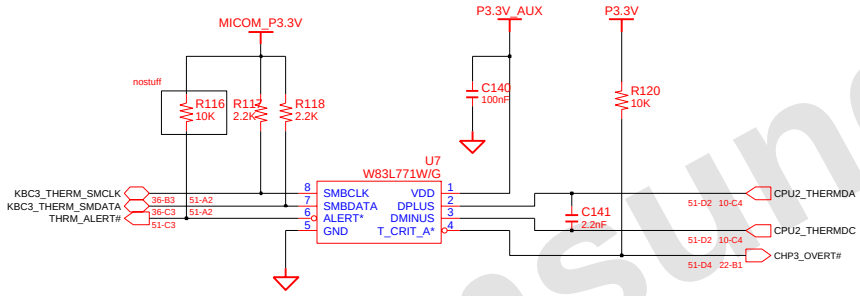


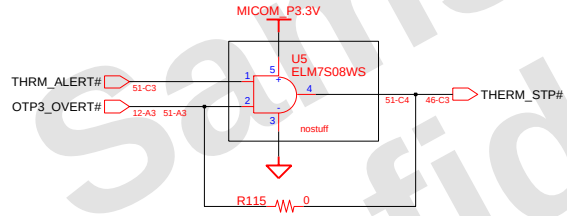
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN YONAH CPU(3/3)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 11 OF 52	

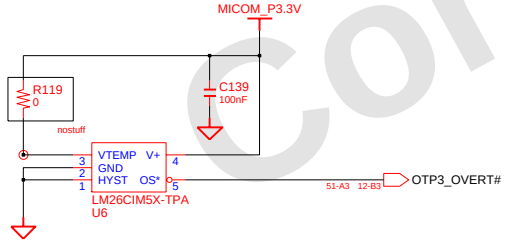
Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

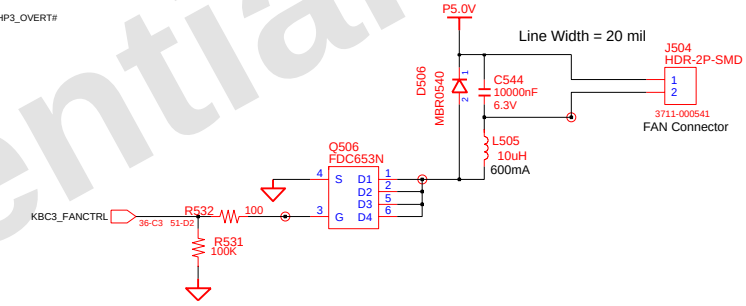
CPU Thermal Sensor

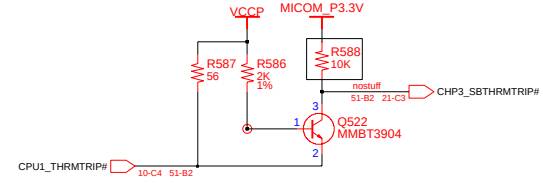




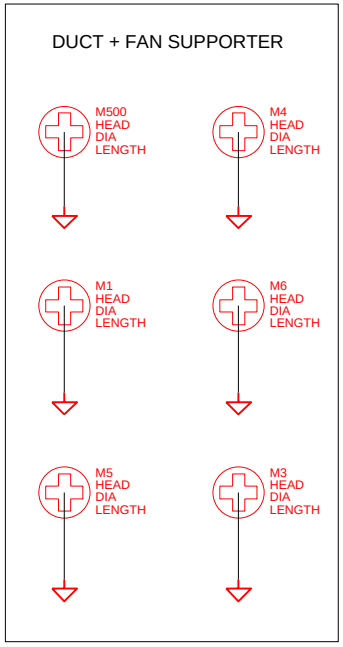


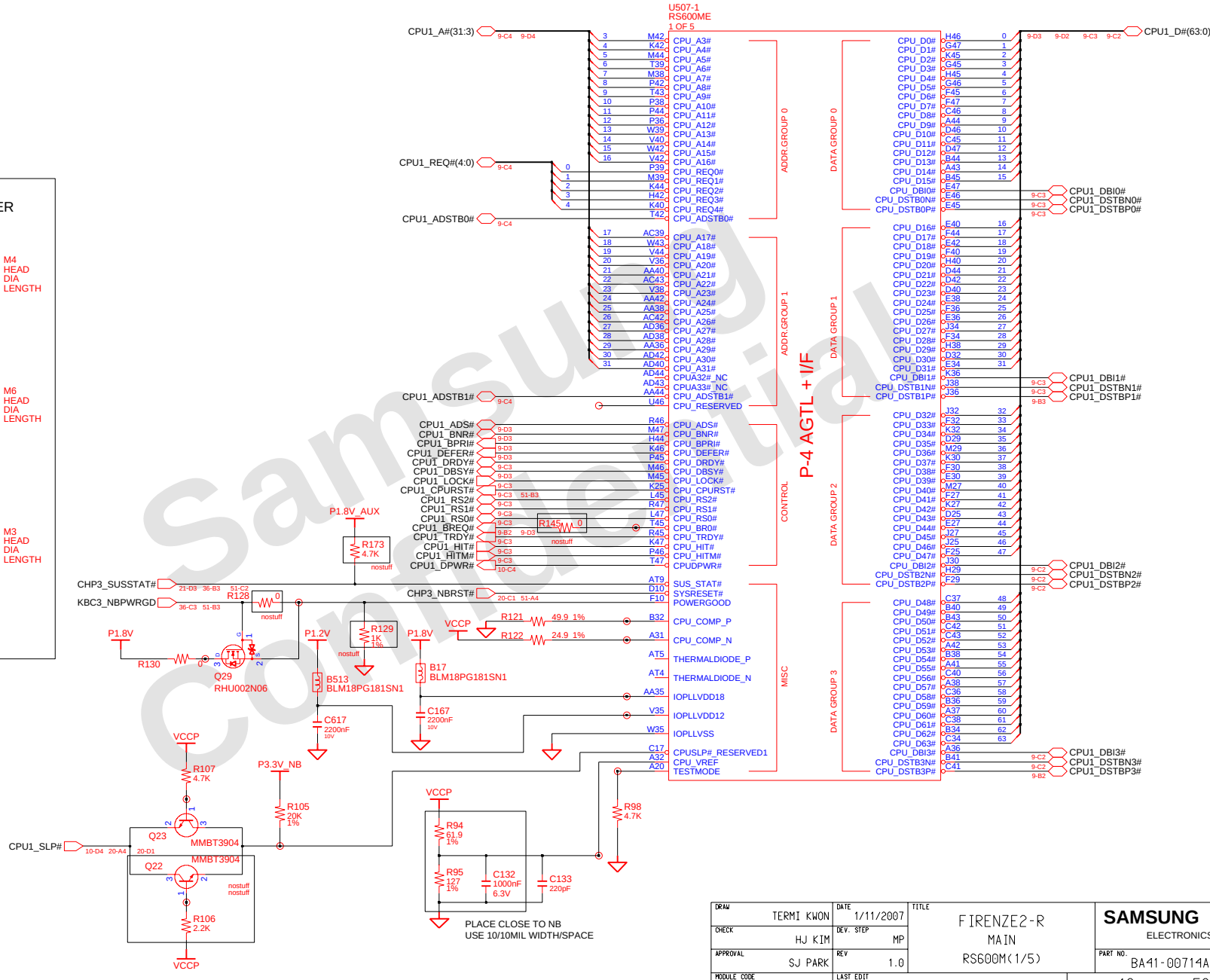
FAN Control Logic



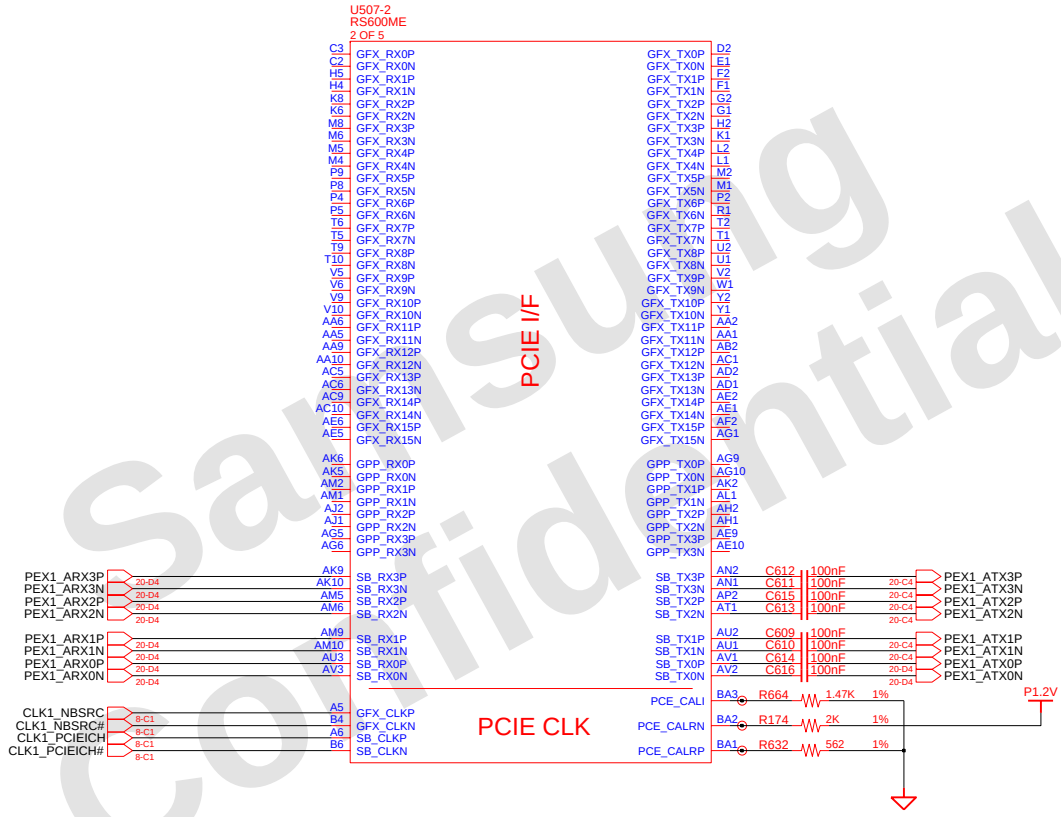


DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN THERMAL SENSOR/FAN CONTRL	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 12 OF 52	

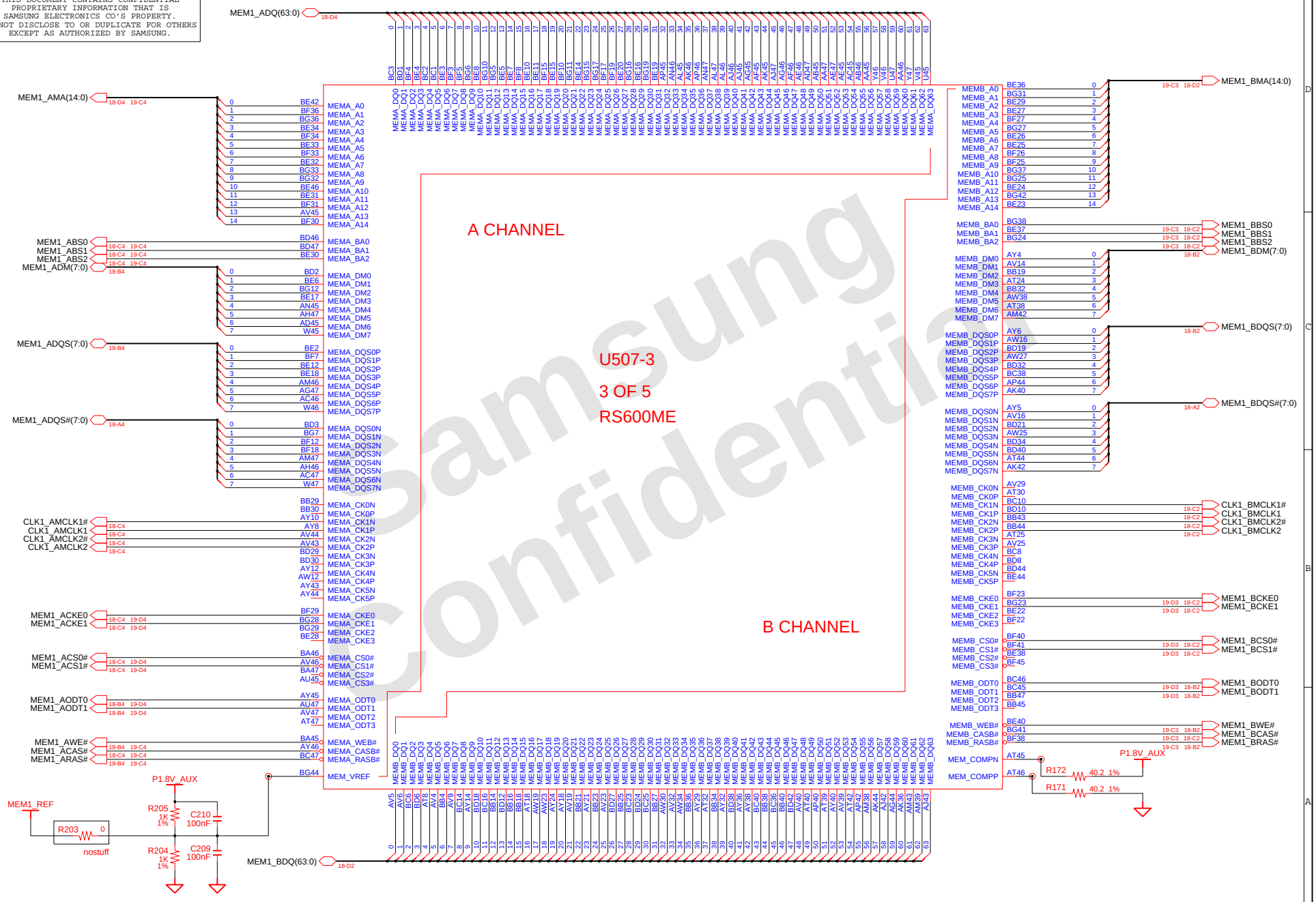




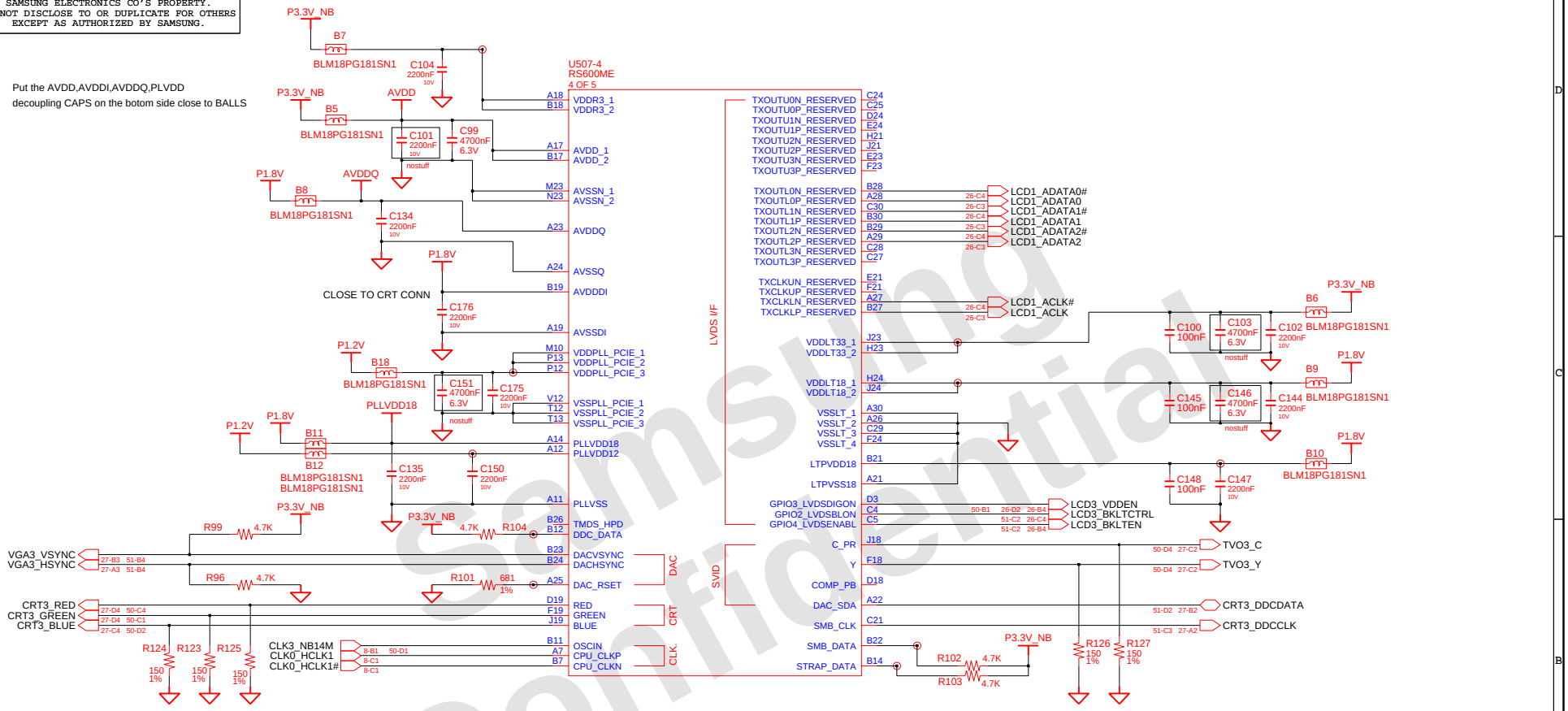
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN RS600M(1/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO. BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 13 OF 52	

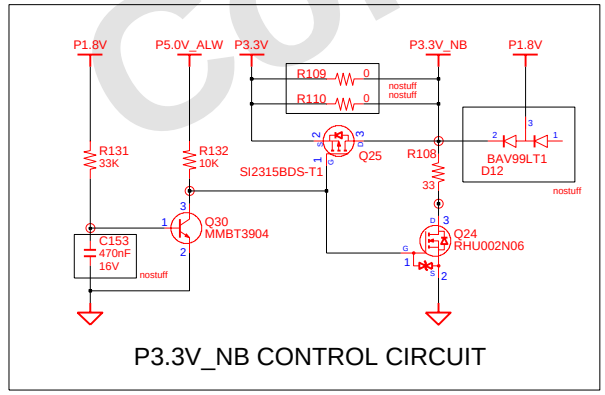


DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN RS600M(2/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 14 OF 52	



Put the AVDD,AVDDI,AVDDQ,PLVDD decoupling CAPS on the botom side close to BALLS



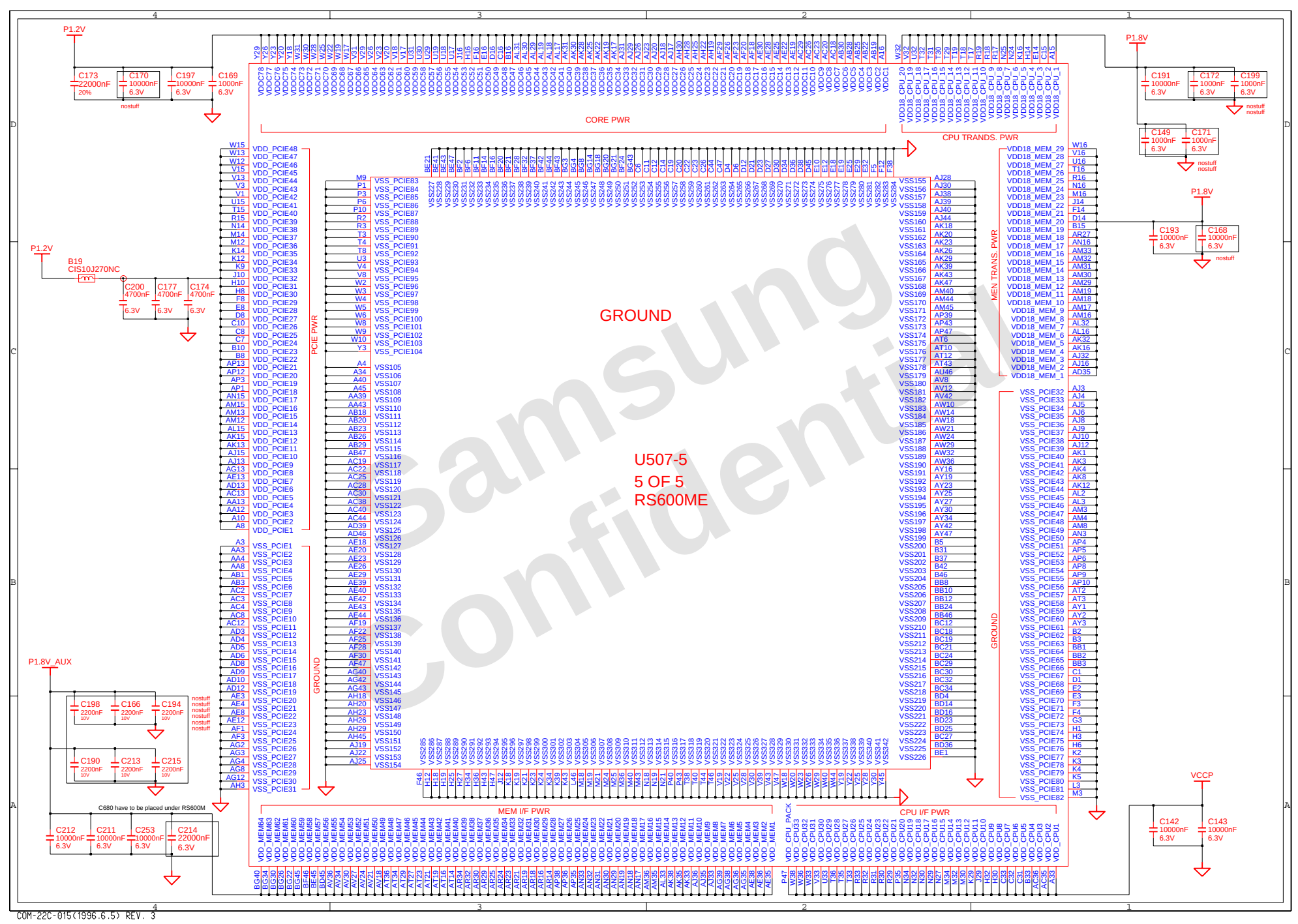


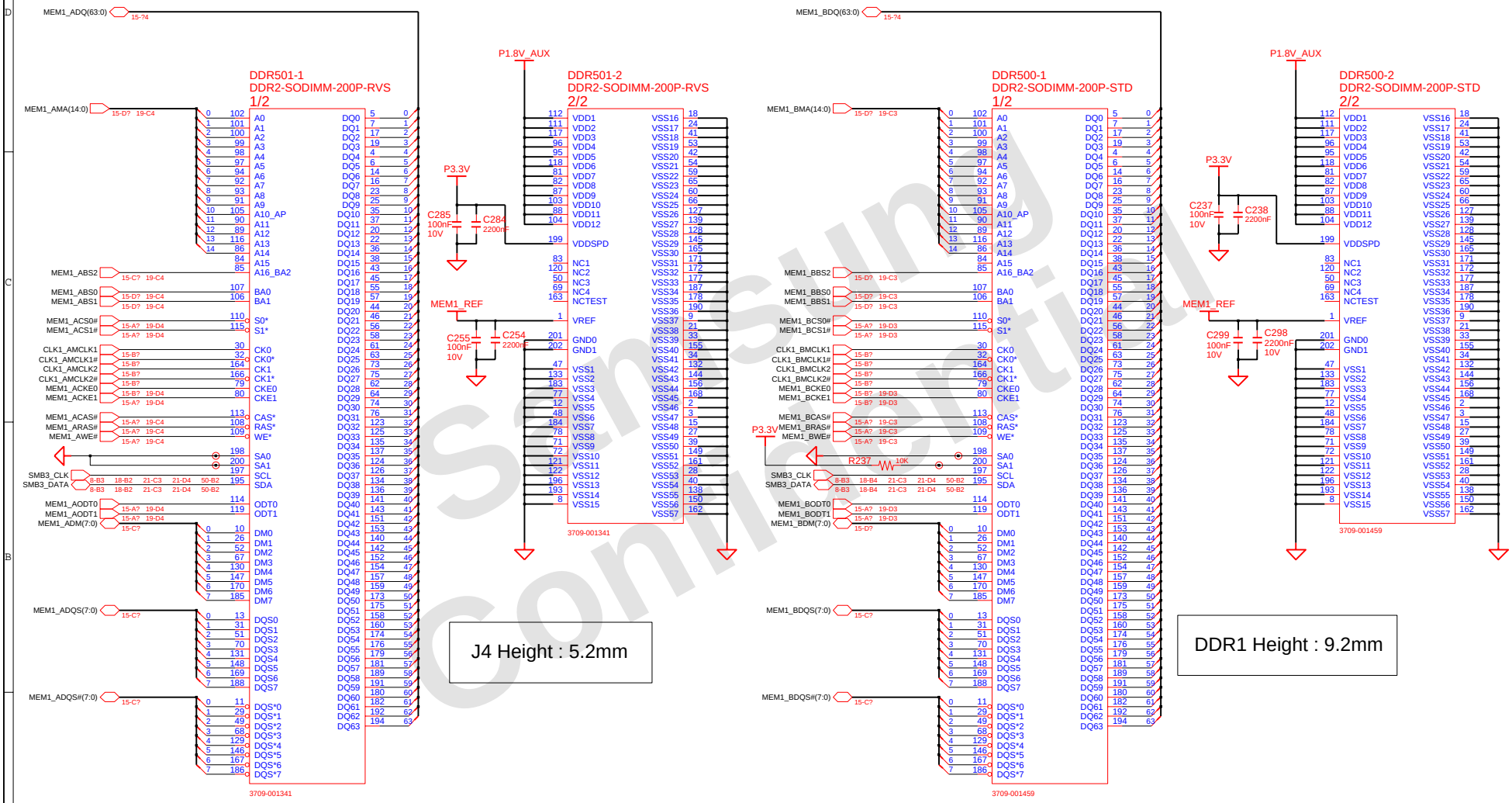
P3.3V_NB CONTROL CIRCUIT

STRAP DEFINITIONS FOR THE RS600M

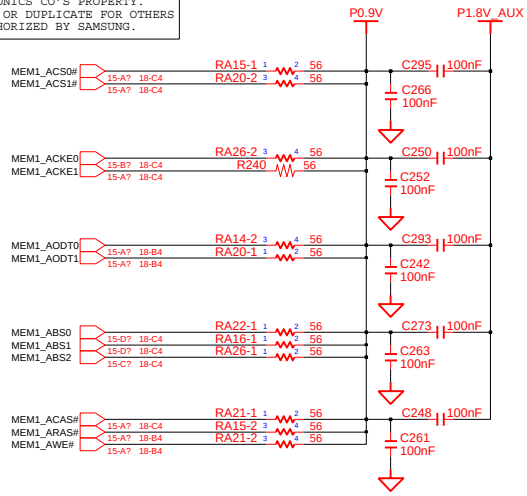
STRAP PIN	DESCRIPTION
DACHSYNC	Enable/Disable integrated graphics. 0 : Enable integrated graphics 1 : Disable integrated graphics
STRP_DATA	Debug strap configuration. This strap should not be set to "0" on production boards. 0 : Select Memory Channel A to be a debug bus 1 : Read debug straps from an external EEPROM, or disable debug mode when an EEPROM is absent.
DACVSYNC	Select configuration of the integrated graphics engine. 0 : Reserved 1 : Required setting for the RS600M
DDC_DATA	Select DDR2 or DDR3 signalling level for the memory interface. 0 : DDR3. On DDR3, it is necessary to put an isolation FET in series with the pull-up resistor on this strap to separate it from the I2C circuit during an NB reset 1 : DDR2

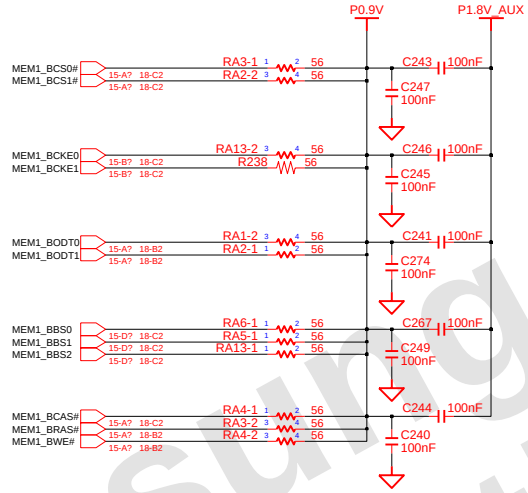
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN RS600M(4/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 16 OF 52	

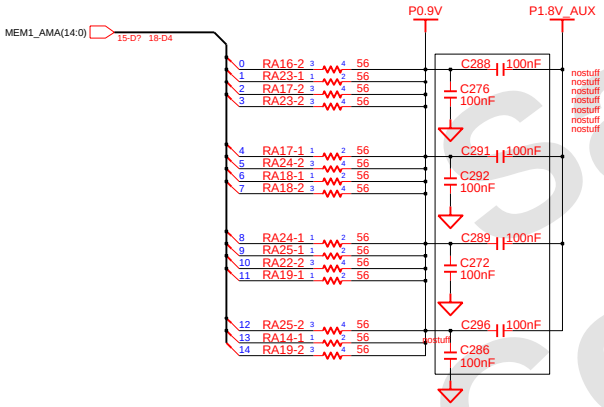

GROUND
U507-5
5 OF 5
RS600ME
CORE PWR
CPU TRANDS. PWR
MEN TRANS. PWR
PCIE PWR
GROUND
MEM I/F PWR
CPU I/F PWR
P1.2V
P1.8V
P1.8V_AUX
VCCP
B19
CIS10J270NC
C680 have to be placed under RS600M
Samsung Confidential

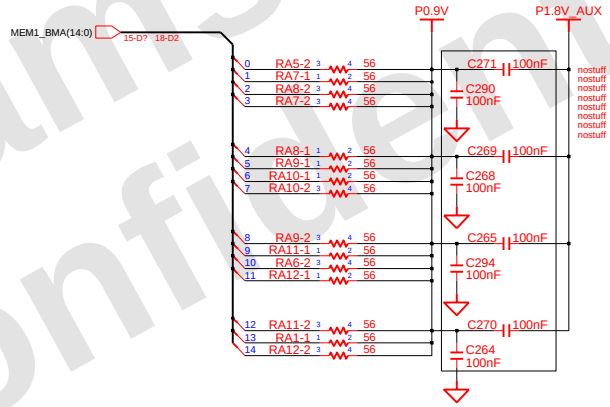


DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN DDR2 - SODIMM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 18 OF 52	



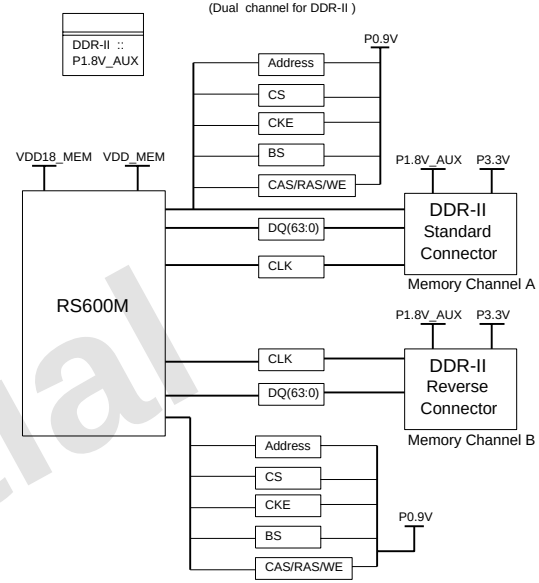


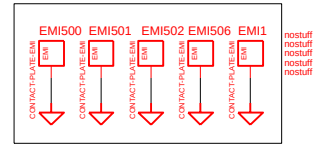


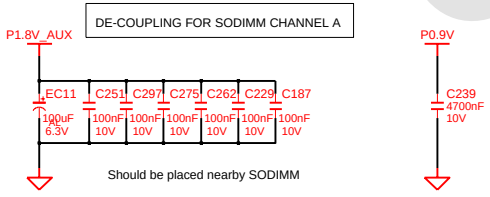


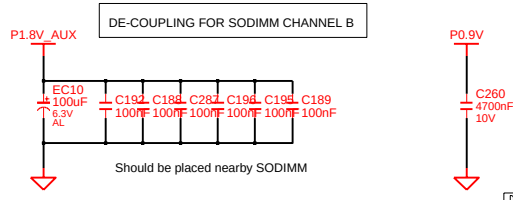
Memory Topology

(Dual channel for DDR-II)









DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN DDR2 - TERMINATION	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 19 OF 52	

U9-1
218S6ECLA21FG
1 / 4

CHP3_ALINK_RST#
R679 8.2K
A_RST*

CLK1_PCIERCLK
CLK1_PCIERCLK#
PCIE_RCLKP
PCIE_RCLKN

PEX1_ARX0P
PEX1_ARX0N
PEX1_ARX1P
PEX1_ARX1N
PEX1_ARX2P
PEX1_ARX2N
PEX1_ARX3P
PEX1_ARX3N
C203 C204 C178 C205 C180 C179 C182 C181 100nF 25V
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N

PEX1_ATX0P
PEX1_ATX0N
PEX1_ATX1P
PEX1_ATX1N
PEX1_ATX2P
PEX1_ATX2N
PEX1_ATX3P
PEX1_ATX3N
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N

PCIE_VDDR
R626 562 1%
R625 2K 1%
R627 0
PCIE_CALRP
PCIE_CALRN
PCIE_CALI

P1.2V
B517 BLM18PG181SN1
C641 10000nF 6.3V
C639 1000nF 6.3V
PCIE_PVDD
PCIE_PVSS

PCIE_VDDR_1
PCIE_VDDR_2
PCIE_VDDR_3
PCIE_VDDR_4
PCIE_VDDR_5
PCIE_VDDR_6
PCIE_VDDR_7
PCIE_VDDR_8
PCIE_VDDR_9
PCIE_VDDR_10
PCIE_VDDR_11
PCIE_VDDR_12
PCIE_VDDR_13

P1.2V
B516 BLM18PG181SN1
C637 22000nF 20%
C604 1000nF 6.3V
C640 1000nF 6.3V
C607 1000nF 6.3V
C605 100nF
C606 100nF
PCIE_VDDR

P3.3V_AUX
U11 ELM7S08WS
PCI3_RSTF# 20-D2 51-C4
R225 8.2K
R234 33 50-B2 38-B2 31-C2 28-A3 PCI3_RST#
R233 0

Y500 32.768KHz
R591 20M nostuff
R590 20M
C584 0.018nF
C583 0.018nF
X1
X2

CPU1_PWRGDCPU
CPU1_INTR
CPU1_NMI
CPU1_INIT#
CPU1_SMI#
CPU1_SLP#
CPU1_IGNNE#
CPU1_A20M#
CPU1_FERR#
CPU1_STPCLK#
CHP3_CPUSTP#
CPU1_DPSLP#
CHP3_DPRSLPVR
CPU_PG_LDT_PG
INTR_LINT0
NMI_LINT1
INIT*
SMI*
SLP*_LDT_STP*
IGNNE*_SIC
A20M*_SID
FERR*
STPCLK*_ALLOW_LDTSTP
CPU_STP*_DPSLP_3V*
DPSLP_OD*_GPIO37
DPRSLPVR
LDT_RST*_DPRSTP*_PROCHOT*

VCCP
R304 4.7K
Q46 MMBT3904
R305 47K
ATI PA for Power on Fail (2007.01.05)
R773 475 1%
CPU1_DPRSTP# 10-D4
R660 0 nostuff

U2 PCICLK0
T2 PCICLK1
U1 PCICLK2
V2 PCICLK3
W3 PCICLK4
U3 PCICLK5
V1 PCICLK6
IO41 SPDIF_OUT_PCICLK7_GPIO41
R195 R641 R194 R640 R196 22
R197 10K nostuff
CLK3_33M_MIN
CLK3_PCLKLAN
CLK3_PCLKCB
STRAP_USB48
C748 0.022nF
C747 0.022nF
CLK3_PCLKMICOM
AJ9 PCIRST*
PCI3_RSTF#
PCI3_AD(31:0)
PCI CLKS

AD0_ROMA18
AD1_ROMA17
AD2_ROMA16
AD3_ROMA15
AD4_ROMA14
AD5_ROMA13
AD6_ROMA12
AD7_ROMA11
AD8_ROMA9
AD9_ROMA8
AD10_ROMA7
AD11_ROMA6
AD12_ROMA5
AD13_ROMA4
AD14_ROMA3
AD15_ROMA2
AD16_ROMD0
AD17_ROMD1
AD18_ROMD2
AD19_ROMD3
AD20_ROMD4
AD21_ROMD5
AD22_ROMD6
AD23_ROMD7
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
PCI EXPRESS INTERFACE

P3.3V
R224 10K nostuff
R221 10K nostuff
CHP3_ALINK_RST# 20-D4 44-A3
R681 33
R680 33
PLT3_RSTF#
CHP3_NBRST#

CBE0*_ROMA10
CBE1*_ROMA1
CBE2*_ROMWE*
CBE3*
FRAME*
DEVSEL*_ROMA0
IRDY*
TRDY*_ROMOE*
PAR_ROMA19
STOP*
PERR*
SERR*
REQ0*
REQ1*
REQ2*
REQ3*_GPIO70
REQ4*_GPIO71
PCI3_CBE0#
PCI3_CBE1#
PCI3_CBE2#
PCI3_CBE3#
PCI3_FRAME#
PCI3_DEVSEL#
PCI3_IRDY#
PCI3_TRDY#
PCI3_PAR
PCI3_STOP#
PCI3_PERR#
PCI3_SERR#
PCI3_REQ0#
PCI3_REQ1#
PCI3_REQ2#

P3.3V
LPC3_LAD(0)
LPC3_LAD(1)
LPC3_LAD(2)
LPC3_LAD(3)
CHP3_SERIRQ
R685 R686 R687 R688 100K
R272 10K

GNT0*
GNT1*
GNT2*
GNT3*_GPIO72
GNT4*_GPIO73
CLKRUN*
LOCK*
PCI3_GNT0#
PCI3_GNT1#
PCI3_GNT2#
CHP3_BIOSWP#
R222 10K nostuff
PCI3_CLKRUN#
PCI3_PLOCK#

INTE*_GPIO33
INTF*_GPIO34
INTG*_GPIO35
INTH*_GPIO36
PCI3_INTA#
PCI3_INTB#
PCI3_INTC#
PCI3_INTD#
LPC3_LAD(3:0)

LAD0
LAD1
LAD2
LAD3
LFRAME*
LDRQ0*
LDRQ1*GNT5*_GPIO68
BMREQ*_REQ5*_GPIO65
SERIRQ
LPC3_LFRAME#
CHP3_SERIRQ
LPC

RTCCLK
RTC_IRQ*_GPIO69
VBAT
RTC_GND
RTC_CLK
RTC

P3.3V
R226 10K nostuff
R227 10K nostuff
R659 10K
R609 10K nostuff nostuff
RTC Battery Connector

MICOM_P3.3V
D22 BAT54C
PRTC_BAT
C647 1000nF 25V nostuff
C312 1000nF
J6 HDR-2P-SMD
3711-000541
For CMOS Reset
Place the bottom of memory door

PRTC_BAT
1% 1K R268
Move to RTC Battery Connector
C591 100nF 25V
C590 1000nF 25V

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN SB600(1/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 20 OF 52	

U9-2
218S6ECLA21FG
2 / 4

ACPI/WAKE UP EVENTS
OSC/RST
GPIO
USB OC
AZALIA
AC97
USB INTERFACE
USB PWR

USB Port 0, 1 : Rear side USB Port
USB Port 2, 3 : Left side USB Port
USB Port 4 : Bluetooth I/F
USB Port 5 : DMB I/F

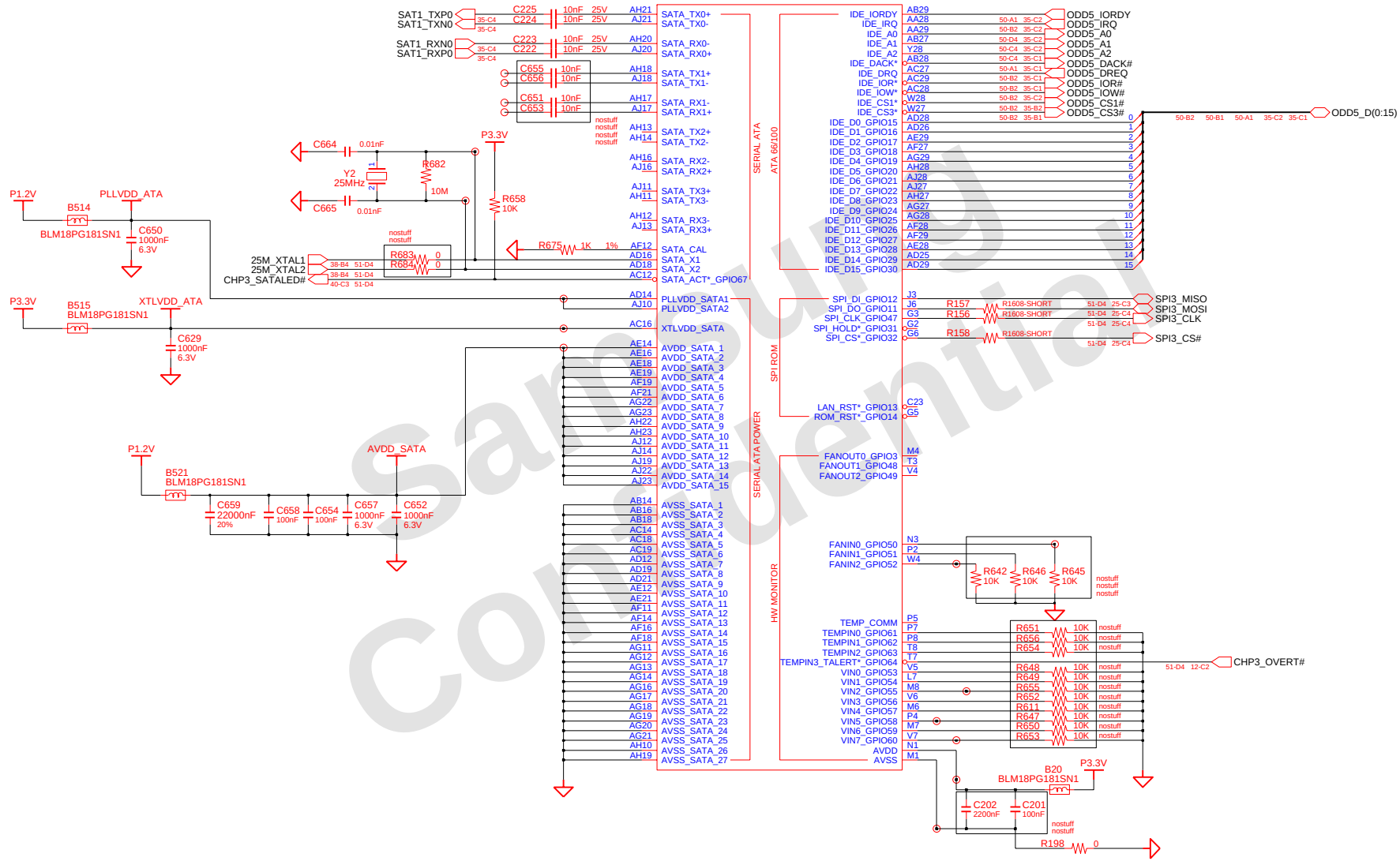
Have to be checked in case of SB600

Add below Components to reduce EMI noise from SB450(060310) (R601, R628, R629, R630, B510, B511)

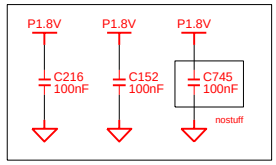
Place on the upper side

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R POWER SB600(2/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 21 OF 52	

U9-3
218S6ECLA21FG
3 / 4



DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN SB600(3/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 22 OF 52	



To Reduce EMI noise from SB450 (060310)

U9-4
218S6ECLA21FG
4 / 4

P3.3V: EC14 220uF 6.3V AL; C621 1000nF 6.3V; C624 1000nF 6.3V; C630 1000nF 6.3V; C634 1000nF 6.3V; C633 1000nF 6.3V; C625 1000nF 6.3V

P1.2V: C631 2200nF 16V; C632 1000nF 6.3V; C627 1000nF 6.3V; C626 1000nF 6.3V; C628 1000nF 6.3V

MICOM_P3.3V: C592 22000nF 6.3V; C593 1000nF 6.3V; C622 1000nF 6.3V

P1.2V_ALW: C594 100nF; C595 100nF; C620 100nF; C619 100nF

P1.2V: C600 1000nF 6.3V; C602 1000nF 6.3V; C603 1000nF 6.3V; C601 1000nF 6.3V

P5.0V: R674 1K 1%

P3.3V: MMBD4148 D515

VCCP: C636 100nF; C649 1000nF 6.3V

P3.3V: B16 BLM18PG181SN1; AVDDCK_3.3V: C162 2200nF

P1.2V: B15 BLM18PG181SN1; AVDDCK_1.2V: C161 2200nF

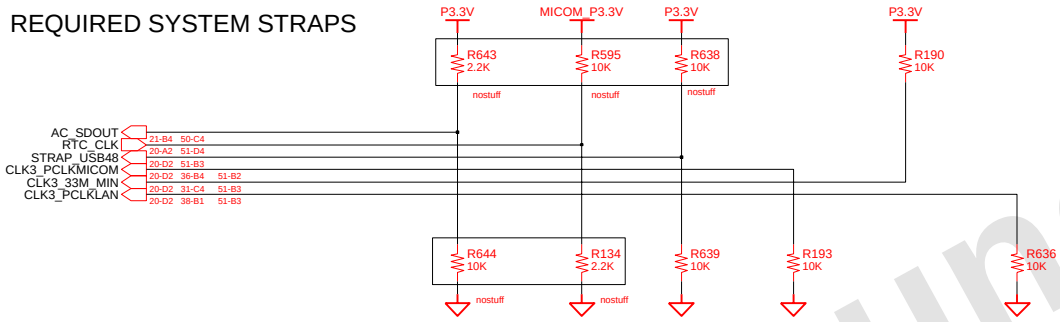
C160 100nF; C163 100nF nostuff nostuff

VDDQ_1	A25	VSS_1	A1
VDDQ_2	A28	VSS_2	A20
VDDQ_3	C29	VSS_3	A21
VDDQ_4	D24	VSS_4	A29
VDDQ_5	L9	VSS_5	B1
VDDQ_6	L21	VSS_6	B7
VDDQ_7	M5	VSS_7	B25
VDDQ_8	P3	VSS_8	C21
VDDQ_9	P9	VSS_9	C22
VDDQ_10	T5	VSS_10	C24
VDDQ_11	V9	VSS_11	D6
VDDQ_12	W2	VSS_12	E24
VDDQ_13	W6	VSS_13	F2
VDDQ_14	W21	VSS_14	F23
VDDQ_15	W29	VSS_15	G1
VDDQ_16	AA12	VSS_16	J1
VDDQ_17	AA16	VSS_17	J8
VDDQ_18	AA19	VSS_18	L6
VDDQ_19	AC4	VSS_19	L8
VDDQ_20	AC23	VSS_20	M9
VDDQ_21	AD27	VSS_21	M12
VDDQ_22	AE1	VSS_22	M15
VDDQ_23	AE9	VSS_23	M18
VDDQ_24	AE23	VSS_24	N13
VDDQ_25	AH29	VSS_25	N17
VDDQ_26	AJ2	VSS_26	P1
VDDQ_27	AJ6	VSS_27	P6
VDDQ_28	AJ26	VSS_28	P21
		VSS_29	R12
VDD_1	M13	VSS_30	R15
VDD_2	M17	VSS_31	R18
VDD_3	N12	VSS_32	T6
VDD_4	N15	VSS_33	T9
VDD_5	N18	VSS_34	U13
VDD_6	R13	VSS_35	U17
VDD_7	R17	VSS_36	V3
VDD_8	U12	VSS_37	V8
VDD_9	U15	VSS_38	V12
VDD_10	U18	VSS_39	V15
VDD_11	V13	VSS_40	V18
VDD_12	V17	VSS_41	V21
		VSS_42	W1
S5_3.3V_1	A2	VSS_43	W9
S5_3.3V_2	A7	VSS_44	Y29
S5_3.3V_3	E1	VSS_45	AA11
S5_3.3V_4	J5	VSS_46	AA14
S5_3.3V_5	J7	VSS_47	AA18
S5_3.3V_6	K1	VSS_48	AC6
		VSS_49	AC24
S5_1.2V_1	G4	VSS_50	AD9
S5_1.2V_2	H1	VSS_51	AD23
S5_1.2V_3	H2	VSS_52	AE3
S5_1.2V_4	H3	VSS_53	AE27
		VSS_54	AG6
USB_PHY_1.2V_1	A18	VSS_55	AJ1
USB_PHY_1.2V_2	A19	VSS_56	AJ25
USB_PHY_1.2V_3	B19	VSS_57	AJ29
USB_PHY_1.2V_4	B20		
USB_PHY_1.2V_5	B21		
		PCIE_VSS_1	D27
CPU_PWR	AA27	PCIE_VSS_2	D28
V5_VREF	AE11	PCIE_VSS_3	D29
		PCIE_VSS_4	F26
AVDDCK_3.3V	A24	PCIE_VSS_5	G23
AVDDCK_1.2V	A22	PCIE_VSS_6	G24
		PCIE_VSS_7	G25
AVSSCK	B22	PCIE_VSS_8	H27
		PCIE_VSS_9	J23
PCIE_VSS_28	P27	PCIE_VSS_10	J26
PCIE_VSS_29	T21	PCIE_VSS_11	J28
PCIE_VSS_30	T24	PCIE_VSS_12	K27
PCIE_VSS_31	T27	PCIE_VSS_13	L22
PCIE_VSS_32	T28	PCIE_VSS_14	L23
PCIE_VSS_33	T29	PCIE_VSS_15	L24
PCIE_VSS_34	U27	PCIE_VSS_16	L27
PCIE_VSS_35	V22	PCIE_VSS_17	L28
PCIE_VSS_36	V23	PCIE_VSS_18	M21
PCIE_VSS_37	V24	PCIE_VSS_19	M24
PCIE_VSS_38	V25	PCIE_VSS_20	M27
PCIE_VSS_39	V26	PCIE_VSS_21	N27
PCIE_VSS_40	V27	PCIE_VSS_22	N28
PCIE_VSS_41	V28	PCIE_VSS_23	P22
PCIE_VSS_42	V29	PCIE_VSS_24	P23
		PCIE_VSS_25	P24
		PCIE_VSS_26	P25
		PCIE_VSS_27	P26

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN SB600(4/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 23 OF 52	

SB600 HAS AN INTERNAL PD FOR AC_SDOUT
SB600 HAS AN INTERNAL PU FOR RTC_CLK

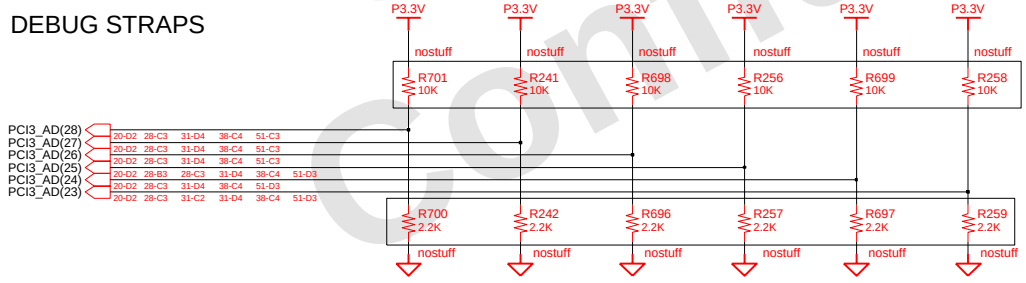
REQUIRED SYSTEM STRAPS



	AC_SDOUT	RTC_CLK	PCI3_CLK4	PCI3_CLK6	PCI3_CLK0 PCI3_CLK1
STRAP HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INTERNAL PLL48	CPU I/F = K8	ROM TYPE H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM
STRAP LOW	IGNORE DEBUG STRAPS	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	USE EXTERNAL 48MHz	CPU I/F = P4	

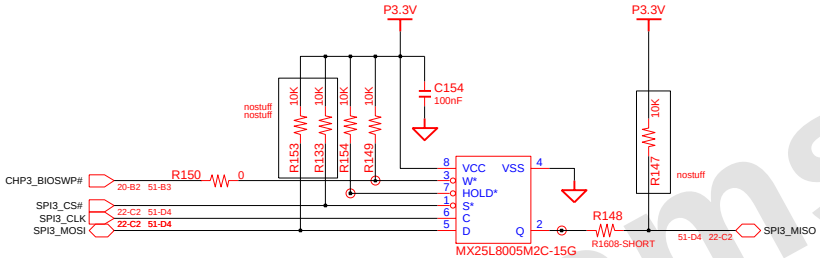
SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

DEBUG STRAPS



	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

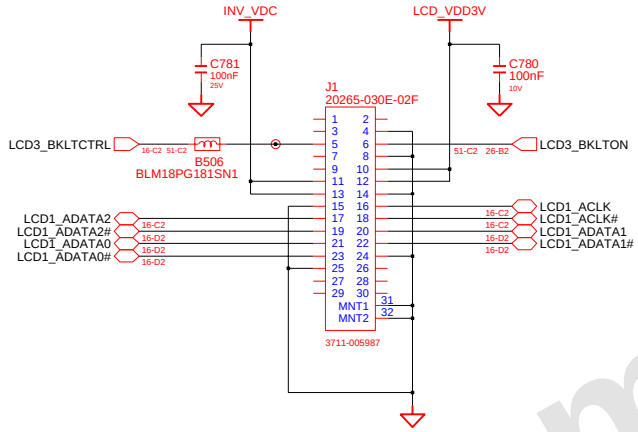
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R STRAPS	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 24 OF 52	



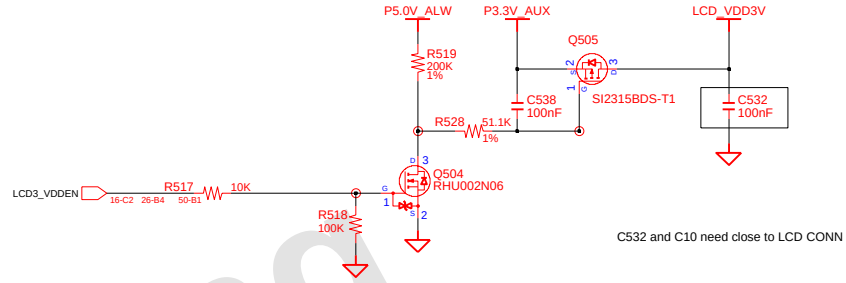
SPI3_CS#
SB600 prior to A21 : Pulled up to P3.3V_ALW with 1Kohm resistor.
SB600 A21 and newer : No external pull-up resistor required.

02 VERIFY REAL MODE	66 CONFIGURE ADVANCE CACHE REG.
03 DISABLE NMI	6A DISPLAY EXTERNAL CACHE SIZE
04 GET CPU TYPE	6C DISPLAY SHADOW MESSAGE
06 INIT. SYSTEM H/W	6E DISPLAY NON-DISPOSABLE SEGMENT
08 INIT. CHIPSET REG.	70 DISPLAY ERROR MESSAGE
09 SET IN POST FLAG	72 CHECK FOR CONFIGURATION ERROR
0A INIT CPU.REG	74 TEST REAL-TIME CLOCK
0B CPU CACHE ON	76 CHECK FOR KEYBOARD EERROR
0C INIT.CACHE TO POST	7C SETUP HARDWARE INTERRUPT VECTOR
OE INIT. I/O VALUE	7E TEST COPROCESSER IF PRESENT
0F ENABLE THE L-BUS IDE	80 DISABLE ON-BOARD I/O PORT
10 INIT. POWER MANAGER	82 DETECT AND INSTALL EXT.RS232C
11 LOAD ALTERNATE REG.	84 DETECT AND INSTALL EXT.PARALLEL
13 PCI BUS MASTER RESET WITH INITIAL POST VALUE	86 RE-INIT. ON-BOARD I/O PORT
	88 INIT. BIOS DATA ROM
14 INIT. KEYBOARD CONTROLLER	8A INIT.EXTENDED BIOS DATA AREA
16 CHECK CHECKSUM	8C INIT. FDD CONTROLLER
18 8254 TIMER INIT.	9A SHADOW OPTION ROMS
1A 8237 DMA CONTROLLER INIT.	9C SETUP POWER MANAGEMENT
1C RESET INTERRUP CONTROLLER	9E ENABLE H/W INTERRUPT
20 TEST DRAM REFRESH	A0 SET TIME OF DAY
22 TEST 8742 KEYBOARD CONTROLLER	A4 INIT. TYPEMATIC RATE
24 SET ES SEGMENT REG. TO 4GB	A8 ERASE F2 PROMPT
26 ENABLE A20	AA SCAN FOR F2 KEY STROKE
28 AUTO SIZING DRAM	AC ENTER SETUP
32 COMPUTE THE CPU SPEED	AE CLEAR IN POST FLAG
34 TESET CMOS RAM	B0 CHECK FOR ERRORS
38 SHADOW SYSTEM BIOS ROM	B2 POST DONE-PREPARE TO BOOT O/S
3A AUTO SIZING CACHE	B4 ONE BEEP
3C CONFIGURE ADVANCED CHIPSET REG.	B6 CHECK PASSWORD (OPTION)
3D LOAD ALTER REG. WITH CMOS VALUE	B7 ACPI INIT
42 INIT. INTERRUPT VECTOR	BA DMI INIT
44 INIT. BIOS INTERRUPT	BE CLEAR SCREEN
46 CHECK ROM COPYRIGHT NOTICE	C0 TRY BOOT WITH INT19
47 INIT. I20 SUPPORT IF INSTALLED	D0 INTERRUPT HANDLER ERROR
48 CHECK VIDEO CONFIGURE AGAINST CMOS	D2 UNKNOWN INTERRUPT ERROR
49 INIT. PCI BUS AND DEVICE	D4 PENDING INTERRUPT ERROR
4A INIT. ALL VIDEO BIOS ROM	D6 SHUTDOWN 5
4C SHADOW VIDEO BIOS ROM	D8 SHUTDOWN ERROR
50 DISPLAY CPU TYPE AND SPEED	DA EXTENDED BLOCK MOVE
52 TEST KEYBOARD	DC SHUTDOWN 10
54 SET KEYCLICK IF ENABLED	89 ENABLE NMI
56 ENABLE KEYBOARD	90 INIT. HDD CONTROLLER
58 TEST FOR UNEXPECTED INTERRUPTS	91 INIT. LOCAL BUS HDD CONTROLLER
5A DISPLAY " PRESS ..... SETUP"	92 JUMP TO USER PATCH 2
5C TEST RAM GETWEEN 512K AND 640K	94 DISABLE A20 ADDRESS LINE
60 TEST EXTENDED MEMORY	96 CLEAR HUGE ES SEGMENT REG.
62 TEST EXTENDED MEMORY ADDRESS LINE	98 SEARCH FOR OPTION ROMS
64 JUMP TO USER PATCH 1	

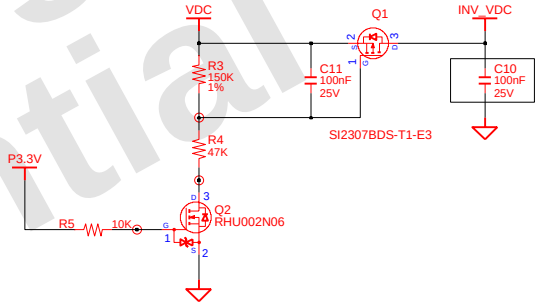
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN FIRMWARE HUB	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 25 OF 52	

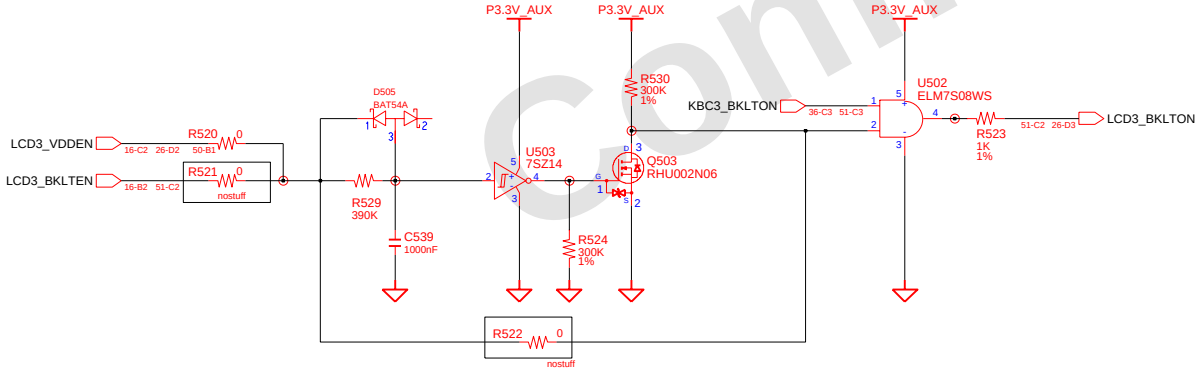


LCD Connector(LVDS)

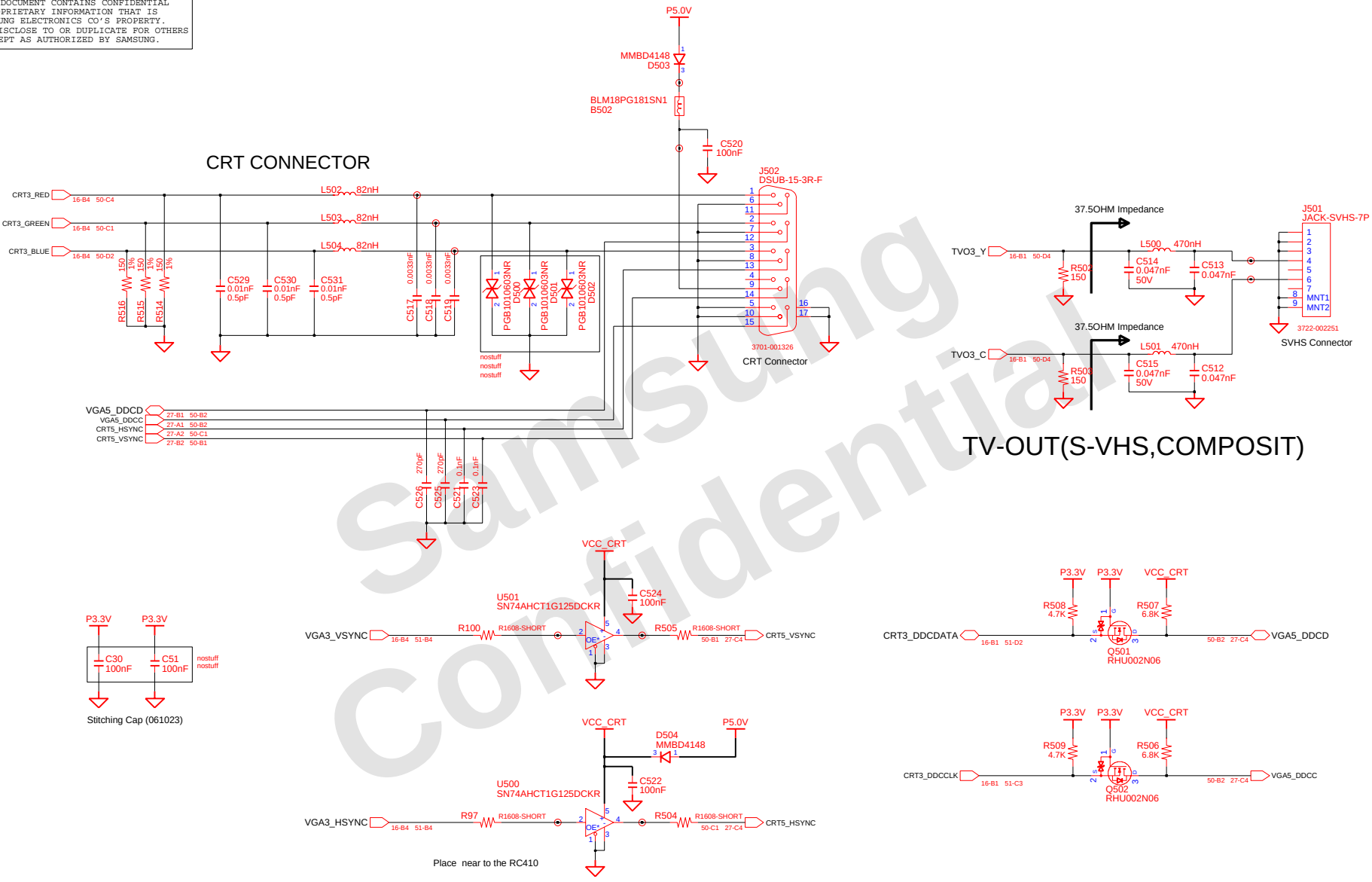


C532 and C10 need close to LCD CONN

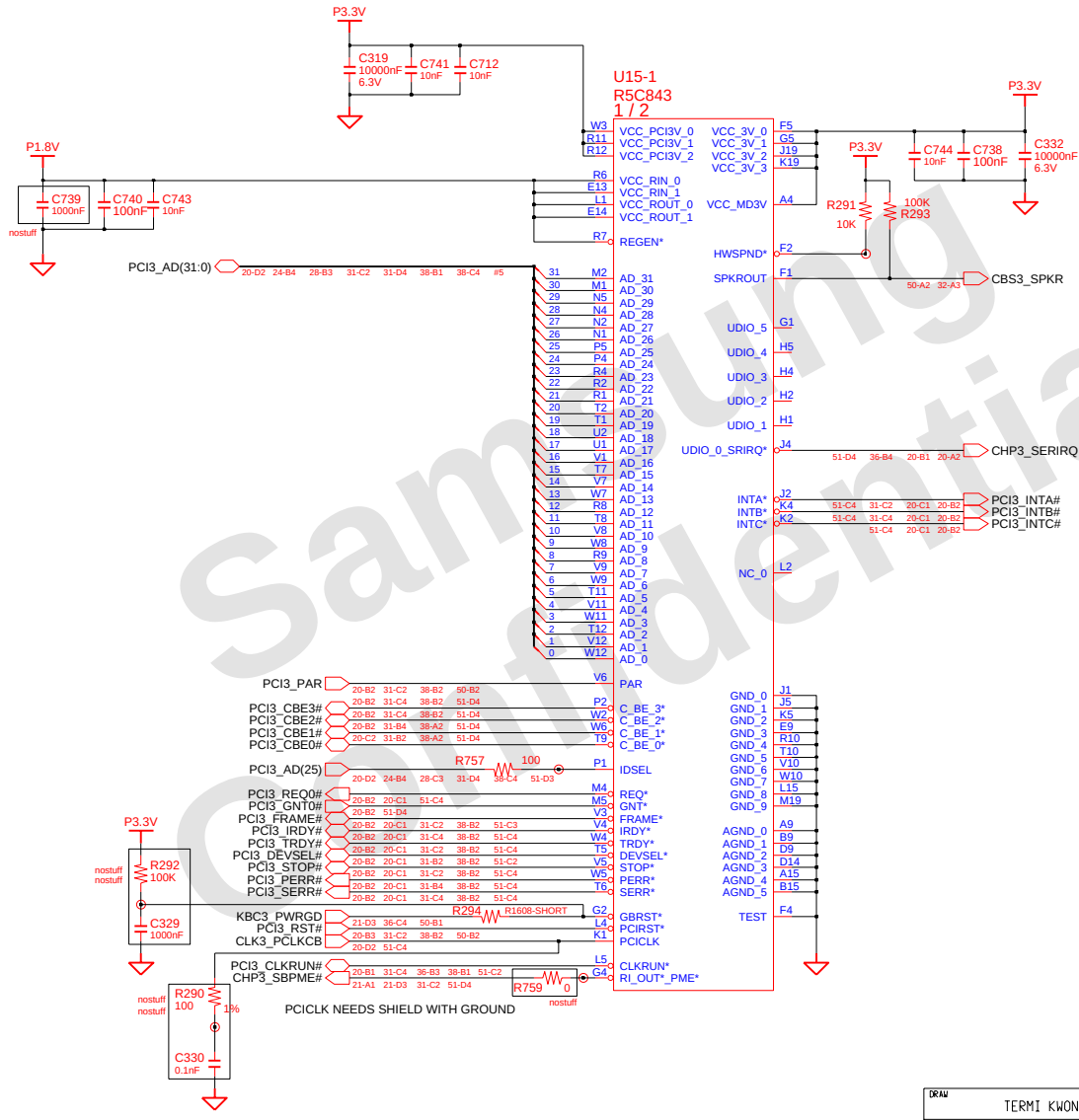




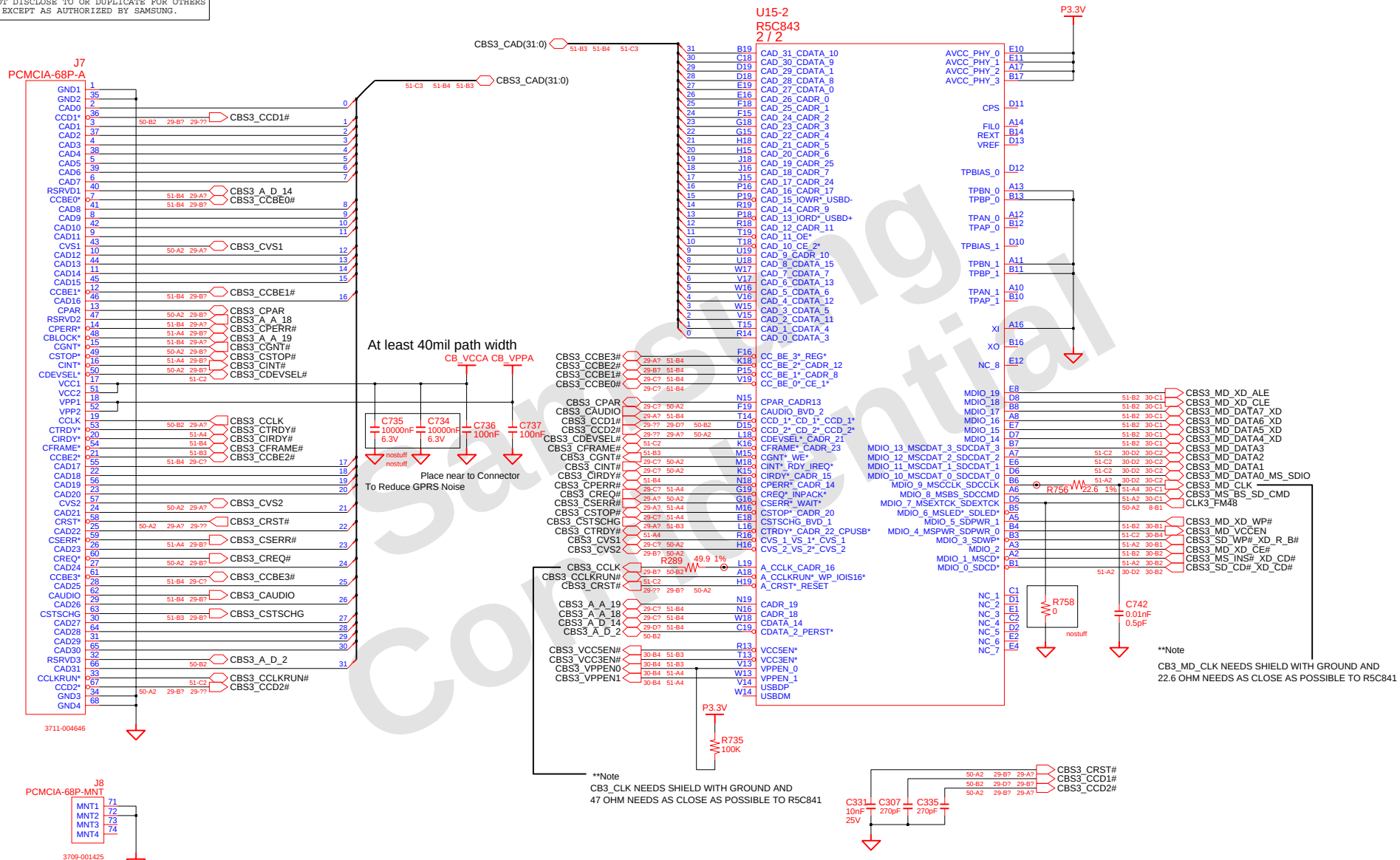
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R LCD Connector & SPREAD SPECTRUM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO. BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 26 OF 52	



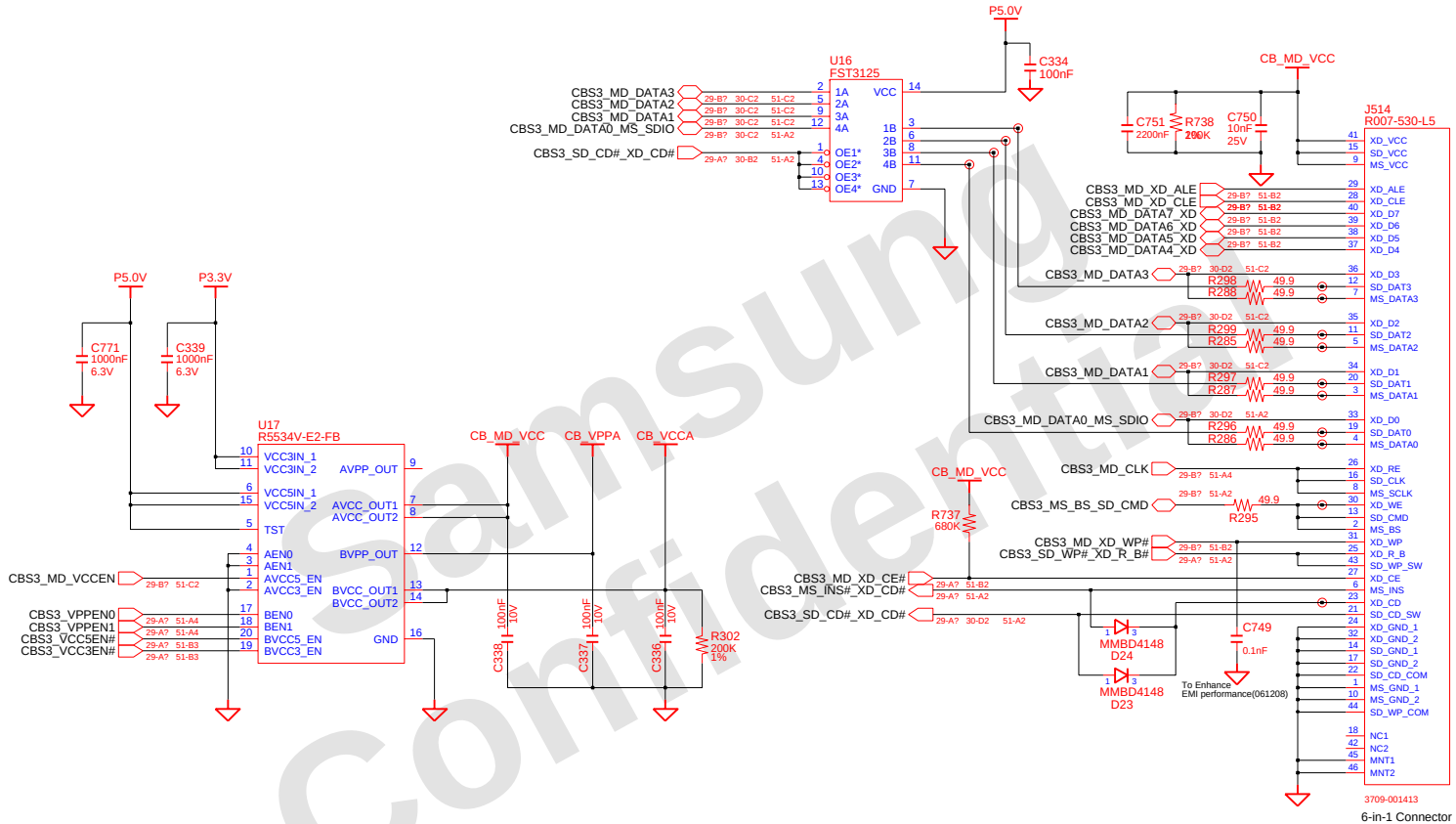
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP	CRT AND TV-OUT	
APPROVAL: SJ PARK	REV: 1.0		PART NO. BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 27 OF 52	



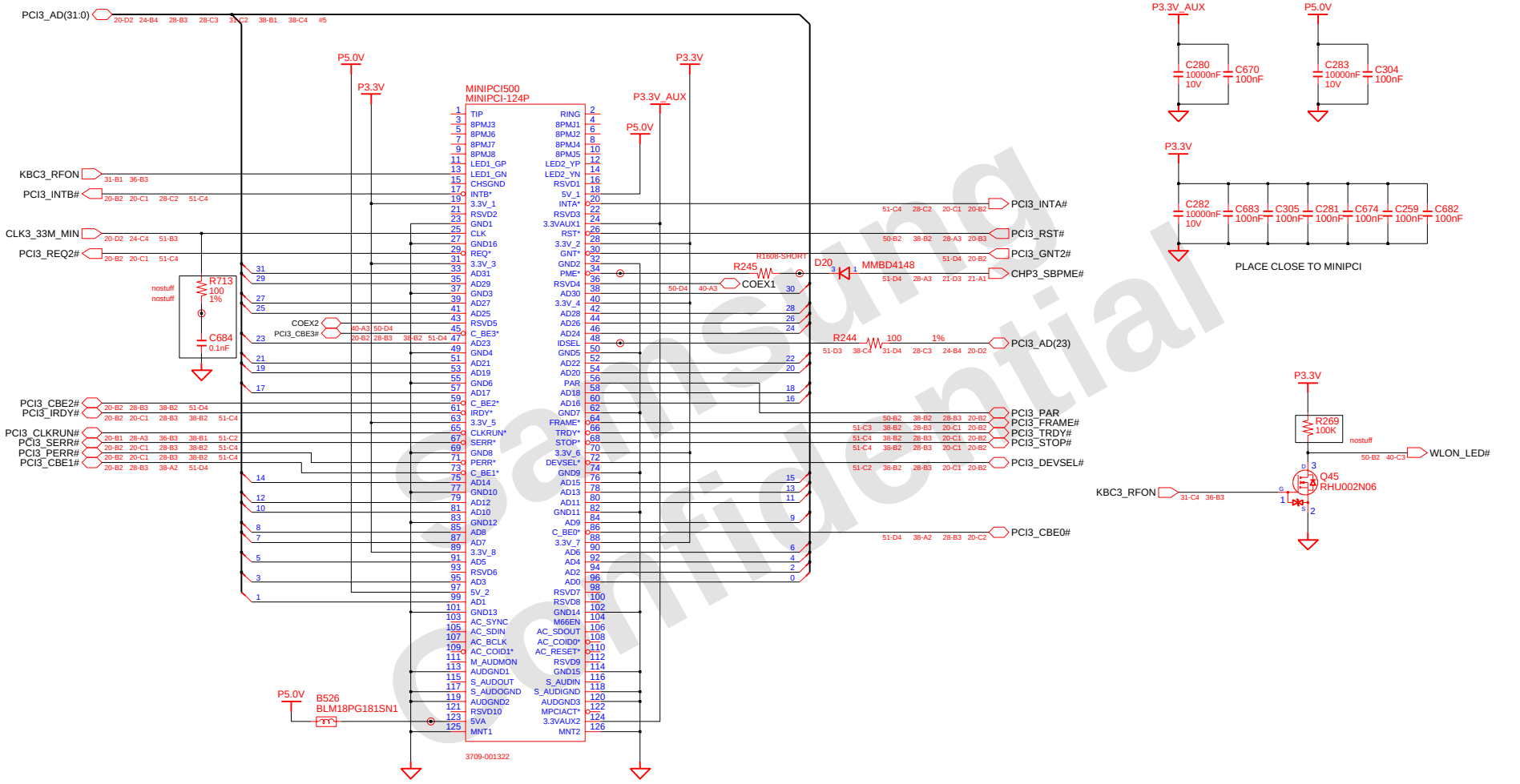
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP	CARDBUS(1/2)	PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 28 OF 52	



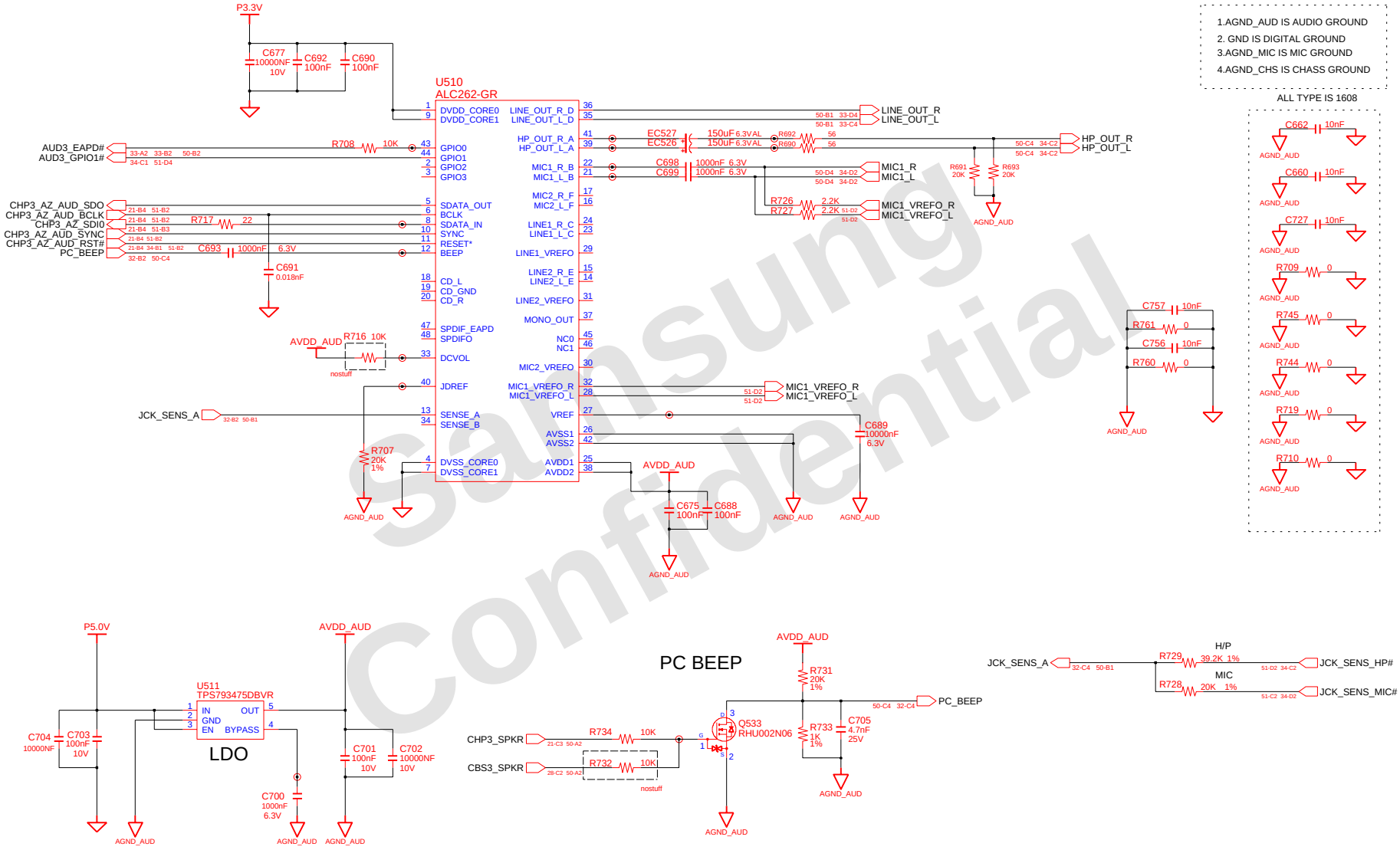
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R CARDBUS(2/2)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 29 OF 52	



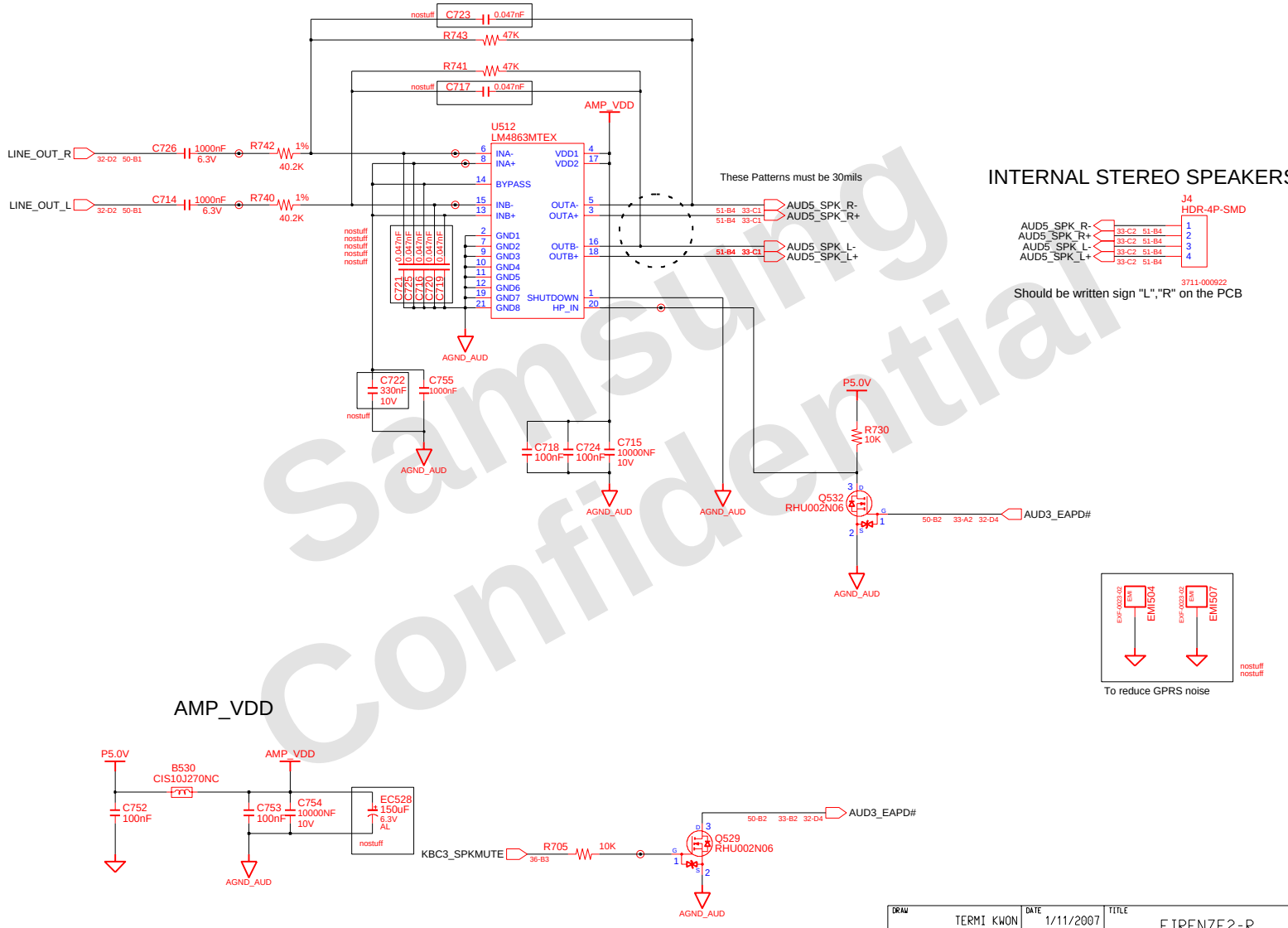
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP	5 in 1 Socket	
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 30 OF 52	



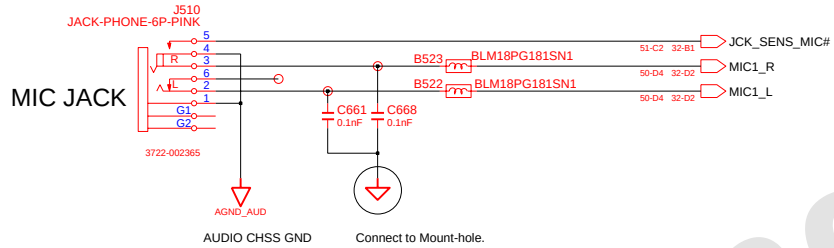
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN MINI PCI	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 31 OF 52	



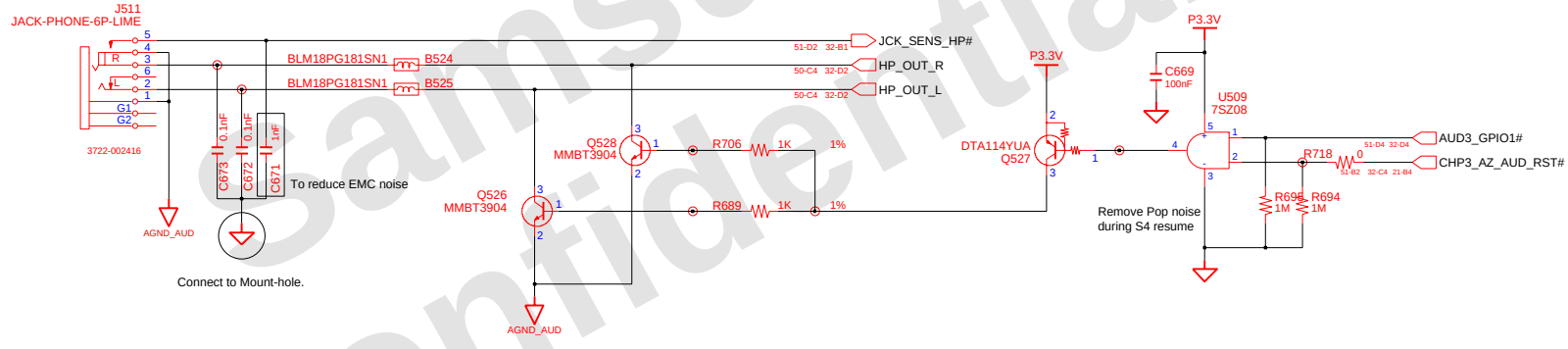
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN AUDIO CODEC	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 32 OF 52	



DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN LIMITER & AMP	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 33 OF 52	



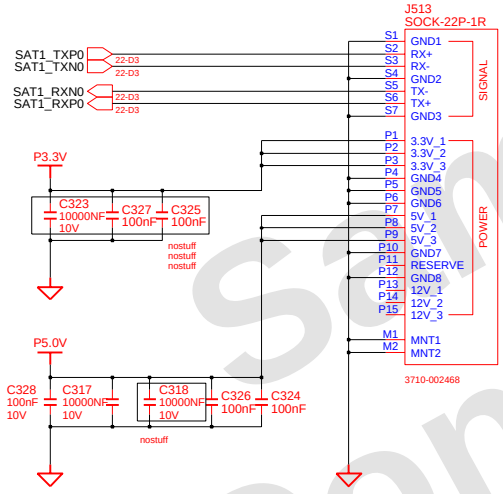
HEADPHONE



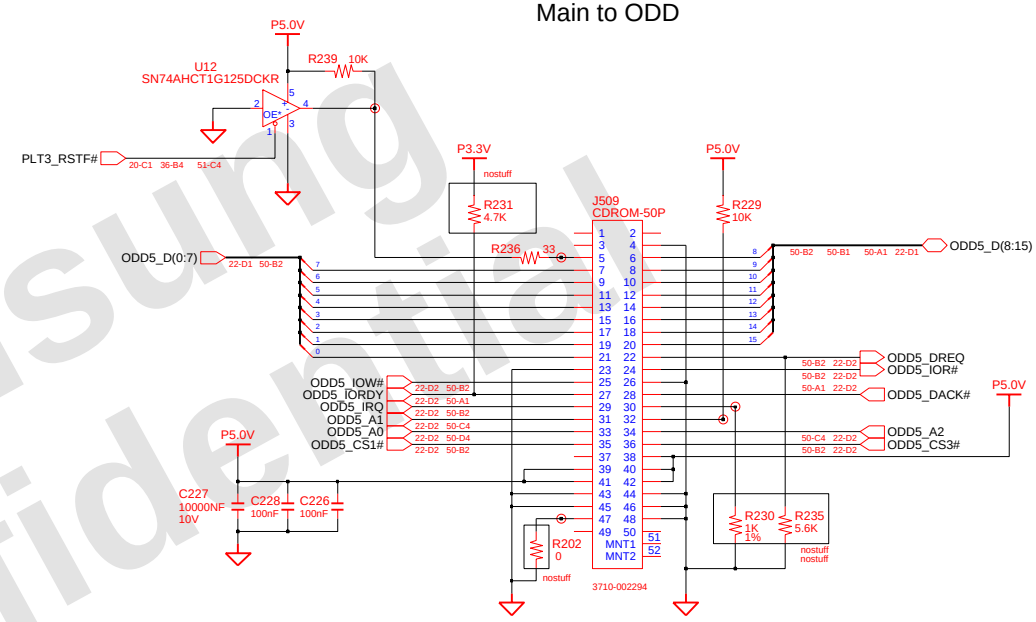
The traces led to Audio Jacks have the width over 10mil

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN UPPER & AUDIO CONN	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 34 OF 52	

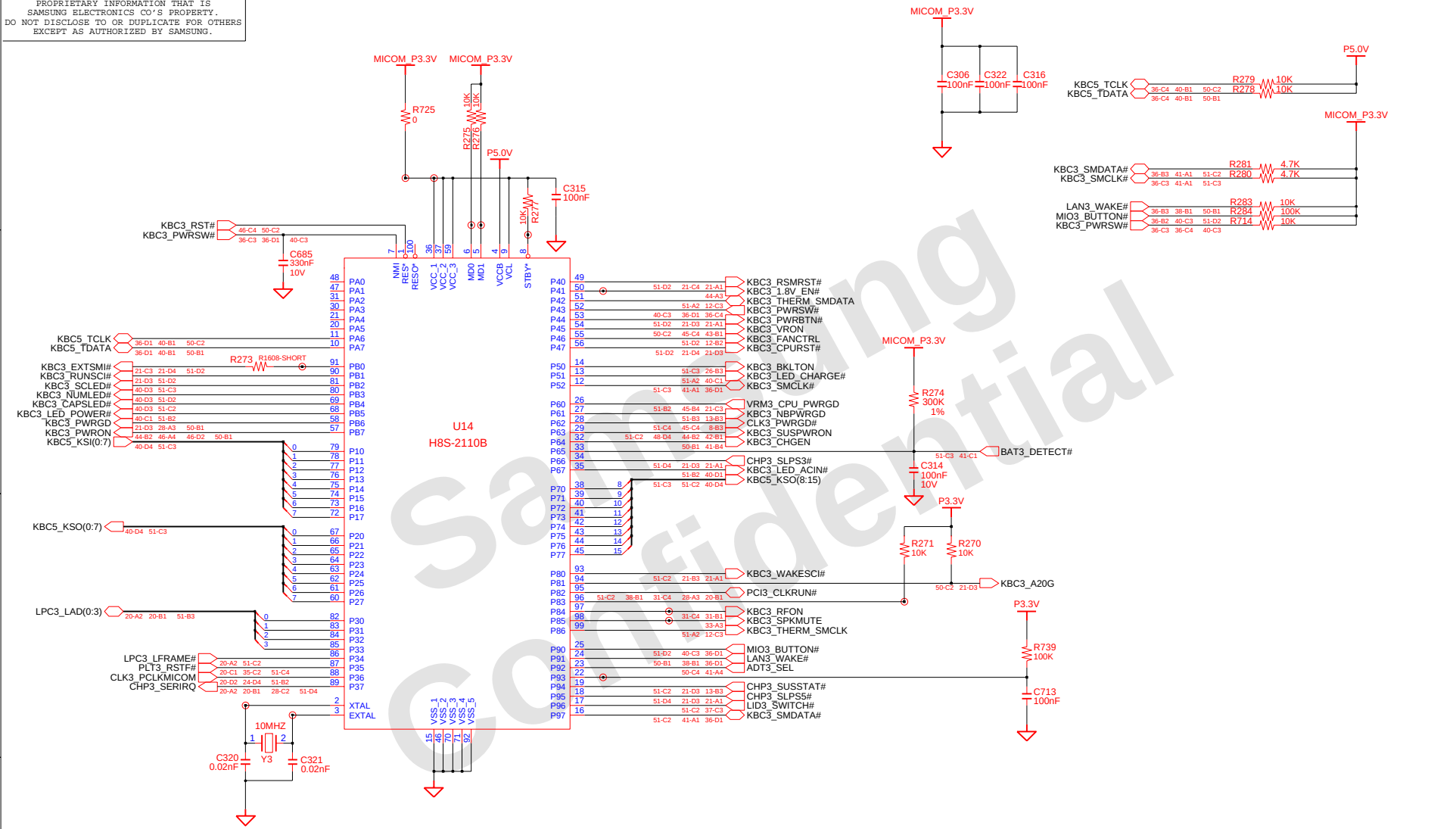
Main to HDD



Main to ODD



DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R POWER HDD & ODD	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 35 OF 52	



MICOM Crisis Update

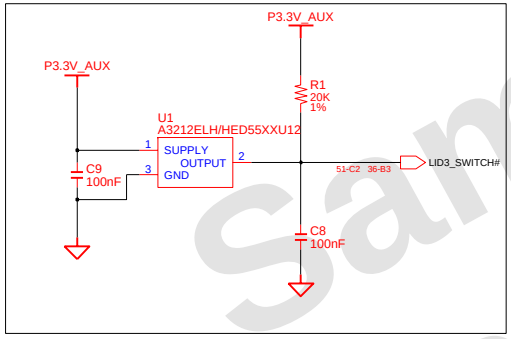
Condition: P90=P91=P92=High(MICOM_P3V)
MD0=MD1=Low(0V)
Serial Port: P84 & P85

The removed signal compaired from 144pin

- KBC5_CAL_THRM*
- THRM_ALERT*
- LCD3_BKLTEN
- FAN3_FDBACK*
- THERM_STP*

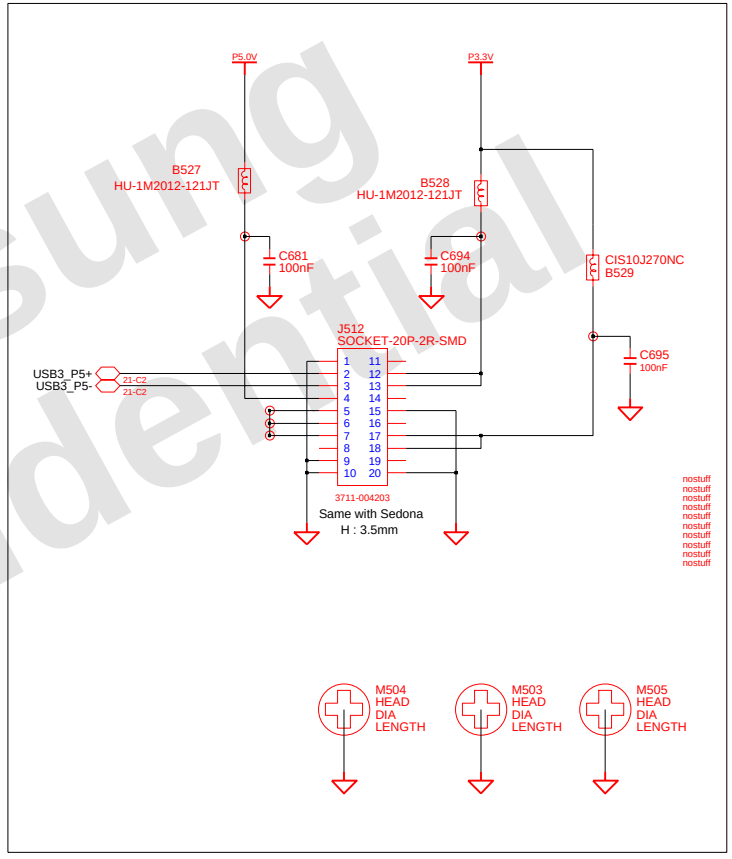
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R POWER MICOM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 36 OF 52	

LID SWITCH



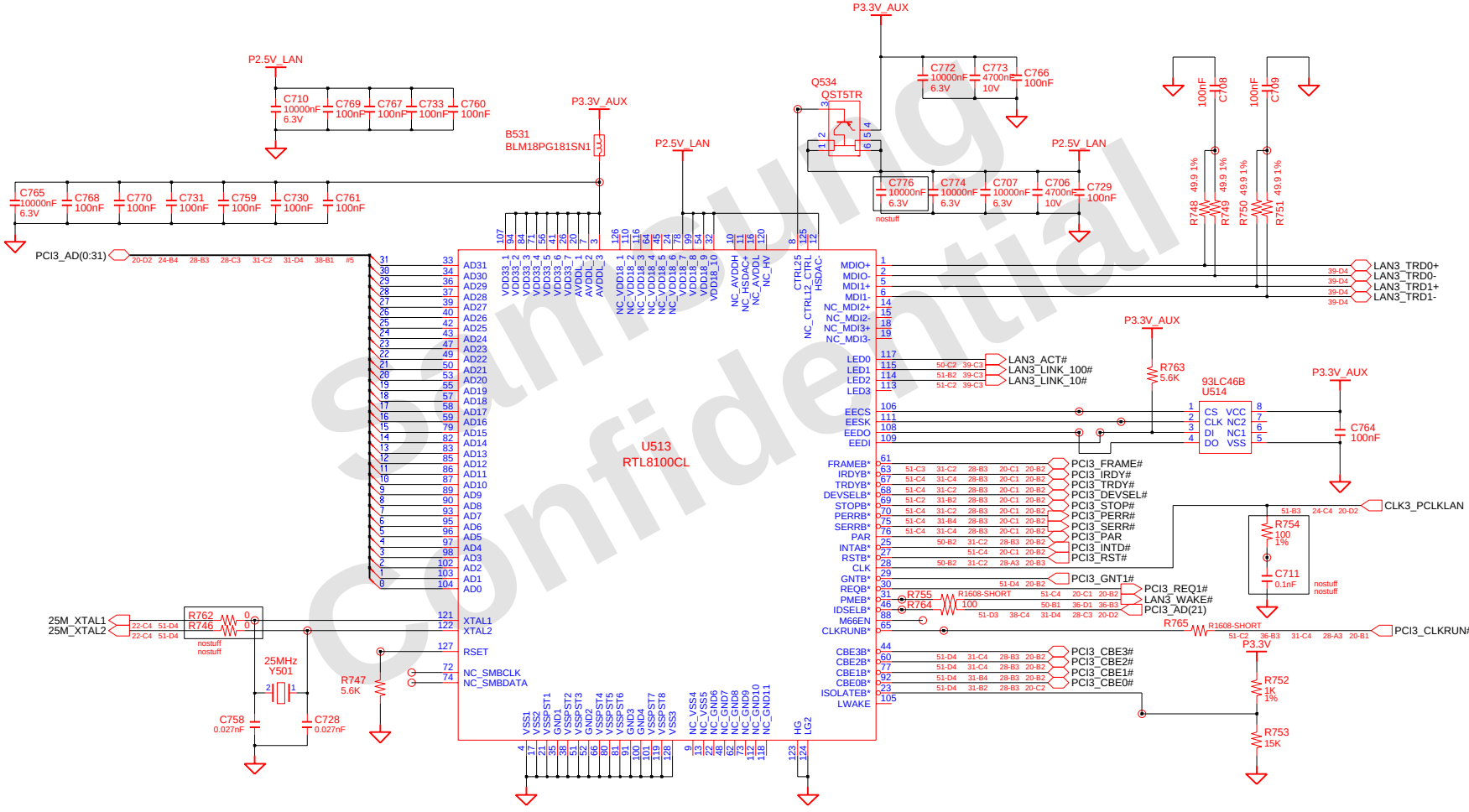
DMB (nostuff)

Factory Option



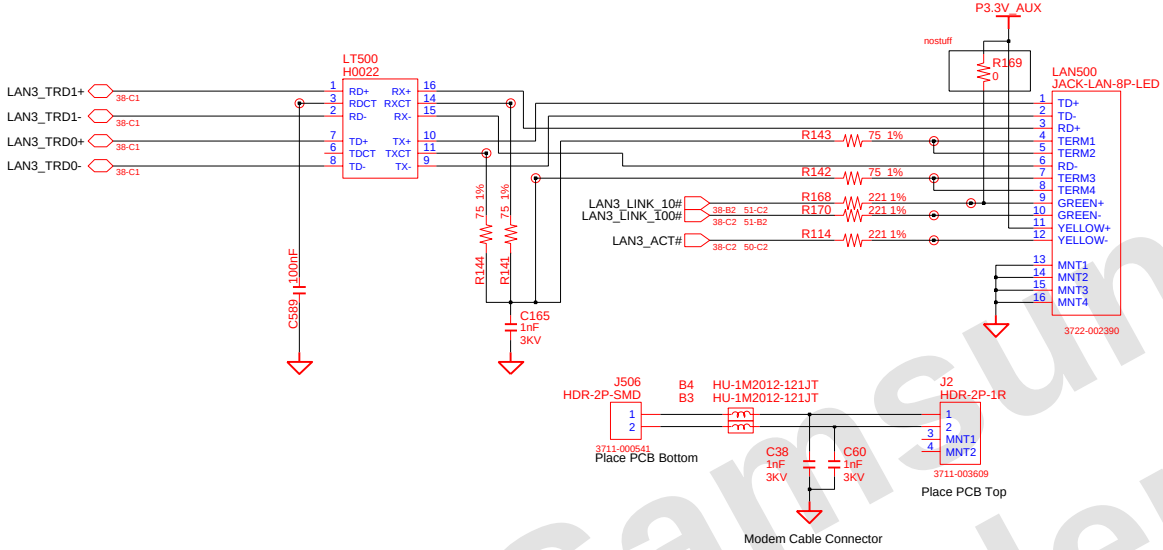
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN LPC	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 37 OF 52	

LAN Controller (Only 10/100M)

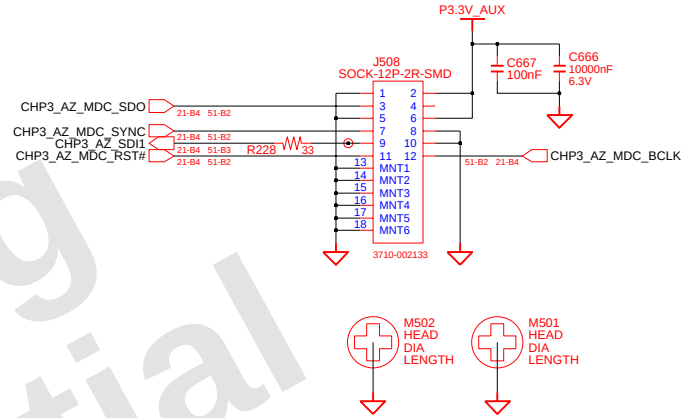


DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN LAN	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 38 OF 52	

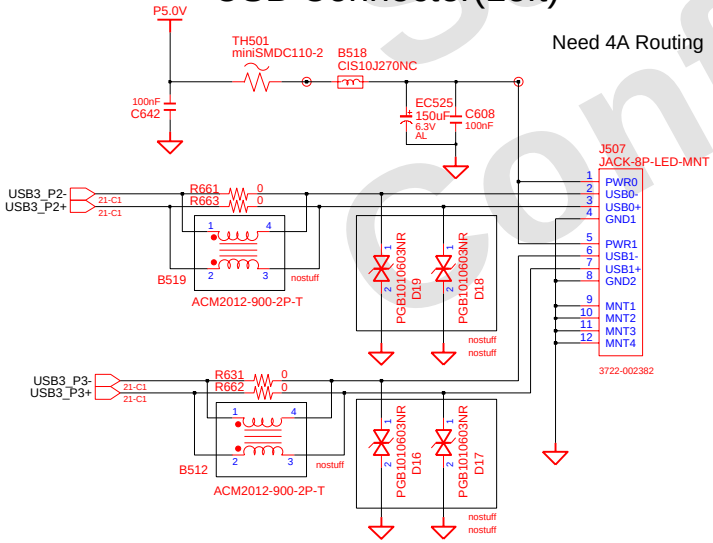
LAN Connector



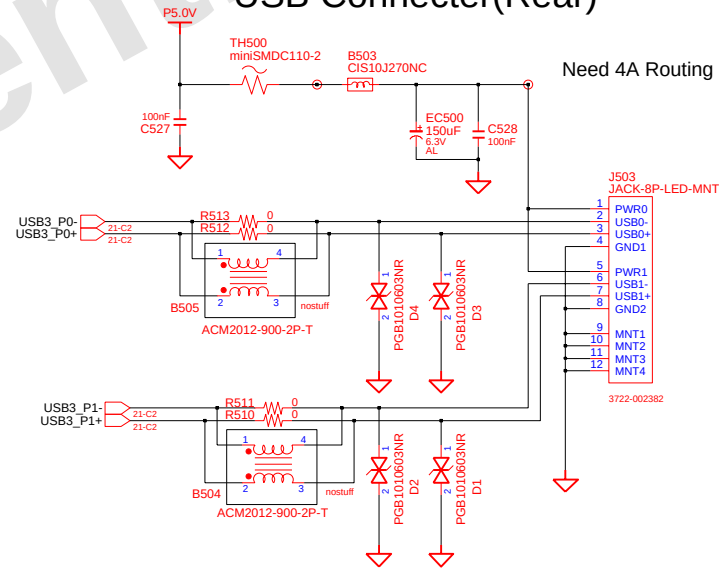
MDC Connecter



USB Connecter(Left)

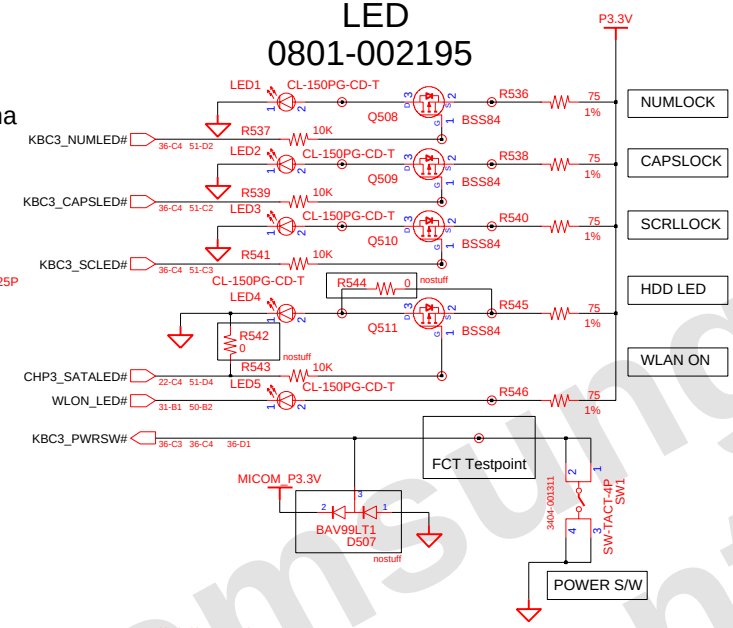


USB Connecter(Rear)

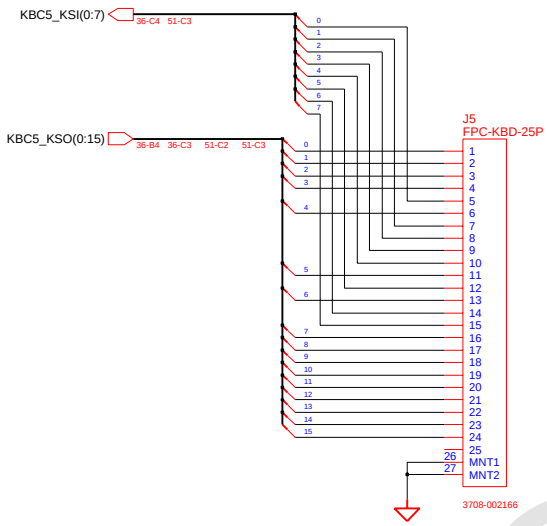


DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN LAN & USB0 & MODEM Conn.	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 39 OF 52	

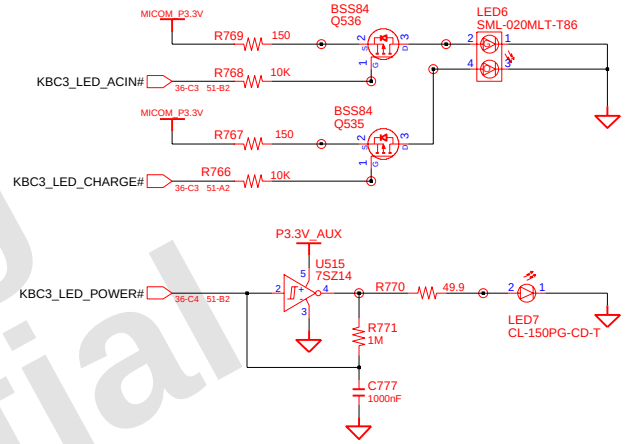
LED
0801-002195



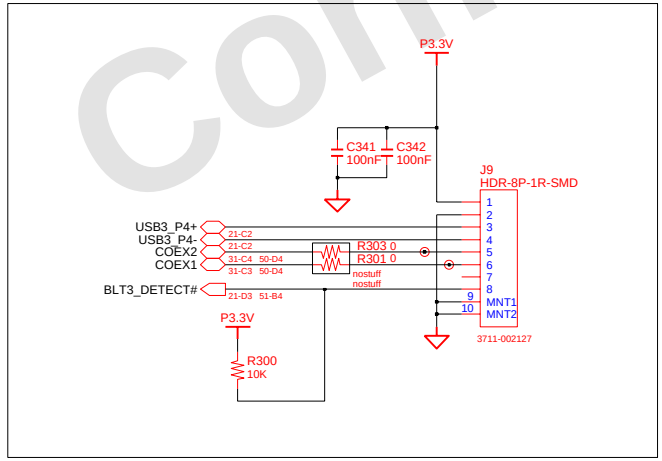
KEYBOARD
Same connector with Sedona



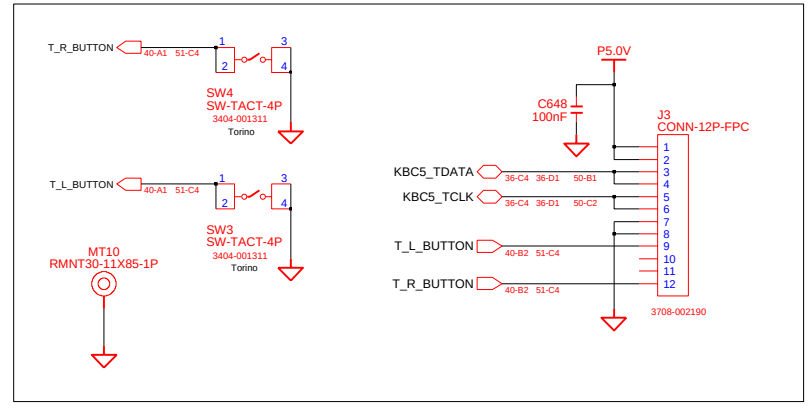
ADAPTERIN/CHARGING LED

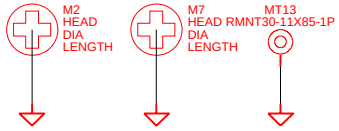


Bluetooth Interface
Factory Option



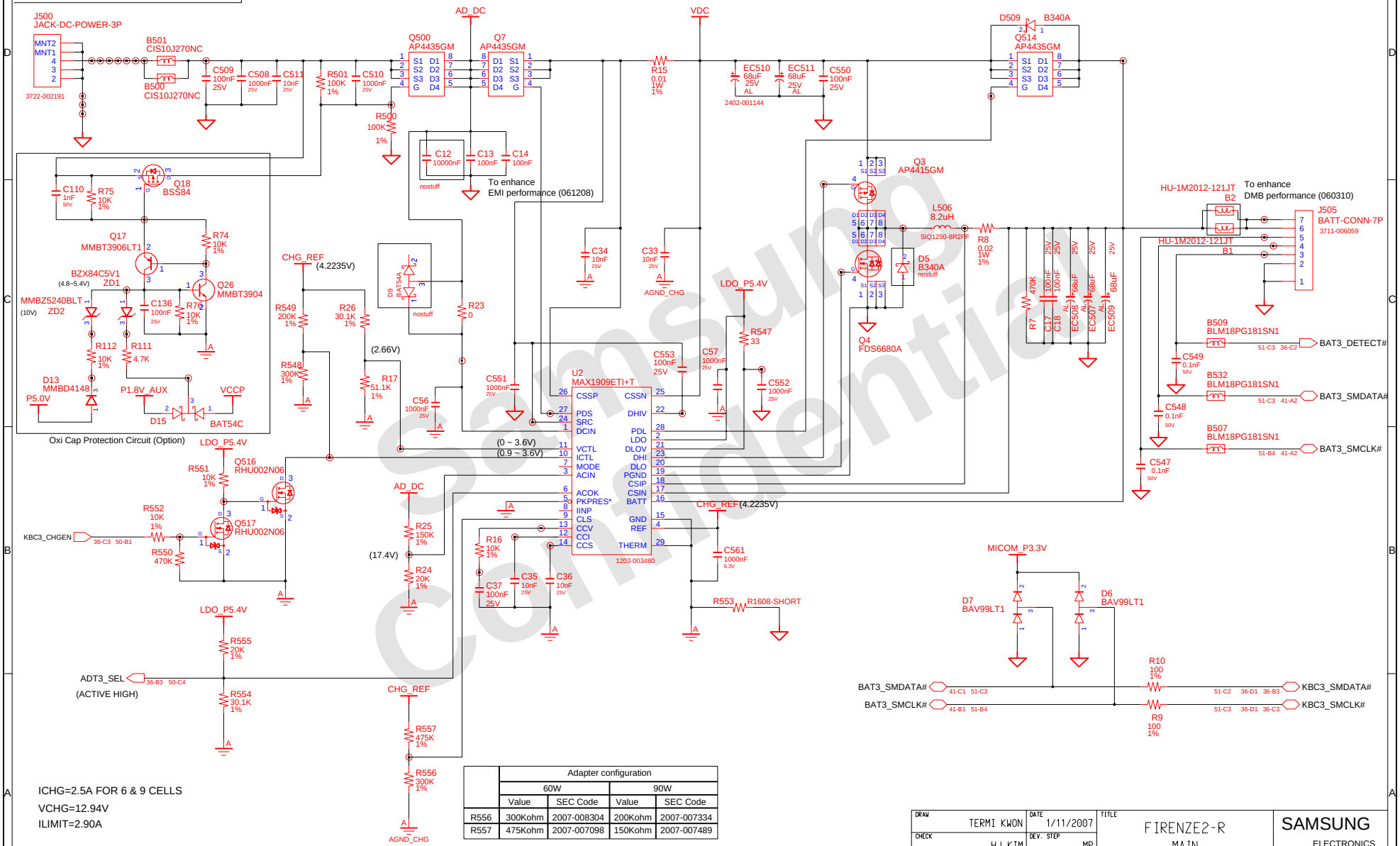
TOUCHPAD





DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN B'D TO B'D CONNECTOR	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 40 OF 52	

CHARGER & POWER MANAGEMENT



ICHG=2.5A FOR 6 & 9 CELLS
VCHG=12.94V
ILIMIT=2.90A

	Adapter configuration			
	60W		90W	
	Value	SEC Code	Value	SEC Code
R556	300Kohm	2007-008304	200Kohm	2007-007334
R557	475Kohm	2007-007098	150Kohm	2007-007489

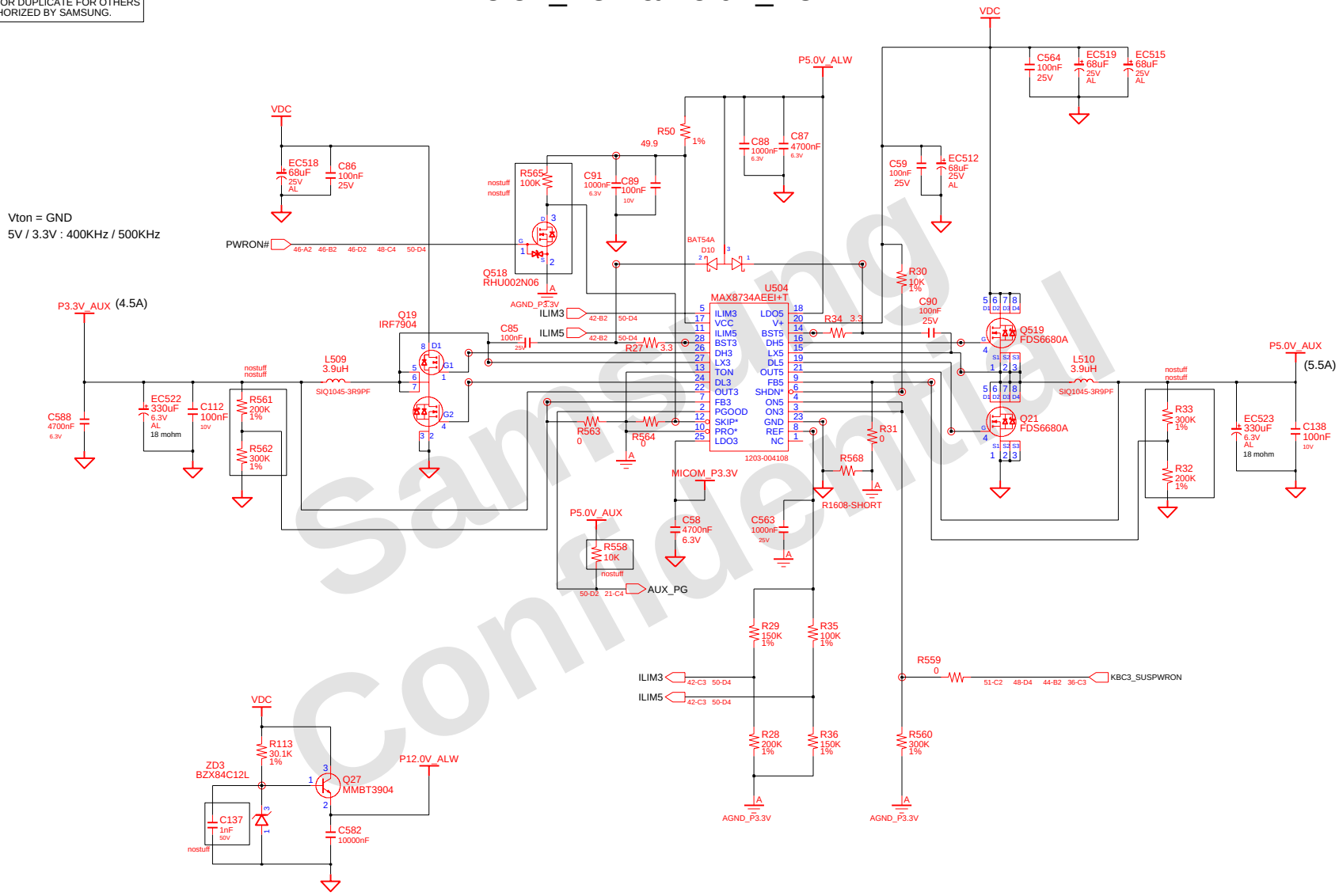
DRAW	TERMI KWON	DATE	1/11/2007
CHECK	HJ KIM	DEV. STEP	MP
APPROVAL	SJ PARK	REV	1.0
MODULE CODE	undefined	LAST EDIT	January 11, 2007 8:27:44 PM

TITLE: FIRENZE2-R MAIN CHARGER

SAMSUNG ELECTRONICS

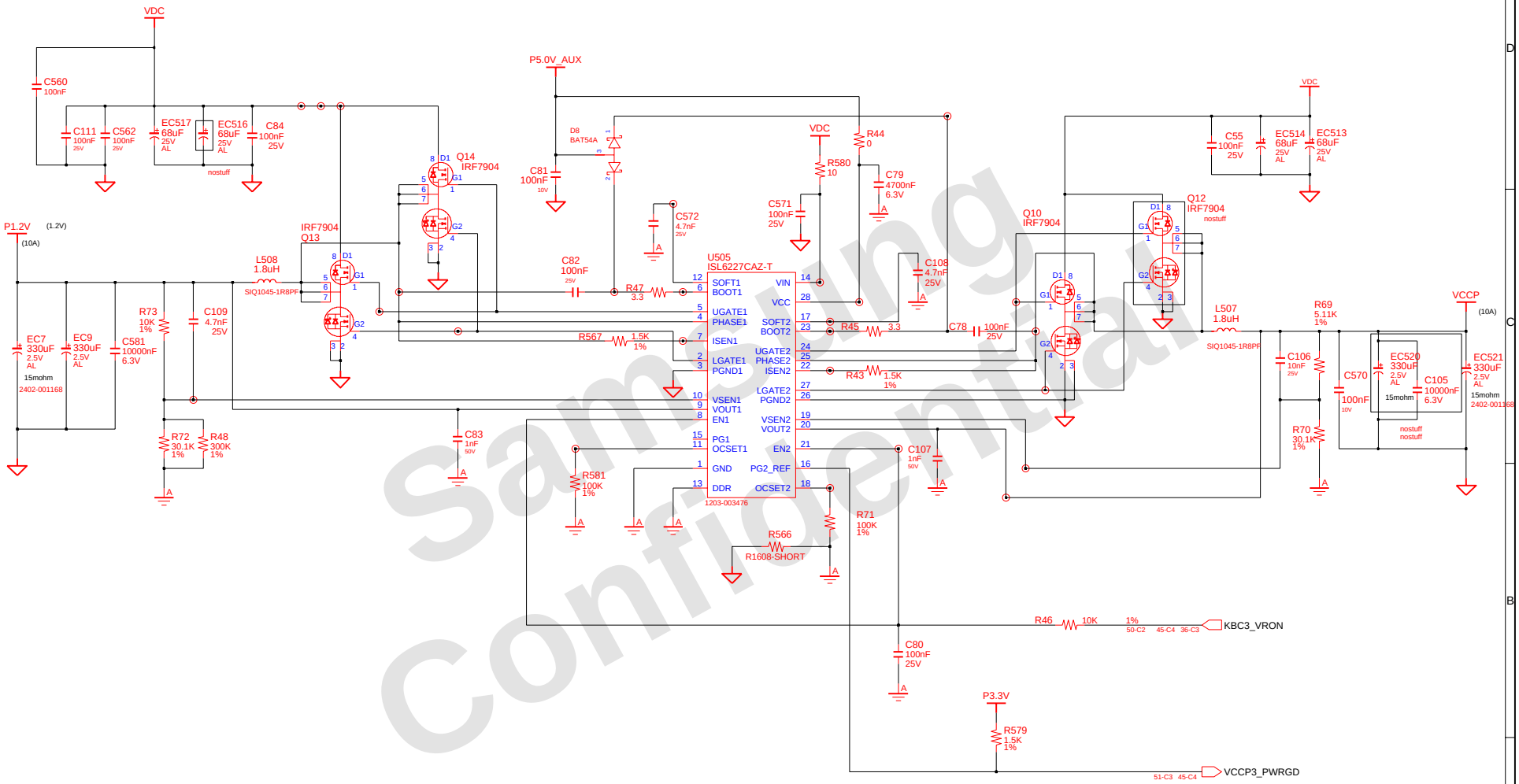
PART NO. BA41-00714A

P3.3V_AUX & P5.0V_AUX



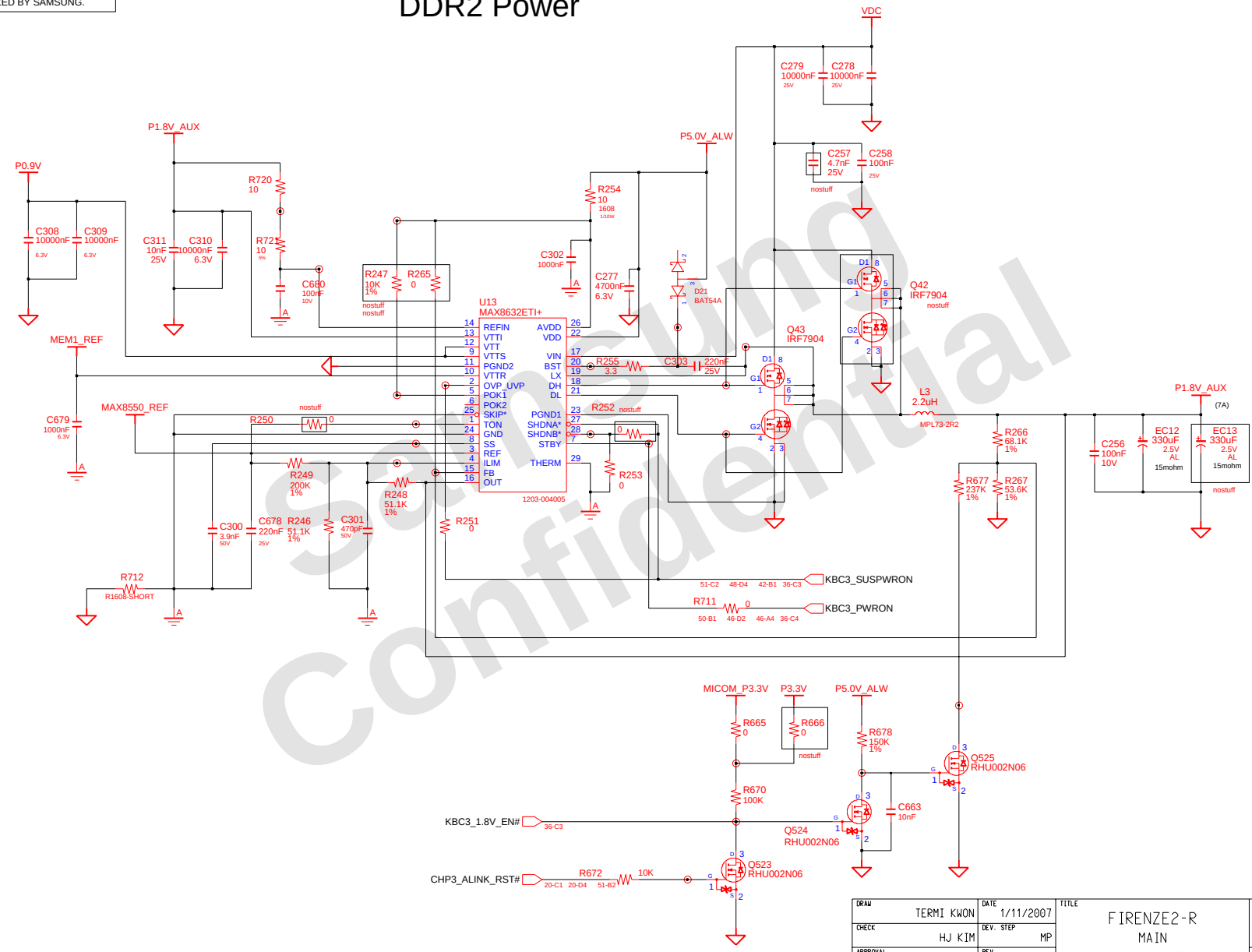
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R POWER P3.3V ALWAYS & P5V_AUX	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 42 OF 52	

P1.2V(VCC_NB) & VCCP (1.05V)



DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R POWER P1.2V & VCCP	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 43 OF 52	

DDR2 Power



DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN DDR POWER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 44 OF 52	

CPU VRM [SEMTECH]

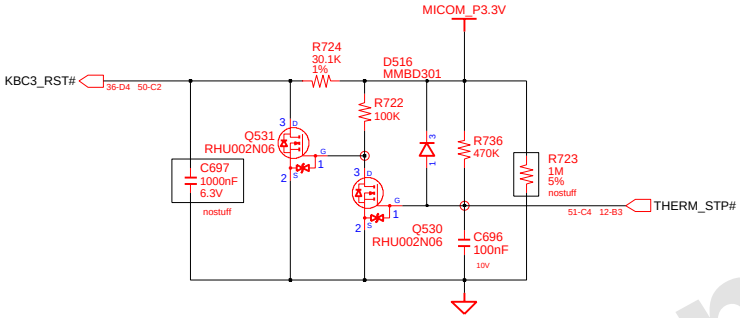
Stuff Q9, Q8, EC3, EC502, EC505
When use T7200 or higher CPU

Note : differential pairs

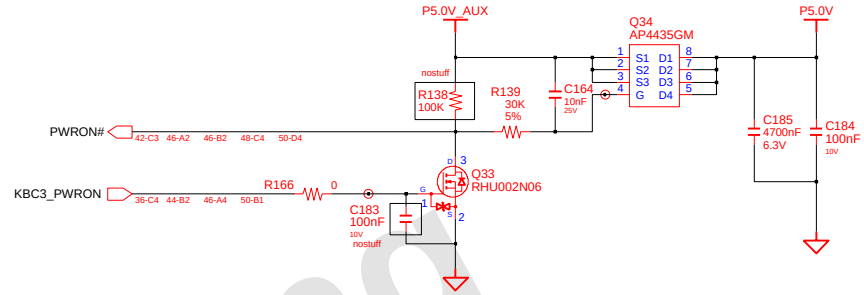
U4 SC452IMLTRT

DRAW	TERMI KWON	DATE	1/11/2007
CHECK	HJ KIM	DEV. STEP	MP
APPROVAL	SJ PARK	REV	1.0
MODULE CODE	undefined	LAST EDIT	January 11, 2007 8:27:44 PM
TITLE	FIRENZE2-R MAIN CPU POWER		
SAMSUNG ELECTRONICS	PART NO.	BA41-00714A	
PAGE	45 OF 52		

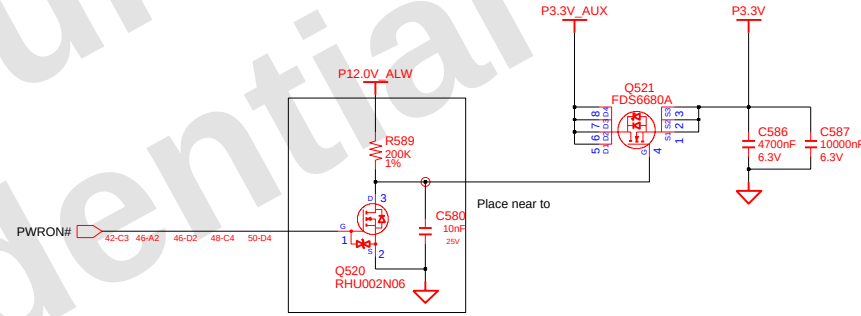
MICOM RESET



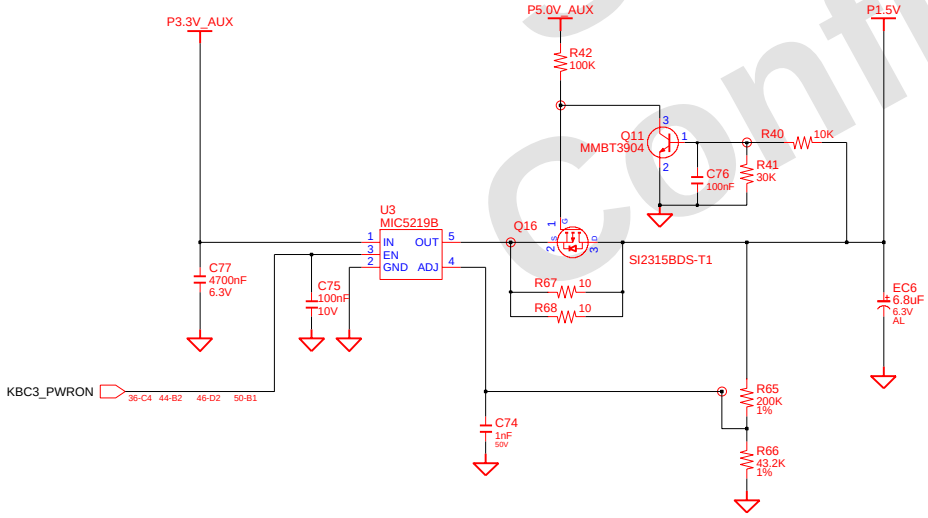
Switched Power On (P5V)

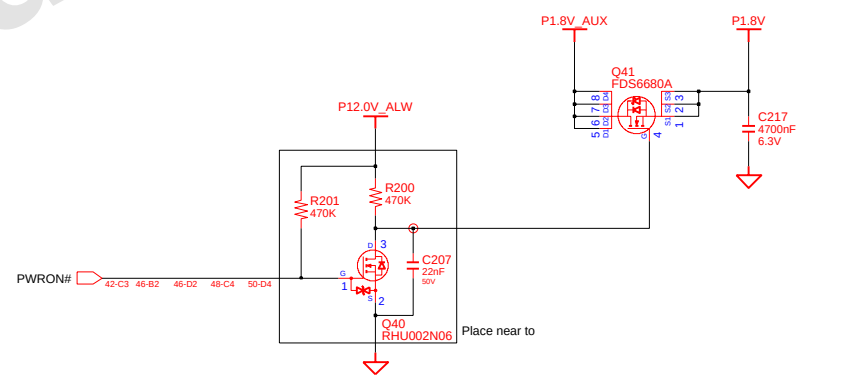


Switched Power On (P3.3V & 1.8V)

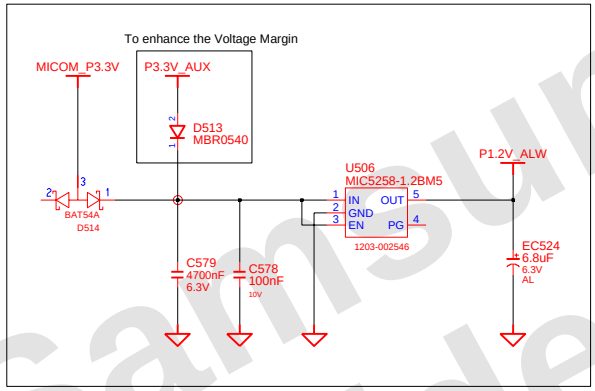


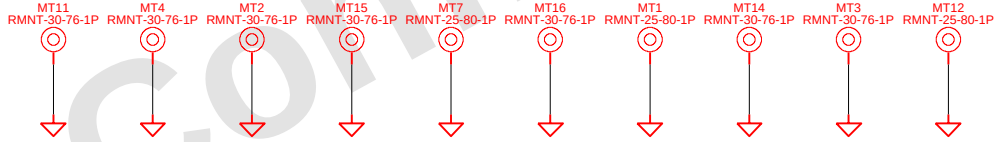
P1.5V POWER



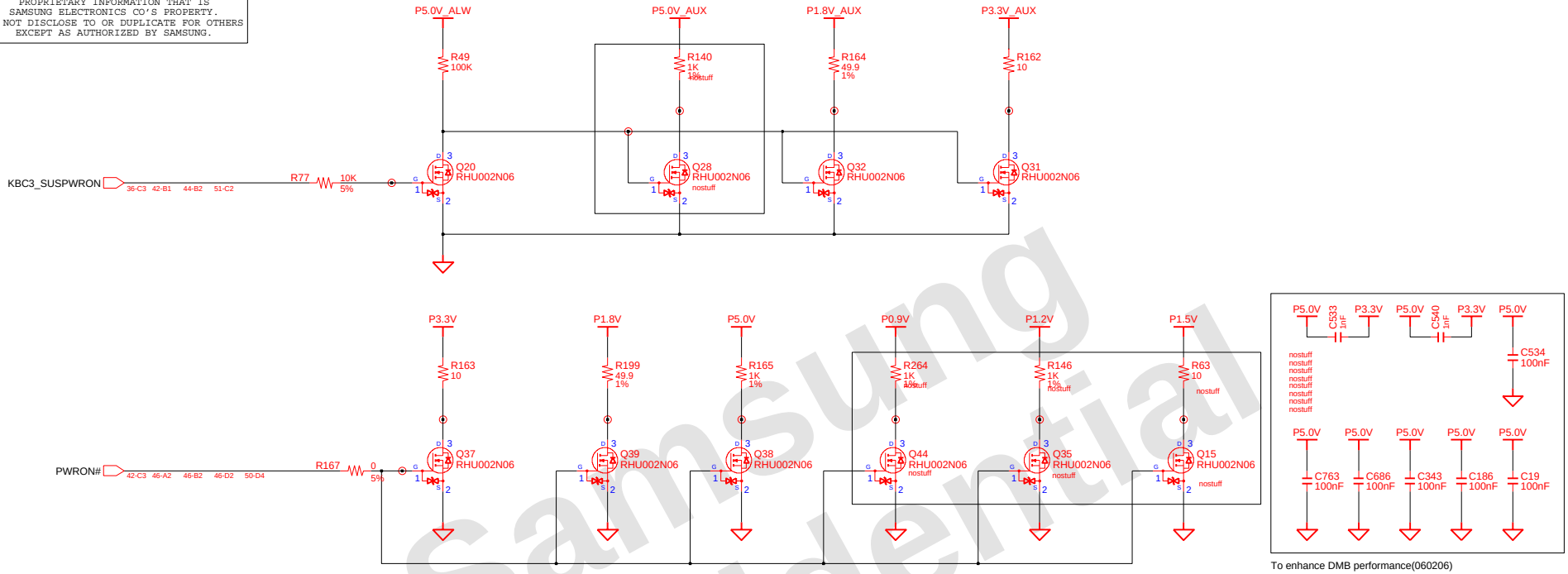


DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN MICOM & SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 46 OF 52	

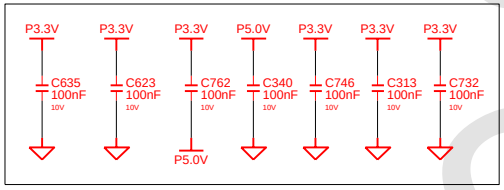




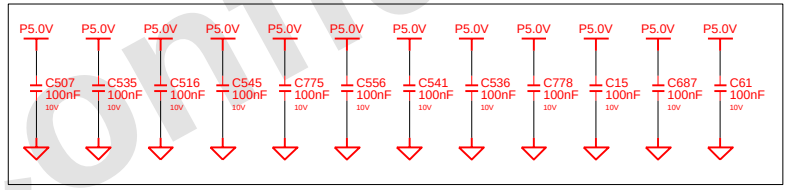
DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP	P1.2V & P2.5V AUX POWER	
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 47 OF 52	



To enhance DMB performance(060206)

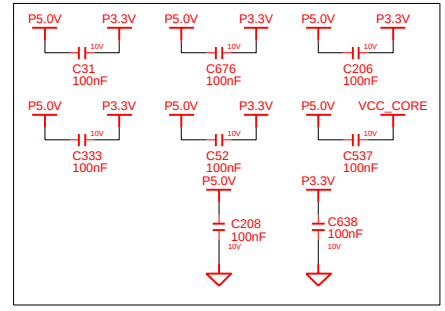


STICHING CAP



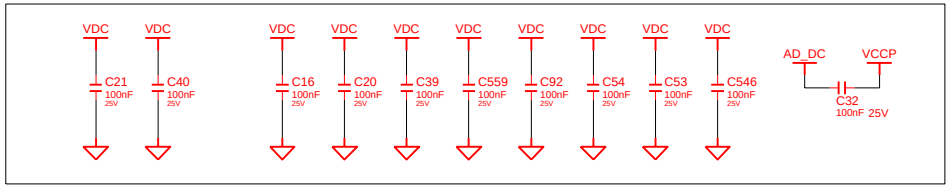
Decap for P5.0V Plane

To reduce BB noise(120 ~ 230MHz) from Power Line (2006/01/24 relate on EMI)



Stiching Cap for Power partition

To reduce BB noise(120 ~ 230MHz) from Power Partition points (2006/01/24 relate on EMI)



Decap for VDC

To reduce BB noise(120 ~ 230MHz) from Power Line (2006/01/24 relate on EMI)

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAINBD POWER ADAPT	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 48 OF 52	

REV1

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0	TP	PART NO.: BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 49 OF 52	

COEX1
COEX2
ILIM3
ILIM5
MIC1_L
MIC1_R
PWRON#
TVO3_C
TVO3_Y

ODD5_A0
ODD5_A1
ODD5_A2
PC_BEEP

AC_SDOUT
ADT3_SEL

CPU1_TCK
CPU1_TDI
CPU1_TMS
CRT3_RED

HP_OUT_L
HP_OUT_R

CLK3_ICH14
CLK3_NB14M
CLK3_USB48

CRT3_BLUE
AUX_PG

KBC3_A20G
KBC3_RST#
KBC3_VRON
KBC5_TCLK
LAN3_ACT#

CRT3_GREEN
CRT5_HSYNC
CRT5_VSYNC

ODD5_CS1#
ODD5_CS3#
ODD5_D(0)
ODD5_D(1)
ODD5_D(2)
ODD5_D(3)
ODD5_D(4)
ODD5_D(5)
ODD5_D(6)
ODD5_D(7)
ODD5_D(8)
ODD5_D(9)
ODD5_DREQ
ODD5_IOR#
ODD5_IOW#

ODD5_IRQ
PCI3_PAR
SMB3_CLK

JCK_SENS_A
KBC3_CHGEN
KBC3_PWRGD
KBC3_PWRON
KBC5_TDATA

PCI3_RST#
SMB3_DATA
VGA5_DDCC
VGA5_DDCD
WLON_LED#
AUD3_EAPD#
CBS3_A_D_2
CBS3_CCD1#
CBS3_CCD2#
CBS3_CGNT#
CBS3_CINT#
CBS3_CREQ#
CBS3_CRST#

LAN3_WAKE#

LCD3_VDDEN
LINE_OUT_L
LINE_OUT_R

CBS3_CCLK
CBS3_CPAR
CBS3_CVS1
CBS3_CVS2
CBS3_SPKR
CHP3_SPKR
CLK3_FM48

ODD5_D(10)
ODD5_D(11)
ODD5_D(12)
ODD5_D(13)
ODD5_D(14)
ODD5_D(15)
ODD5_DACK#
ODD5_IORDY
PCI3_AD(0)
PCI3_AD(1)
PCI3_AD(2)
PCI3_AD(3)

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R TP	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 50 OF 52	

- PCI3_AD(4)
- PCI3_AD(5)
- PCI3_AD(6)
- PCI3_AD(7)
- PCI3_AD(8)
- PCI3_AD(9)
- PCI3_CBE0#
- PCI3_CBE1#
- PCI3_CBE2#
- PCI3_CBE3#
- PCI3_GNT0#
- PCI3_GNT1#
- PCI3_GNT2#

- PCI3_INTA#
- PCI3_INTB#
- PCI3_INTC#
- PCI3_INTD#
- PCI3_IRDY#
- PCI3_PERR#
- PCI3_REQ0#
- PCI3_REQ1#
- PCI3_REQ2#
- PCI3_RSTF#

- PCI3_SERR#
- PCI3_STOP#
- PCI3_TRDY#

- PLT3_RSTF#
- THERM_STP#
- T_L_BUTTON
- T_R_BUTTON
- VGA3_HSYNC
- VGA3_VSYNC

- AUD5_SPK_L+
- AUD5_SPK_L-
- AUD5_SPK_R+
- AUD5_SPK_R-
- BAT3_SMCLK#
- BLT3_DETECT#
- CBS3_A_A_18
- CBS3_A_A_19
- CBS3_A_D_14
- CBS3_CAD(0)
- CBS3_CAD(1)
- CBS3_CAD(2)
- CBS3_CAD(3)
- CBS3_CAD(4)
- CBS3_CAD(5)
- CBS3_CAD(6)
- CBS3_CAD(7)
- CBS3_CAD(8)
- CBS3_CAD(9)
- CBS3_CAUDIO
- CBS3_CCBE0#
- CBS3_CCBE1#
- CBS3_CCBE2#
- CBS3_CCBE3#
- CBS3_CIRDY#
- CBS3_CPERR#
- CBS3_CSERR#
- CBS3_CSTOP#
- CBS3_CTRDY#
- CBS3_MD_CLK
- CBS3_VPPEN0
- CBS3_VPPEN1

- CHP3_NBRST#

- CHP3_OVERT#
- CHP3_SBPME#
- CHP3_SERIRQ
- CHP3_SLPS3#
- CHP3_SLPS5#
- 25M_XTAL1
- 25M_XTAL2
- AUD3_GPIO1#
- CHP3_SATALED#
- RTC_CLK
- SPI3_CLK
- SPI3_CS#
- SPI3_MISO
- SPI3_MOSI

- CLK3_PCLKCB
- CLK3_PWRGD#

- CPU1_VID(0)
- CPU1_VID(1)
- CPU1_VID(2)
- CPU1_VID(3)
- CPU1_VID(4)
- CPU1_VID(5)
- CPU1_VID(6)
- CRT3_DDCCLK

- KBC3_BKLTON
- KBC3_SCLED#
- KBC3_SMCLK#
- KBC5_KSI(0)
- KBC5_KSI(1)
- KBC5_KSI(2)
- KBC5_KSI(3)
- KBC5_KSI(4)
- KBC5_KSI(5)
- KBC5_KSI(6)
- KBC5_KSI(7)
- KBC5_KSO(0)
- KBC5_KSO(1)
- KBC5_KSO(2)
- KBC5_KSO(3)
- KBC5_KSO(4)
- KBC5_KSO(5)
- KBC5_KSO(6)
- KBC5_KSO(7)
- KBC5_KSO(8)
- KBC5_KSO(9)

- LPC3_LAD(0)
- LPC3_LAD(1)
- LPC3_LAD(2)
- LPC3_LAD(3)

- OTP3_OVERT#
- PCI3_AD(10)

- PCI3_AD(11)
- PCI3_AD(12)
- PCI3_AD(13)
- PCI3_AD(14)
- PCI3_AD(15)
- PCI3_AD(16)
- PCI3_AD(17)
- PCI3_AD(18)
- PCI3_AD(19)
- PCI3_AD(20)
- PCI3_AD(21)
- PCI3_AD(22)
- PCI3_AD(23)
- PCI3_AD(24)
- PCI3_AD(25)
- PCI3_AD(26)
- PCI3_AD(27)
- PCI3_AD(28)
- PCI3_AD(29)
- PCI3_AD(30)
- PCI3_AD(31)
- PCI3_FRAME#
- PCI3_PLOCK#
- THRM_ALERT#
- VCCP3_PWRGD
- BAT3_DETECT#
- BAT3_SMDATA#
- CBS3_CAD(10)
- CBS3_CAD(11)
- CBS3_CAD(12)
- CBS3_CAD(13)
- CBS3_CAD(14)
- CBS3_CAD(15)
- CBS3_CAD(16)
- CBS3_CAD(17)
- CBS3_CAD(18)
- CBS3_CAD(19)
- CBS3_CAD(20)
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- CBS3_CAD(23)
- CBS3_CAD(24)
- CBS3_CAD(25)
- CBS3_CAD(26)
- CBS3_CAD(27)
- CBS3_CAD(28)
- CBS3_CAD(29)
- CBS3_CAD(30)
- CBS3_CAD(31)
- CBS3_CFRAME#
- CBS3_CSTSCHG
- CBS3_VCC3EN#
- CBS3_VCCSEN#
- CHP3_AZ_SDI0
- CHP3_AZ_SDI1
- CHP3_BIOSWP#
- CHP3_CPUSTP#
- KBC3_NBPWRGD

- CLK3_33M_MIN

- CLK3_PCLKLAN
- STRAP_USB48

- CPU1_CPURST#
- CPU1_BREQ#
- CPU1_BSEL0
- CPU1_BSEL1
- CPU1_BSEL2
- CPU1_DPRSTP#
- CPU1_DPSLP#
- CPU1_FERR#
- CPU1_SLP#
- CPU1_TRST#

- CPU1_STPCLK#
- CPU2_THERMDA
- CPU2_THERMDC
- CRT3_DDCDATA
- ITP3_SYSRST#
- ITP3_DBRESET#
- JCK_SENS_HP#

- KBC3_CPURST#
- KBC3_EXTSMI#
- KBC3_FANCTRL
- KBC3_NUMLED#
- KBC3_PWRBTN#
- KBC3_RSMRST#
- KBC3_RUNSCI#
- KBC3_SMDATA#
- KBC5_KSO(10)
- KBC5_KSO(11)
- KBC5_KSO(12)
- KBC5_KSO(13)
- KBC5_KSO(14)
- KBC5_KSO(15)

- LID3_SWITCH#
- LPC3_LFRAME#

- MIC1_VREFO_L
- MIC1_VREFO_R
- MIO3_BUTTON#
- PCI3_CLKRUN#
- PCI3_DEVSEL#
- CBS3_CCLKRUN#
- CBS3_CDEVSEL#
- CBS3_MD_DATA1
- CBS3_MD_DATA2
- CBS3_MD_DATA3
- CBS3_MD_VCCEN

- CHP3_DPRSLPVR
- CHP3_SUSSTAT#

- CPU1_PWRGDCPU
- CPU1_VCCSENSE
- CPU1_VSSSENSE
- JCK_SENS_MIC#
- KBC3_CAPSLED#
- KBC3_SUSPWRON
- KBC3_WAKESCI#
- LAN3_LINK_10#
- LCD3_BKLTCTRL
- LCD3_BKLTEN
- LCD3_BKLTON

- CBS3_MD_XD_ALE
- CBS3_MD_XD_CE#
- CBS3_MD_XD_CLE
- CBS3_MD_XD_WP#

- CLK3_PCLKMICOM
- CPU1_THRMTRIP#
- KBC3_LED_ACIN#
- LAN3_LINK_100#
- VRM3_CPU_PWRGD
- CHP3_ALINK_RST#
- CHP3_AZ_AUD_SDO
- CHP3_AZ_MDC_SDO

- KBC3_LED_POWER#
- CBS3_MD_DATA4_XD
- CBS3_MD_DATA5_XD
- CBS3_MD_DATA6_XD
- CBS3_MD_DATA7_XD
- CHP3_AZ_AUD_BCLK
- CHP3_AZ_AUD_RST#
- CHP3_AZ_AUD_SYNC
- CHP3_AZ_MDC_BCLK
- CHP3_AZ_MDC_RST#
- CHP3_AZ_MDC_SYNC
- CHP3_SBTHRMTRIP#
- KBC3_LED_CHARGE#
- KBC3_THERM_SMCLK
- CBS3_MS_BS_SD_CMD
- KBC3_THERM_SMDATA
- CBS3_SD_CD#_XD_CD#
- CBS3_MS_INS#_XD_CD#
- CBS3_SD_WP#_XD_R_B#
- CBS3_MD_DATA0_MS_SDIO

- AVDD_AUD
- AVDD_AUD

- AD_DC
- AD_DC
- AD_DC
- AD_DC
- AD_DC
- AVDDQ

- AMP_VDD
- AMP_VDD

- AVDD

- AGND_AUD
- AGND_AUD
- AGND_AUD
- AGND_AUD
- AGND_AUD
- AGND_CHG

- AGND_P3.3V

- CGND

- C_AGND

- CB_VCCA

- CB_VPPA

- CHG_REF

- CB_MD_VCC

- D_AGND

- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND

- INV_VDC
- INV_VDC

- LCD_VDD3V
- LCD_VDD3V

- LDO_P5.4V

- MEM1_REF

- MAX8550_REF

- MICOM_P3.3V
- MICOM_P3.3V

- P0.9V
- P0.9V
- P0.9V
- P0.9V
- P0.9V
- P1.2V
- P1.2V
- P1.2V
- P1.2V
- P1.2V
- P1.5V
- P1.5V

- P1.8V
- P1.8V
- P1.8V
- P1.8V
- P1.8V
- P3.3V

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R TP	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
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P3.3V
P3.3V
P3.3V
P3.3V
P5.0V
P5.0V
P5.0V
P5.0V
P5.0V
PLLVDD18

VCC_CRT

VCC_CORE
VCC_CORE
VCC_CORE
VCC_CORE
VCC_CORE

C1 0.1nF
C2 0.01nF 0.5pF
C3 0.018nF
C4 0.022nF
C5 0.027nF
C6 0.047nF
C7 0.0033nF

PRTC_BAT
P1.2V_ALW

C500 0.1nF
C501 0.01nF 0.5pF
C502 0.018nF
C503 0.022nF
C504 0.027nF
C505 0.047nF
C506 0.0033nF

P1.8V_AUX
P1.8V_AUX
P1.8V_AUX
P1.8V_AUX
P1.8V_AUX
P2.5V_LAN
P2.5V_LAN
P2.5V_LAN
P2.5V_LAN
P2.5V_LAN
P3.3V_AUX
P3.3V_AUX
P3.3V_AUX
P3.3V_AUX
P3.3V_AUX
P5.0V_ALW
P5.0V_ALW
P5.0V_ALW
P5.0V_ALW
P5.0V_ALW
P5.0V_AUX
P5.0V_AUX
P5.0V_AUX
P5.0V_AUX
P5.0V_AUX

PCIE_VDDR

P12.0V_ALW
P12.0V_ALW
P12.0V_ALW
P12.0V_ALW
P12.0V_ALW
VDC
VDC
VDC
VDC
VDC
VCCP
VCCP
VCCP
VCCP
VCCP

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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