

PRAHA (SRI)

CPU : **Intel Merom (800MHz)**
 Chip Set : RS600ME & SB600
 Remarks : Mobility Platform

Model Name : PRAHA
 PBA Name : MAIN
 PCB Code : TPT : BA41-00791A
 GCE : BA41-00792A
 NAN : BA41-00811A
 Dev. Step : MP1.0 (8-Layer)
 Revision : 1.0
 T.R. Date : 2007.07.02

DRAW	CHECK	APPROVAL

■ **Owner : SEC Mobile R & D** **Signature :** **X**

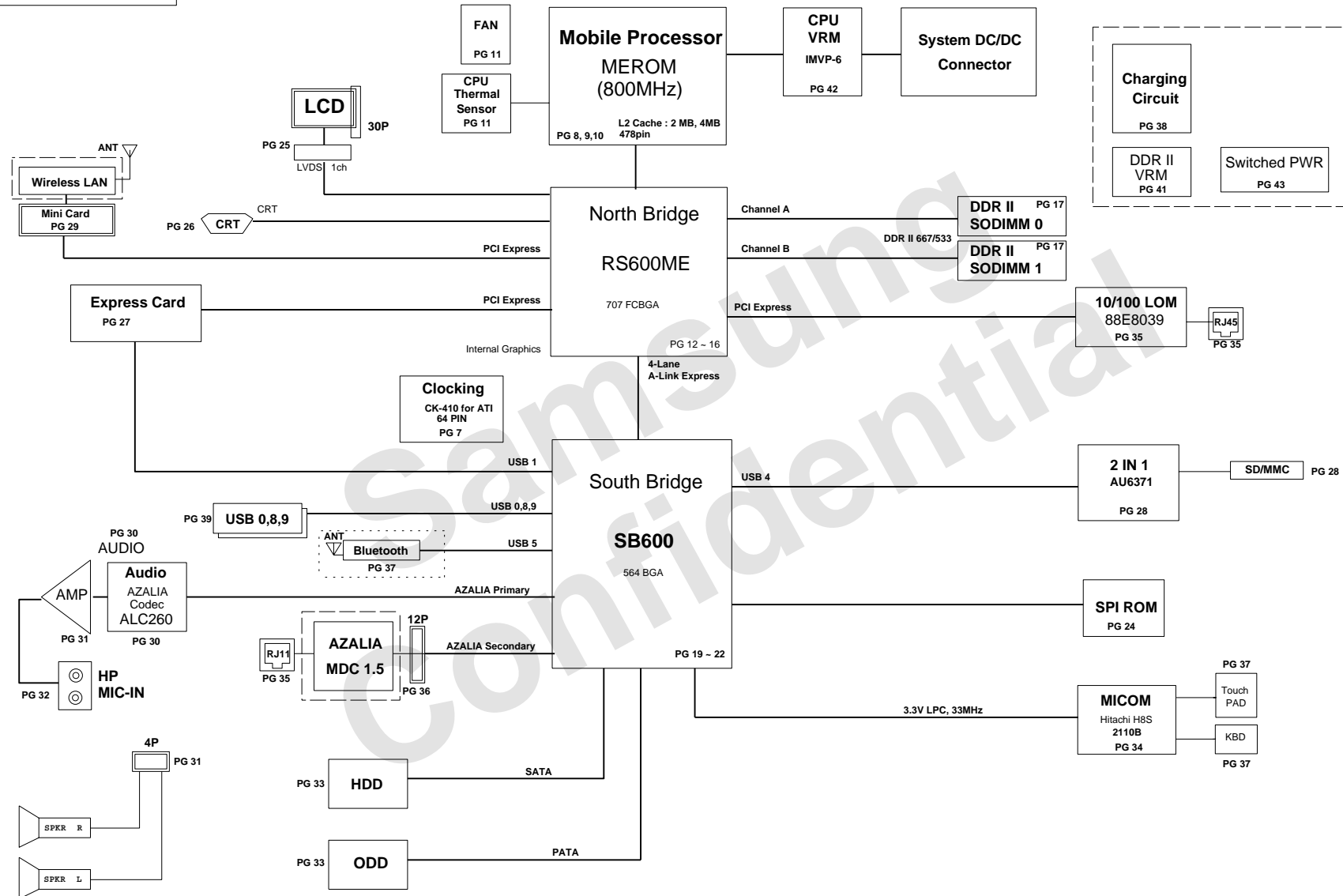
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USE ICT PORT

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	COVER	PART NO.	
APPROVAL	SJ PARK	REV	1.0		BA41-00791A	
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	1	OF 47

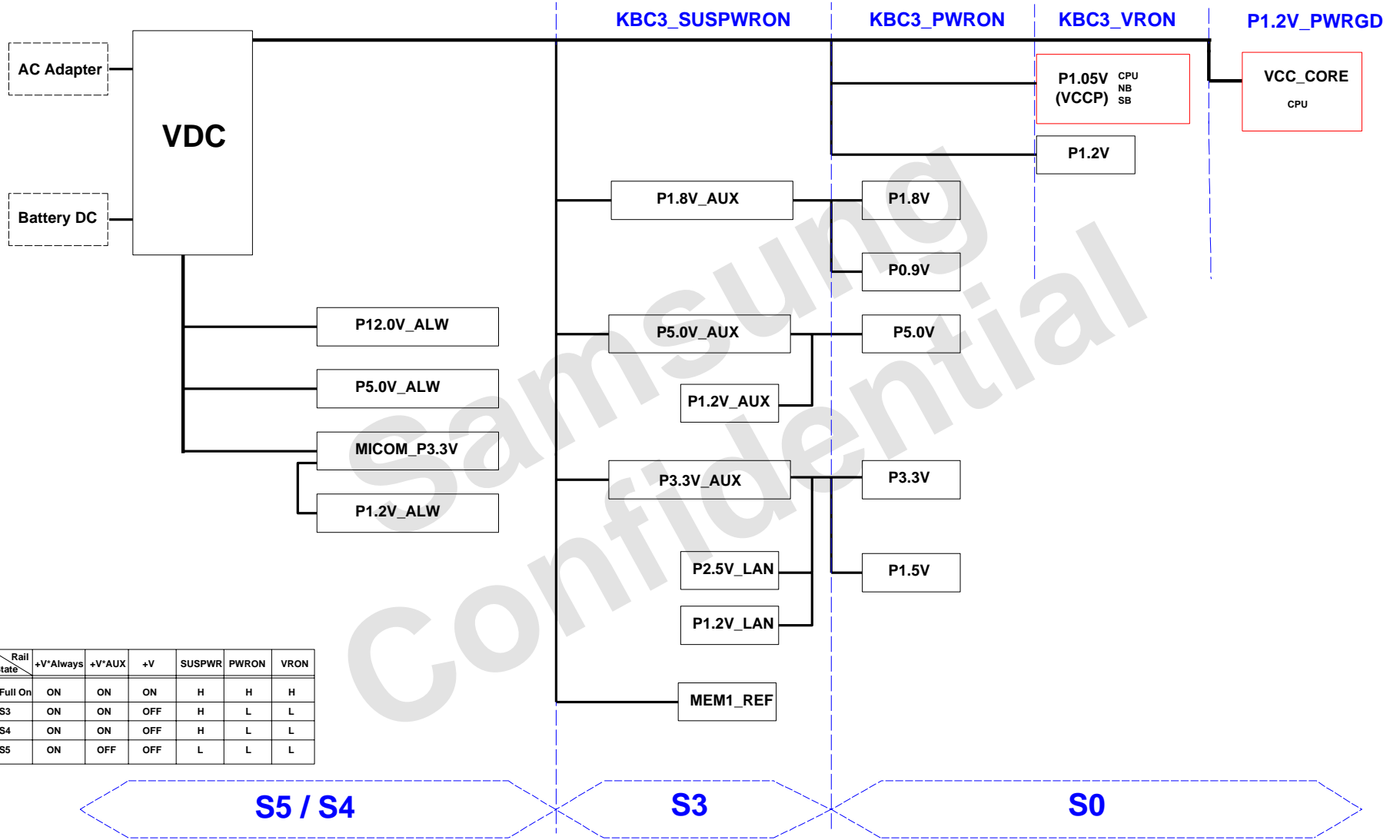
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DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	OPERATION BLOCK DIAGRAM		
APPROVAL	SJ PARK	REV	1.0	PART NO. BA41-00791A		PAGE 2 OF 47
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM			

Power Diagram

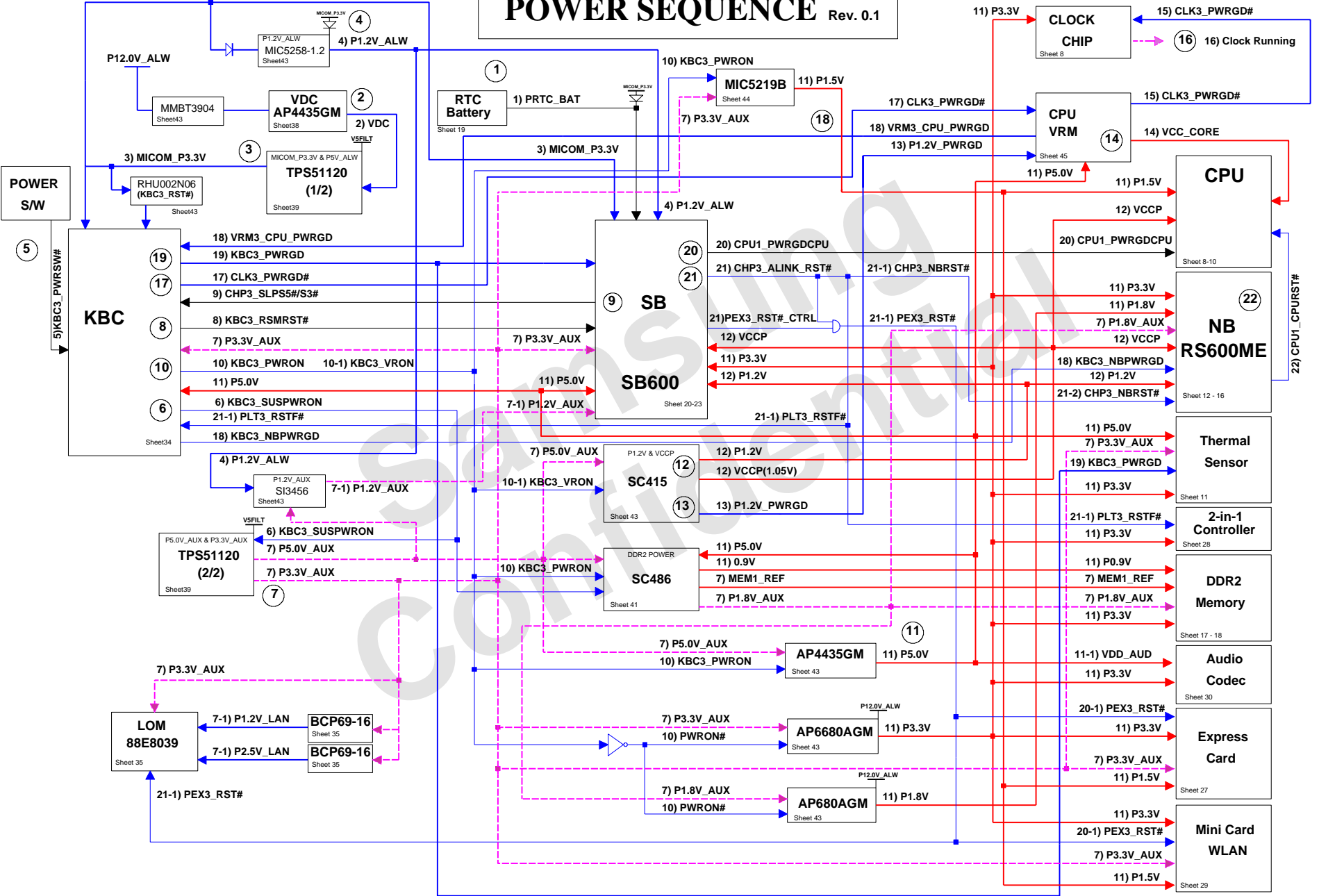
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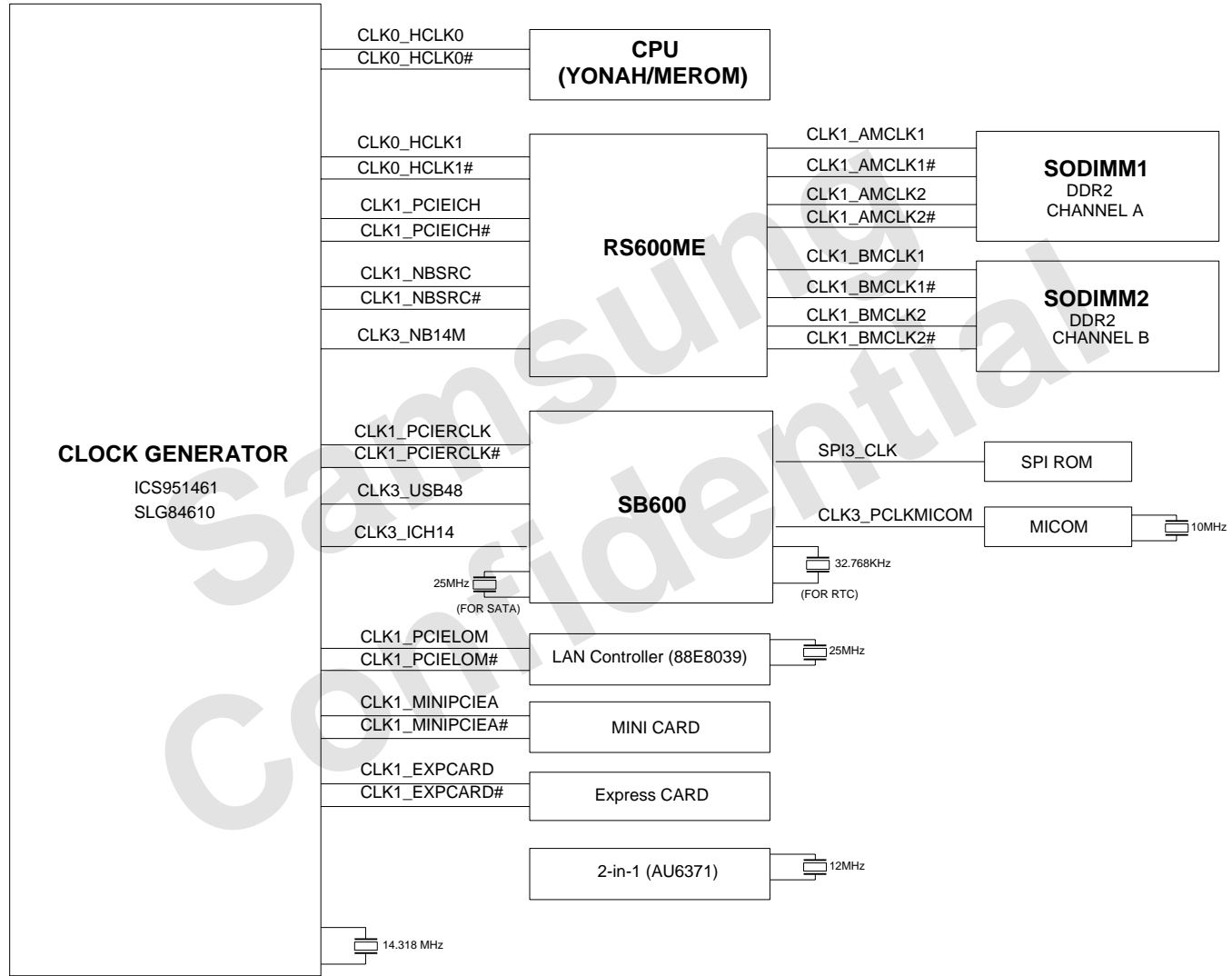
Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	MAIN	PART NO.	
APPROVAL	SJ PARK	REV	1.0	POWER DIAGRAM	BA41-00791A	
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	3 OF 47	

POWER SEQUENCE Rev. 0.1



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DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) CLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	PART NO.		
APPROVAL	SJ PARK	REV	1.0	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 5 OF 47
MODULE CODE						

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
USB	AD30(internal)		
Hub to PCI	AD31(internal)		
LPC bridge/IDE/AC97/SMBUS	AD31(internal)		
Internal MAC	AD31(internal)		
AC Link	-		

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for YONAH (0~1.5V)
VCCP	YONAH Processor System Bus(PSB) Termination (1.05V)
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P1.8V_ALWS	1.8V power rail (Always On)
P2.5V_LAN	2.5V power rail (off in S4-S5)
MICOM_P3.3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P5.0V_ALWS	5.0V power rail (Always On)
P12V_ALWS	12V power rail (Always On)

I²C / SMB Address

Devices	Address	Hex	Bus
SB600	Master	-	SMBUS Master
SODIMM0	1010 0100	A4h	
SODIMM1	1010 0110	A6h	
CK-410 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	Left side USB Port
1	USB Express Card
4	2-in-1 Memory Card
5	Bluetooth
8, 9	Rear side USB Port

System Power States

- CHP3_SLPS1* S1, Powered-On-Suspend(POS)** : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- CHP3_SLPS3* S3, Suspend-To-RAM(STR)** : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLPS4* S4, Suspend-To-Disk(STD)** : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3_SLPS5* S5, Soft Off(SOFF)** : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB600	Real Time Clock
Crystal	25MHz	SB600	SATA
Crystal	10MHz	MICOM	H8S-2110B
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	25MHz	LAN	LOM
Crystal	12MHz	2-in-1	2-in-1 (SD/MMC)

CPU Core Voltage Table

IMVP-6

Active Mode			Active/Deeper Sleep Dual Mode Region			Deeper Sleep/Extended Deeper Sleep Dual Mode Region		
VID(6:0)	Voltage		VID(6:0)	Voltage		VID(6:0)	Voltage	
0 0 0 0 0 0 0	1.5000 V		0 1 0 1 0 0 0	1.0000 V		1 0 1 0 0 0 1	0.4875 V	
0 0 0 0 0 0 1	1.4875 V		0 1 0 1 0 0 1	0.9875 V		1 0 1 0 0 1 0	0.4750 V	
0 0 0 0 0 1 0	1.4750 V		0 1 0 1 0 1 0	0.9750 V		1 1 1 0 0 1 1	0.4625 V	
0 0 0 0 0 1 1	1.4625 V		0 1 0 1 0 1 1	0.9625 V		1 0 1 0 1 0 0	0.4500 V	
0 0 0 0 1 0 0	1.4500 V		0 1 0 1 1 0 0	0.9500 V		1 0 1 0 1 0 1	0.4375 V	
0 0 0 0 1 0 1	1.4375 V		0 1 0 1 1 0 1	0.9375 V		1 0 1 0 1 1 0	0.4250 V	
0 0 0 0 1 1 0	1.4250 V		0 1 0 1 1 0 1	0.9250 V		1 1 0 1 0 1 1	0.4125 V	
0 0 0 0 1 1 1	1.4125 V		0 1 0 1 1 1 1	0.9125 V		1 0 1 1 0 0 0	0.4000 V	
0 0 0 1 0 0 0	1.4000 V		0 1 1 0 0 0 0	0.9000 V		1 0 1 1 0 0 1	0.3875 V	
0 0 0 1 0 0 1	1.3875 V		0 1 1 0 0 0 1	0.8875 V		1 0 1 1 0 1 0	0.3750 V	
0 0 0 1 0 1 0	1.3750 V		0 1 1 0 0 1 0	0.8750 V		1 0 1 1 0 1 1	0.3625 V	
0 0 0 1 0 1 1	1.3625 V		0 1 1 0 0 1 1	0.8625 V		1 0 1 1 1 0 0	0.3500 V	
0 0 0 1 1 0 0	1.3500 V		0 1 1 0 1 0 0	0.8500 V		1 0 1 1 1 0 1	0.3375 V	
0 0 0 1 1 0 1	1.3375 V		0 1 1 0 1 0 1	0.8375 V		1 0 1 1 1 1 0	0.3250 V	
0 0 0 1 1 1 0	1.3250 V		0 1 1 0 1 1 0	0.8250 V		1 0 1 1 1 1 1	0.3125 V	
0 0 0 1 1 1 1	1.3125 V		0 1 1 0 1 1 1	0.8125 V		1 1 1 0 0 0 0	0.3000 V	
0 0 1 0 0 0 0	1.3000 V		0 1 1 1 0 0 0	0.8000 V		1 1 1 0 0 0 1	0.2875 V	
0 0 1 0 0 0 1	1.2875 V		0 1 1 1 0 0 1	0.7875 V		1 1 1 0 0 1 0	0.2750 V	
0 0 1 0 0 1 0	1.2750 V		0 1 1 1 0 1 0	0.7750 V		1 1 1 0 0 1 1	0.2625 V	
0 0 1 0 0 1 1	1.2625 V		0 1 1 1 1 0 1	0.7625 V		1 1 1 0 0 1 1	0.2500 V	
0 0 1 0 1 0 0	1.2500 V		0 1 1 1 1 0 1	0.7500 V		1 1 1 0 0 1 1	0.2375 V	
0 0 1 0 1 0 1	1.2375 V		0 1 1 1 1 0 1	0.7375 V		1 1 1 0 0 1 1	0.2250 V	
0 0 1 0 1 1 0	1.2250 V		0 1 1 1 1 1 0	0.7250 V		1 1 1 0 0 1 1	0.2125 V	
0 0 1 0 1 1 1	1.2125 V		0 1 1 1 1 1 1	0.7125 V		1 1 1 0 1 0 0	0.2000 V	
0 0 1 1 0 0 0	1.2000 V		1 0 0 0 0 0 0	0.7000 V		1 1 1 0 1 0 1	0.1875 V	
0 0 1 1 0 0 1	1.1875 V		1 0 0 0 0 0 1	0.6875 V		1 1 1 0 1 0 1	0.1750 V	
0 0 1 1 0 1 0	1.1750 V		1 0 0 0 0 1 0	0.6750 V		1 1 1 0 1 0 1	0.1625 V	
0 0 1 1 0 1 1	1.1625 V		1 0 0 0 0 1 1	0.6625 V		1 1 1 0 1 1 0	0.1500 V	
0 0 1 1 1 0 0	1.1500 V		1 0 0 0 1 0 0	0.6500 V		1 1 1 0 1 1 0	0.1375 V	
0 0 1 1 1 0 1	1.1375 V		1 0 0 0 1 0 1	0.6375 V		1 1 1 0 1 1 1	0.1250 V	
0 0 1 1 1 1 0	1.1250 V		1 0 0 0 1 1 0	0.6250 V		1 1 1 0 1 1 1	0.1125 V	
0 0 1 1 1 1 1	1.1125 V		1 0 0 0 1 1 1	0.6125 V		1 1 1 0 1 0 0	0.1000 V	
0 1 0 0 0 0 0	1.1000 V		1 0 0 1 0 0 0	0.6000 V		1 1 1 0 0 0 1	0.0875 V	
0 1 0 0 0 0 1	1.0875 V		1 0 0 1 0 0 1	0.5875 V		1 1 1 0 0 1 0	0.0750 V	
0 1 0 0 0 1 0	1.0750 V		1 0 0 1 0 1 0	0.5750 V		1 1 1 0 0 1 1	0.0625 V	
0 1 0 0 0 1 1	1.0625 V		1 0 0 1 0 1 1	0.5625 V		1 1 1 0 1 0 0	0.0500 V	
0 1 0 0 1 0 0	1.0500 V		1 0 0 1 1 0 0	0.5500 V		1 1 1 0 1 0 1	0.0375 V	
0 1 0 0 1 0 1	1.0375 V		1 0 0 1 1 0 1	0.5375 V		1 1 1 0 1 0 1	0.0250 V	
0 1 0 0 1 1 0	1.0250 V		1 0 0 1 1 1 0	0.5250 V		1 1 1 0 1 0 1	0.0125 V	
0 1 0 0 1 1 1	1.0125 V		1 0 0 1 1 1 1	0.5125 V		1 1 1 1 0 0 0	0.0000 V	
0 1 0 1 0 0 0	0.5000 V		1 0 1 0 0 0 0	0.5000 V		1 1 1 1 0 0 1	0.0000 V	
			1 0 1 0 0 0 1	0.0000 V		1 1 1 1 0 1 0	0.0000 V	
			1 1 1 1 0 0 0	0.0000 V		1 1 1 1 0 1 0	0.0000 V	
			1 1 1 1 0 0 1	0.0000 V		1 1 1 1 1 0 0	0.0000 V	
			1 1 1 1 1 0 0	0.0000 V		1 1 1 1 1 0 1	0.0000 V	
			1 1 1 1 1 0 1	0.0000 V		1 1 1 1 1 1 0	0.0000 V	
			1 1 1 1 1 1 0	0.0000 V		1 1 1 1 1 1 1	0.0000 V	
			1 1 1 1 1 1 1	0.0000 V		1 1 1 1 1 1 1	0.0000 V	

Active Deeper Slp

DPRSLPVR 0 DPRSLPVR 1

DPRSTP* 1 DPRSTP* 0

PSI2* 0 or 1 PSI2* 0 or 1

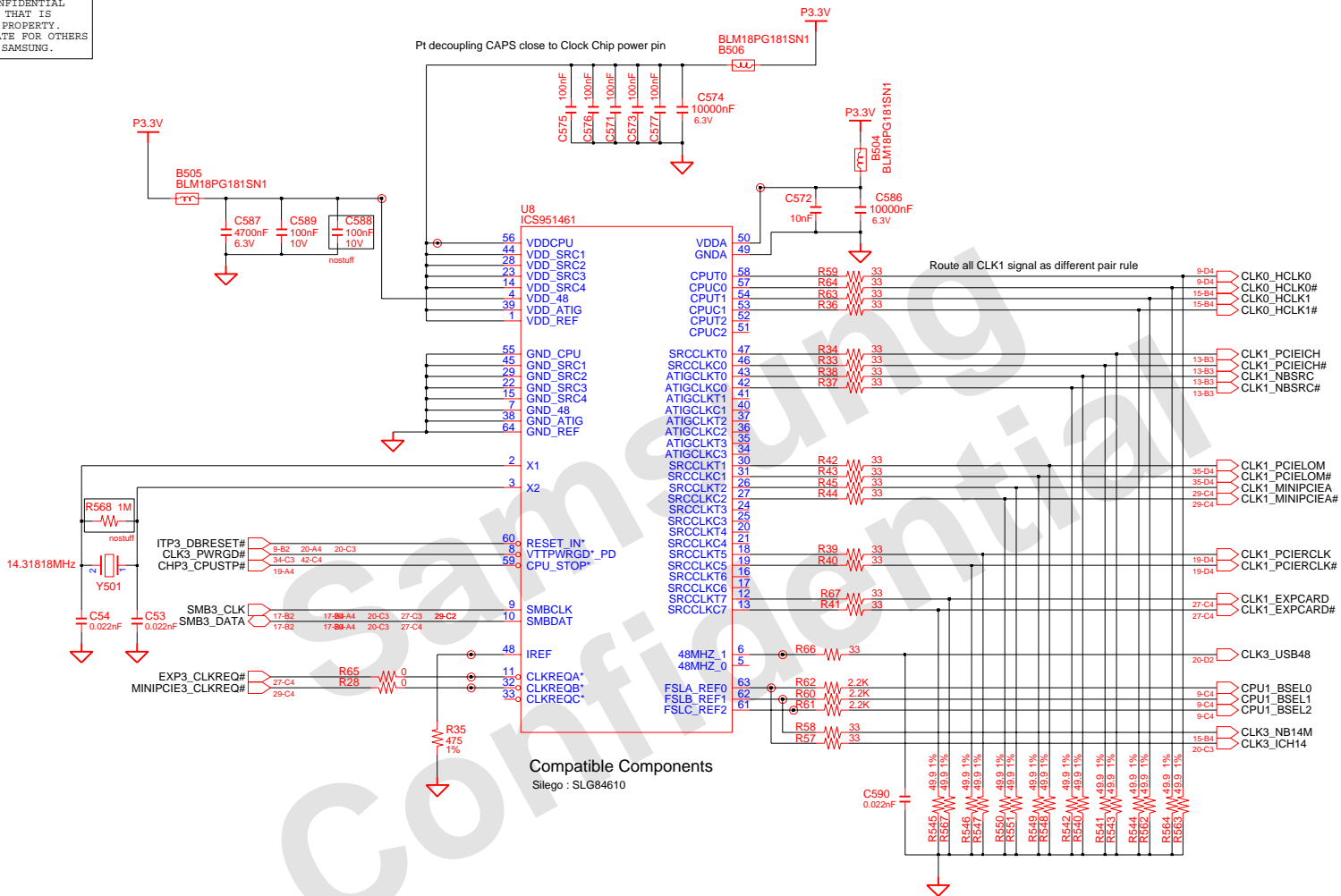
**11111111* : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		MAIN	
APPROVAL	SJ PARK	REV	1.0	BOARD INFORMATION		PART NO. BA41-00791A
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	6	OF 47

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Compatible Components
Silego : SLG84610

Place all te serias termination resistor as close as Clock Chip as possible

FSA, FSB, FSC of Clock chip are low threshold inputs
 $V_{ih_fs_min} = 0.7V$
 $V_{il_fs_max} = 0.35V$

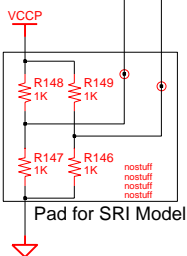
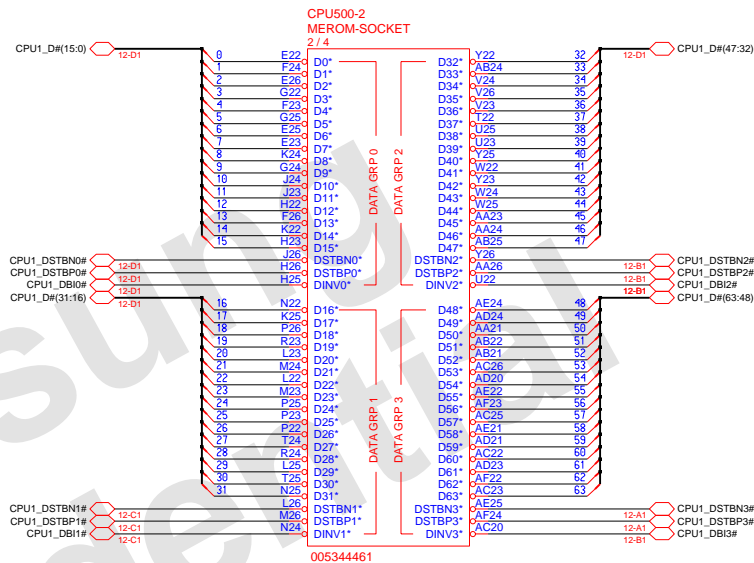
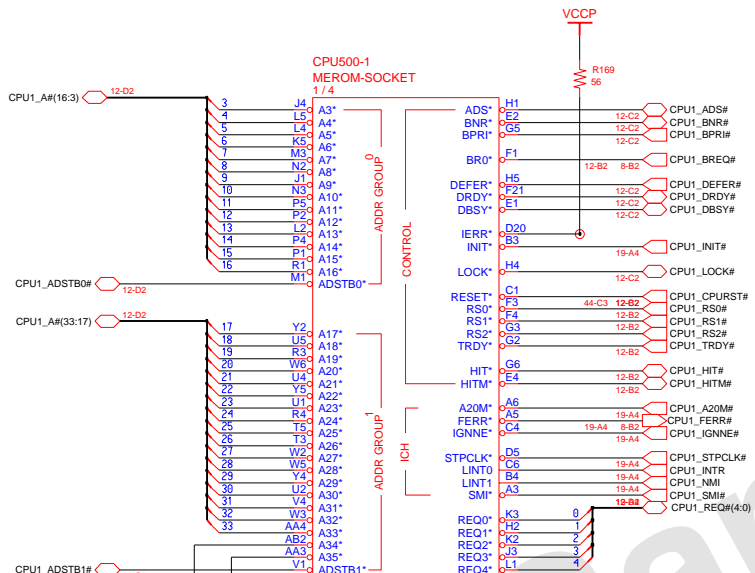
CPU	FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD

Merom 800MHz
 Celeron 533MHz
 Merom 667MHz

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		MAIN	
APPROVAL	SJ PARK	REV	1.0		CLOCK GENERATOR	PART NO. BA41-00791A
MODULE CODE		LAST EDIT				

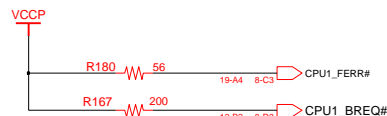
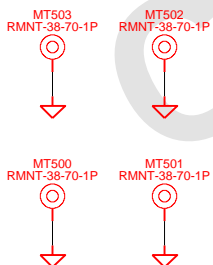
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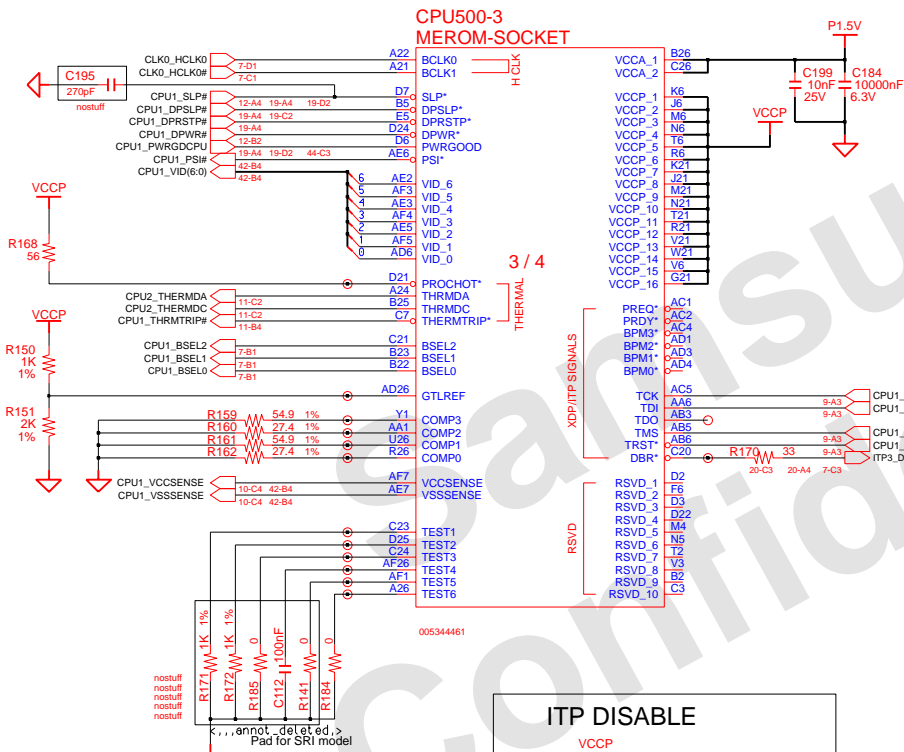


**NOTE

CPU Bracket Hole



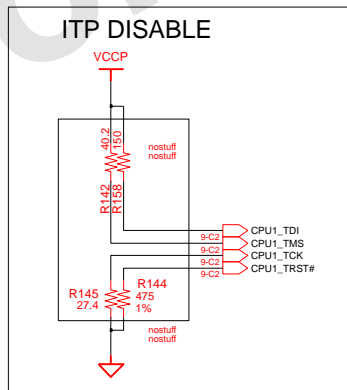
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN MEROM CPU (1/3)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 8 OF 47		
					PART NO.	BA41-00791A



GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.



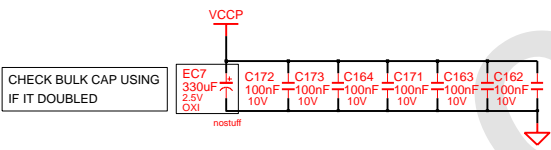
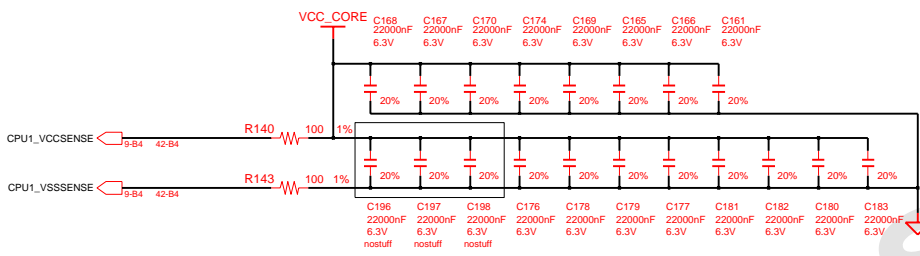
CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 0	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 0 1	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 0	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 1 0 0 0	1.4125 V	0 1 1 0 1 0 0	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 1	1.4000 V	0 1 1 0 1 0 1	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 1 0	1.3875 V	0 1 1 0 1 1 0	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 1	1.3750 V	0 1 1 0 1 1 1	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 1 0 0	1.3625 V	0 1 1 1 0 0 0	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 1	1.3500 V	0 1 1 1 0 0 1	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 1 0	1.3375 V	0 1 1 1 0 1 0	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 1	1.3250 V	0 1 1 1 0 1 1	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 1 0 0 0 0	1.3125 V	0 1 1 1 1 0 0	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 1	1.3000 V	0 1 1 1 1 0 1	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 1 0	1.2875 V	0 1 1 1 1 1 0	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 1	1.2750 V	0 1 1 1 1 1 1	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 1 0 0	1.2625 V	0 1 1 1 1 0 0	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 1	1.2500 V	0 1 1 1 1 0 1	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 1 0	1.2375 V	0 1 1 1 1 1 0	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 1	1.2250 V	0 1 1 1 1 1 1	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 1 0 0 0	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 1	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 1 0	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 1	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 1 0 0	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 1	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 1 0	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 1	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 1 0 0 0 0 0	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 1	1.1000 V	1 0 0 0 1 1 1	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 1 0	1.0875 V	1 0 0 1 0 0 0	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 1	1.0750 V	1 0 0 1 0 0 1	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 1 0 0	1.0625 V	1 0 0 1 0 1 0	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 1	1.0500 V	1 0 0 1 0 1 1	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 1 0	1.0375 V	1 0 0 1 1 0 0	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 1	1.0250 V	1 0 0 1 1 0 1	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 1 0 0 0	1.0125 V	1 0 0 1 1 1 0	0.5125 V	1 1 1 1 0 0 0	0.0000 V
0 1 0 1 0 0 1	1.0125 V	1 0 0 1 1 1 1	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

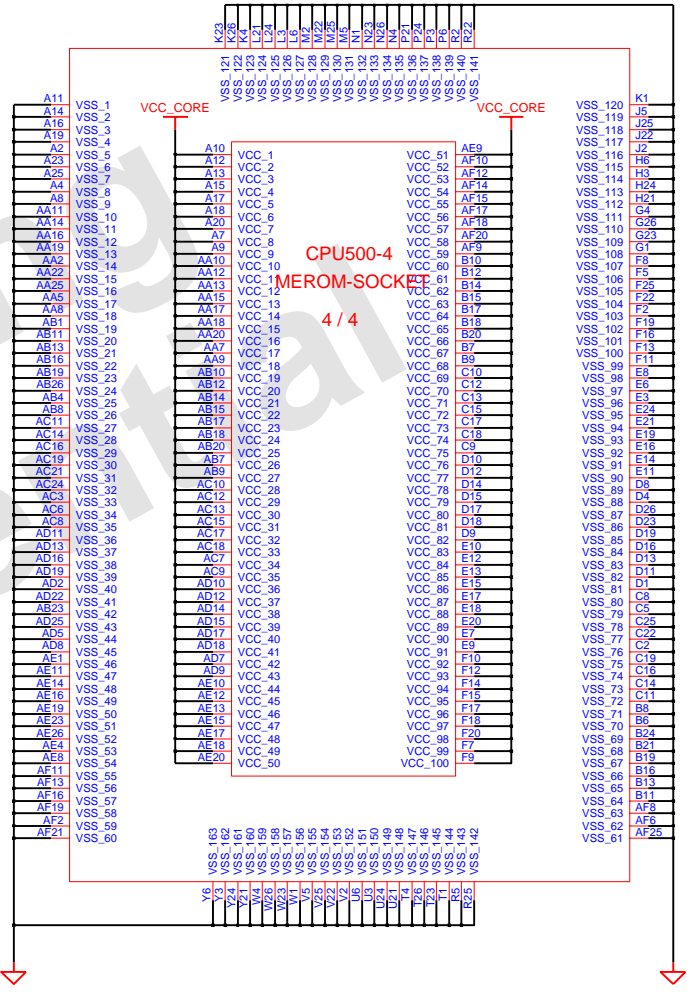
*Yonah Processor (2.33 GHz / 800 MHz : TBD)

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Deleted 13 De-cap (Only use 19pcs out of 32)

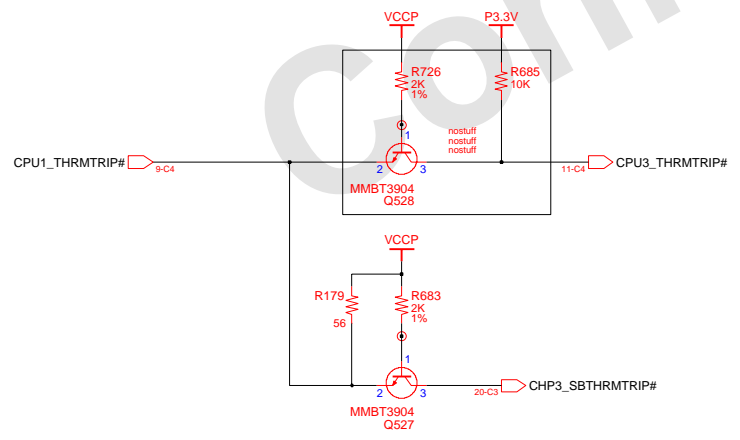
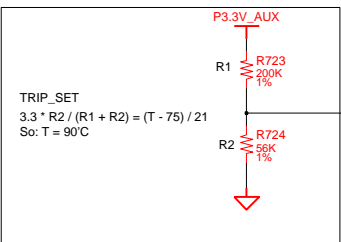
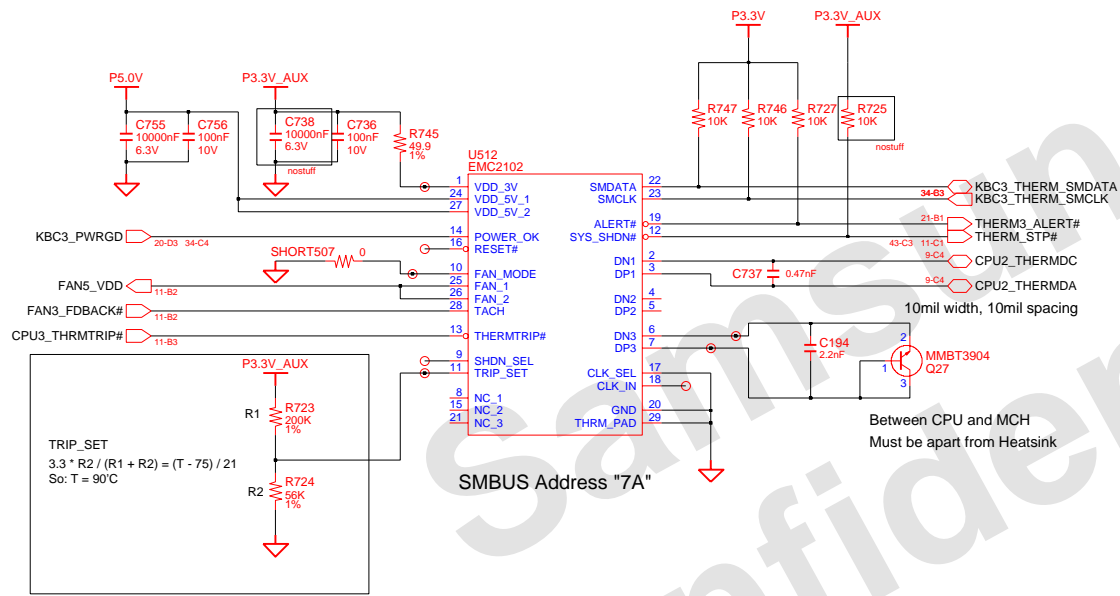


CHECK BULK CAP USING
 IF IT DOUBLED



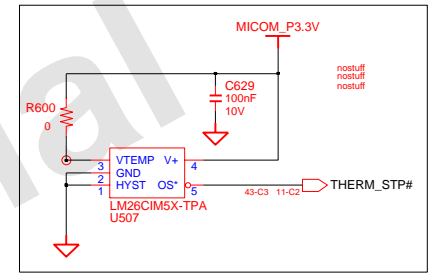
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		MAIN	
APPROVAL	SJ PARK	REV	1.0		MEROM CPU(3/3)	PART NO. BA41-00791A
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	10	OF 47

Thermal Monitor

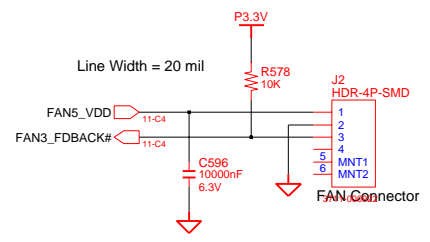


- Refer To Thermal Sensor Layout Guidelines.
- Place the Thermal Sensor close to a remote diode.
 - Keep traces away from high voltage (+12V bus)
 - Keep traces away from fast data buses and CRT signal.
 - Use recommended trace widths and spacings (10mil)
 - Place a ground plane under the traces.
 - Use guard traces flanking DXP and DXN and connecting to GND

OTP (NOSTUFF)

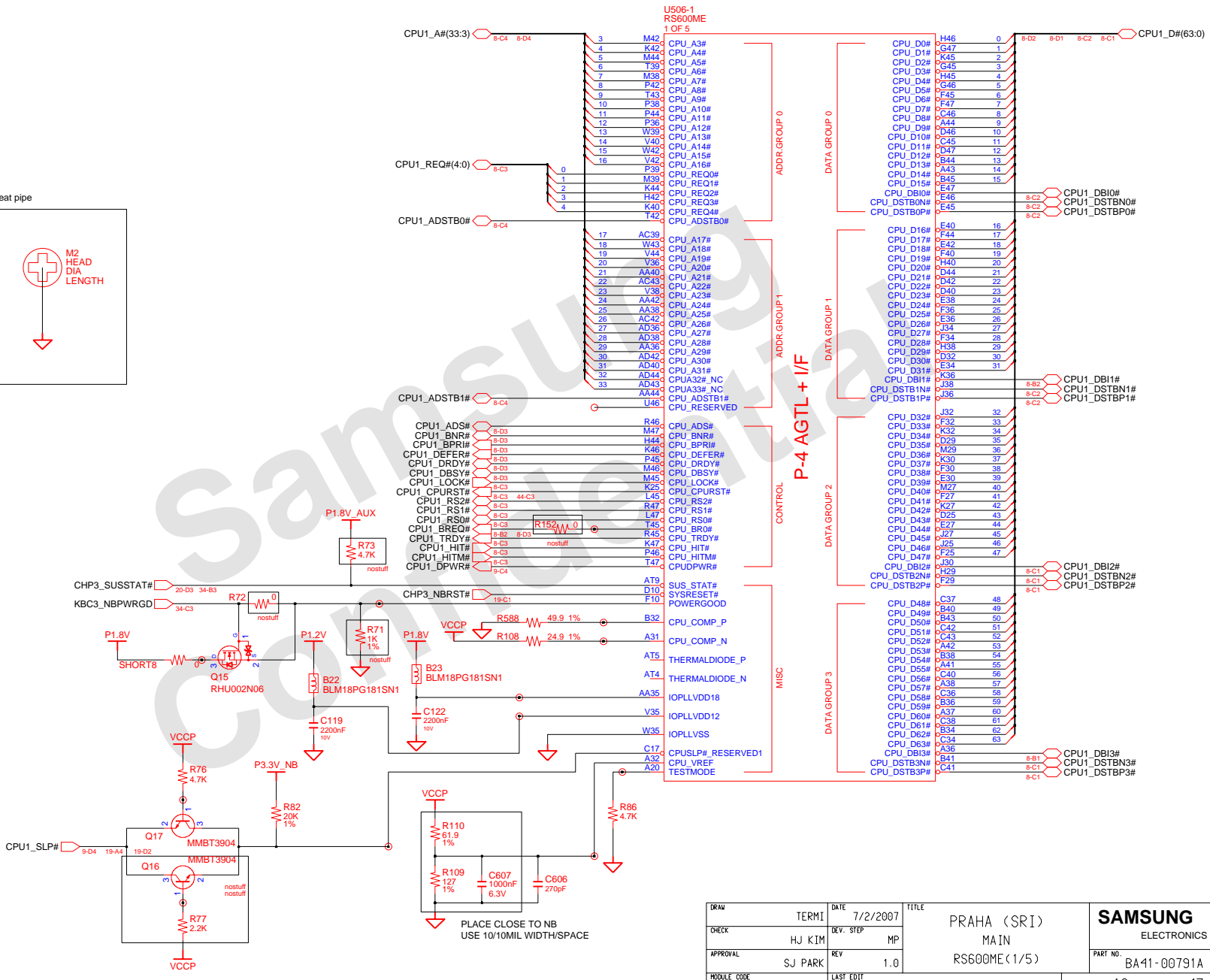
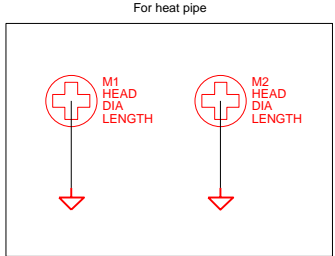


FAN Control



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	MAIN		
APPROVAL	SJ PARK	REV	1.0	THERMAL SENSOR/FAN CNTRL		PART NO. BA41-00791A
MODULE CODE	LAST EDIT		July 2, 2007 11:28:38 PM		PAGE	11 OF 47

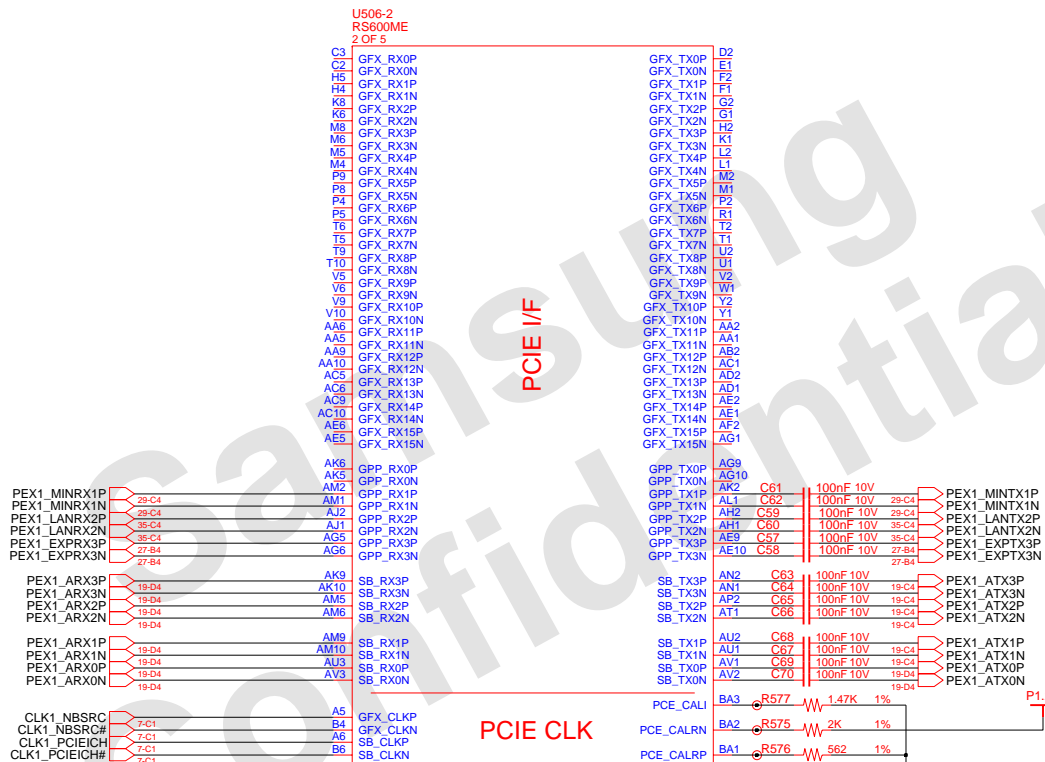
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DRAW	TERMI	DATE	TITLE	PRAHA (SRI) MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	7/2/2007	DEV. STEP		
APPROVAL	SJ PARK	REV	1.0	RS600ME(1/5)	PART NO. BA41-00791A
MODULE CODE		LAST EDIT		July 2, 2007 11:28:38 PM	PAGE 12 OF 47

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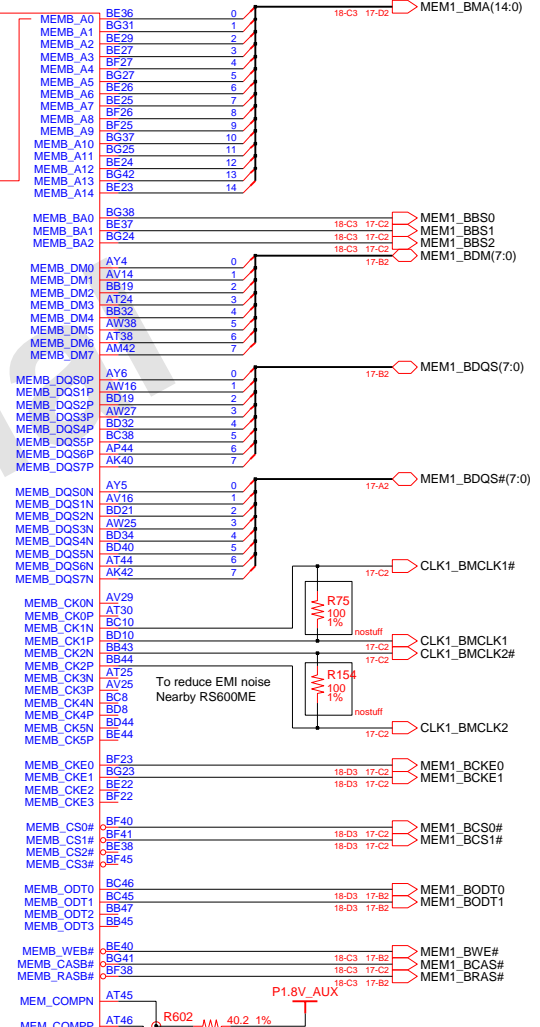
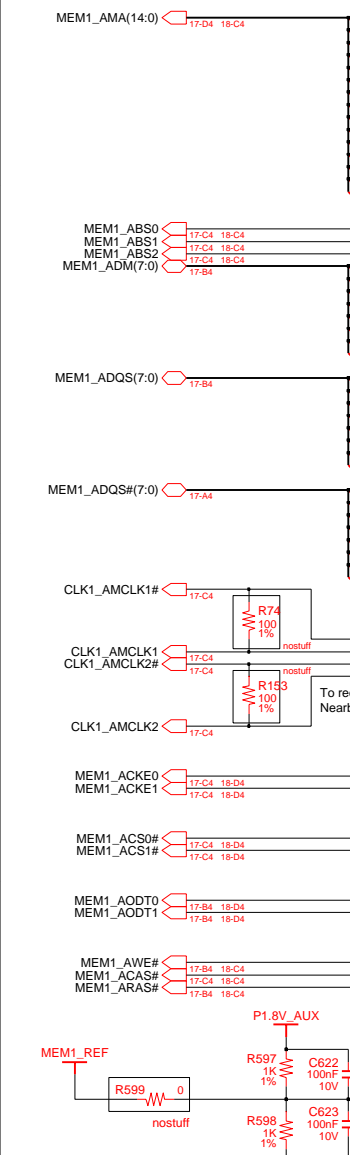
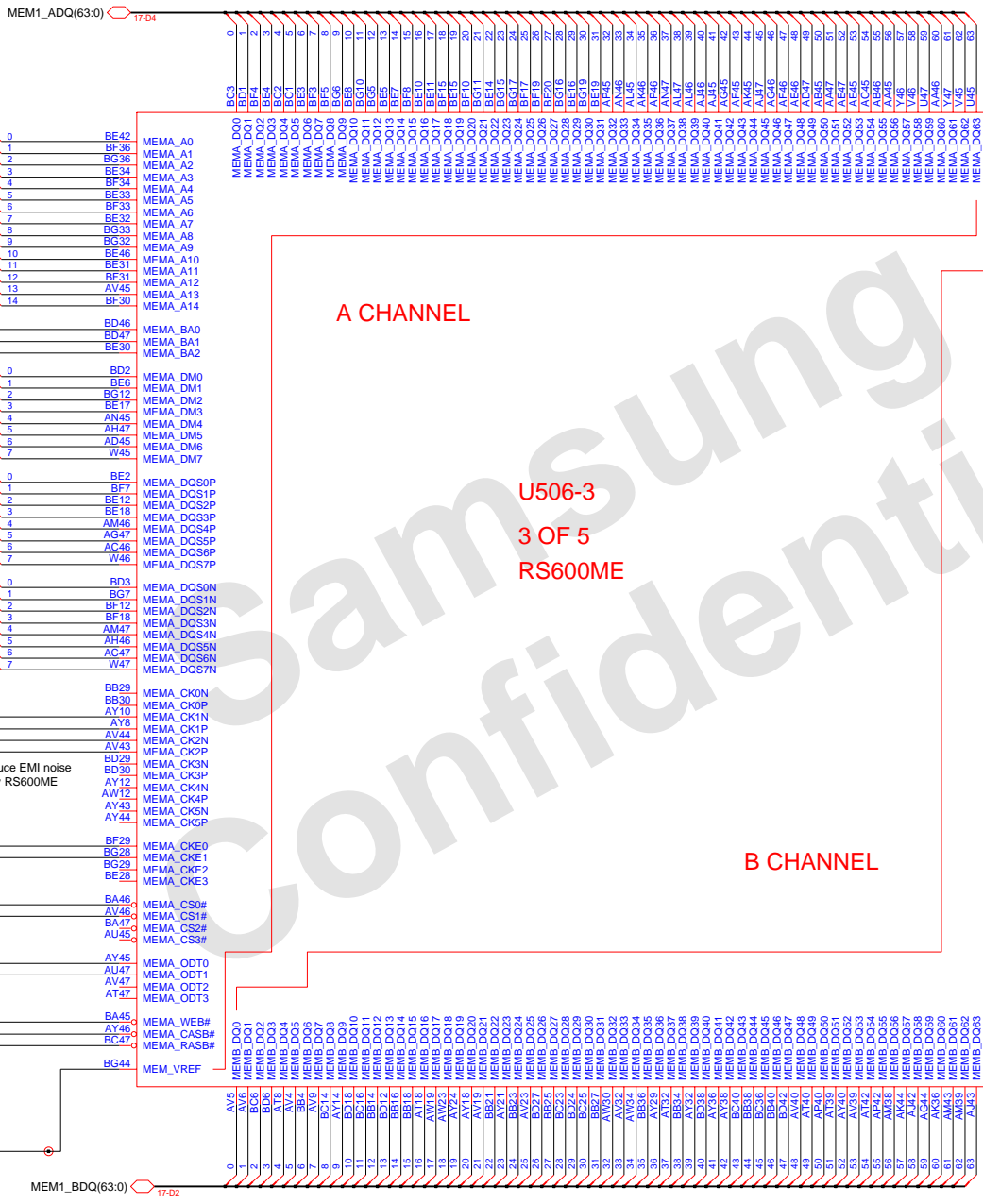
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PEX1_MIN	Mini Card I/F
PEX1_LAN	LOM I/F
PEX1_EXP	Express Card I/F

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	RS600ME(2/5)		
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00791A
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	13	OF 47

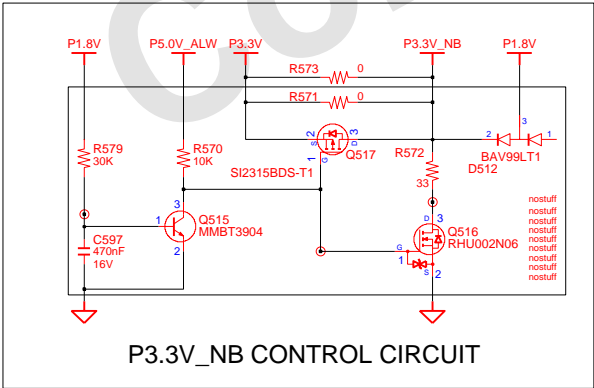
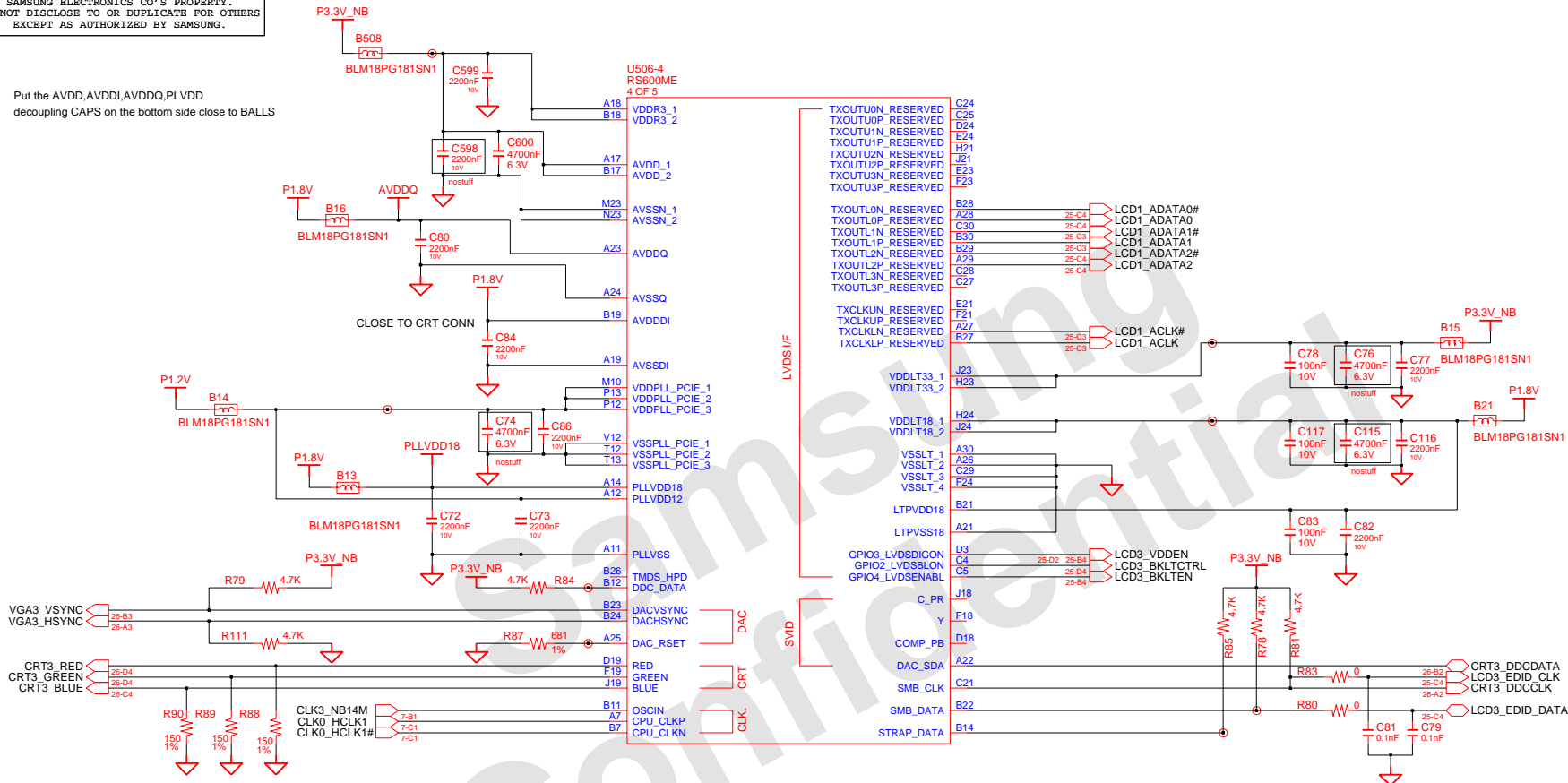
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Put the AVDD, AVDDI, AVDDQ, PLVDD decoupling CAPS on the bottom side close to BALLS



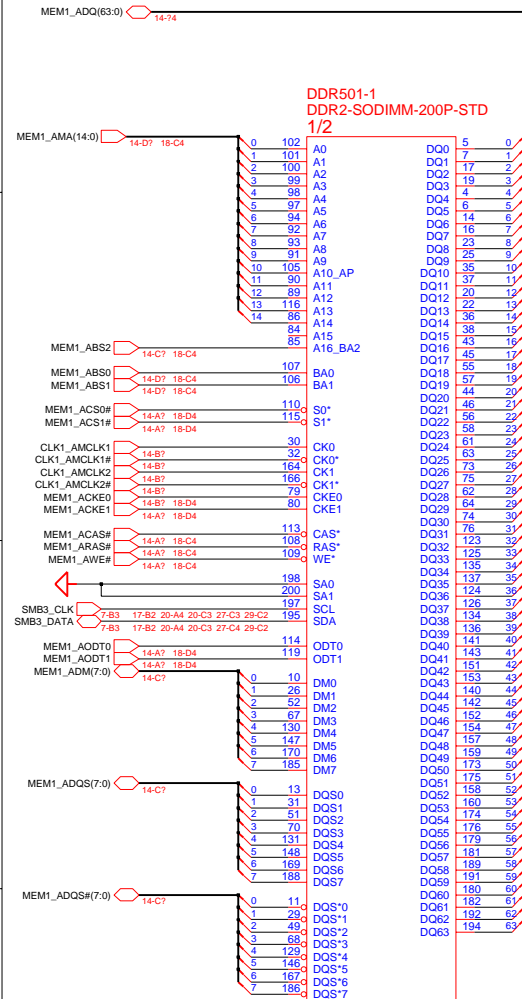
P3.3V_NB CONTROL CIRCUIT

STRAP DEFINITIONS FOR THE RS600M	
STRAP PIN	DESCRIPTION
DACHSYNC	Enable/Disable integrated graphics. 0 : Enable integrated graphics 1 : Disable integrated graphics
STRP_DATA	Debug strap configuration. This strap should not be set to "0" on production boards. 0 : Select Memory Channel A to be a debug bus 1 : Read debug straps from an external EEPROM, or disable debug mode when an EEPROM is absent.
DACVSYNC	Select configuration of the integrated graphics engine. 0 : Reserved 1 : Required setting for the RS600M
DDC_DATA	Select DDR2 or DDR3 signalling level for the memory interface. 0 : DDR3. On DDR3, it is necessary to put an isolation FET in series with the pull-up resistor on this strap to separate it from the I2C circuit during an NB reset 1 : DDR2

DRAW	TERMI	DATE	TITLE	PRAHA (SRI) MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	7/2/2007	7/2/2007		
APPROVAL	SJ PARK	REV	1.0	RS600ME(4/5)	PART NO.
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	15 OF 47

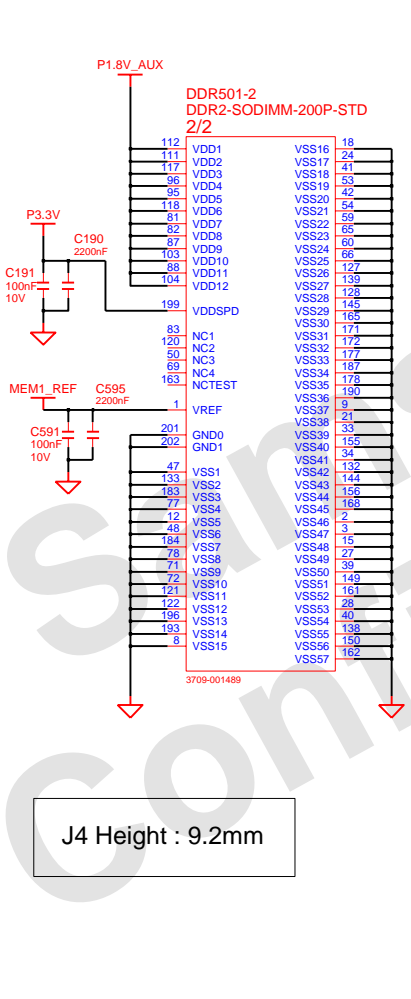
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DDR501-1
DDR2-SODIMM-200P-STD
1/2

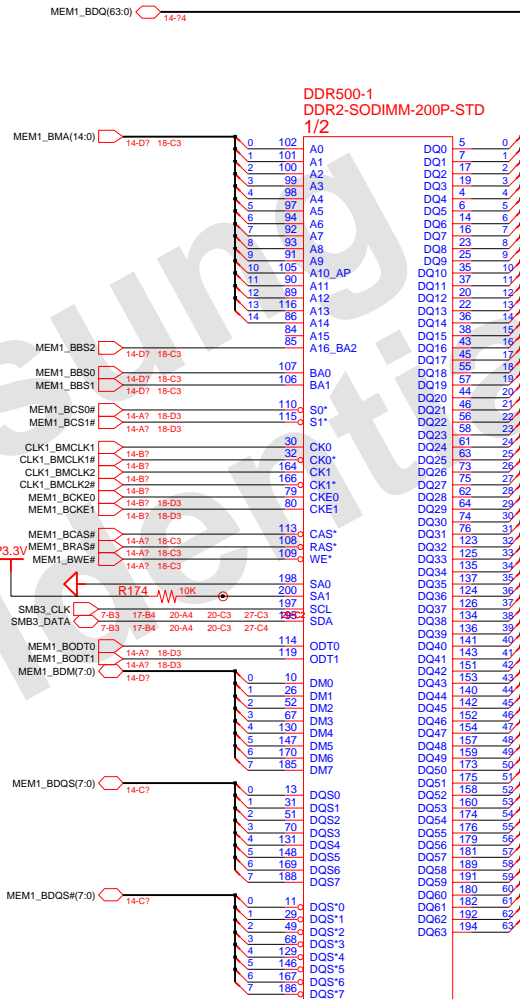
3709-001489



DDR501-2
DDR2-SODIMM-200P-STD
2/2

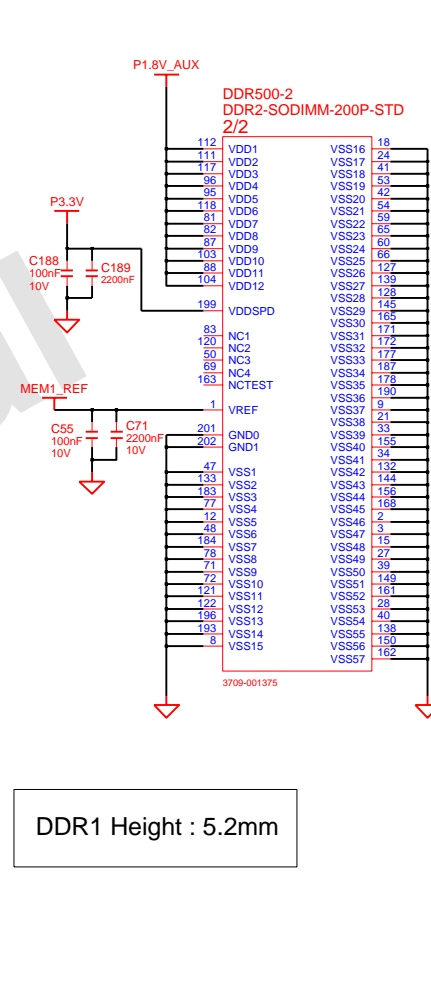
J4 Height : 9.2mm

3709-001489



DDR500-1
DDR2-SODIMM-200P-STD
1/2

3709-001375

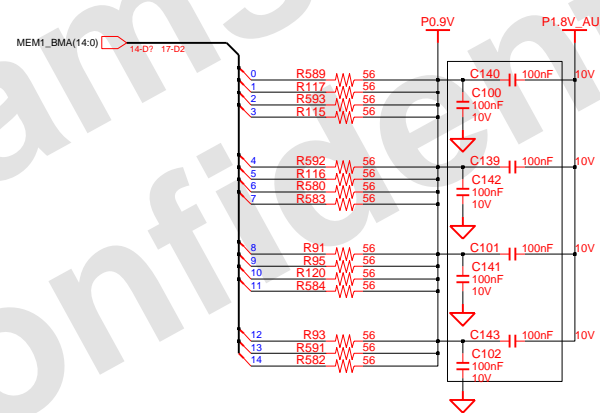
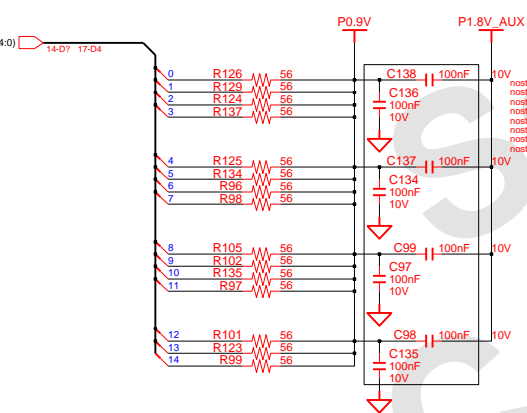
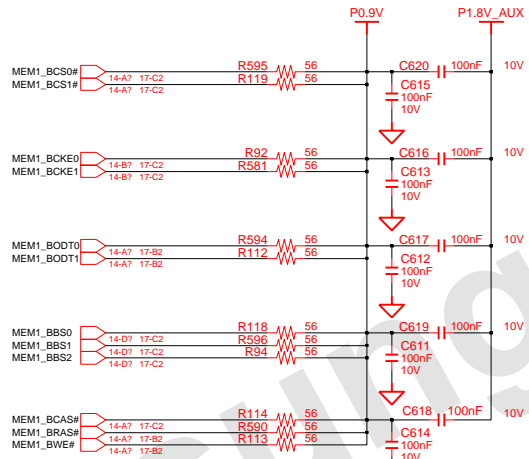
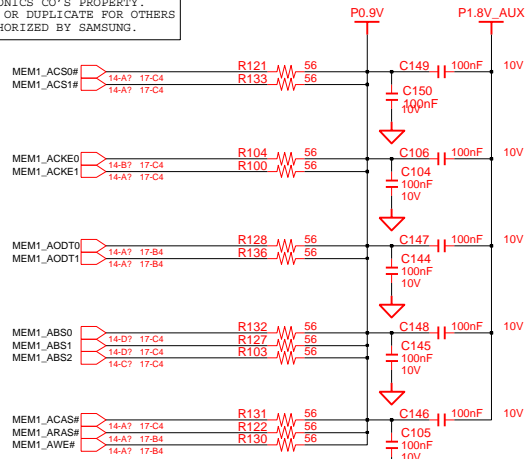


DDR500-2
DDR2-SODIMM-200P-STD
2/2

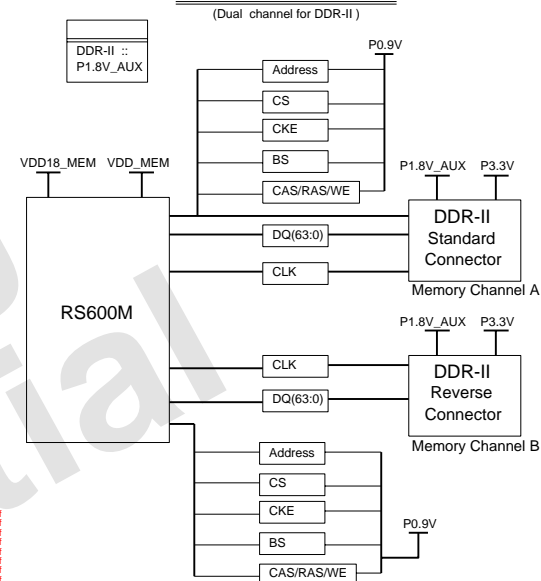
DDR1 Height : 5.2mm

3709-001375

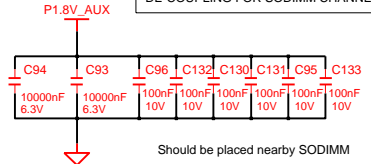
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CHECK	HJ KIM	DEV. STEP	MP	MAIN		
APPROVAL	SJ PARK	REV	1.0	DDR2 - SODIMM		PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	17	OF 47



Memory Topology

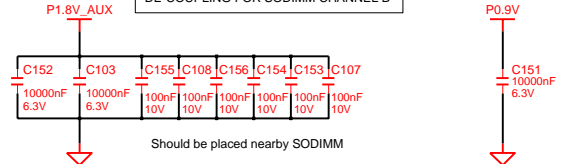


DE-COUPLING FOR SODIMM CHANNEL A



Should be placed nearby SODIMM

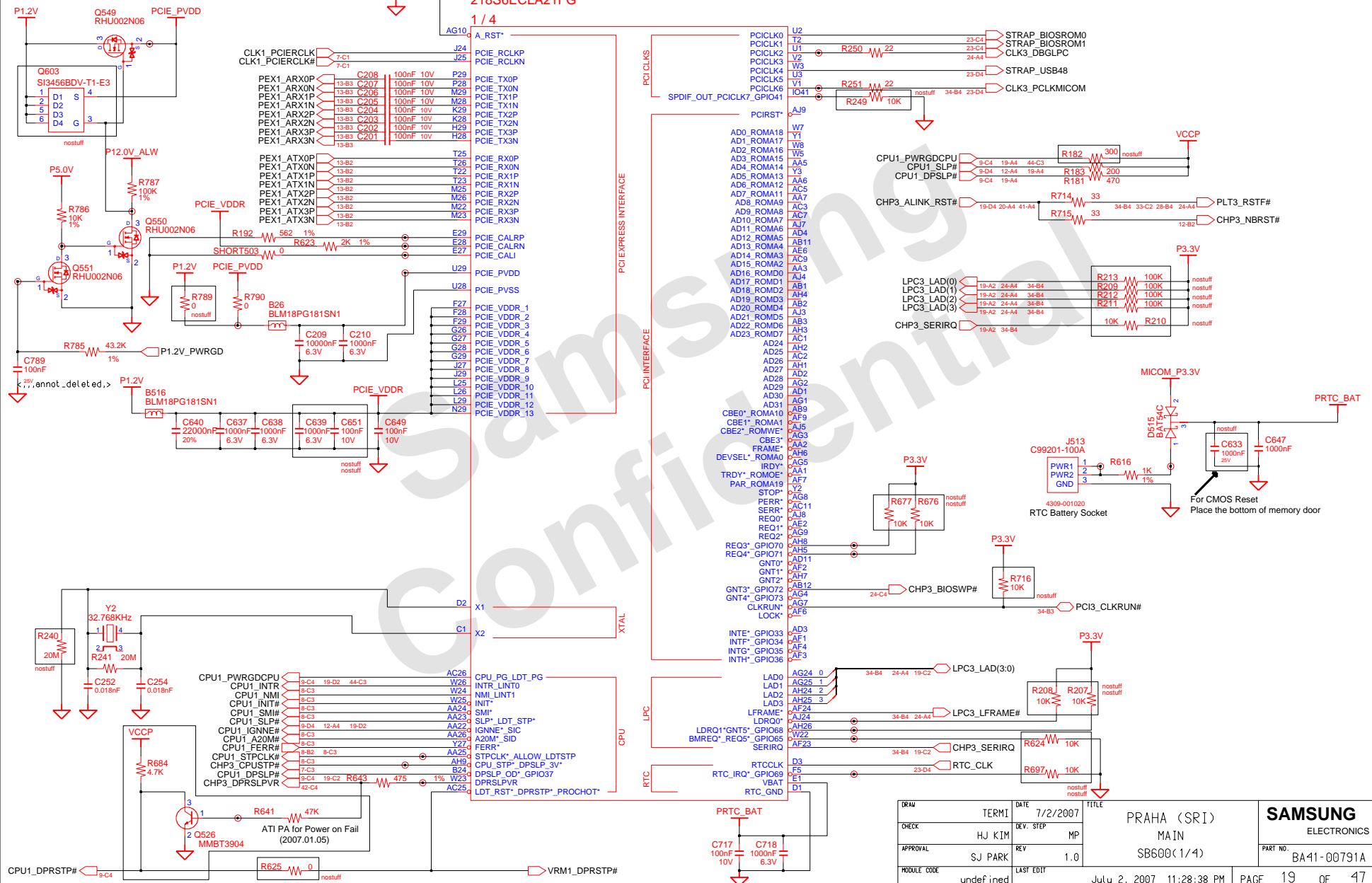
DE-COUPLING FOR SODIMM CHANNEL B



Should be placed nearby SODIMM

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	DDR2 - TERMINATION		
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	18	OF 47

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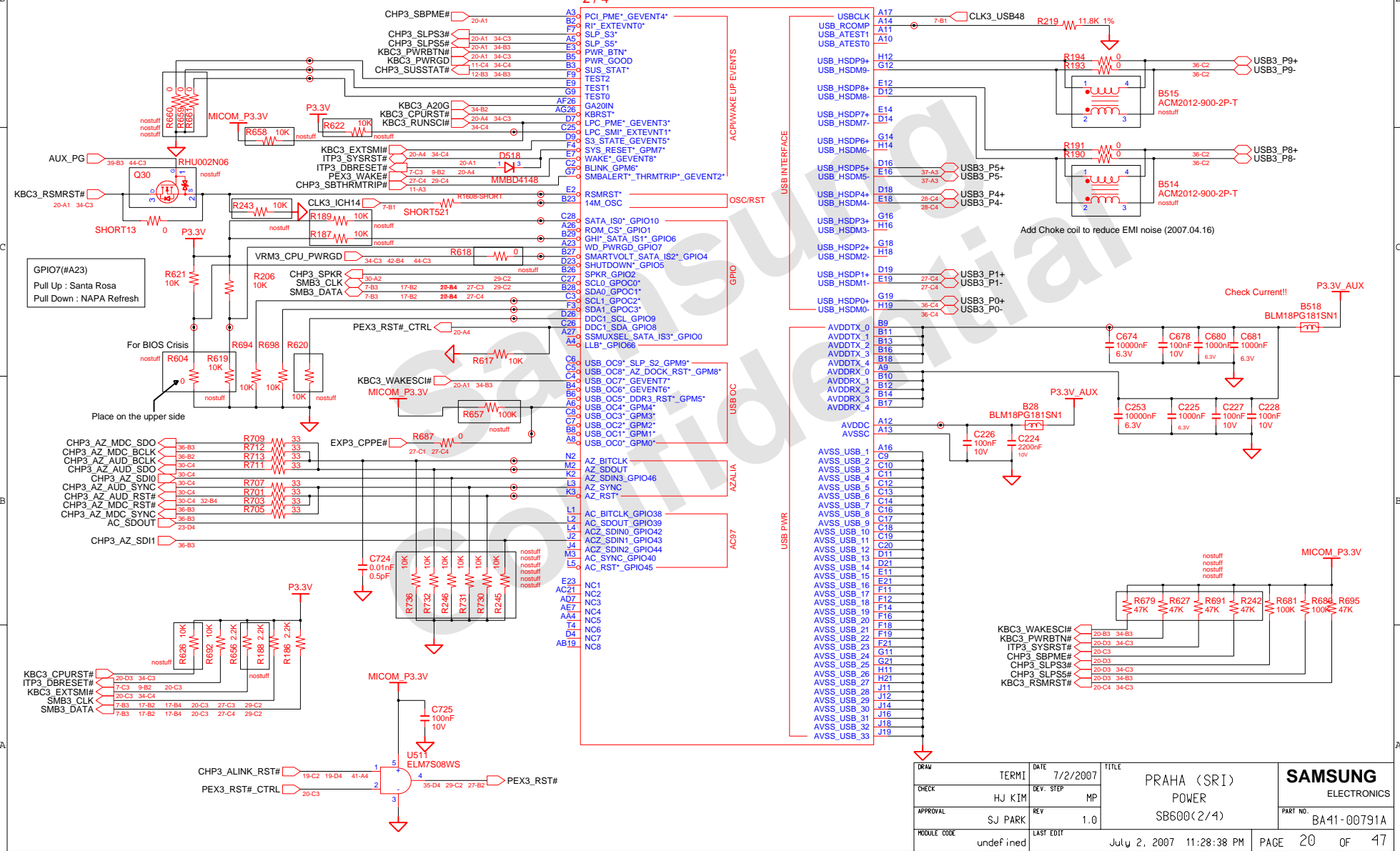
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CHECK	HJ KIM	7/2/2007	PRAHA (SRI) MAIN	
APPROVAL	SJ PARK	REV	1.0	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 19 OF 47

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USB Port 0 : Left side USB Port
USB Port 1 : Express Card
USB Port 4 : 2-in-1 Memory Card
USB Port 5 : Bluetooth I/F
USB Port 8, 9 : Rear side USB Port

U11-2
218S6ECLA21FG
2 / 4



GPIO7(#A23)
Pull Up : Santa Rosa
Pull Down : NAPA Refresh

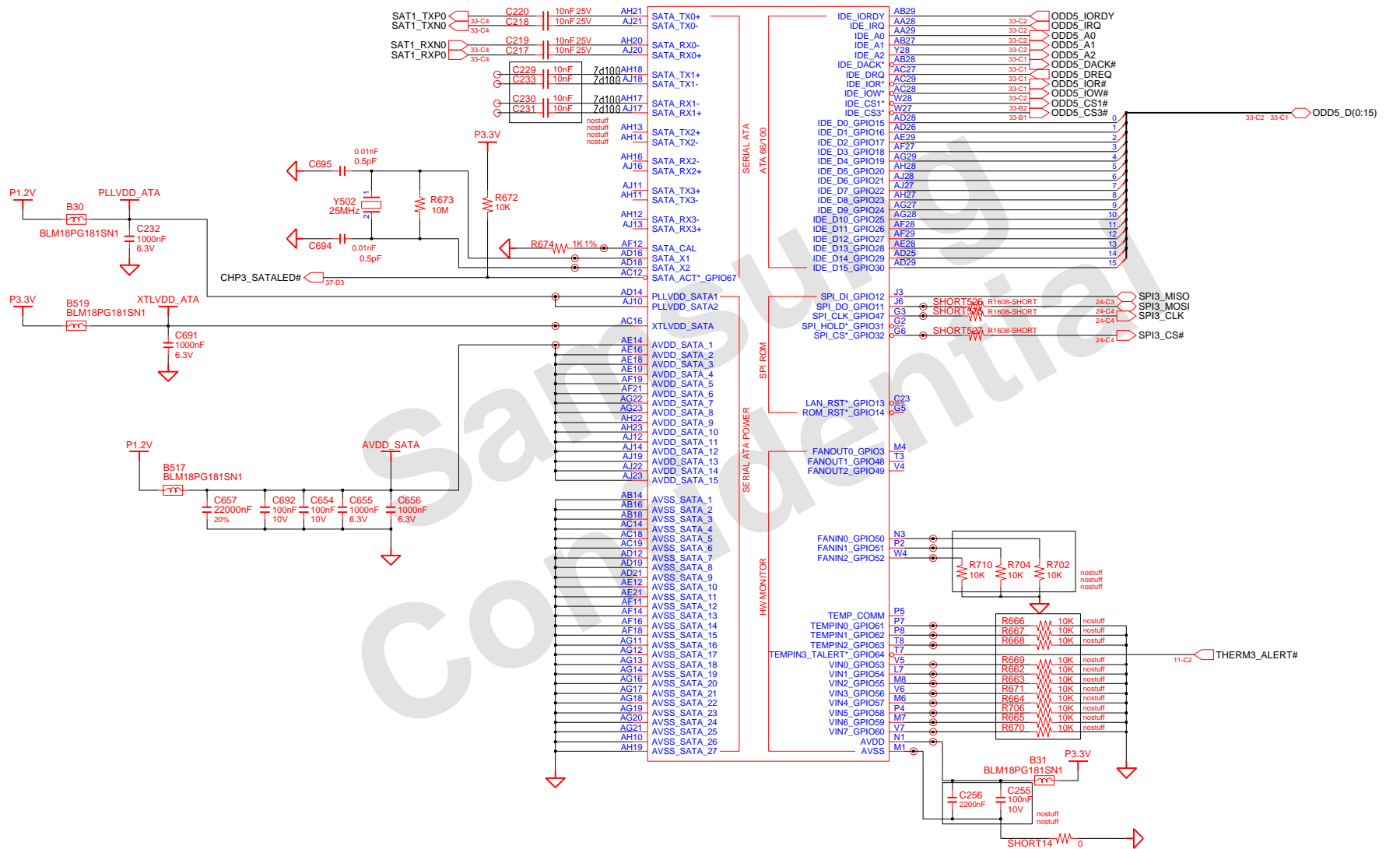
Add Choke coil to reduce EMI noise (2007.04.16)

Check Current!!!

Table with 4 columns: DRAW, CHECK, APPROVAL, MODULE CODE, TERMI, DEV. STEP, REV, LAST EDIT, DATE, TITLE, PRAHA (SRI) POWER SB600(2/4), SAMSUNG ELECTRONICS, PART NO. BA41-00791A, and page number 20 OF 47.

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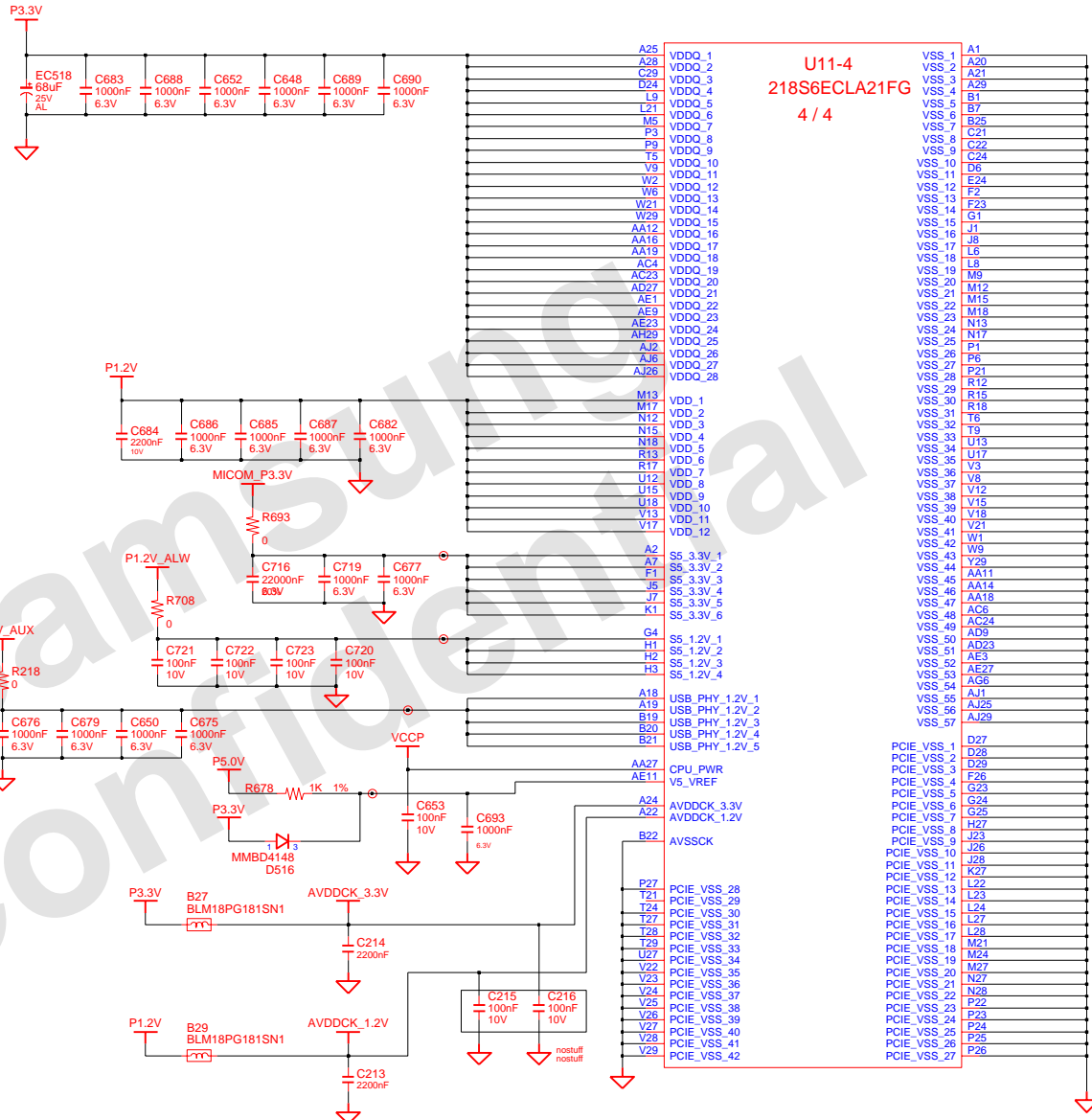
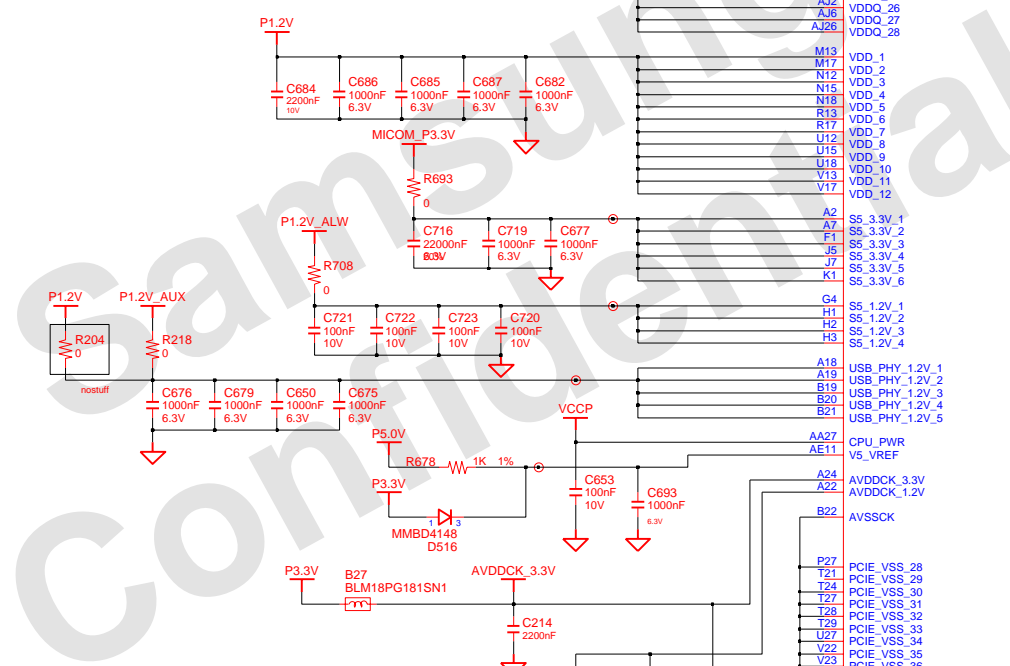
U11-3
 218S6ECLA21FG
 3 / 4



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		MAIN	
APPROVAL	SJ PARK	REV	1.0		SB600(3/4)	PART NO.
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	21	OF 47

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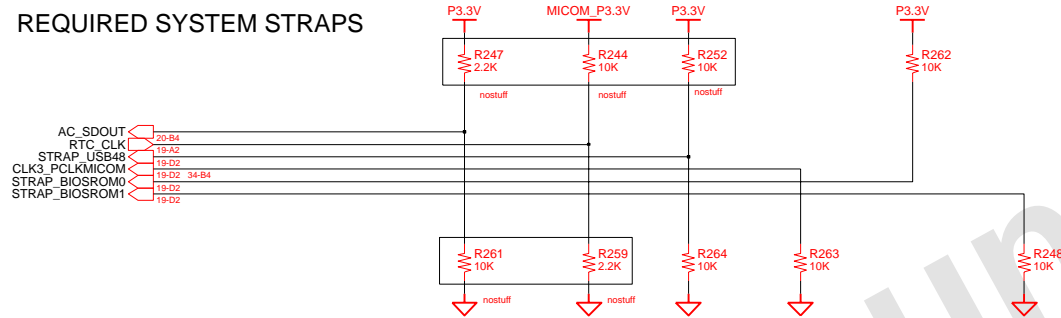
U11-4
218S6ECLA21FG
4 / 4

A25	VDDQ_1	VSS_1	A1
A26	VDDQ_2	VSS_2	A20
C29	VDDQ_3	VSS_3	A21
B24	VDDQ_4	VSS_4	A29
L9	VDDQ_5	VSS_5	B1
L21	VDDQ_6	VSS_6	B7
M5	VDDQ_7	VSS_7	B25
P3	VDDQ_8	VSS_8	C21
P9	VDDQ_9	VSS_9	C22
T5	VDDQ_10	VSS_10	C24
V9	VDDQ_11	VSS_11	D6
W2	VDDQ_12	VSS_12	F2
W6	VDDQ_13	VSS_13	F23
W21	VDDQ_14	VSS_14	F24
W29	VDDQ_15	VSS_15	G1
AA12	VDDQ_16	VSS_16	J1
AA16	VDDQ_17	VSS_17	J8
AA19	VDDQ_18	VSS_18	L6
AC4	VDDQ_19	VSS_19	L8
AC23	VDDQ_20	VSS_20	M9
AE27	VDDQ_21	VSS_21	M12
AE11	VDDQ_22	VSS_22	M15
AE9	VDDQ_23	VSS_23	M18
AE23	VDDQ_24	VSS_24	N13
AH29	VDDQ_25	VSS_25	N17
AJ2	VDDQ_26	VSS_26	P1
AJ6	VDDQ_27	VSS_27	P6
AJ26	VDDQ_28	VSS_28	P21
M13	VDD_1	VSS_29	R12
M17	VDD_2	VSS_30	R15
N12	VDD_3	VSS_31	R18
N15	VDD_4	VSS_32	T6
N18	VDD_5	VSS_33	T9
R13	VDD_6	VSS_34	U13
R17	VDD_7	VSS_35	U17
U12	VDD_8	VSS_36	V8
U15	VDD_9	VSS_37	V12
U18	VDD_10	VSS_38	V15
V13	VDD_11	VSS_39	V18
V17	VDD_12	VSS_40	V21
A2	S5_3.3V_1	VSS_41	W1
A7	S5_3.3V_2	VSS_42	W9
F1	S5_3.3V_3	VSS_43	Y29
J5	S5_3.3V_4	VSS_44	AA11
J7	S5_3.3V_5	VSS_45	AA14
K1	S5_3.3V_6	VSS_46	AA18
G4	S5_1.2V_1	VSS_47	AC6
H1	S5_1.2V_2	VSS_48	AC24
H2	S5_1.2V_3	VSS_49	AD9
H3	S5_1.2V_4	VSS_50	AD23
A18	USB_PHY_1.2V_1	VSS_51	AE3
A19	USB_PHY_1.2V_2	VSS_52	AE7
B19	USB_PHY_1.2V_3	VSS_53	AG6
B20	USB_PHY_1.2V_4	VSS_54	AJ1
B21	USB_PHY_1.2V_5	VSS_55	AJ25
AA27	CPU_PWR	VSS_56	AJ29
AE11	V5_VREF	VSS_57	D27
A24	AVDDCK_3.3V	PCIE_VSS_1	D28
A22	AVDDCK_1.2V	PCIE_VSS_2	D29
B22	AVSSCK	PCIE_VSS_3	F26
P27	PCIE_VSS_28	PCIE_VSS_4	G23
T21	PCIE_VSS_29	PCIE_VSS_5	G24
T24	PCIE_VSS_30	PCIE_VSS_6	G25
T27	PCIE_VSS_31	PCIE_VSS_7	H27
T28	PCIE_VSS_32	PCIE_VSS_8	J23
T29	PCIE_VSS_33	PCIE_VSS_9	J26
U27	PCIE_VSS_34	PCIE_VSS_10	K27
V22	PCIE_VSS_35	PCIE_VSS_11	K27
V23	PCIE_VSS_36	PCIE_VSS_12	L22
V24	PCIE_VSS_37	PCIE_VSS_13	L23
V25	PCIE_VSS_38	PCIE_VSS_14	L24
V26	PCIE_VSS_39	PCIE_VSS_15	L27
V27	PCIE_VSS_40	PCIE_VSS_16	L28
V28	PCIE_VSS_41	PCIE_VSS_17	M21
V29	PCIE_VSS_42	PCIE_VSS_18	M24
		PCIE_VSS_19	M27
		PCIE_VSS_20	N27
		PCIE_VSS_21	N28
		PCIE_VSS_22	P22
		PCIE_VSS_23	P24
		PCIE_VSS_24	P25
		PCIE_VSS_25	P26

DRAW	TERMI	DATE	TITLE	PRAHA (SRI) MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	7/2/2007	MP		
APPROVAL	SJ PARK	REV	1.0	SB600(4/4)	PART NO.
MODULE CODE	undef ined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	22 OF 47

SB600 HAS AN INTERNAL PD FOR AC_SDOUT
 SB600 HAS AN INTERNAL PU FOR RTC_CLK

REQUIRED SYSTEM STRAPS



	AC_SDOUT	RTC_CLK	PCI3_CLK4	PCI3_CLK6	PCI3_CLK0	PCI3_CLK1
STRAP HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INTERNAL PLL48	CPU I/F = K8	ROM TYPE H, H = PCI ROM H, L = SPI ROM	
STRAP LOW	IGNORE DEBUG STRAPS	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	USE EXTERNAL 48MHz	CPU I/F = P4	L, H = LPC ROM L, L = FWH ROM	

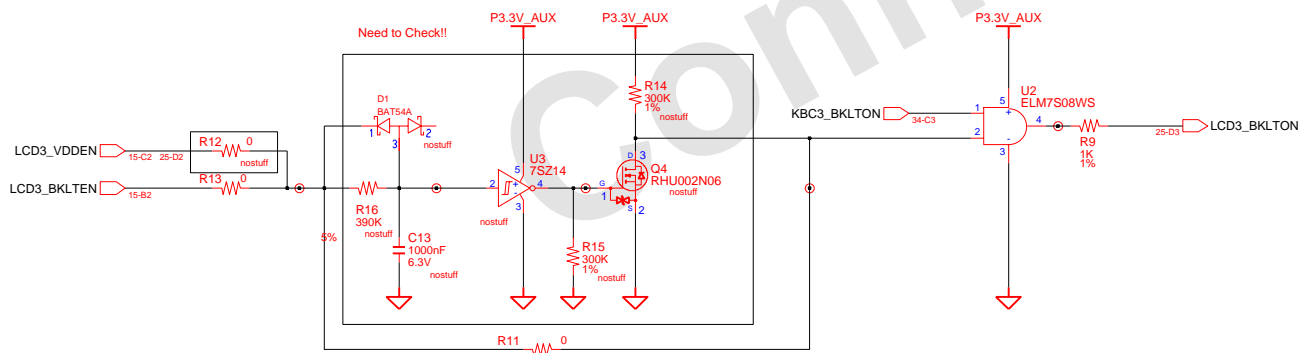
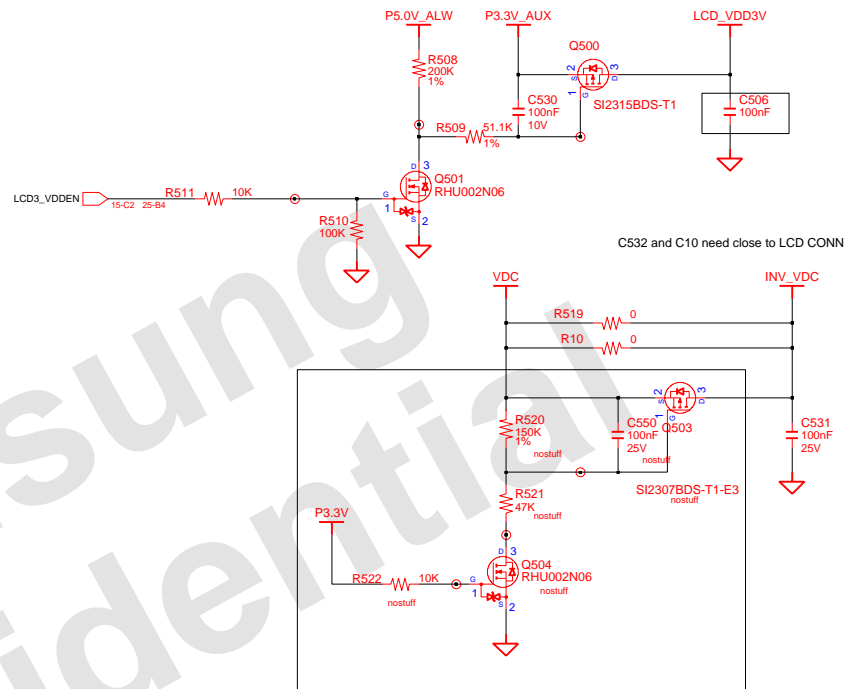
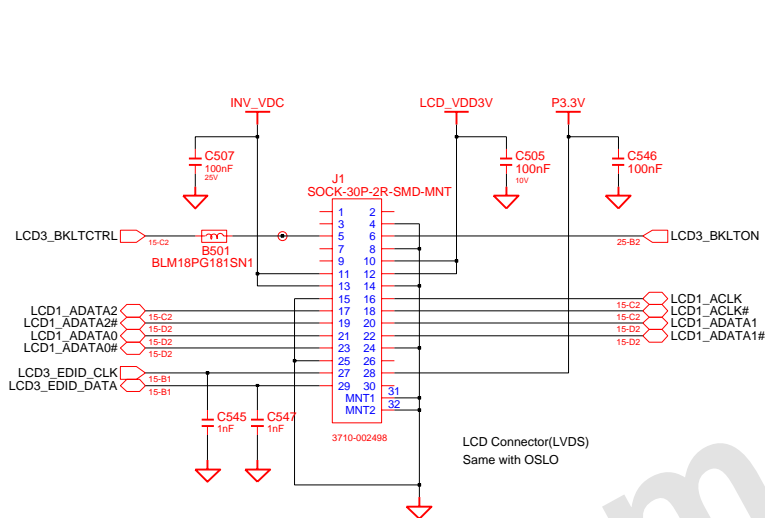
DEBUG STRAPS

	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0	STRAPS		PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	23	OF 47

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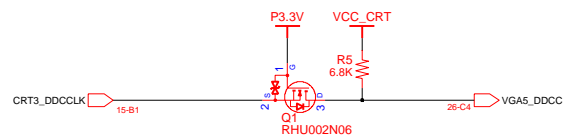
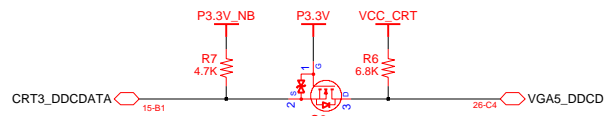
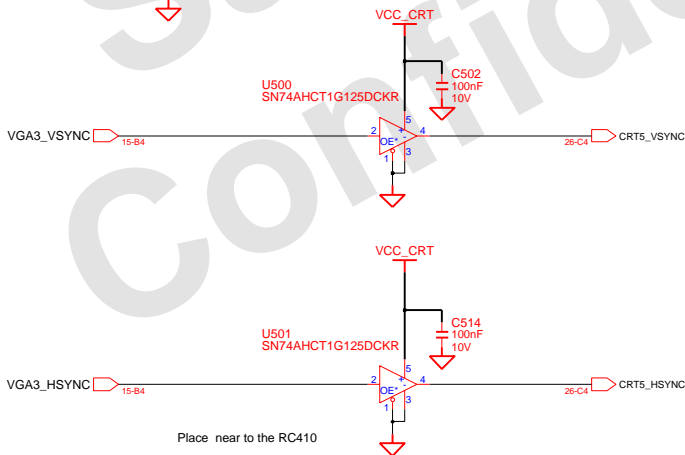
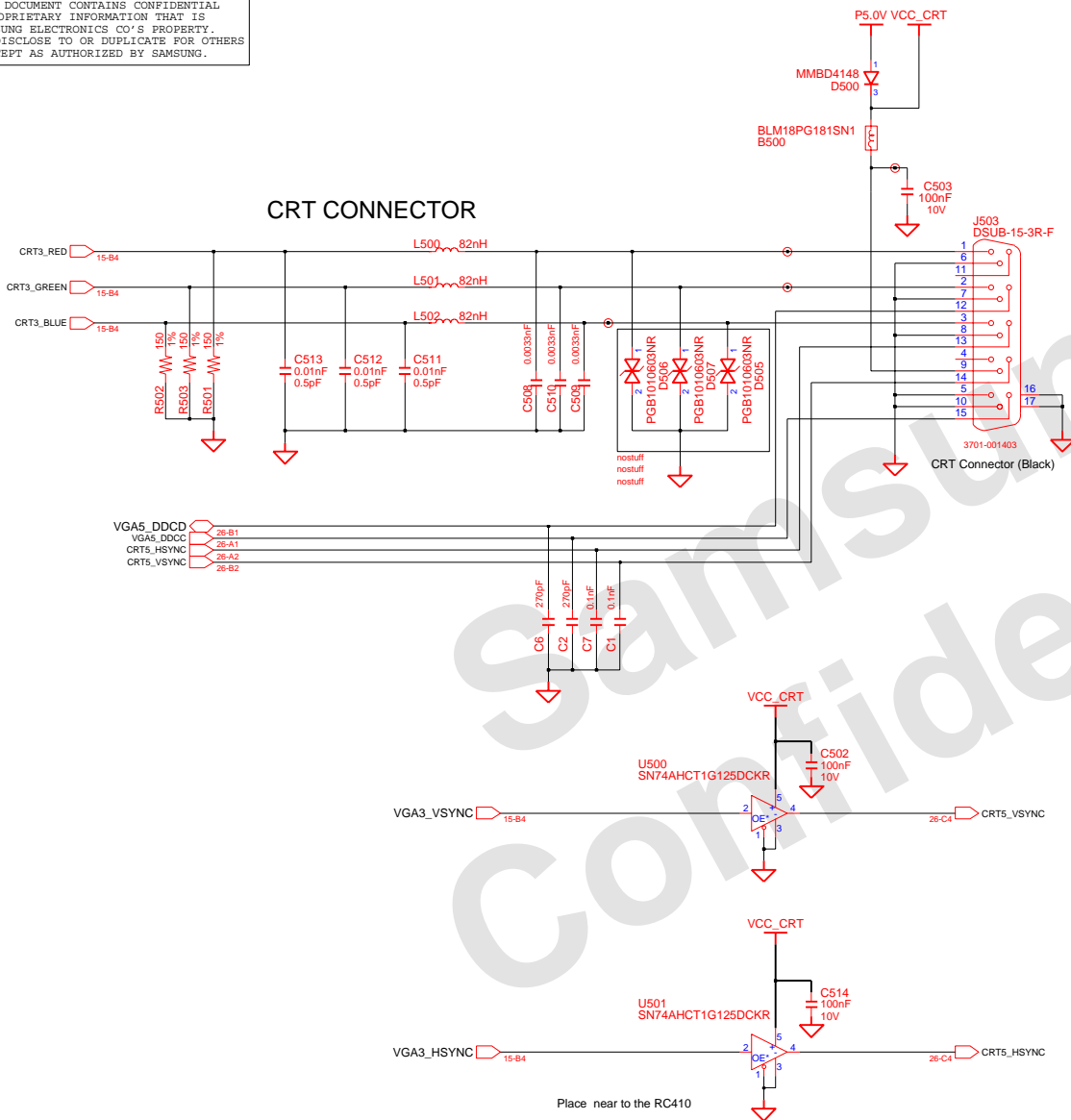


DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) LCD Connector & SPREAD SPECTRUM	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	PART NO.		
APPROVAL	SJ PARK	REV	1.0	July 2, 2007 11:28:38 PM		BA41-00791A
MODULE CODE	undefined	LAST EDIT		PAGE	25	OF 47

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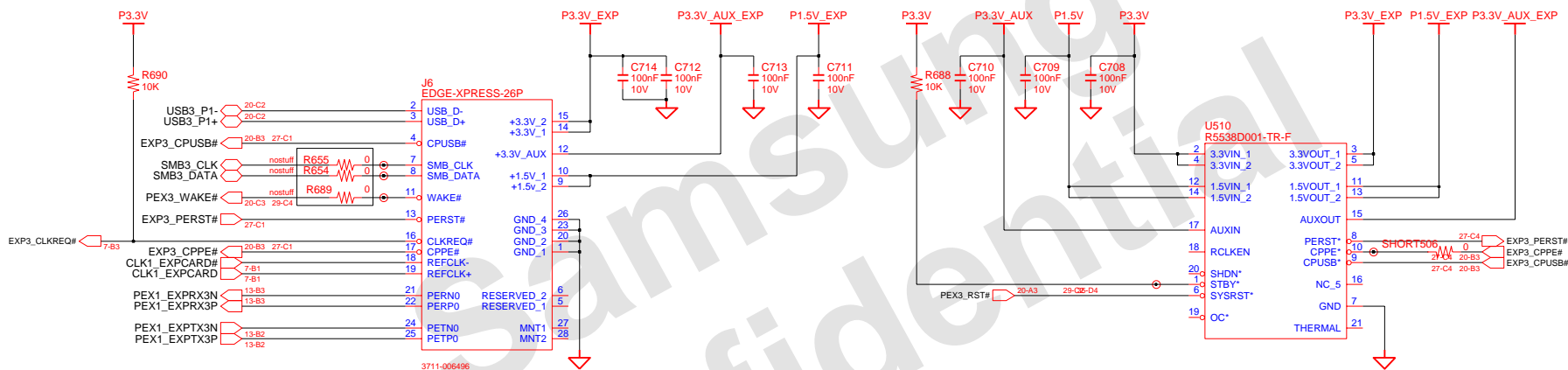
CRT CONNECTOR



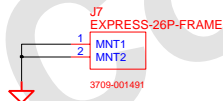
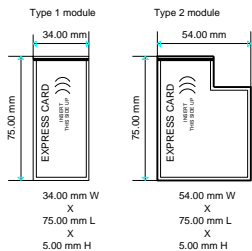
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS	
CHECK	HJ KIM	DEV. STEP	MP				
APPROVAL	SJ PARK	REV	1.0		CRT	PART NO.	
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM			BA41-00791A	
						PAGE	26 OF 47

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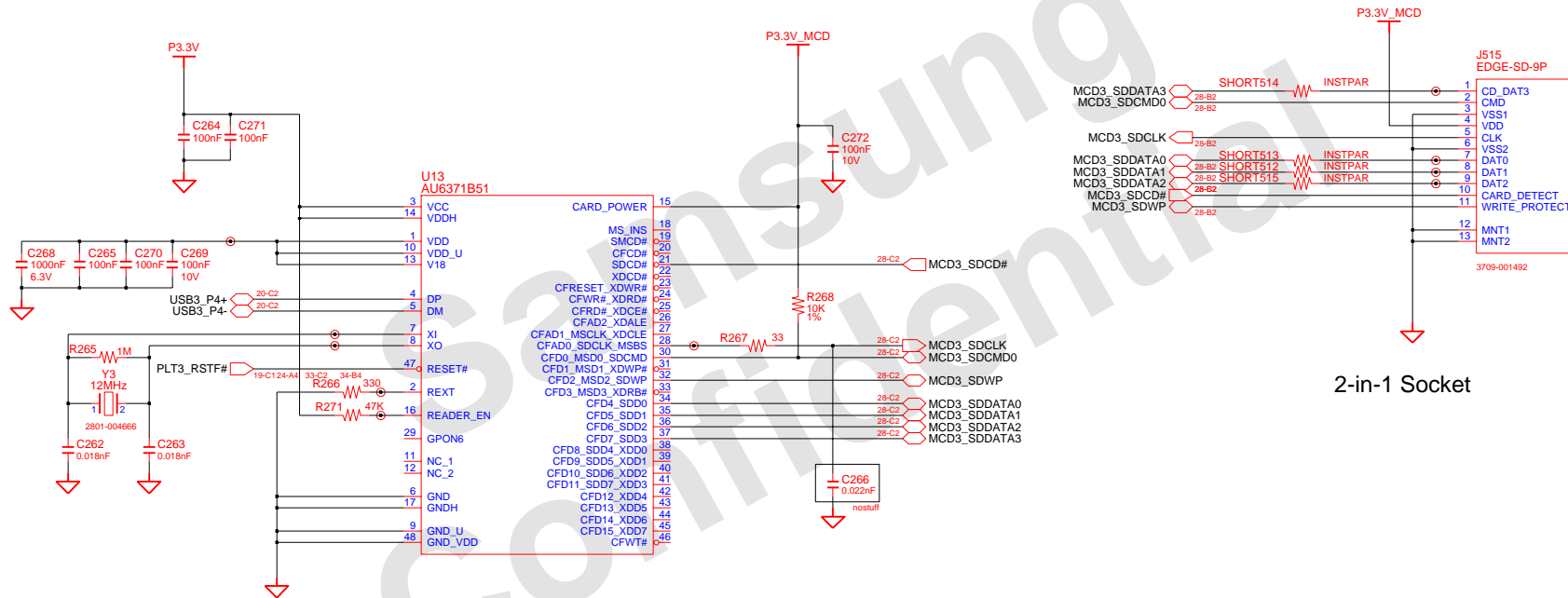


EXPRESS CARD



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0	EXPRESS CARD	PART NO.	BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	27	OF 47

2 IN 1 CARD

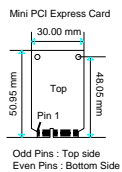
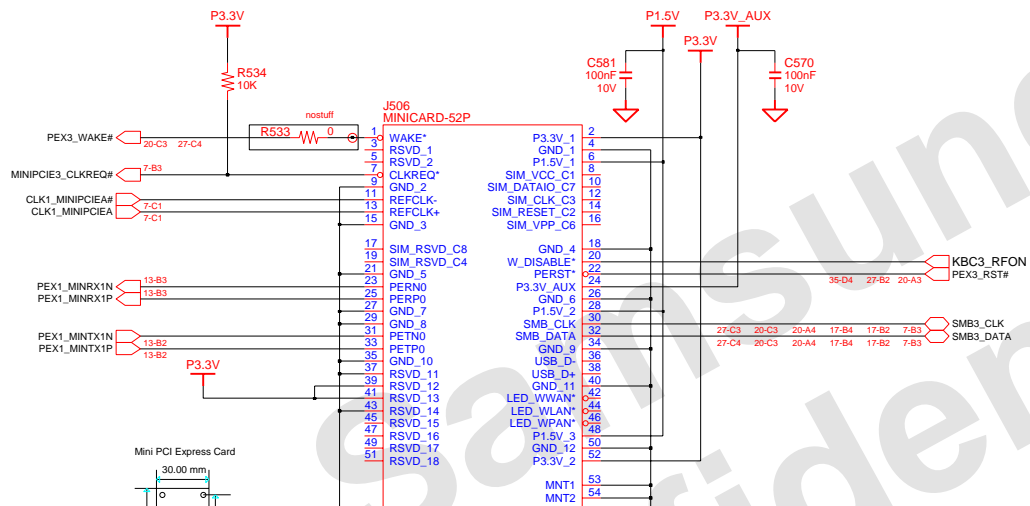


2-in-1 Socket

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0	2 in 1 Socket		PART NO.
MODULE CODE	LAST EDIT			July 2, 2007 11:28:38 PM	PAGE	28 OF 47

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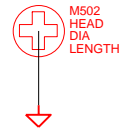
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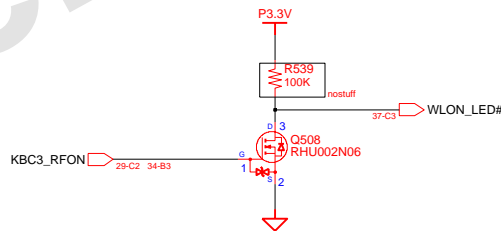
Odd Pins : Top side
Even Pins : Bottom Side

**7mm Height
Mini PCI Express**

PCI Express Mini Card ElectroMechanical Spec. 1.0



**4.5mm Height
For MiniCard**



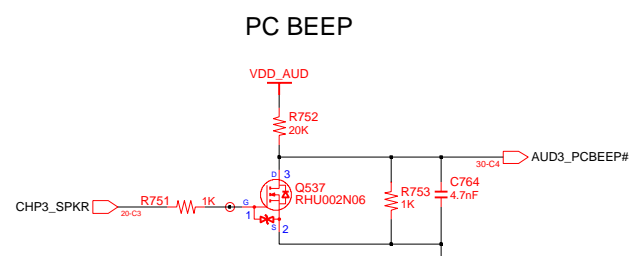
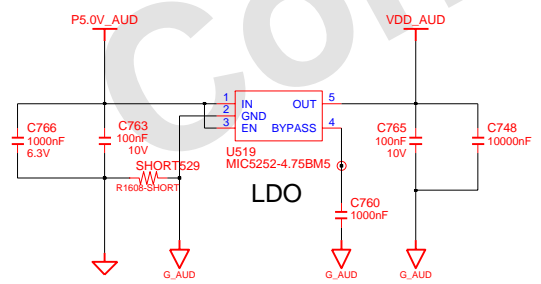
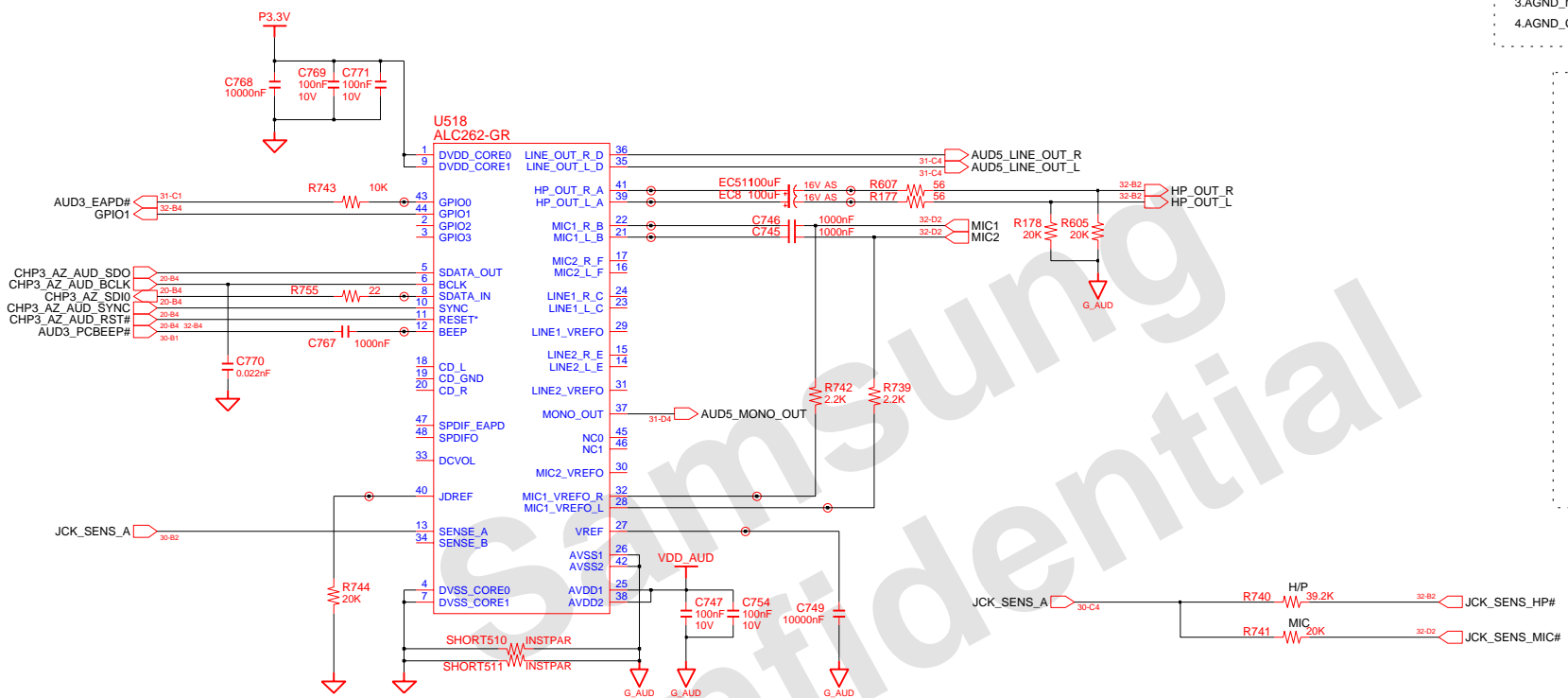
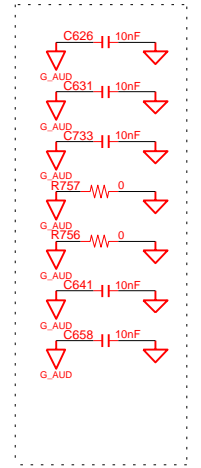
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN MINI CARD	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	29	OF 47
					PART NO.	BA41-00791A

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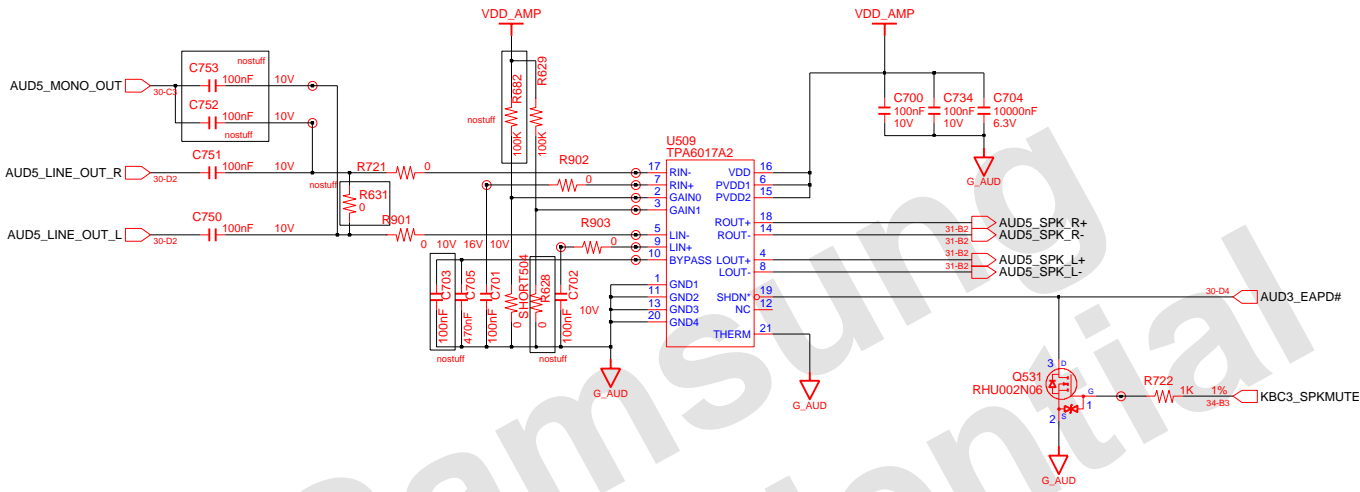
- 1.AGND_AUD IS AUDIO GROUND
- 2.GND IS DIGITAL GROUND
- 3.AGND_MIC IS MIC GROUND
- 4.AGND_CHS IS CHASS GROUND

ALL TYPE IS 1608

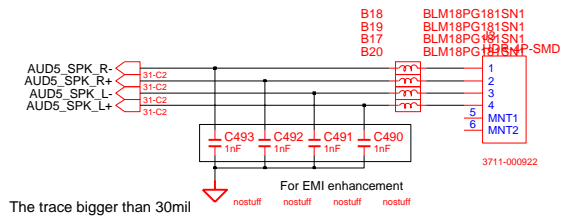
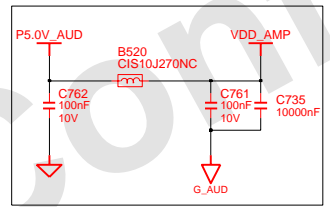


DRAW	TERMI	DATE	TITLE	PRAHA (SRI) MAIN AUDIO CODEC	SAMSUNG ELECTRONICS
CHECK	HJ KIM	7/2/2007	DEV. STEP		
APPROVAL	SJ PARK	REV	1.0		PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 30	OF 47

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AMP_VDD INTERNAL STEREO SPEAKERS

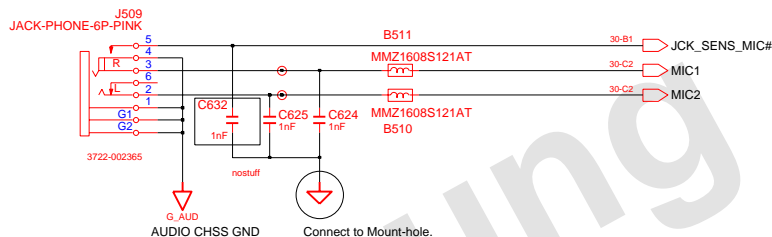


DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN LIMITER & AMP	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	31	OF 47

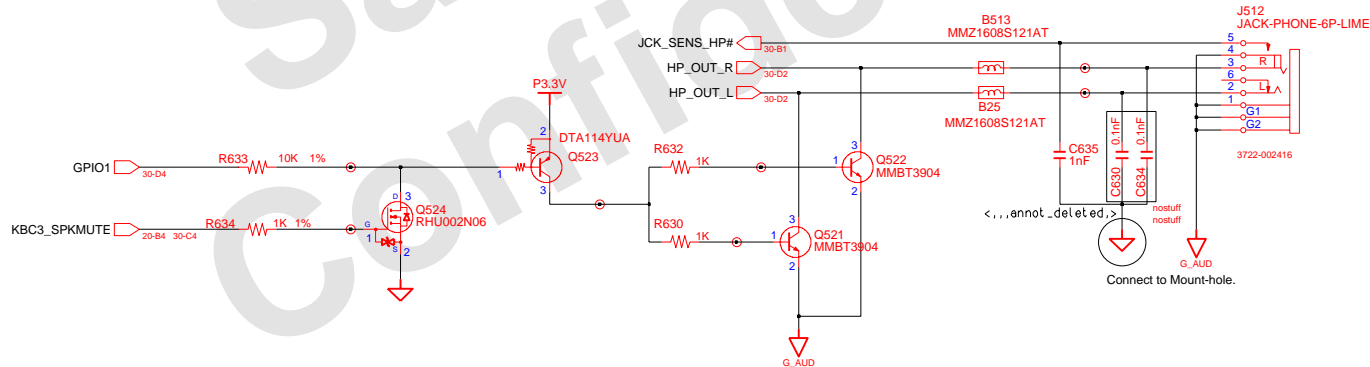
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MIC JACK



HEADPHONE



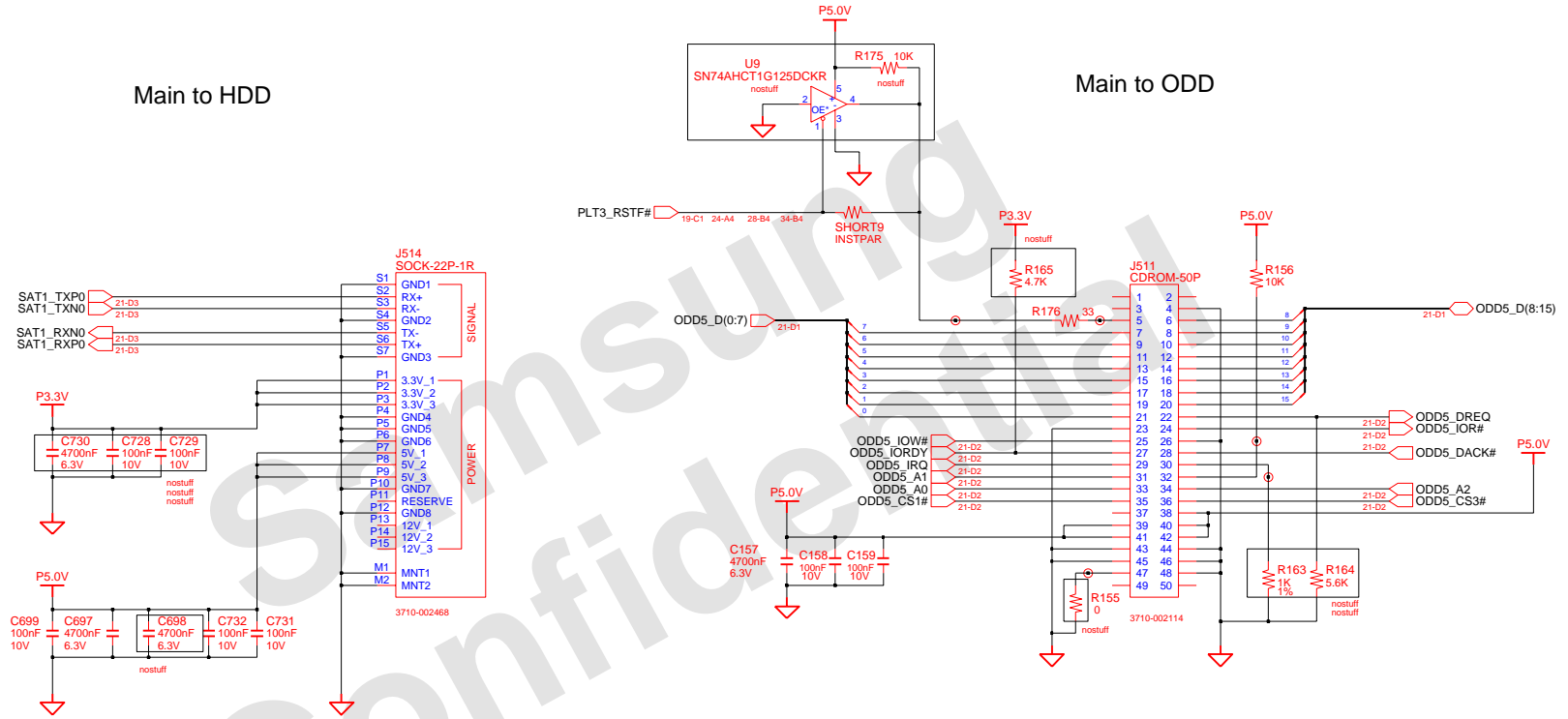
The traces led to Audio Jacks have the width over 10mil

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN MIC & HEADPHONE	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	PART NO.		
APPROVAL	SJ PARK	REV	1.0	LAST EDIT		PAGE 32 OF 47
MODULE CODE	undefined	July 2, 2007 11:28:38 PM				

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Main to HDD

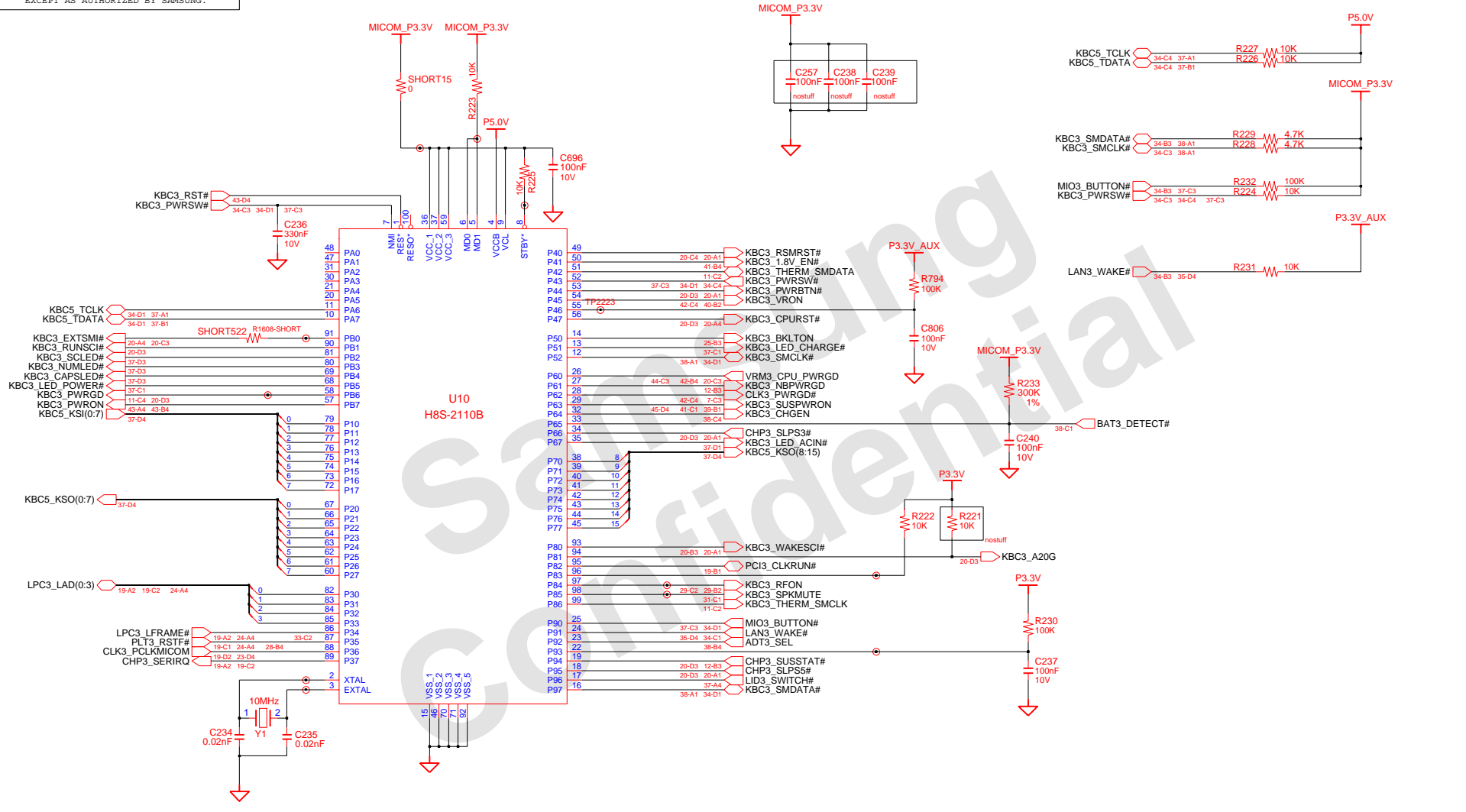
Main to ODD



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) POWER HDD & ODD	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	33	OF 47

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MICOM Crisis Update
 Condition: P90=P91=P92=High(MICOM_P3V)
 MD0=MD1=Low(0V)
 Serial Port: P84 & P85

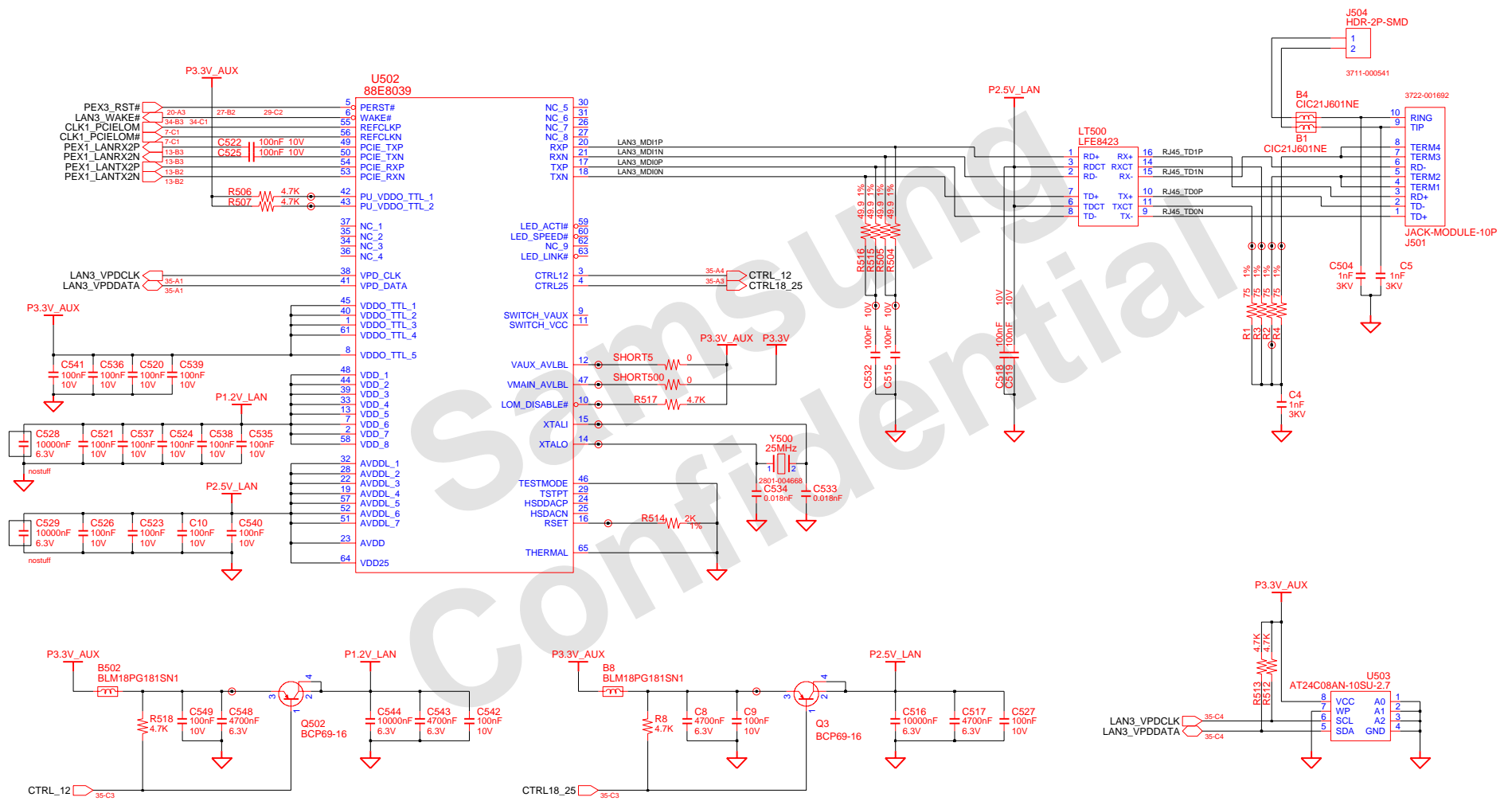
The removed signal compared from 144pin

- KBC5_CAL_THRM*
- THRM_ALERT*
- LCD3_BKLTEN
- FAN3_FDBACK*
- THERM_STP*

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		POWER	
APPROVAL	SJ PARK	REV	1.0		MICOM	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	34	OF 47

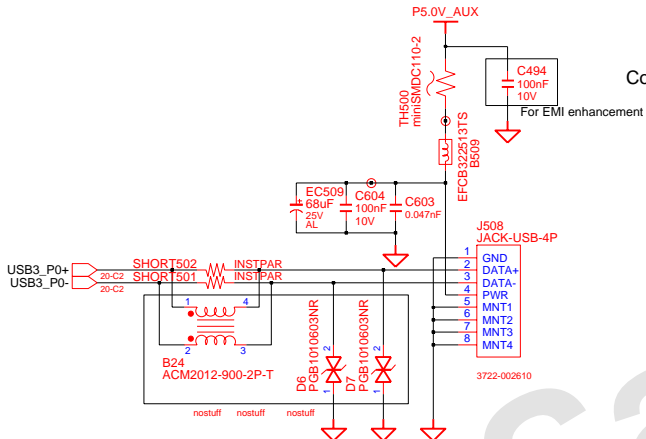
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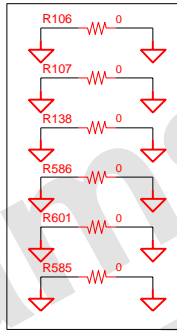
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	MAIN		
APPROVAL	SJ PARK	REV	1.0	LAN		PART NO.
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 35		OF 47

Side USB Connector



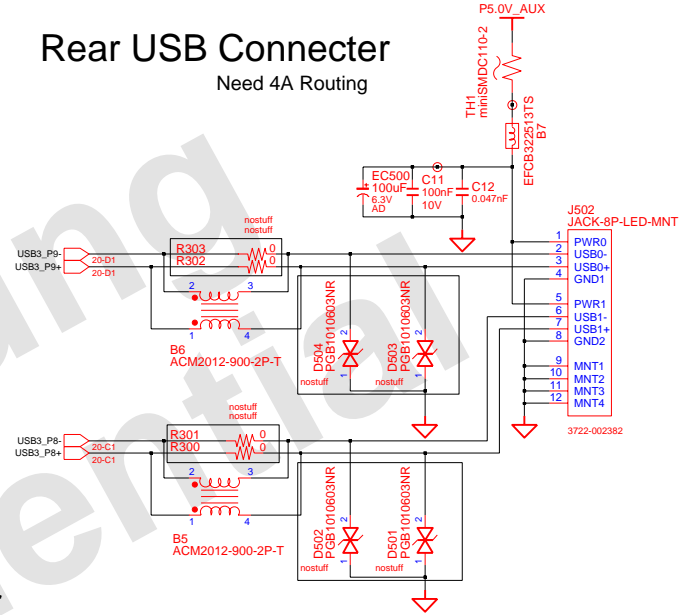
Connect left side USB GND with CPU GND

Top : 3EA Bottom : 3EA

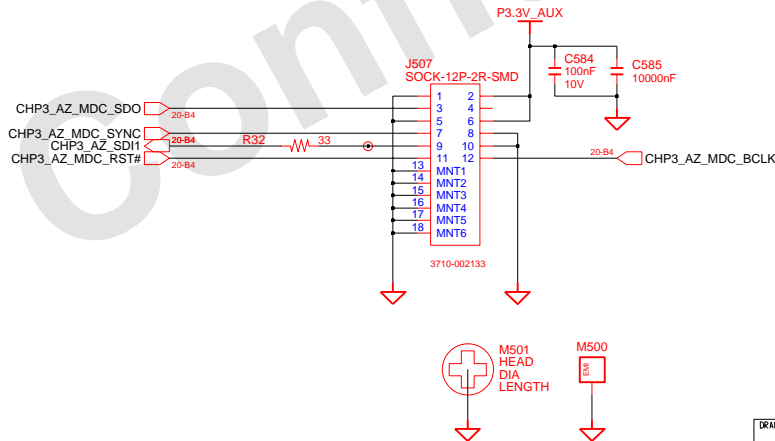


Rear USB Connector

Need 4A Routing



MDC Connector

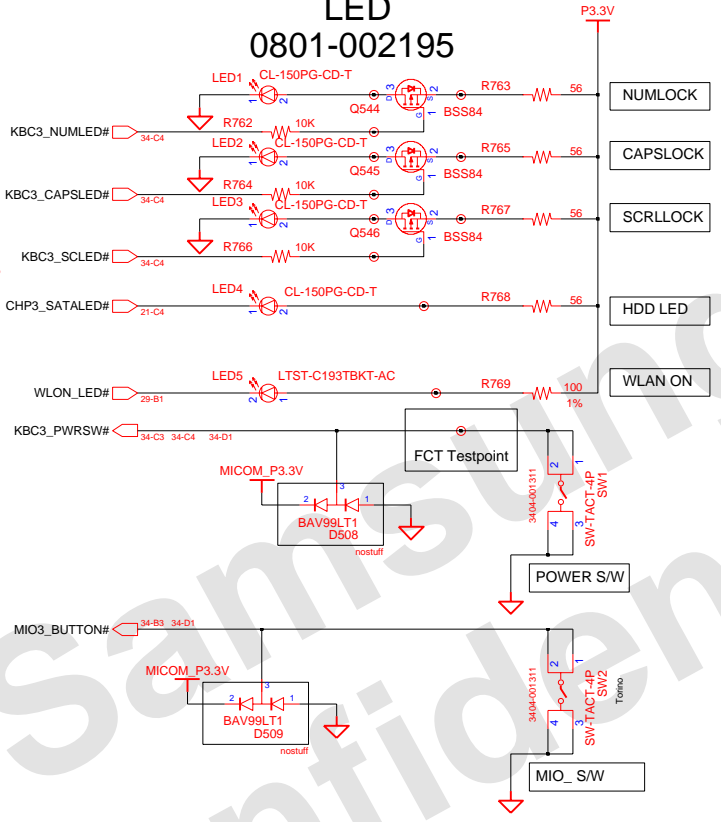
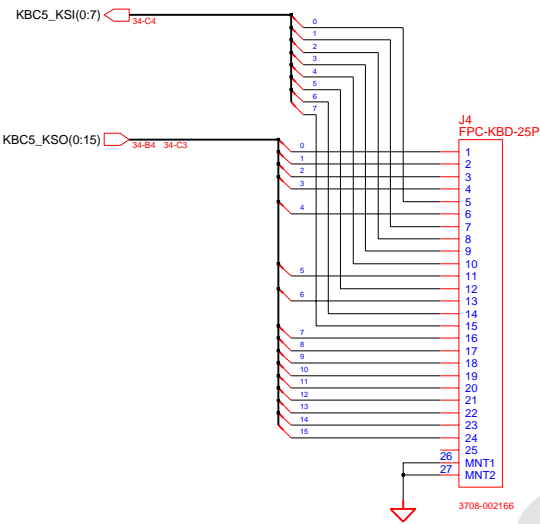


DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	USB PORT & MDC Conn.		
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	36	OF 47

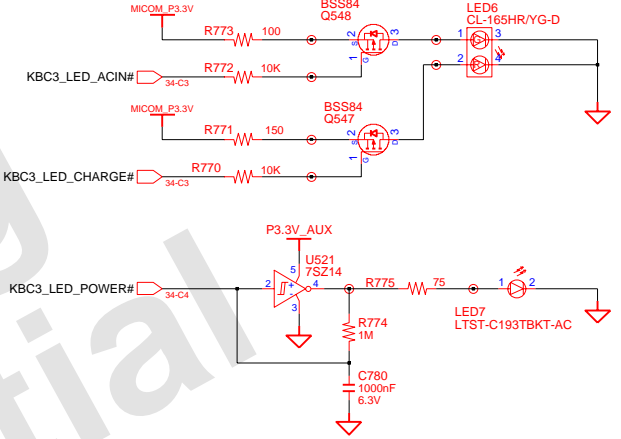
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LED 0801-002195

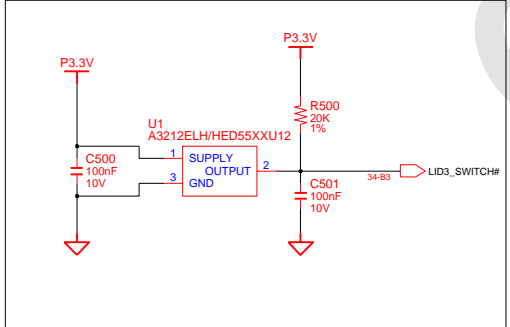
KEYBOARD



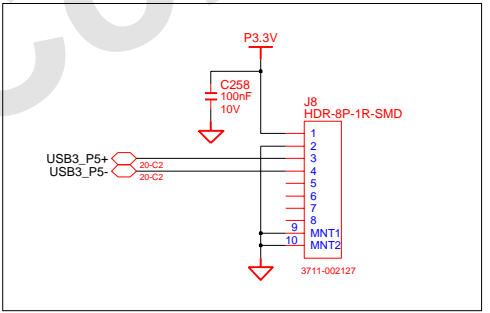
ADAPTERIN/CHARGING LED



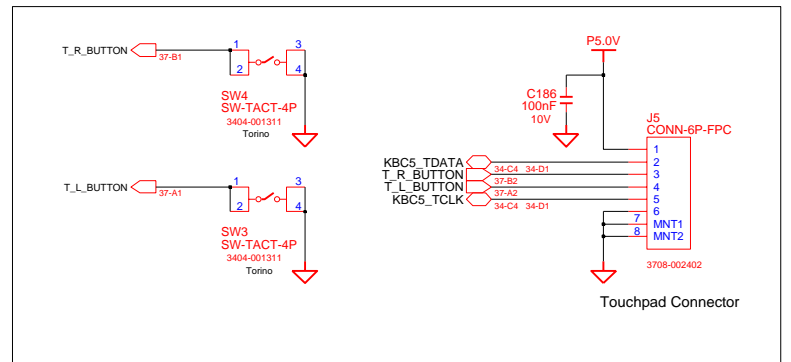
LID SWITCH



Bluetooth Interface Factory Option



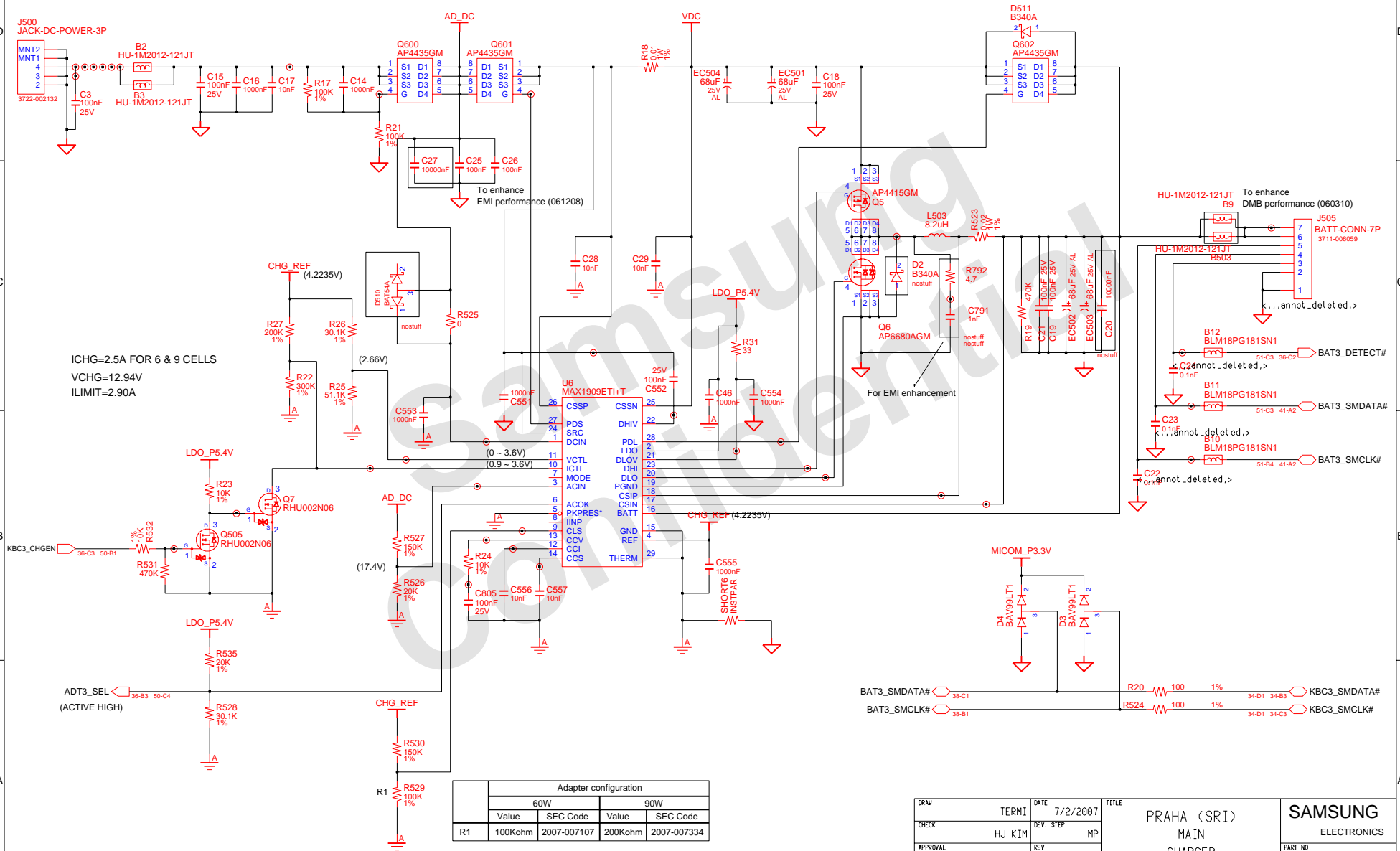
TOUCHPAD



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	LED & BLUETOOTH		
APPROVAL	SJ PARK	REV	1.0	TOUCHPAD & KBD & LID S/W		PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	37	OF 47

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CHARGER & POWER MANAGEMENT



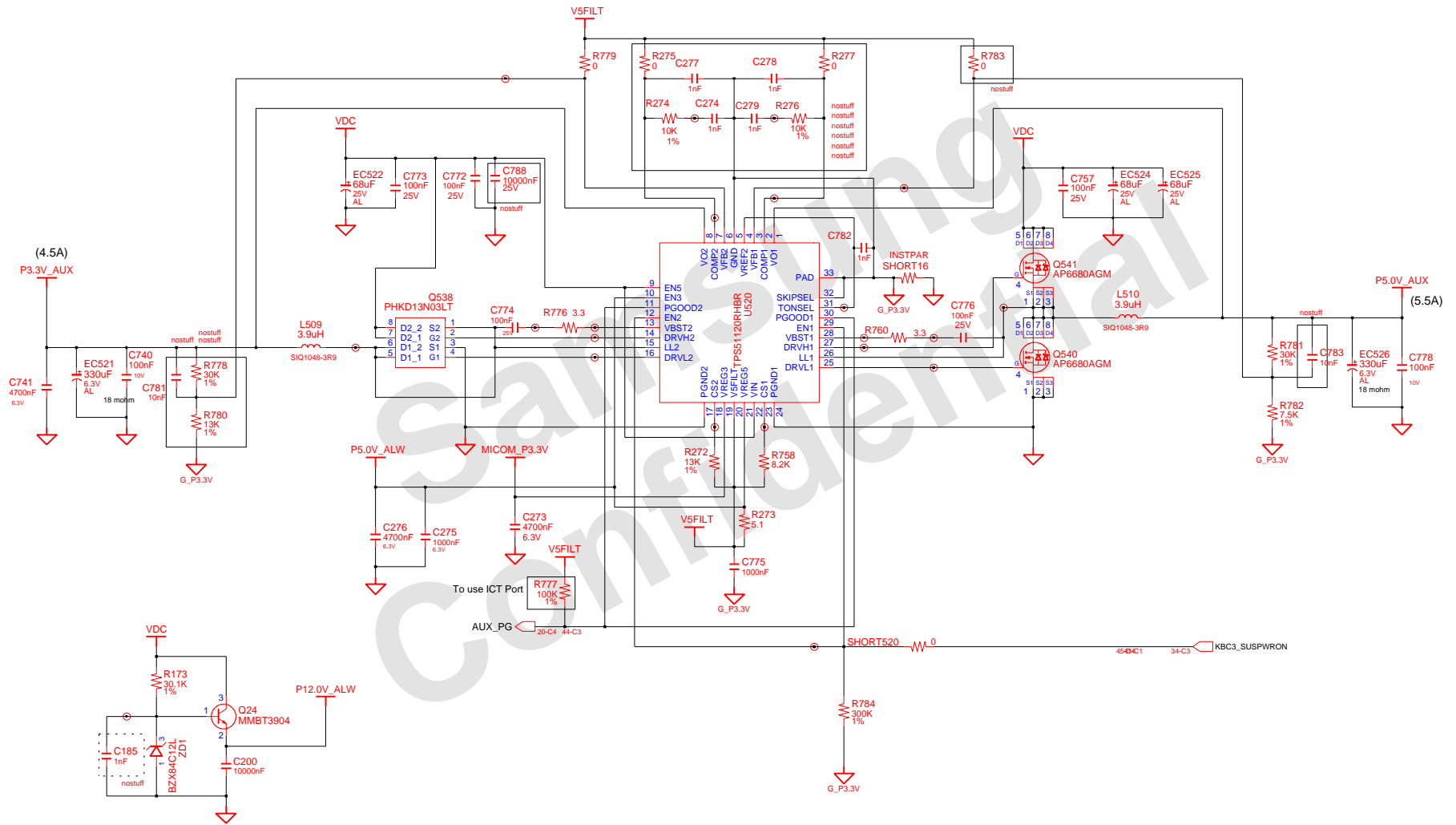
ICHG=2.5A FOR 6 & 9 CELLS
 VCHG=12.94V
 ILIMIT=2.90A

Adapter configuration			
60W		90W	
Value	SEC Code	Value	SEC Code
R1	100Kohm	200Kohm	2007-007334

GRW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN CHARGER	SAMSUNG ELECTRONICS PART NO. BA41-00791A
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 38 OF 47		

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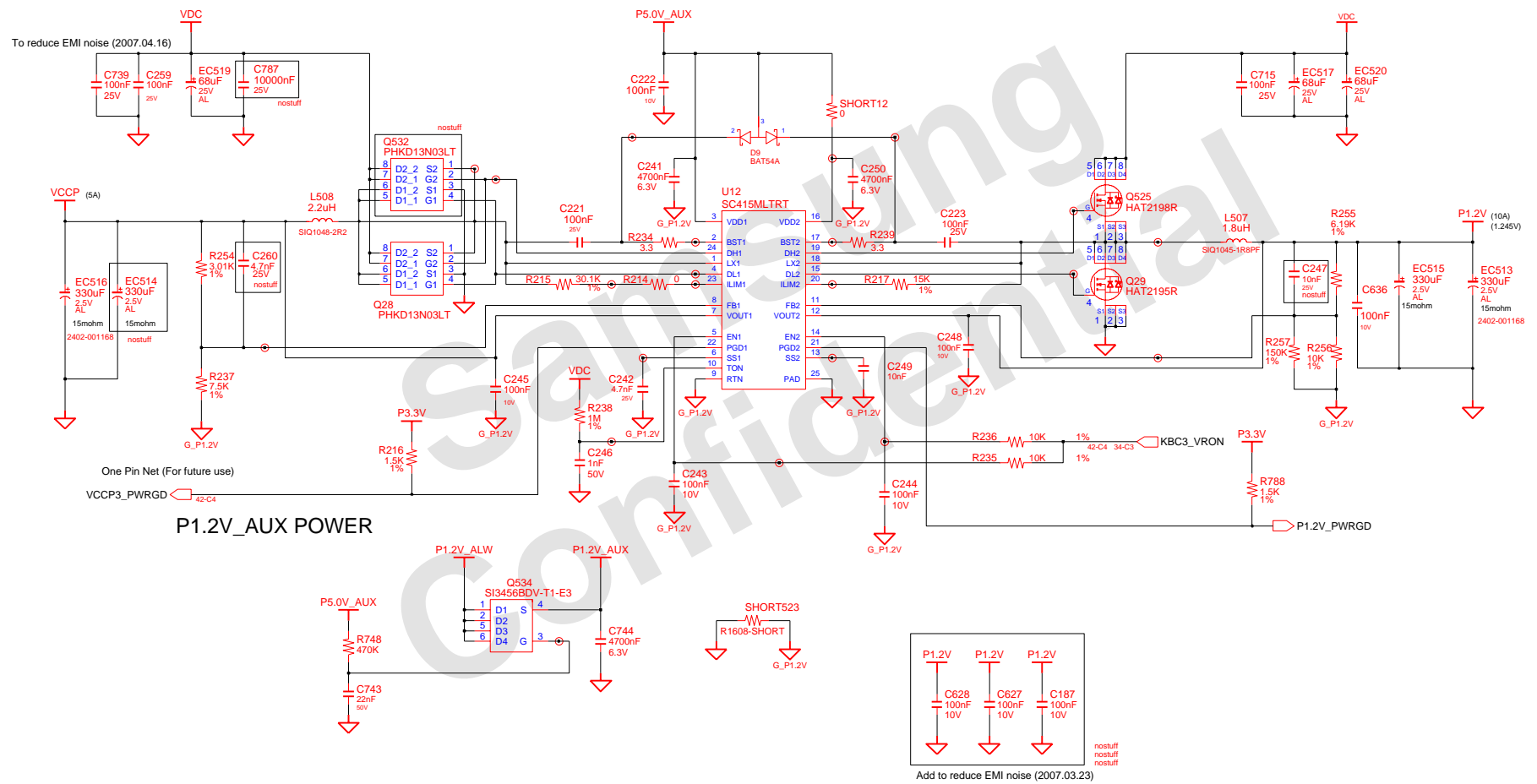
P3.3V_AUX & P5V_AUX



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) POWER P3.3V_AUX & P5V_AUX	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	REV		
APPROVAL	SJ PARK	REV	1.0	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 39 OF 47
MODULE CODE	undefined			PART NO. BA41-00791A		

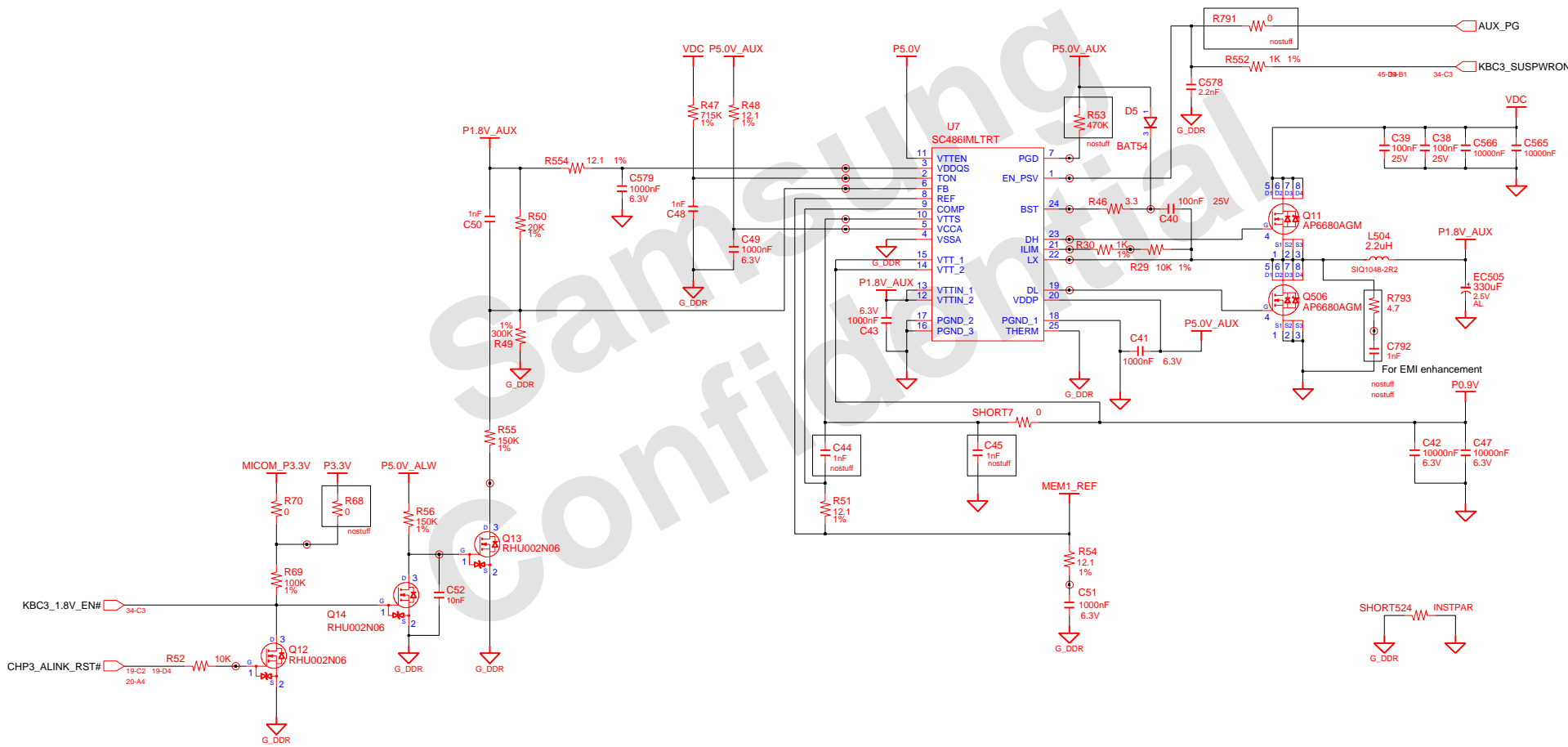
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P1.2V & VCCP_CORE(1.05V)



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) POWER	SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV. STEP	MP	REV		
APPROVAL	SJ PARK	REV	1.0	P1.2V & P1.2V_AUX & VCCP		PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	40	OF 47

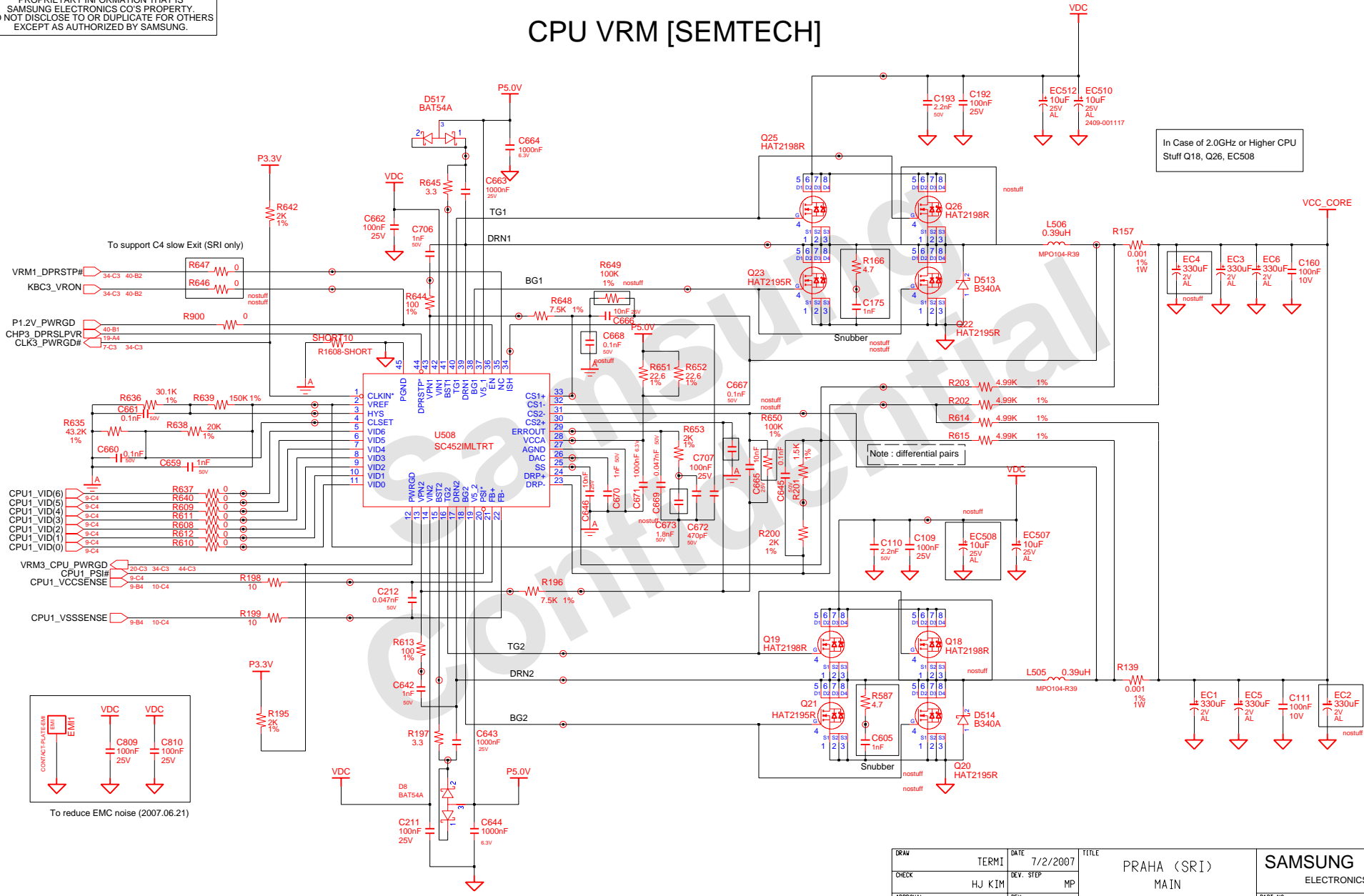
DDR2 Power



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS	
CHECK	HJ KIM	DEV. STEP	MP		MAIN		
APPROVAL	SJ PARK	REV	1.0		DDR2 POWER	PARTNO.	
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM			BA41-00791A	
						PAGE	41 OF 47

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CPU VRM [SEMTECH]

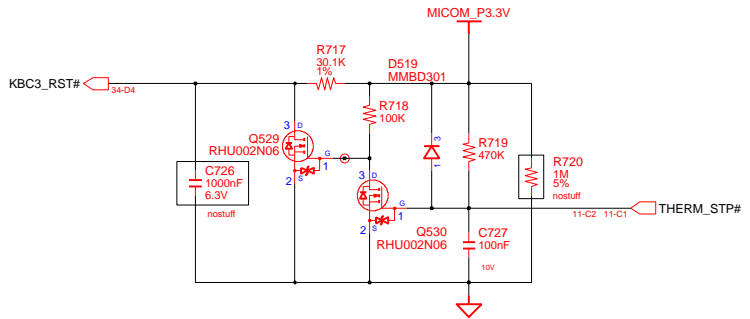


In Case of 2.0GHz or Higher CPU
 Stuff Q18, Q26, EC508

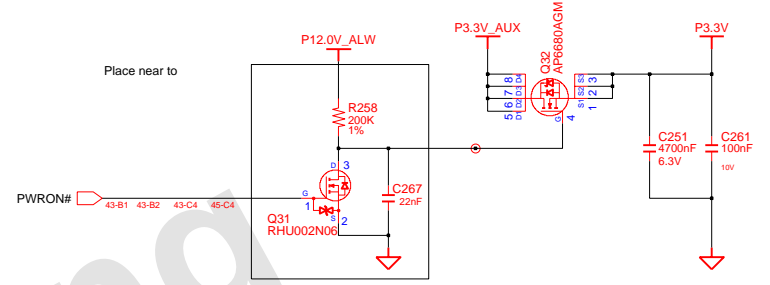
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN CPU VRM	SAMSUNG ELECTRONICS PART NO. BA41-00791A
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 42 OF 47		

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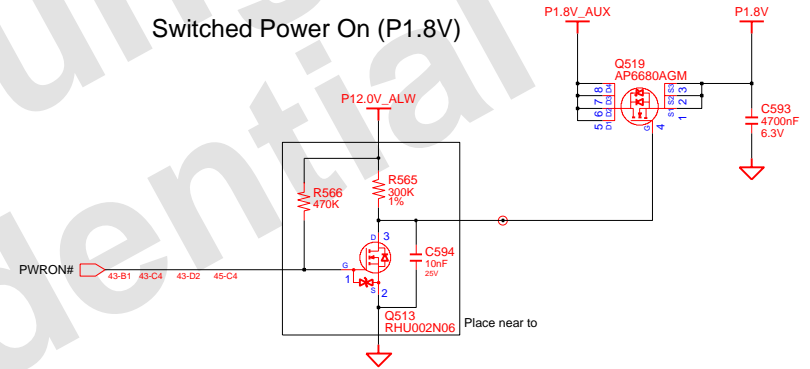
MICOM RESET



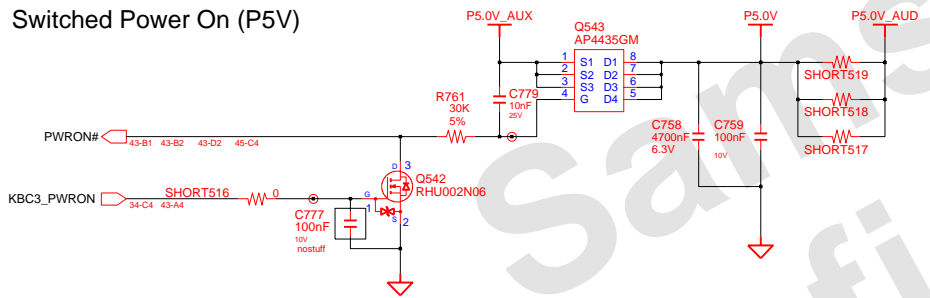
Switched Power On (P3.3V)



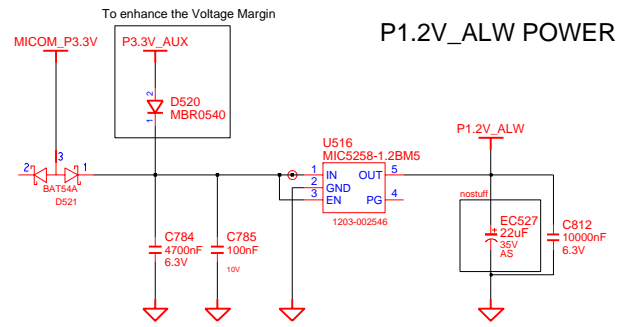
Switched Power On (P1.8V)



Switched Power On (P5V)



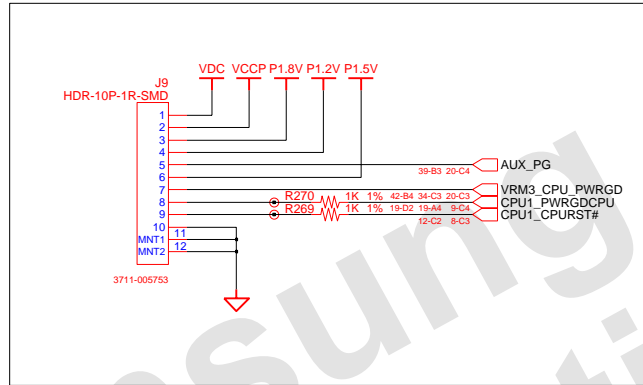
P1.2V_ALW POWER



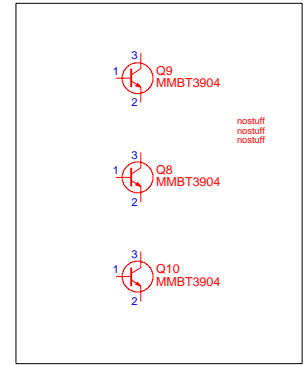
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	MICOM & SWITCHED POWER		
APPROVAL	SJ PARK	REV	1.0	PART NO.	BA41-00791A	
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	43	OF 47

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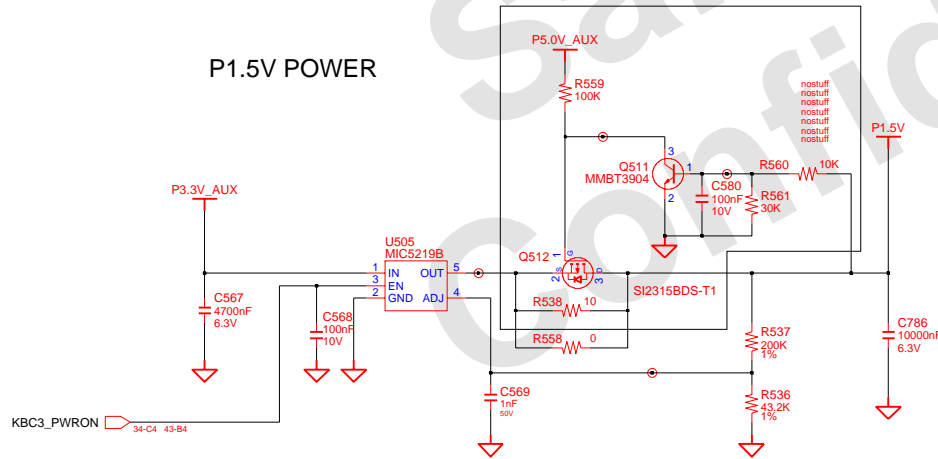
ICT PORT



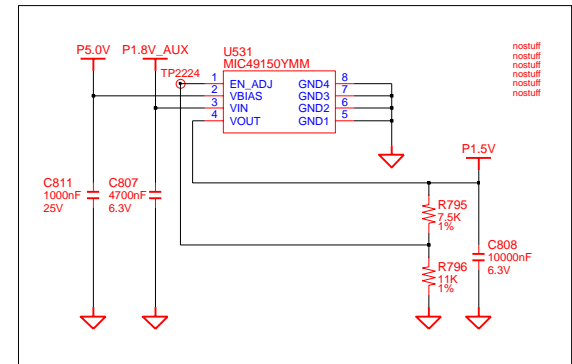
For Debugging



P1.5V POWER



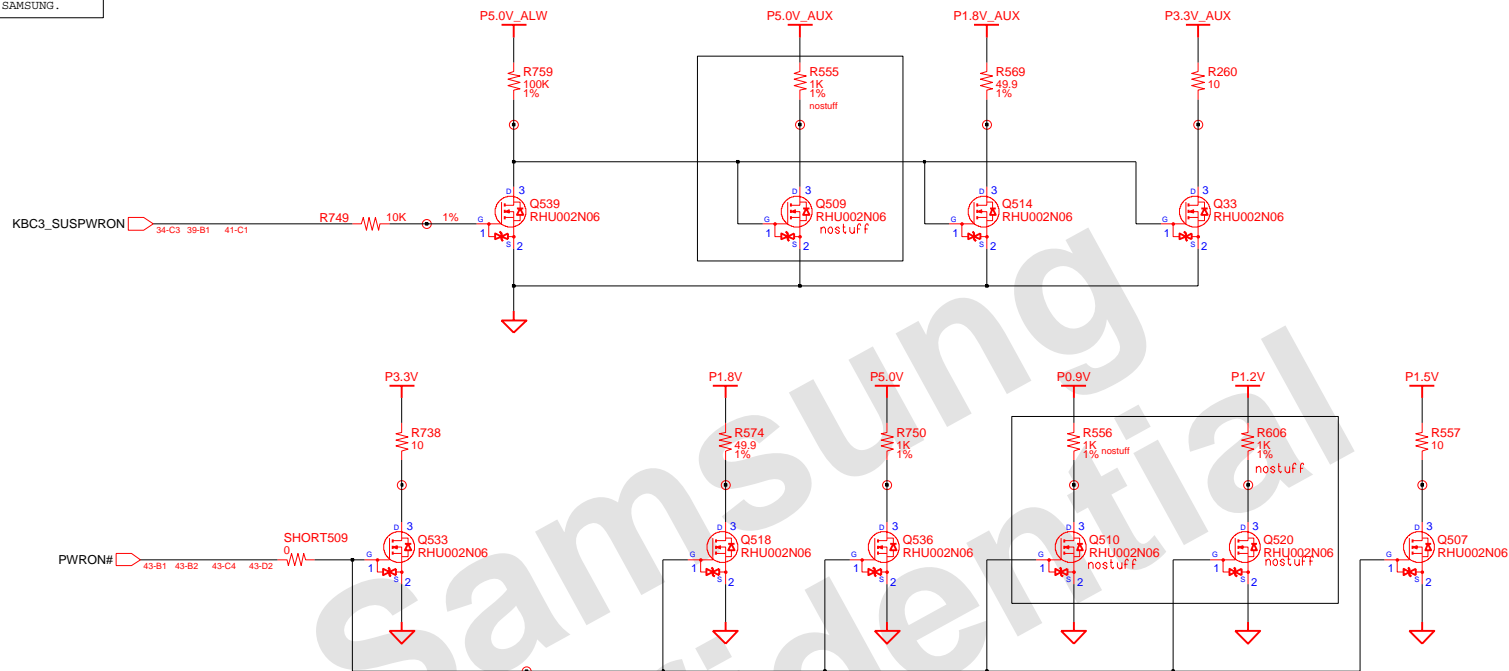
To make up PCI Express 1.5V rail current margin (nostuff)



GRAM	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		ICT PORT	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM			PAGE 44 OF 47

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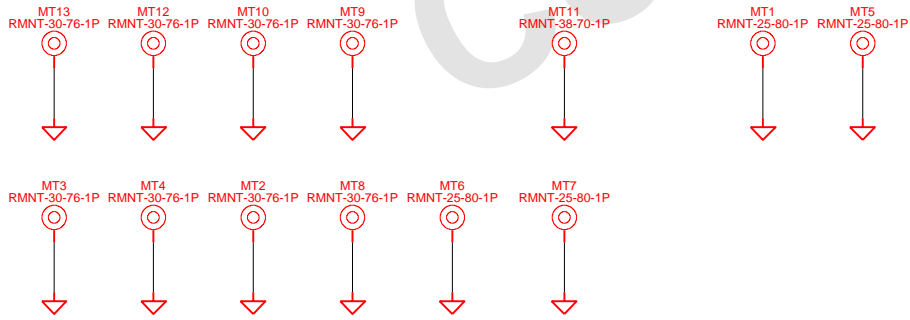
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System

Board

Located in lower left corner of PCB



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAINBD	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	POWER DRAW & MNT HOLE		
APPROVAL	SJ PARK	REV	1.0	PART NO. BA41-00791A		PAGE 45 OF 47
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM			

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REV1
 1 O
 2 O O3

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		TP	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	46	OF 47

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○AC_SDOUT
 ○AD3_SEL
 ○AUD3_EAPD#
 ○AUD3_PCBEPP#
 ○AUD5_LINE_OUT_L
 ○AUD5_LINE_OUT_R
 ○AUD5_MONO_OUT
 ○AUD5_SPK_L+
 ○AUD5_SPK_L-
 ○AUD5_SPK_R+
 ○AUD5_SPK_R-
 ○AUX_PG
 ○BAT3_DETECT#
 ○BAT3_SMCLK#
 ○BAT3_SMDATA#
 ○CHP3_ALINK_RST#
 ○CHP3_AZ_AUD_BCLK
 ○CHP3_AZ_AUD_RST#
 ○CHP3_AZ_AUD_SDO
 ○CHP3_AZ_AUD_SYNC
 ○CHP3_AZ_MDC_BCLK
 ○CHP3_AZ_MDC_RST#
 ○CHP3_AZ_MDC_SDO
 ○CHP3_AZ_MDC_SYNC
 ○CHP3_AZ_SDIO
 ○CHP3_AZ_SDIO1
 ○CHP3_BIOSWP#
 ○CHP3_DPRSPLPWR
 ○CHP3_NBRST#
 ○CHP3_SATALED#
 ○CHP3_SBPME#
 ○CHP3_SBTMRTRIP#
 ○CHP3_SERIRO
 ○CHP3_SLP3#
 ○CHP3_SLP35#
 ○CHP3_SPKR
 ○CHP3_SUSSTAT#
 ○CPU1_A20M#
 ○CPU1_ADS#

 ○CPU1_BNR#
 ○CPU1_BPRI#
 ○CPU1_BREQ#
 ○CPU1_BSEL0
 ○CPU1_BSEL1
 ○CPU1_BSEL2
 ○CPU1_CPURST#
 ○CLK3_DBGCLPC
 ○CLK3_IQH14
 ○CLK3_NB14M
 ○CLK3_PCLKMICOM
 ○CLK3_PWRGD#
 ○CLK3_USB48

 ○CPU1_DBSY#
 ○CPU1_DEFER#
 ○CPU1_DPRSPTP#
 ○CPU1_DPSP#
 ○CPU1_DPWR#
 ○CPU1_DRDY#

○CPU1_FERR#
 ○CPU1_HIT#
 ○CPU1_HITM#
 ○CPU1_IGNNE#
 ○CPU1_INIT#
 ○CPU1_INTR#
 ○CPU1_LOCK#
 ○CPU1_NMI#
 ○CPU1_PSI#
 ○CPU1_PWRGDCCPU

 ○CPU1_RS0#
 ○CPU1_RS1#
 ○CPU1_RS2#
 ○CPU1_SLP#
 ○CPU1_SMI#
 ○CPU1_TCK
 ○CPU1_TDI
 ○CPU1_THRMTRIP#
 ○CPU1_TMS
 ○CPU1_TRDY#
 ○CPU1_TRST#
 ○CPU1_VCCSENSE
 ○CPU1_VID(0)
 ○CPU1_VID(1)
 ○CPU1_VID(2)
 ○CPU1_VID(3)
 ○CPU1_VID(4)
 ○CPU1_VID(5)
 ○CPU1_VID(6)
 ○CPU1_VSSSENSE
 ○CPU2_THERMIDA
 ○CPU2_THERMDC
 ○CPU3_THRMTRIP#
 ○CRT3_BLUE
 ○CRT3_DDCCLK
 ○CRT3_DODDATA
 ○CRT3_GREEN
 ○CRT3_RED
 ○CRT5_HSYNC
 ○CRT5_VSYNC
 ○CTRL18_25
 ○CTRL12
 ○EXP3_CLKREQ#
 ○EXP3_CPPE#

○EXP3_CPUSB#
 ○EXP3_PPERST#
 ○CPU1_HITM#
 ○FANS_FBEEP#
 ○FANS_VDD
 ○GPI01
 ○HP_OUT_L
 ○HP_OUT_R
 ○ITP3_DBRESET#
 ○ITP3_SYSRST#
 ○JCK_SENS_A
 ○JCK_SENS_HP#
 ○JCK_SENS_MIC#
 ○KBC3_18V_EN#
 ○KBC3_A20G
 ○KBC3_BKLTON
 ○KBC3_CAPSLED#
 ○KBC3_CHGEN
 ○KBC3_CPURST#
 ○KBC3_EXTSMI#
 ○KBC3_LED_ACIN#
 ○KBC3_LED_CHARGE#
 ○KBC3_LED_POWER#
 ○KBC3_NBPWRGD
 ○KBC3_NUMLED#
 ○KBC3_PWRBTN#
 ○KBC3_PWRON
 ○KBC3_SMRST#
 ○KBC3_RST#
 ○KBC3_RUNSCI#
 ○KBC3_SCLE#
 ○KBC3_SMCLK#
 ○KBC3_SMDATA#
 ○KBC3_SUSPWRON
 ○KBC3_THERM_SMCLK
 ○KBC3_THERM_SMDATA
 ○KBC3_VIRON
 ○KBC3_WAKESCI#
 ○KBC5_KSI(0)
 ○KBC5_KSI(1)
 ○KBC5_KSI(2)
 ○KBC5_KSI(3)
 ○KBC5_KSI(4)
 ○KBC5_KSI(5)
 ○KBC5_KSI(6)
 ○KBC5_KSI(7)
 ○KBC5_KSI(8)
 ○KBC5_KSI(9)
 ○KBC5_KSO(1)
 ○KBC5_KSO(10)
 ○KBC5_KSO(11)
 ○KBC5_KSO(12)
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 ○KBC5_KSO(14)
 ○KBC5_KSO(15)
 ○KBC5_KSO(2)
 ○KBC5_KSO(3)
 ○KBC5_KSO(4)
 ○KBC5_KSO(5)
 ○KBC5_KSO(6)
 ○KBC5_KSO(7)
 ○KBC5_KSO(8)
 ○KBC5_KSO(9)
 ○KBC5_TCLK
 ○KBC5_TDATA

○LCD3_BKLTON
 ○LCD3_EDID_CLK
 ○LCD3_EDID_DATA
 ○CD3_VDDEN
 ○ID3_SWITCH#
 ○PC3_LAD(0)
 ○PC3_LAD(1)
 ○PC3_LAD(2)
 ○PC3_LAD(3)
 ○PC3_LFRAME#
 ○MCD3_SDCD#
 ○MCD3_SDCLK
 ○MCD3_SDCMD0
 ○MCD3_SDDATA0
 ○MCD3_SDDATA1
 ○MCD3_SDDATA2
 ○MCD3_SDDATA3
 ○MCD3_SDWP

○MIC1
 ○MIC2
 ○MINIPCIE3_CLKREQ#
 ○MIO3_BUTTON#

○LAN3_VPDCLK
 ○LAN3_VPDATA
 ○LAN3_WAKE#

○LCD3_BKLCTRL
 ○LCD3_BKLTON



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS	
CHECK	HJ KIM	DEV. STEP	MP				
APPROVAL	SJ PARK	REV	1.0			PART NO.	
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	47	OF	47

