HABANA

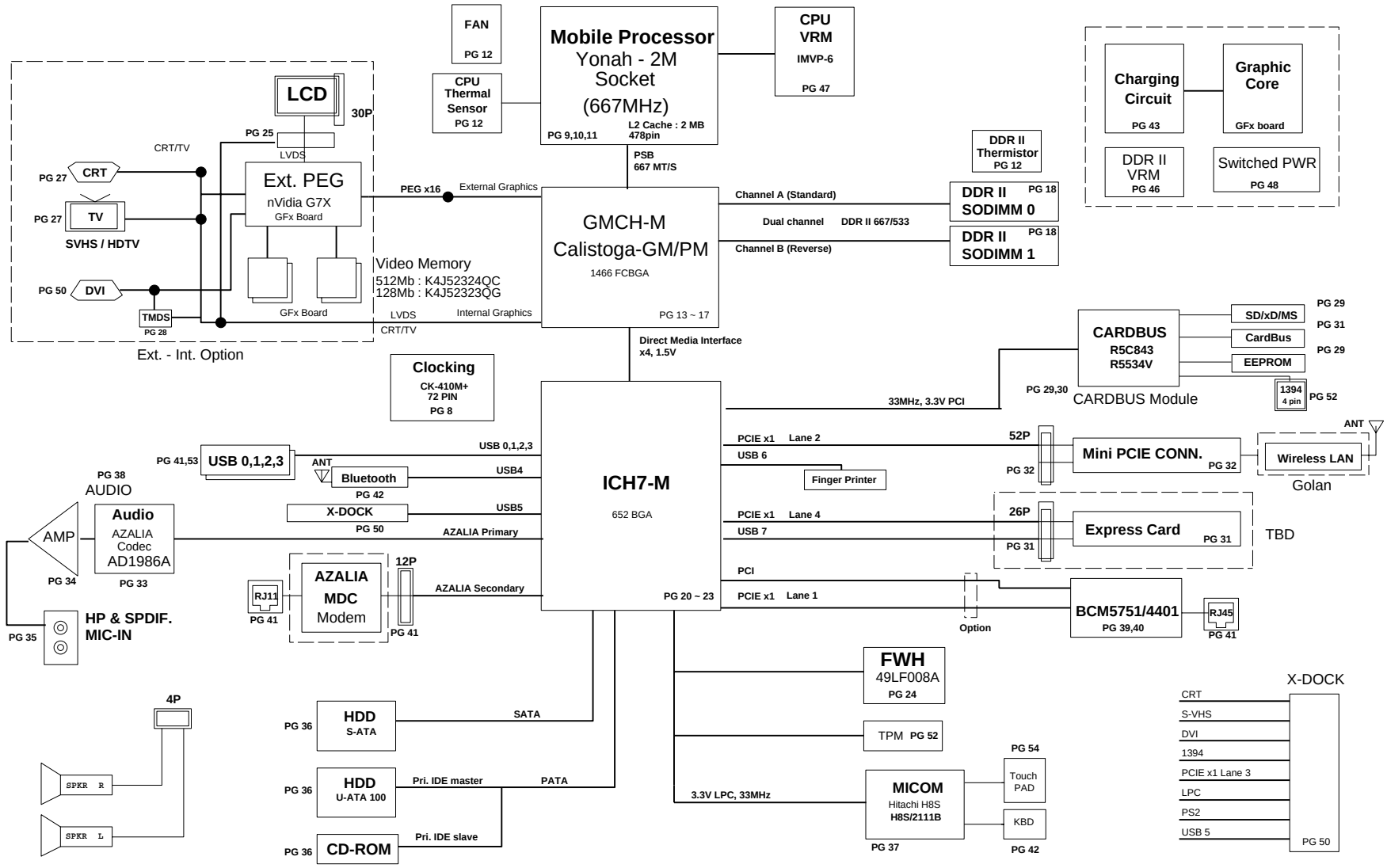
CPU : Intel Yonah -2M/1M
Chip Set : Intel Calistoga PM/GM & ICH7-M
Remarks : Mobility Platform

Model Name : HABANA
PBA Name : MAIN
PCB Code : BA41-#####A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2005.11.16

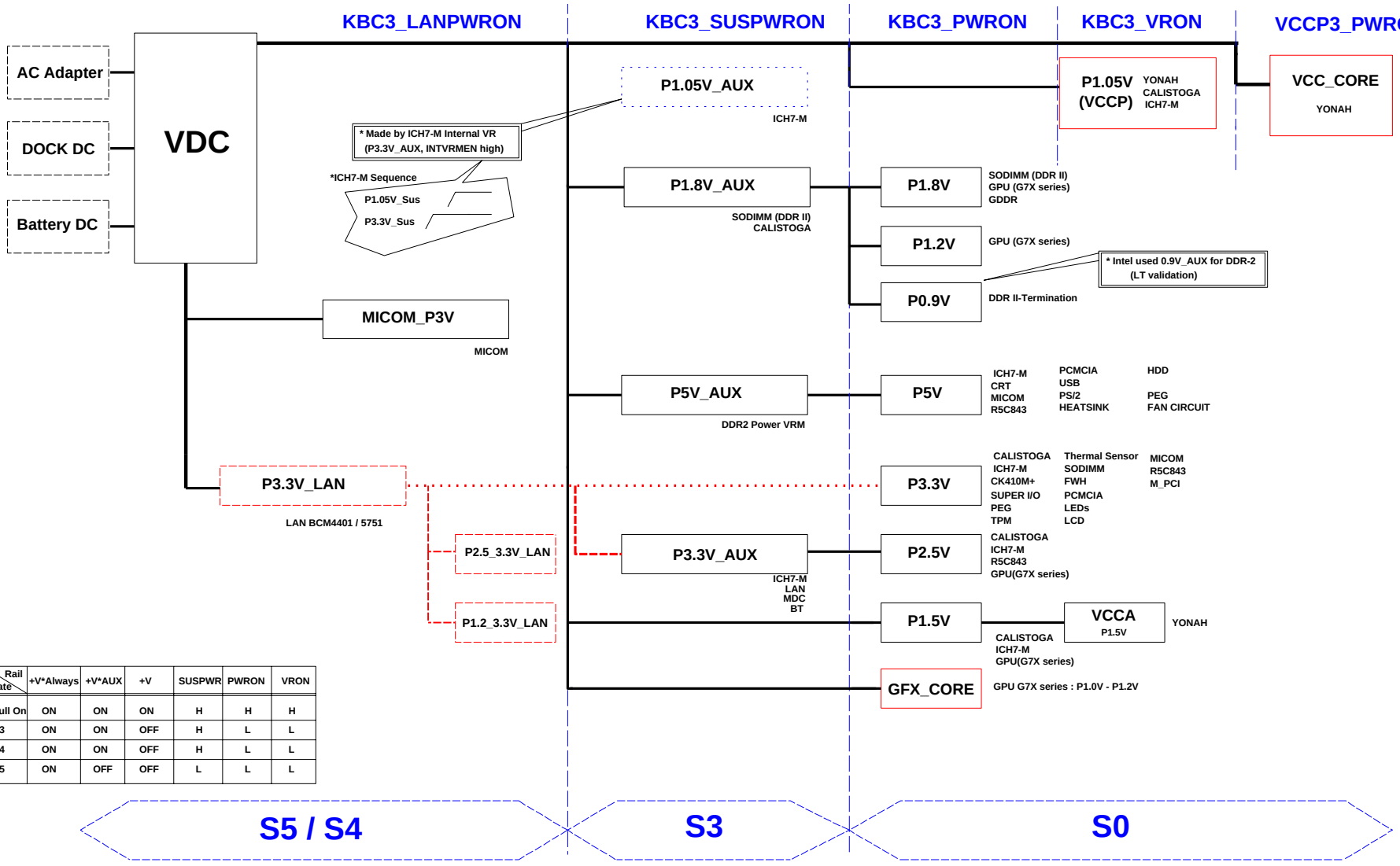
DRAW	CHECK	APPROVAL
SE LEE	ES CHO	BL LEE

■ ***Owner : SEC Mobile R & D*** ***Signature :*** ***X***

Table of Contents

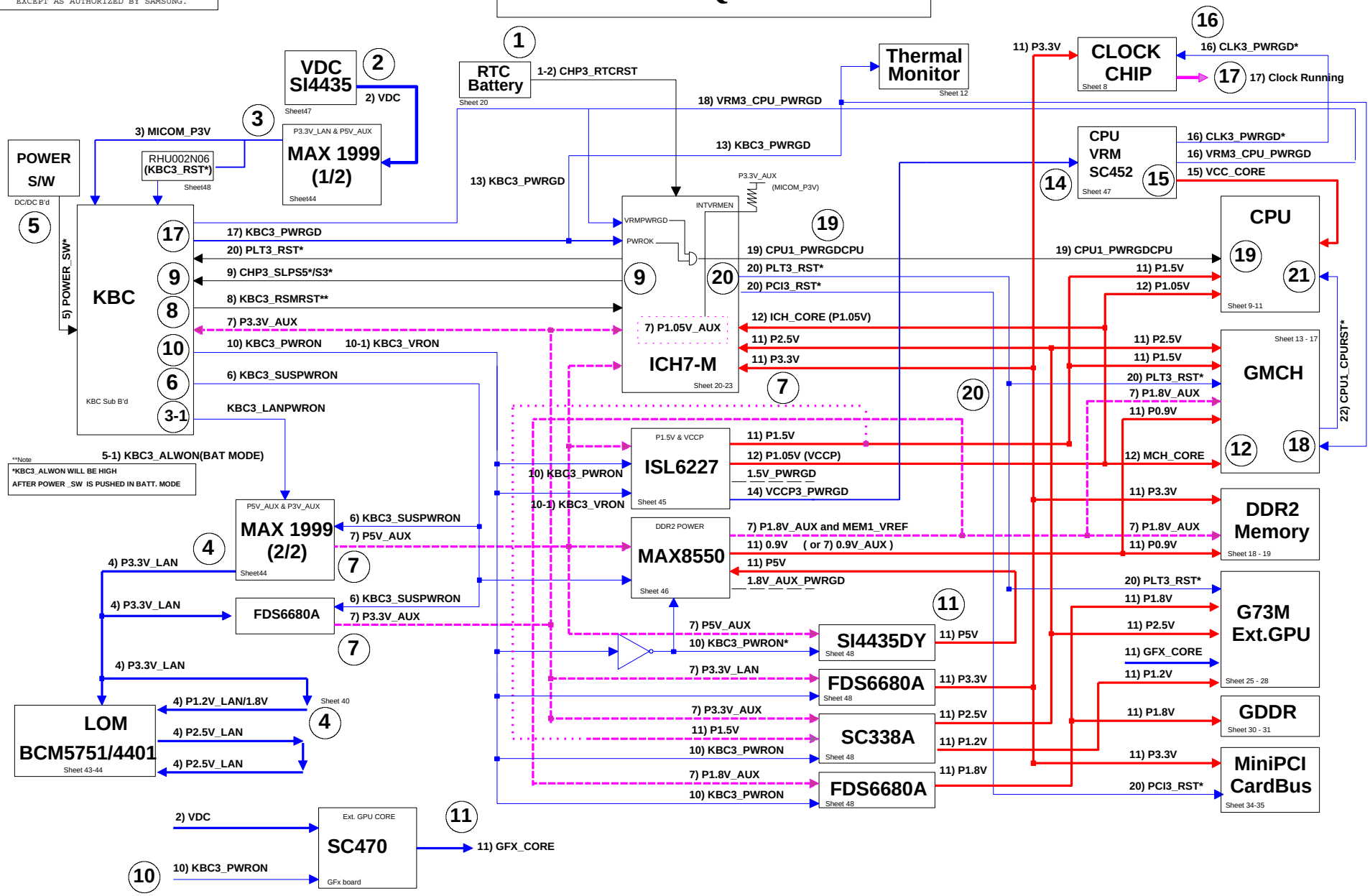


Power Diagram



Rail / State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

POWER SEQUENCE Rev. 0.8



POWER RAILS ANALYSIS Rev. 0.8

S0 - S5
S0 - S3
OFF IN S3 - S5

This sheet should be updated !!!

Adapter
Battery

3.3V_AUX (TBD A)
5V_AUX (TBD A)
MICOM 3V (TBD A)
1.8V (TBD A)
CPU CORE (TBD A)
1.05V (TBD A)
1.5V (TBD A)
2.5V (TBD A)
3.3V (TBD A)
5V (TBD A)
1.8V_AUX (TBD A)
0.9V_AUX (TBD A)
P3.3V_ALW (TBD A)
P2.5V_ALW (TBD A)
P1.2V_ALW (TBD A)
VDC INV (TBD A)
PEX IO (TBD A)
VGA CORE (TBD A)
RTC_Battery

1.05V — 0.1 A (TBD) — ITP

CPU CORE — 28A
1.05V (VCCP) — 2.5A
1.5V — 0.3 A (TBD)
Yonah-2M (31 W)

1.05V (MCH CORE) — 4.8 A (TBD)
1.05V (VCCP) — 2A
1.5V — 1.3 A (TBD)
2.5V — 0.2 A (TBD)
3.3V — 0.12 A (TBD)
1.8V_AUX — 2.7 A (TBD)
*1.5V : 13.4 A (TBD)
Calistoga GMCH (8 - 8.5 W)

1.05V (ICH CORE) — 1.3 A (TBD)
1.05V (VCCP) — 0.4 A (TBD)
1.5V — 1.3 A (TBD)
3.3V — 0.2 A (TBD)
3.3V_AUX — 0.12 A (TBD)
5V — 2.7 A (TBD)
5V_AUX — 2.7 A (TBD)
RTC_Battery — 0.01 A (TBD)
ICH7-M (~ 2.0 W)

1V-1.2V (VGA CORE) — 13A
1.8V — 2.5A
2.5V — 0.28 A (TBD)
1.2V (PEX IO,PLLVDD) — 1.9A
3.3V — 0.8A
G7X Ext.GFX

1.8V_AUX — 3.1 A (TBD)
0.9V_AUX — 1 A (TBD)
DDR-2 (Dual slots) (~ 5.0 W)

1.8V — 3.1 A (TBD) — **GDDR**

3.3V (LCD 3V, 0.23A)
19V (VDC INV, 0.23A) — 0.7A / 0.5A (TBD) — **LCD**

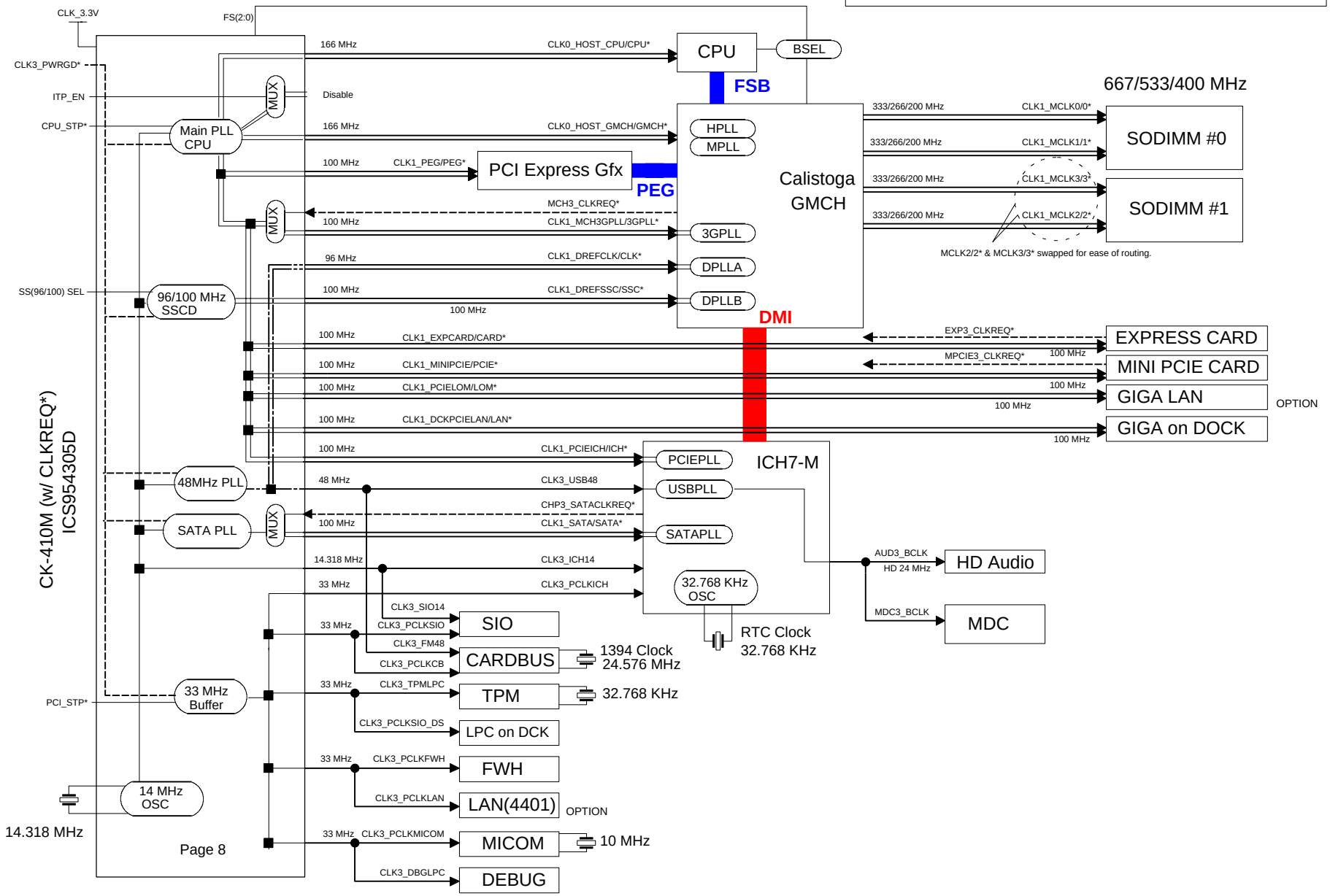
P1.2V_ALWAYS
P2.5V_ALWAYS
P3.3V_ALWAYS
TBD A (TBD)
TBD A (TBD)
TBD A (TBD)
LAN (TBD)

3.3V — 0.1 A (TBD) — Thermal Sensor
3.3V — 0.02 A (TBD) — **SIO**
3.3V — 0.3 A (TBD) — **CLOCK**
3.3V — 0.2 A (TBD) — **KeyBoard**
3.3V — 0.02 A (TBD) — **FWH**
3.3V / 5V — 0.06 A (TBD) / 0.07 A (TBD) — **HD Audio**
5V / 5V — 1 A (TBD) / 1 A (TBD) — HDD / ODD — **PATA**
5V — 1A — **SATA HDD**
5V — 0.3A — **FAN**
5V — 1 A (TBD) — **Audio AMP**
5V — 2 A (TBD) — **USB (x 4)**
5V — 0.2 A (TBD) — **Touch Pad**

MICOM 3V / 3.3V — 0.08 A (TBD) / 0.08 A (TBD) — **KBC**
MICOM 3V — 0.1 A (TBD) — **PWR LED**
1.8V / 3.3V / 3.3V_AUX — 0.14 A (TBD) / 0.1 A (TBD) / 0.1 A (TBD) — **R5C843**
3.3V_AUX / 5V_AUX — 1.2 A (TBD) / 1 A (TBD) — **Card Bus**
3.3V / 3.3V_AUX / 1.5V — 0.7 A (TBD) / 0.2 A (TBD) / 0.4 A (TBD) — **Mini PCIE**
3.3V / 3.3V_AUX / 5V — 0.3 A (TBD) / 0.01 A (TBD) / 0.3 A (TBD) — **MDC**

Value by Datasheet/Application notes (Value by measurement)

CLOCK DISTRIBUTION Rev. 0.7



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	E,F,G
LAN	AD21	1	G
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308~1.068V)
VCCP	YONAH/CALISTOGA Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P5V	5.0V switched power rail (off in S3-S5)
MEM1_VREF	0.9V power rail (off in S4-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P5V_ALWS	5V power rail (Always On)
P12V_ALWS	12V power rail (Always On)

I²C / SMB Address

Devices	Address	Hex	Bus
ICH7	Master	-	SMBUS Master
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A4h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

Devices	Address	Hex	Bus
MICOM	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	0101 111X	5Eh	Thermal Sensor
BATTERY	-	-	-
GFX thermal sensor	1001 000X	90h	Thermal Sensor

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0,1	SYSTEM PORT A
2,3	SYSTEM PORT B
3	SYSTEM PORT C
4	BLUETOOTH
5	PORT REPLICATOR
6	FINGER PRINT
7	EXPRESS CARD

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other criticial subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.

CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH7-M	Real Time Clock
Crystal	10MHz	MICOM	H8S/2111B
Crystal	14.318MHz	CLOCK-Generator	CK-410M+
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	BROADCOM LAN
Crystal	24MHz	Finger Printer	AES2501A

CPU Core Voltage Table IMVP-6

Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 **1** **1**	1.4125 V	0 1 0 1 **1** **1**	0.9125 V	1 0 1 1 0 **0** 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 **1** 0 1 **1** **1**	1.2125 V	0 1 **1** 1 1 **1** **1**	0.7125 V	1 1 **0** 1 0 0 **0**	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 **1** 0 0 **1** **1** 1	1.0125 V	1 **0** 0 1 **1** **1** 1	0.5125 V	1 **1** 1 1 0 **0** 0	0.0000 V
		1 **0** 1 0 **0** **0** 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 0 0 0	0.0000 V
				1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active	
DPRSLPVR	0
DPRSTP*	1
PSI2*	0 or 1

Deeper Slp	
DPRSLPVR	1
DPRSTP*	0
PSI2*	0 or 1

*"1111111" : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

FCTSEL1(43,44,47,48)	1 : 27M & SRC0	0 : DOT96 &LCD100
ITP_EN (5,6)	1 : CPU_ITP pair	0 : SRC pair

CPU	FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD

SILEGO : SLG84452

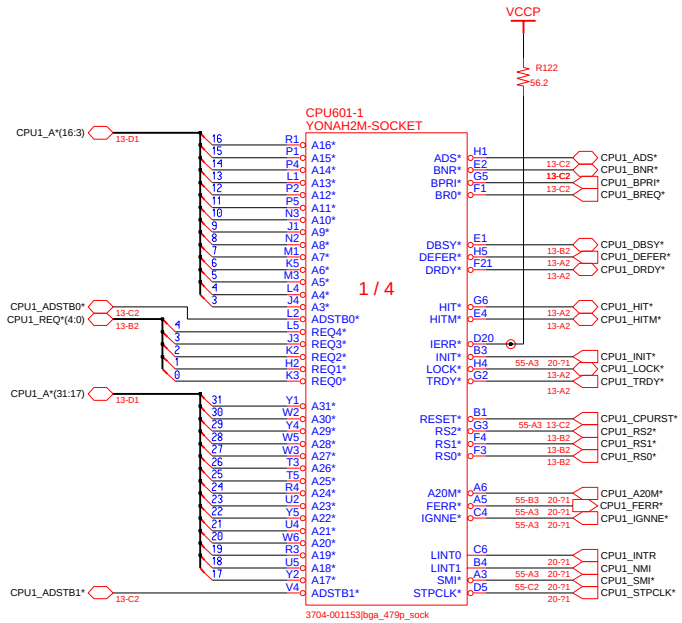
U9

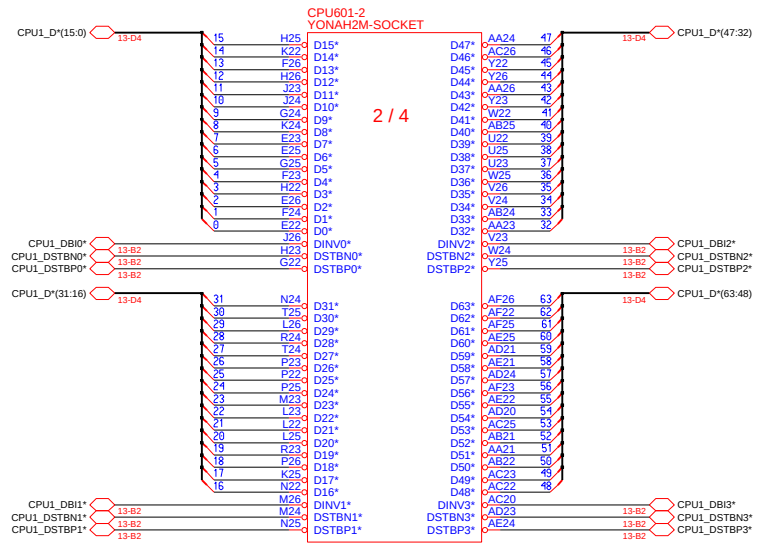
ICS954305D

Place 14.318MHz within 500mils of Clock chip

Place Termination close to CK-410M

CK-410M+	
w/ CLKREQ	ICS954305
w/ SS Clock	SLG8LP455
	CY28447





**NOTE

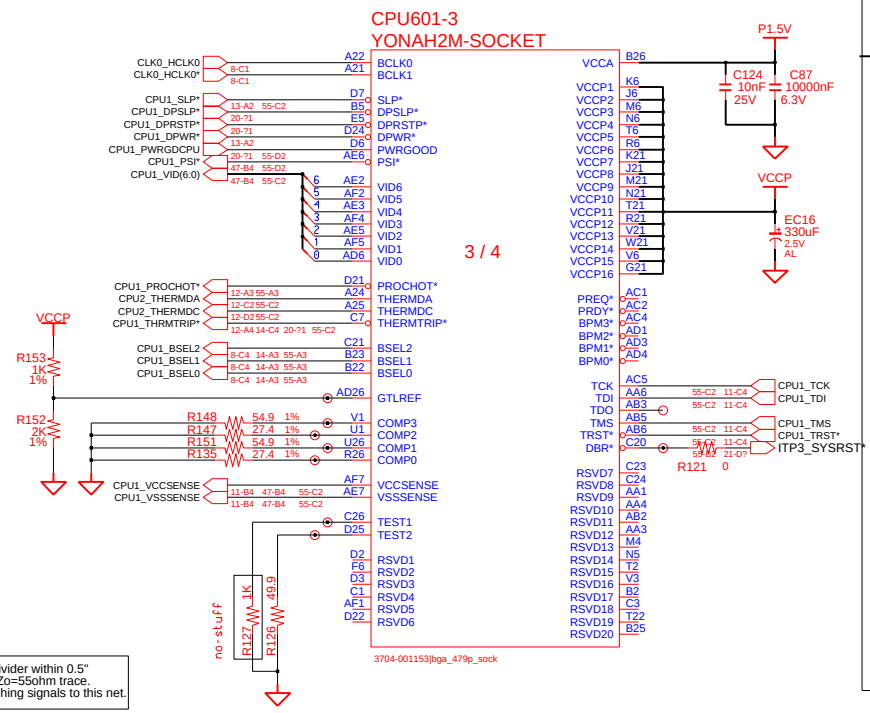
MT610 RMNT-25-45-1P

MT611 RMNT-25-45-1P

MT613 RMNT-25-45-1P

MT614 RMNT-25-45-1P

RHE SUPPORTER(CICHLID2 BASED)



GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

CPU Core Voltage Table IMVP-6

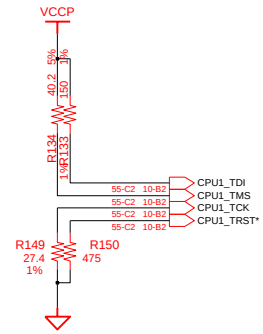
Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 **1** **1**	1.4125 V	0 1 0 1 1 **1** **1**	0.9125 V	1 0 1 1 0 **0** 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 **1** 0 1 **1** **1**	1.2125 V	0 1 **1** 1 1 **1** **1**	0.7125 V	1 1 **0** 1 0 0 **0**	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 **1** 0 0 **1** **1** 1	1.0125 V	1 **0** 0 1 **1** **1** 1	0.5125 V	1 **1** 1 1 0 **0** 0	0.0000 V
		1 **0** 1 0 **0** **0** 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

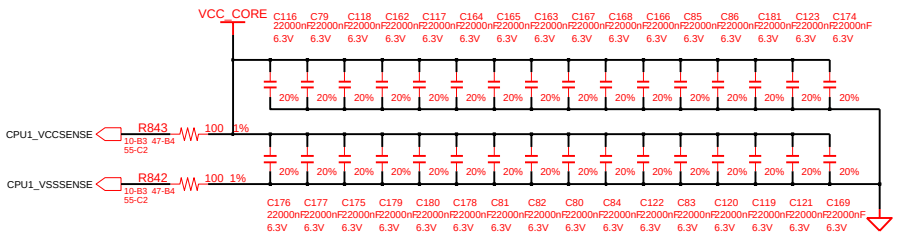
Active
DPRSLPVR 0
DPRSTP* 1
PSI2* 0 or 1

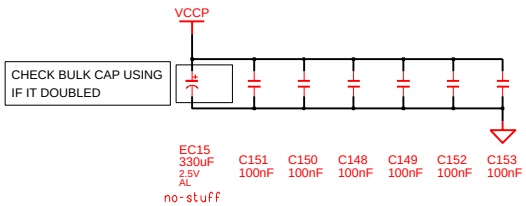
Deeper Slp
DPRSLPVR 1
DPRSTP* 0
PSI2* 0 or 1

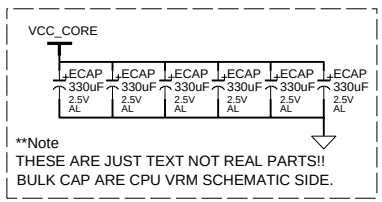
*"1111111" : 0V power good asserted.

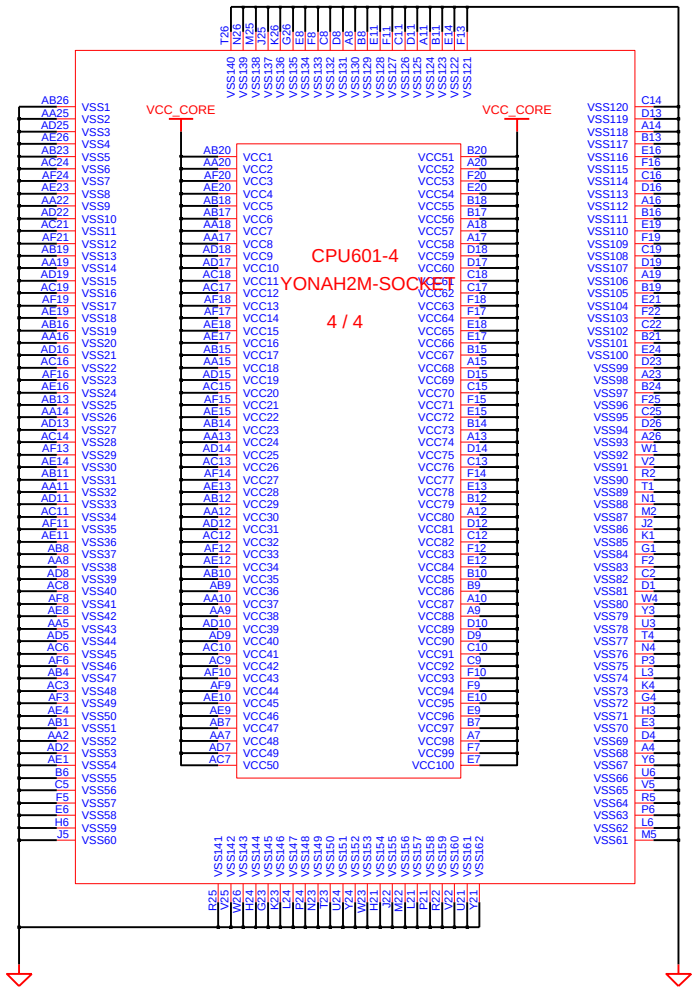
*Yonah Processor (2.33 GHz / 800 MHz : TBD)







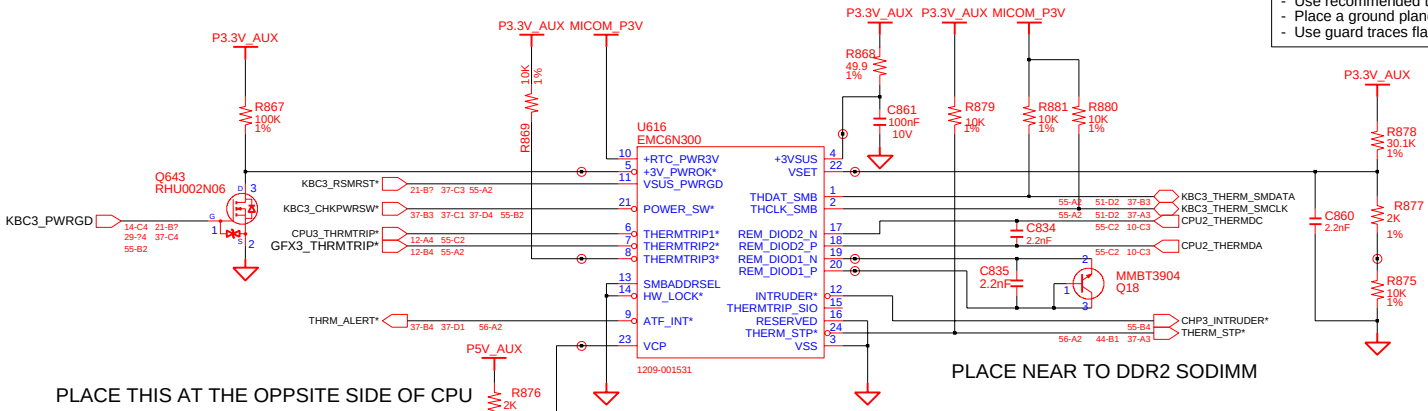




CPU / DDR2 Thermal Sensor

Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND



PLACE THIS AT THE OPPSITE SIDE OF CPU

PLACE NEAR TO DDR2 SODIMM

Vset = (Tp-75)/16 Where Tp=75 to 106 degree C

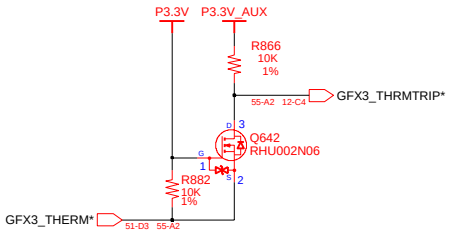
Set Trip point = 9-degreeC

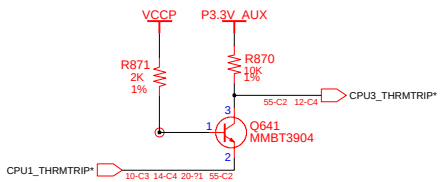
Vset = (90-75)/16 = 0.9375V

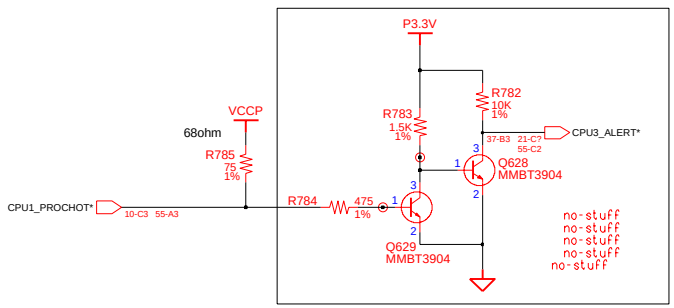
Guardian Temp-torelance = +/- 3 degree C

TH1:
Panasonic 1% 0603 10K ohm @ 25 degree C.P/N: ERTJ1VG103FA
Mitsubishi 1% 0603 10K ohm @ 25 degree C.P/N: TH11-3H103FT

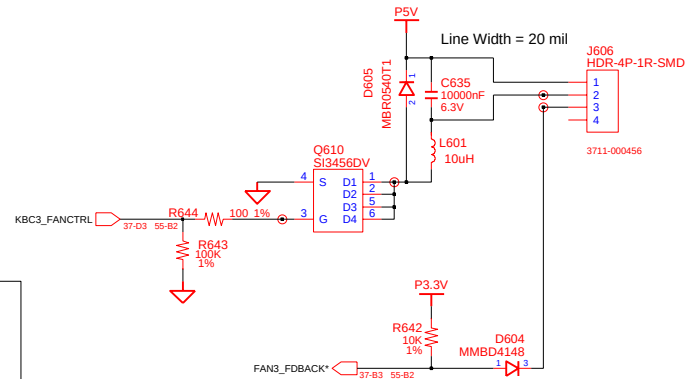
VCP voltage = 5V * TH1/(TH1+2.21K)
When TH1 is 10Kohm, VCP is 4.1V.
If TH1 is 1Kohm, VCP is 1.56V.

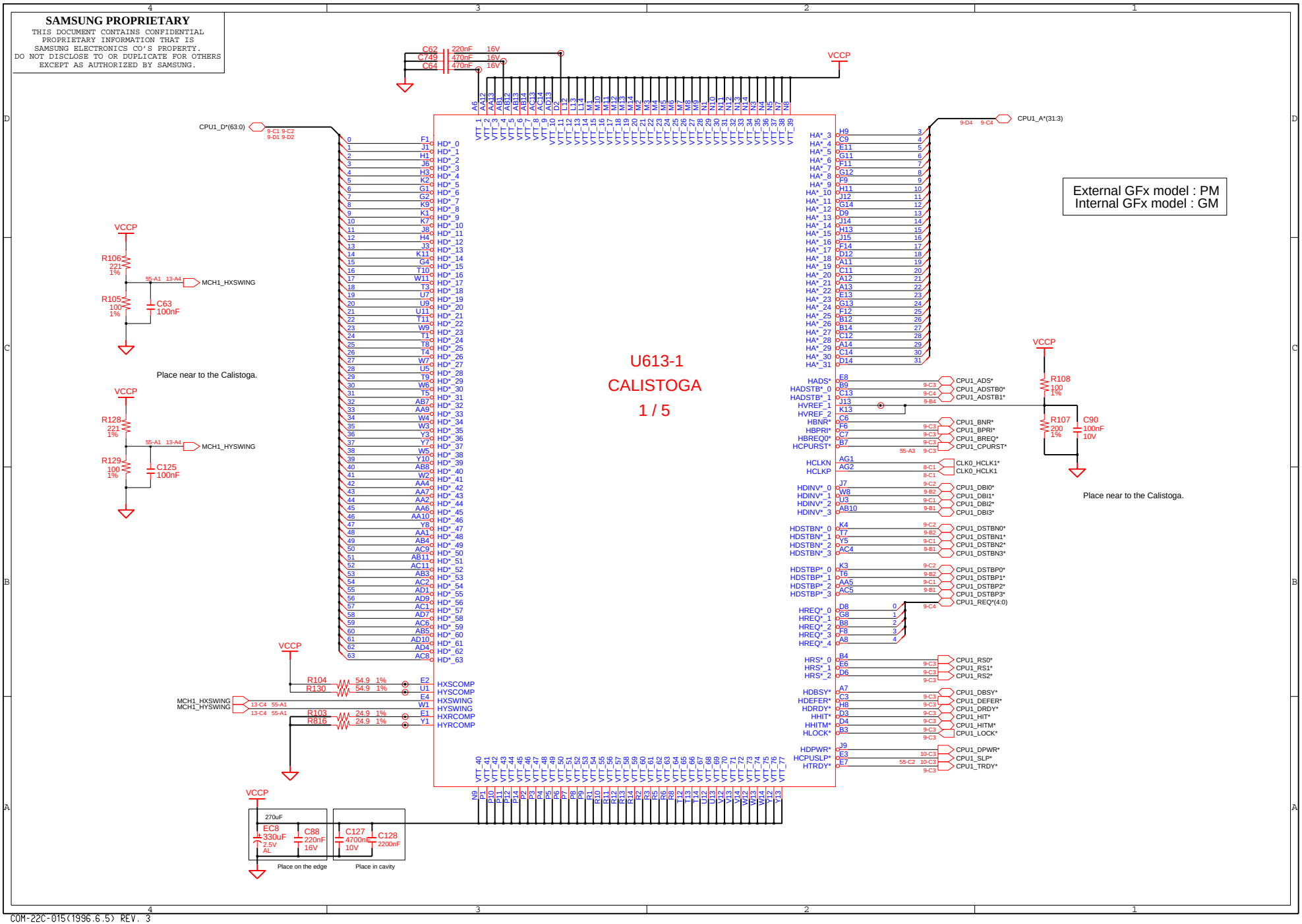






FAN Control Logic





CRT DISABLE GUIDE(FOR PM)

Signal	Recommendation
VCCA_CRTDAC	GMCH CORE
VSSA_CRTDAC	GND
VCC_SYNC	GND
HSYNC,VSYNC	GND
R,G,B PAIRS	GMCH CORE

U613-2

CALISTOGA

2 / 5

PCIE GFX

DMI

DDR MUX

CLK

PM

VGA

TV

LVDS

CFG

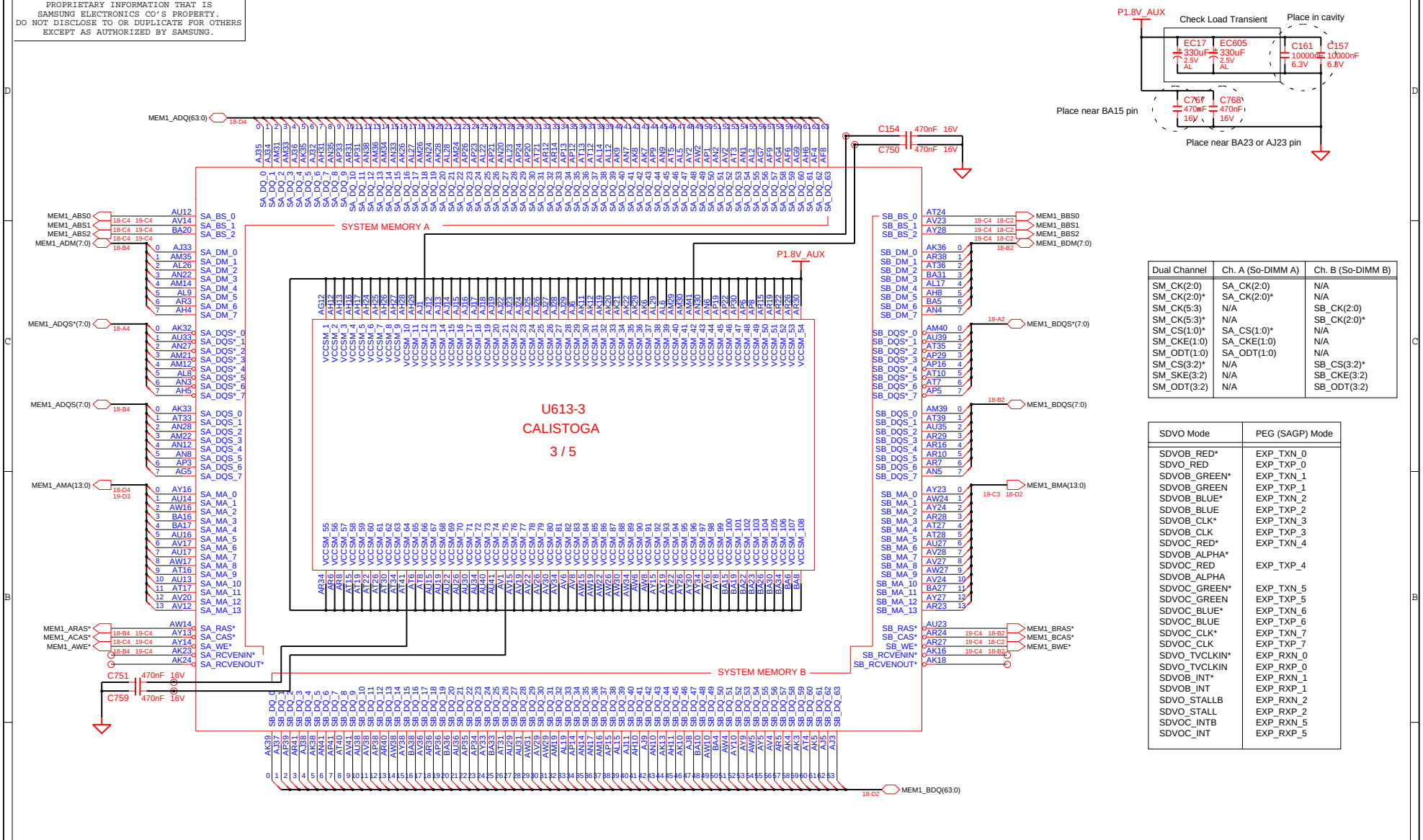
RSVD

NC

TVDAC_A : CVBS, Pb
TVDAC_B : Y
TVDAC_C : C, Pr

WHEN NOT USED(FOR PM)
LEFT AS NO CONNECTION

Route as short as possible



Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)*	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)*	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOB_ALPHA*	
SDVOC_RED	EXP_TXP_4
SDVOB_ALPHA	
SDVOC_GREEN*	EXP_TXN_5
SDVOC_GREEN	EXP_TXP_5
SDVOC_BLUE*	EXP_TXN_6
SDVOC_BLUE	EXP_TXP_6
SDVOC_CLK*	EXP_TXN_7
SDVOC_CLK	EXP_TXP_7
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

U613-4
CALISTOGA
4 / 5

Caps should be on top layer

Caps should be placed in cavity

Caps should be within 250mils of edge

100nF Caps used in 1.5V_DLVDS, 2.5V_ALVDS, 2.5V_TXLVDS, 2.5V_3GBG should be placed within 200mils of edge

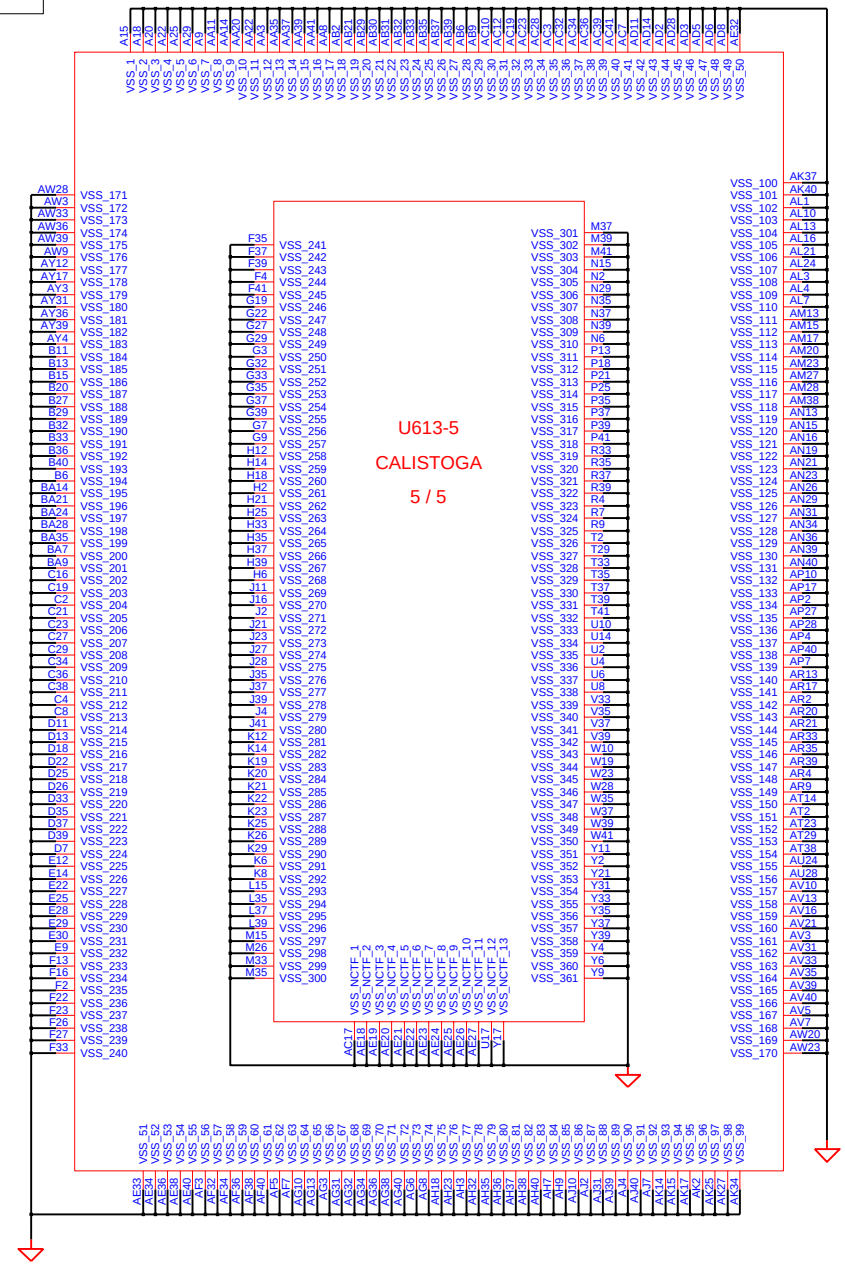
100nF Caps used in 1.5V_TVDAC, 1.5V_QTVDAC within 250mils of edge

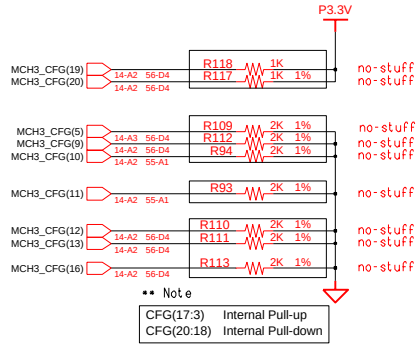
NO STUFF
Check Load Transient

100nF caps need to be located within 250mils

100nF caps need to be located as edge caps within 200mils

Why need LDO for TVDAC 3.3V ??

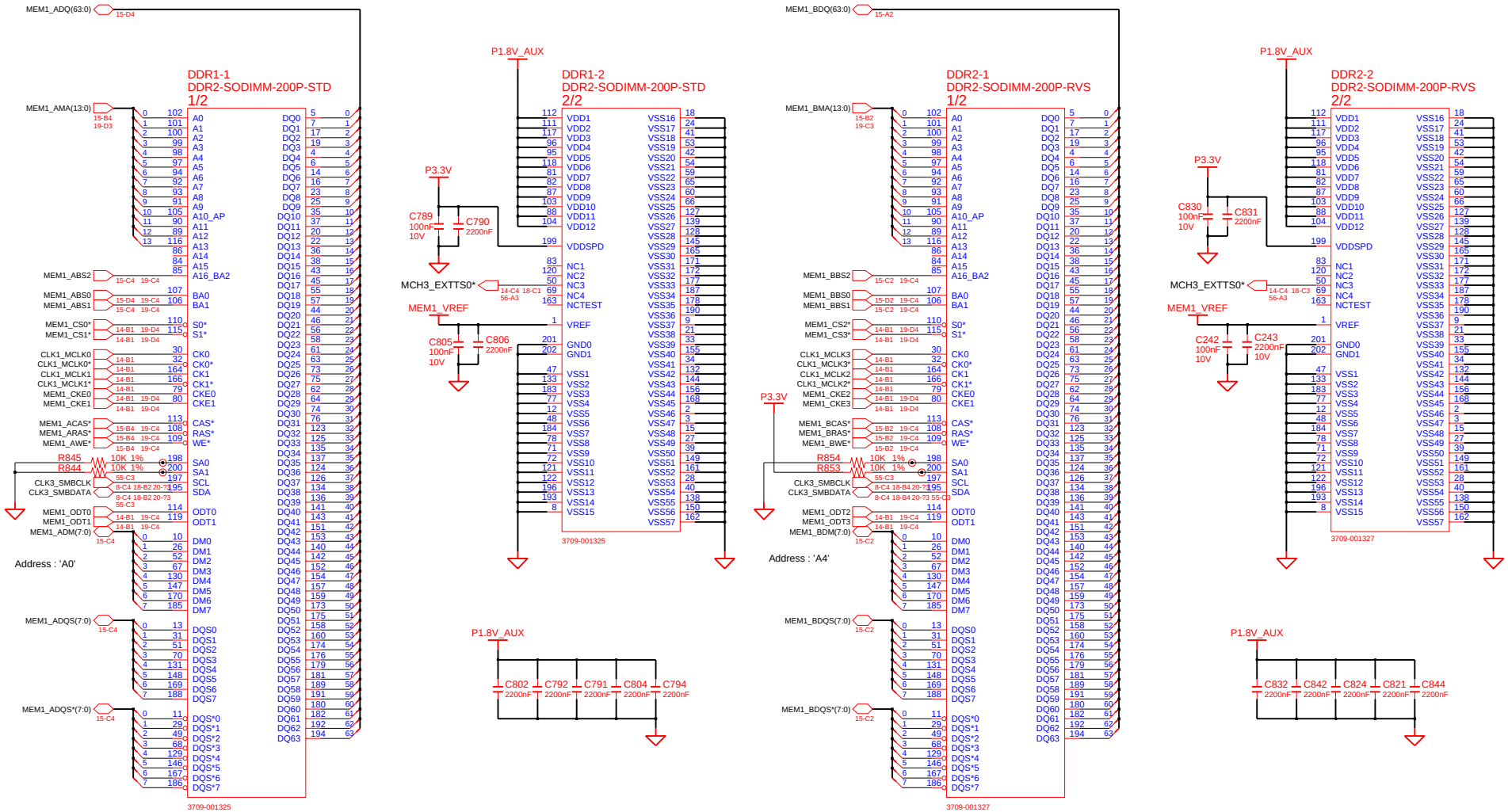


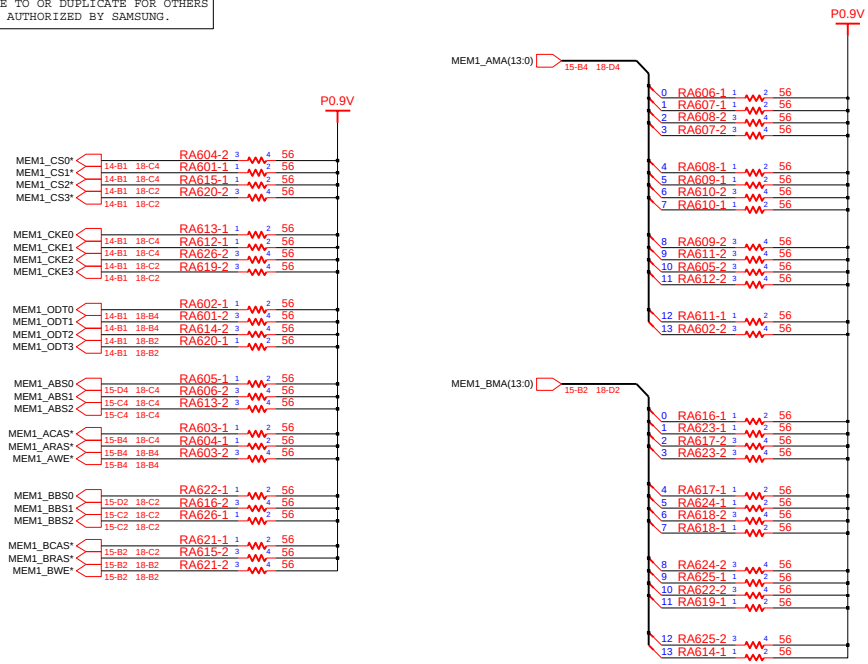


**** Note** ***POCAFEB-10 Only (Remove in MP Model)***

Current Setting (def. : default Option)		
CFG#	Low	High
CFG(5)	DMIx2	**DMIx4 (def.)**
CFG(6)	Reserved	**DDR-II (def.)**
CFG(7)	DT/Transportable	**Mobile CPU (def.)**
CFG(9)	PEG Reversal	**Normal**
CFG(16)	Dynamic ODT Disabled	**Dynamic ODT Enabled (def.)**
CFG(18)	**VCC 1.05V (def.)**	VCC 1.5V
CFG(19)	**DMI Lane Normal**	DMI Lane Reversal
CFG(20)	**SDVO or PCIE X1 Only(def.)**	SDVO and PCIE X1 Simultaneously

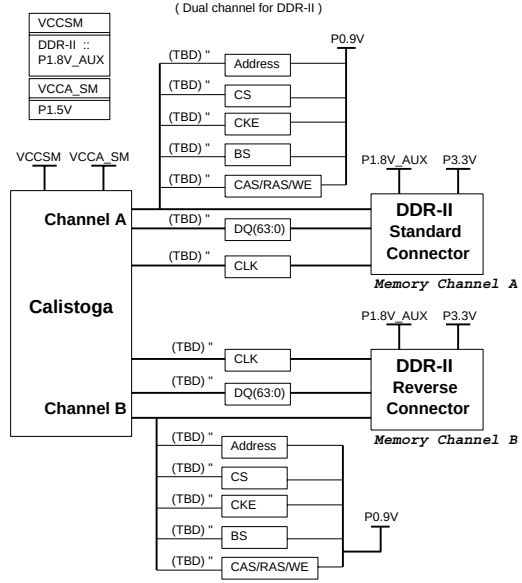
When CFG 13:12 are pulled down to '00', certain clocks within Calistoga will become free-running clocks.
This will lead to a rise in avg. power, but eliminates any possible clock-timing marginalities involved in clock power-up/power-down.
Intel strongly recommends leaving CFG 13:12 = NC (Internal PU to '11') to ensure low avg.power.

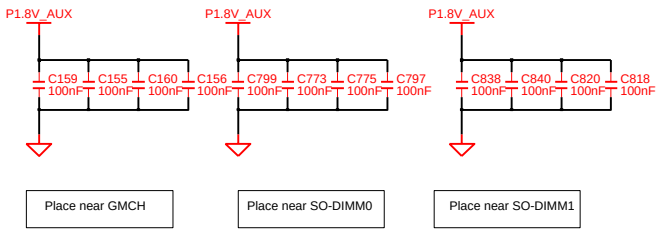


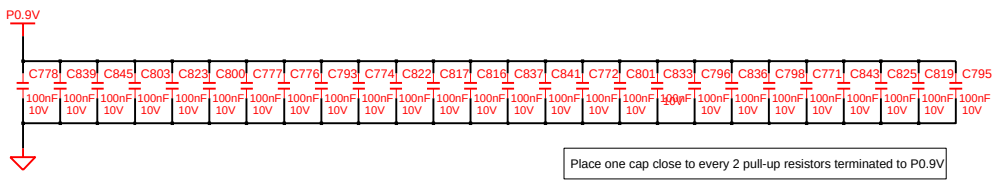


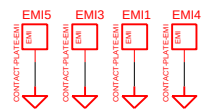
Memory Topology

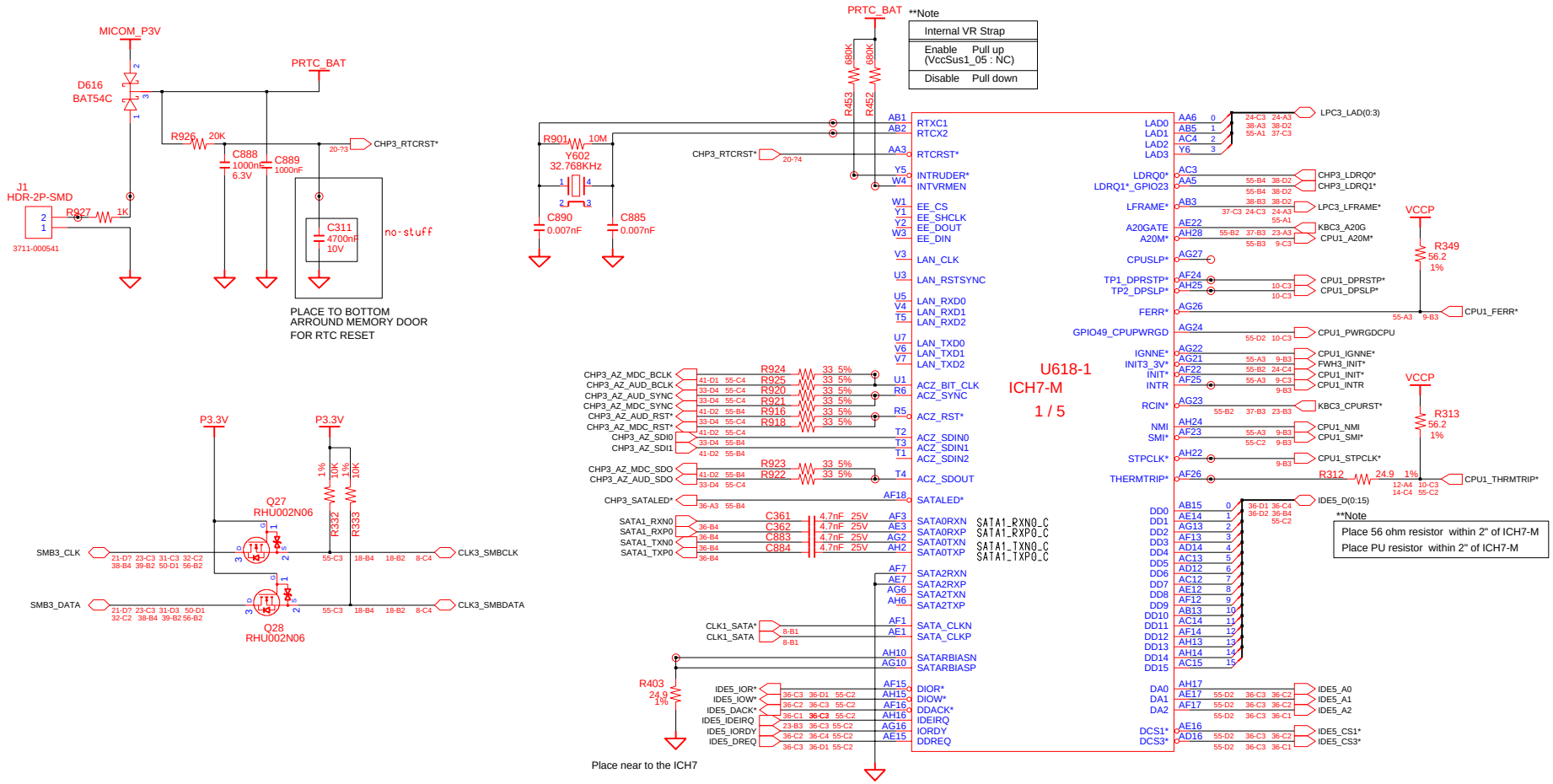
(Dual channel for DDR-II)











AC caps : PCIE need to be within 250mils of the driver
Resistor for Test : Place Stuffing Option to minimize stubs

U618-2 ICH7-M 2 / 5

U618-3 ICH7-M 3 / 5

CHP3_SATADET0*

PCI3_AD(31:0)

PCI3_INTA* PCI3_INTB* PCI3_INTC* PCI3_INTD*

SATA1RXN SATA1RXP SATA1TXN SATA1TXP SATA3RXN SATA3RXP SATA3TXN SATA3TXP

PCI3_REQ0* PCI3_GNT0* PCI3_REQ1* PCI3_GNT1* PCI3_REQ2* PCI3_REQ3*

CHP3_BIOSWP* CHP3_1394_ROMW* CHP3_BIOSTBL*

PCI3_CBE0* PCI3_CBE1* PCI3_CBE2* PCI3_CBE3*

PCI3_IRDY* PCI3_PAR PCI3_RST* PCI3_DEVSEL* PCI3_PERR* PCI3_PLOCK* PCI3_SERR* PCI3_STOP* PCI3_TRDY* PCI3_FRAME*

PLT3_RST* CLK3_PCLKICH

PCI3_INTE* PCI3_INTF* PCI3_INTG* PCI3_INTH*

MCH3_ICHSYNC*

GPIO21_SATA0GP GPIO19_SATA1GP GPIO36_SATA2GP GPIO37_SATA3GP

SMBCLK SMBDATA LINKALERT* SMLINK0 SMLINK1 RI* SPKR SUS_STAT* SYS_RST* GPIO0_BM_BUSY* SMBALERT*_GPIO11 GPIO18_STPPCI* GPIO20_STPCPU* GPIO26 GPIO27 GPIO28 GPIO32_CLKRUN* GPIO33_AZ_DOCK_EN* GPIO34_AZ_DOCK_RST* WAKE* SERIRQ THRM* VRMPWRGD CLK14 CLK48 SUSCLK SLP_S3* SLP_S4* SLP_S5* PWROK GPIO16_DPRSLPVR TP0_BATLOW* PWRBTN* LAN_RST* RSMRST* GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO12 GPIO13 GPIO14 GPIO15 GPIO24 GPIO25 GPIO35_SATACLKREQ* GPIO38 GPIO39 SPI_CLK SPI_CS* SPI_ARB SPI_MISO SPI_MOSI

SMB3_CLK SMB3_DATA SMB3_LINKALERT* CHP3_SMLINK0 CHP3_SMLINK1

CHP3_SPKR CHP3_SUSSTAT*

ITP3_SYSRST* MCH3_BMBUSY*

SMB3_ALERT*

CHP3_PCISTP* CHP3_CPUSTP*

CHP3_NUMLED*

CHP3_SCLED* CHP3_CAPSLED*

PCI3_CLKRUN*

PEX3_WAKE* CHP3_SERIRQ

CPU3_ALERT*

VRM3_CPU_PWRGD

CLK3_ICH14 CLK3_USB48

CHP3_SLPS3* CHP3_SLPS4* CHP3_SLPS5*

KBC3_PWRGD

CHP3_DPRSLPVR

KBC3_PWRBTN*

PLT3_RST*

KBC3_RSMRST*

BLT_DETECT* KBC3_RUNSCI* KBC3_EXTSMI*

CHP3_SATA_DET* KBC3_WAKESCI*

DCKLAN_RSTF* CHP3_WKON_LAN_D

CHP3_SATACLKREQ*

PERN1 PERP1 PETN1 PETP1 PERN2 PERP2 PETN2 PETP2 PERN3 PERP3 PETN3 PETP3 PERN4 PERP4 PETN4 PETP4 PERN5 PERP5 PETN5 PETP5 PERN6 PERP6 PETN6 PETP6

PEX1_LANTXN1_C PEX1_LANTXP1_C PEX1_MINTXN2_C PEX1_MINTXP2_C PEX1_DCKTXN3_C PEX1_DCKTXP3_C PEX1_EXPTXN4_C PEX1_EXPTXP4_C

PEX1_LANRXN1 PEX1_LANRXP1 PEX1_LANTXN1 PEX1_LANTXP1 PEX1_MINRXN2 PEX1_MINRXP2 PEX1_MINTXN2 PEX1_MINTXP2 PEX1_DCKRXN3 PEX1_DCKRXP3 PEX1_DCKTXN3 PEX1_DCKTXP3 PEX1_EXPRXN4 PEX1_EXPRXP4 PEX1_EXPTXN4 PEX1_EXPTXP4

DMI0RXN DMI0RXP DMI0TXN DMI0TXP DMI1RXN DMI1RXP DMI1TXN DMI1TXP DMI2RXN DMI2RXP DMI2TXN DMI2TXP DMI3RXN DMI3RXP DMI3TXN DMI3TXP

DMI1_RXN0 DMI1_RXP0 DMI1_TXN0 DMI1_TXP0 DMI1_RXN1 DMI1_RXP1 DMI1_TXN1 DMI1_TXP1 DMI1_RXN2 DMI1_RXP2 DMI1_TXN2 DMI1_TXP2 DMI1_RXN3 DMI1_RXP3 DMI1_TXN3 DMI1_TXP3

DMI_CLKN DMI_CLKP CLK1_PCIEICH* CLK1_PCIEICH

DMI_ZCOMP DMI_IRCOMP

P1.5V_PCIE P3.3V_AUX

OC0* OC1* OC2* OC3* OC4* GPIO29_OC5* GPIO30_OC6* GPIO31_OC7*

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P

USB3_P0- USB3_P0+ USB3_P1- USB3_P1+ USB3_P2- USB3_P2+ USB3_P3- USB3_P3+ USB3_P4- USB3_P4+ USB3_P5- USB3_P5+ USB3_P6- USB3_P6+ USB3_P7- USB3_P7+

USBRBIAS* USBRBIAS

**Note

USB

USB 0,1 : SYSTEM Right
USB 2,3 : SYSTEM Rear
USB 4 : BLUETOOTH
USB 5 : PORT REPLICATOR
USB 6 : FINGER PRINTER
USB 7 : EXPRESS CARD

SIO3_DET*

Low : SIO model
High : No SIO model

TPM-model GIGA-model PM-model no-stuff 10/100-model GM-model FMEM-model

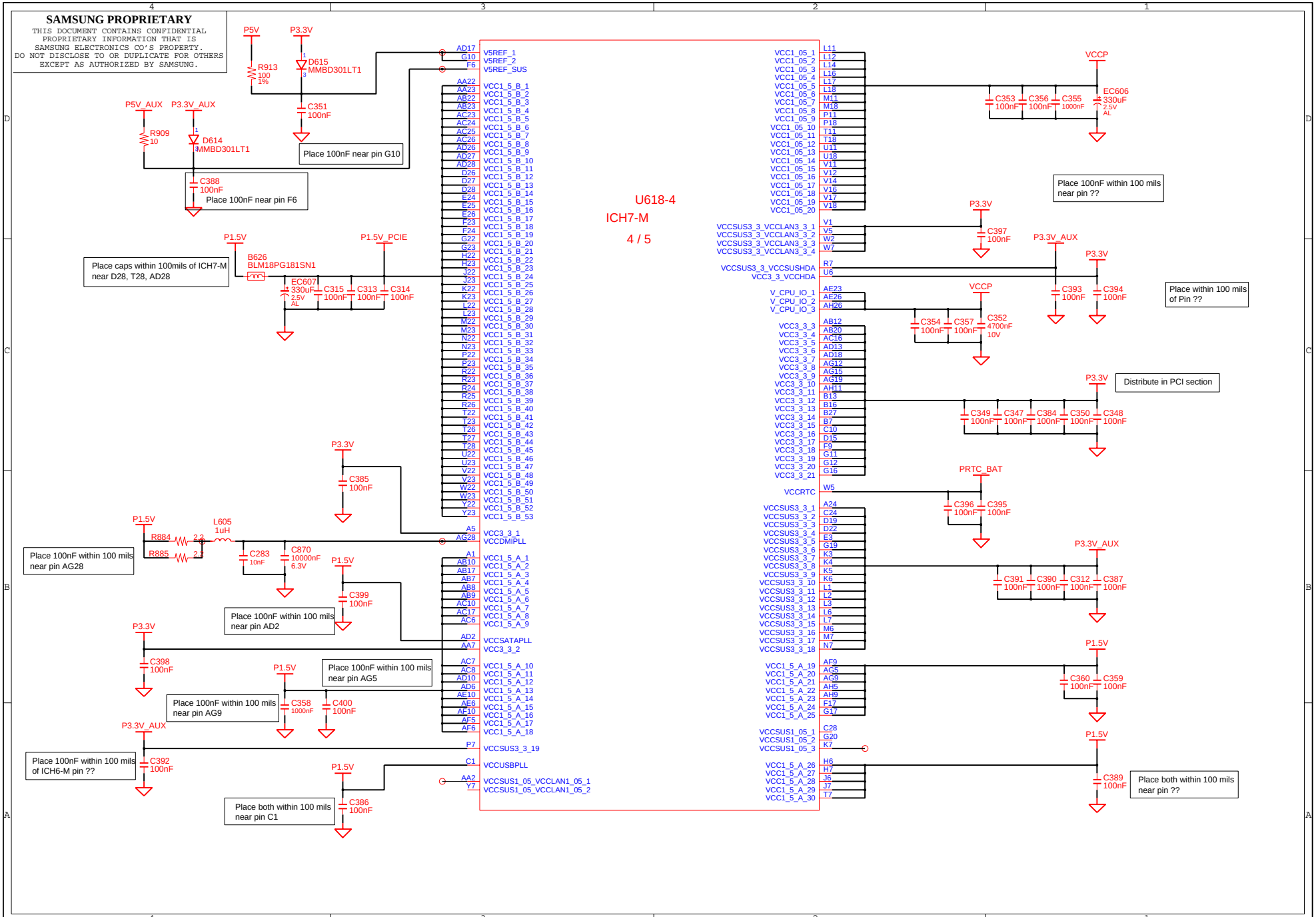
BIOS RESET

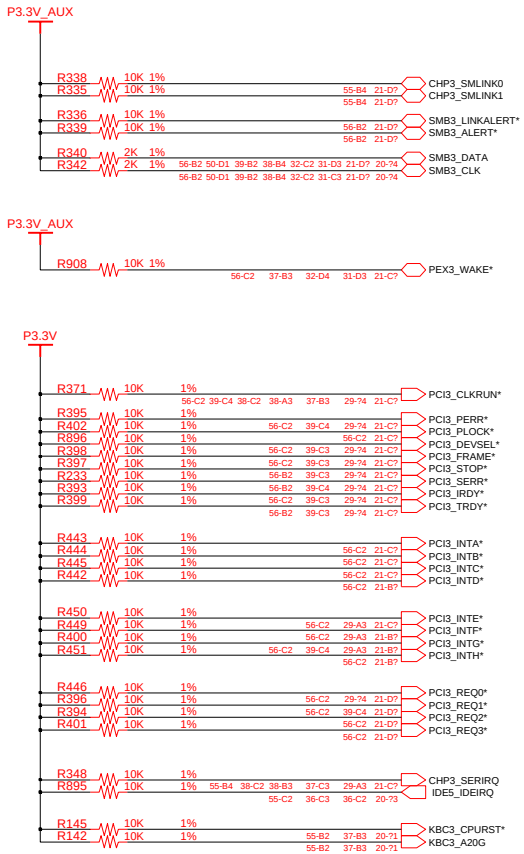
U621 7SZ08

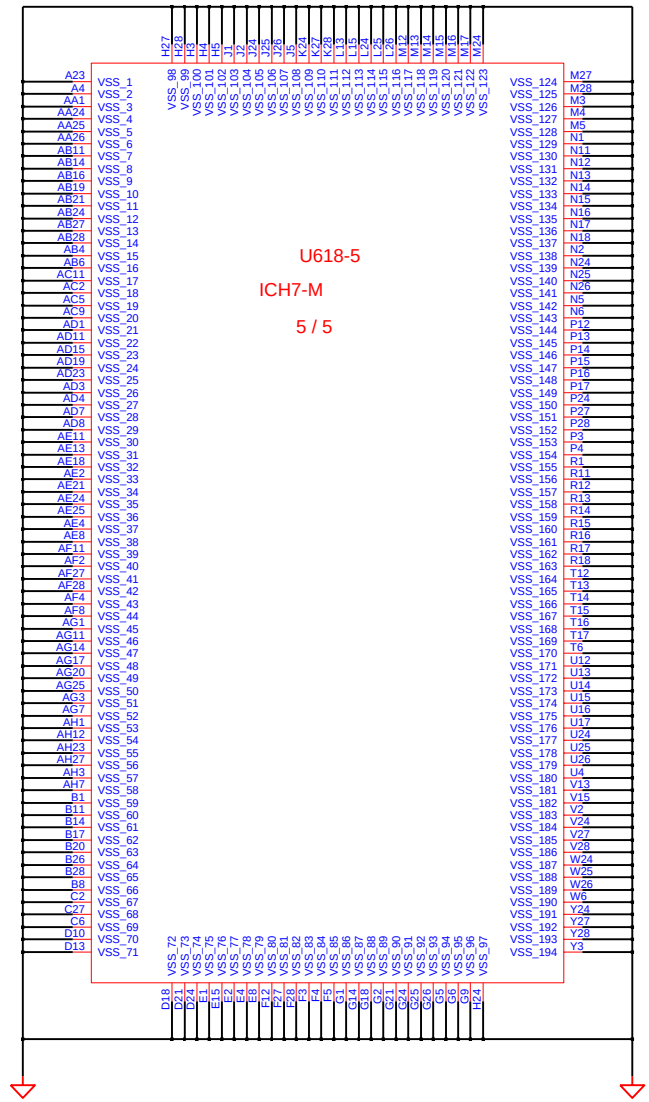
PLT3_RSTF*

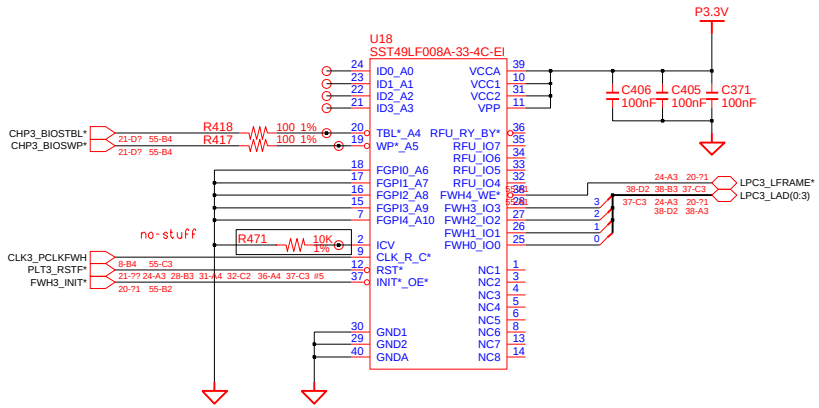
ICH7-m Options

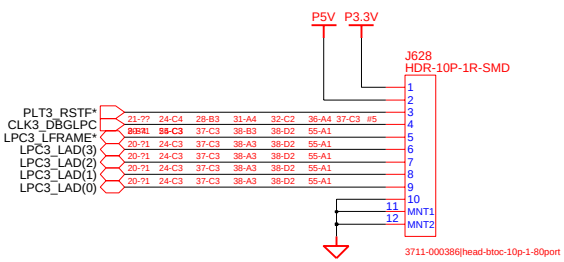
	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_GNT3	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
CHP3_GNT(5:4)	Boot BIOS Option	



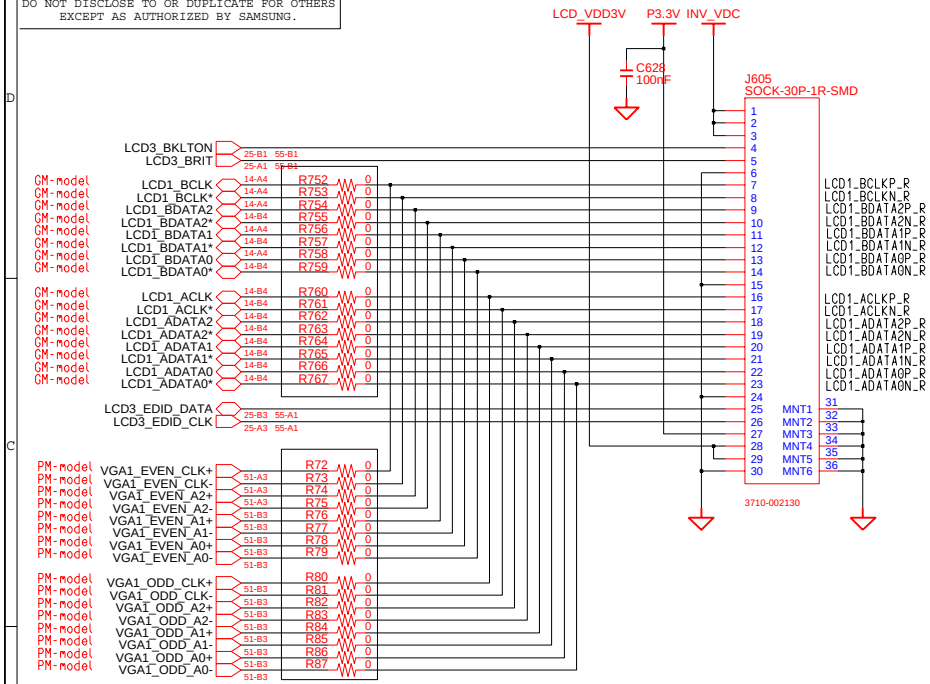


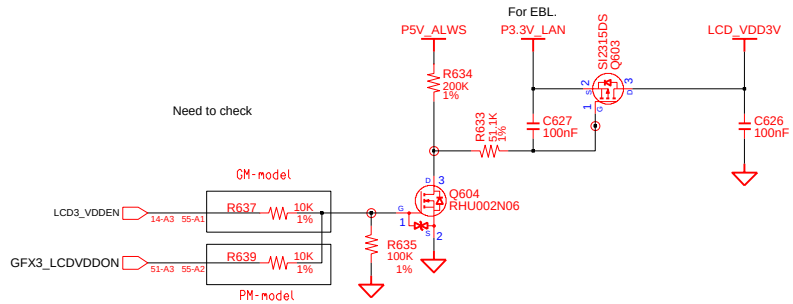


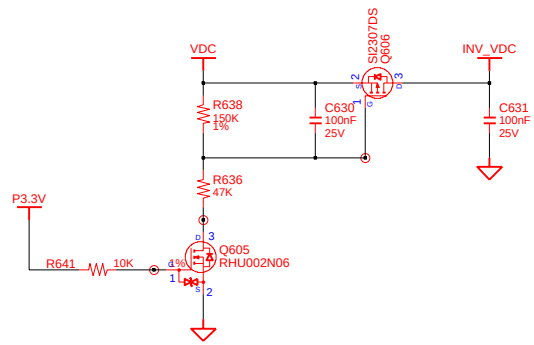


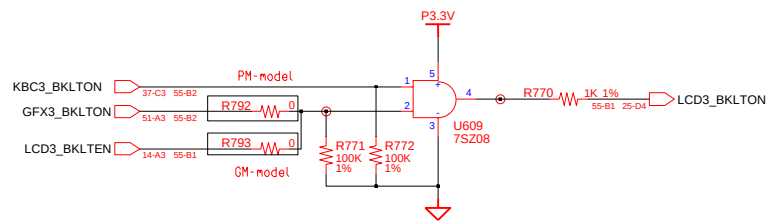


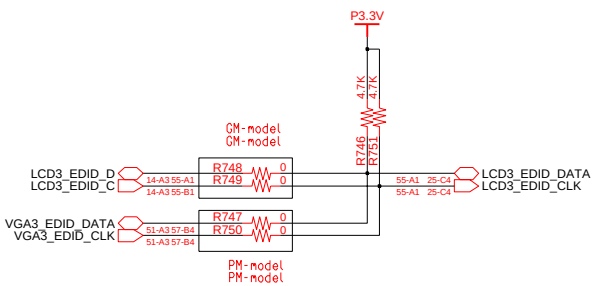
INSERT BIOS CODE

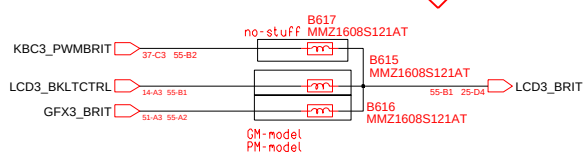


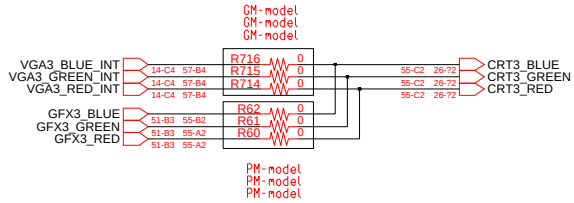


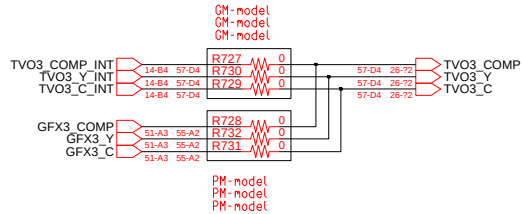


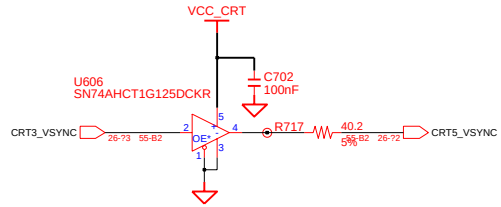


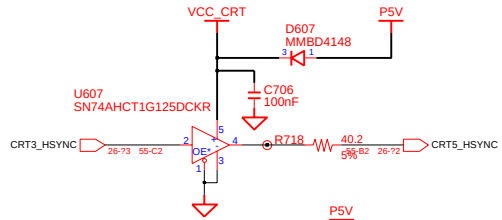


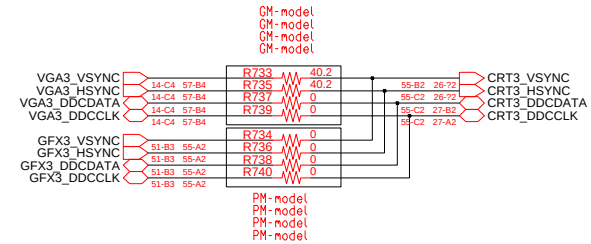


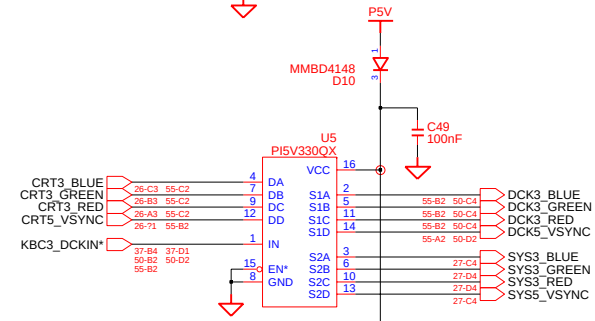


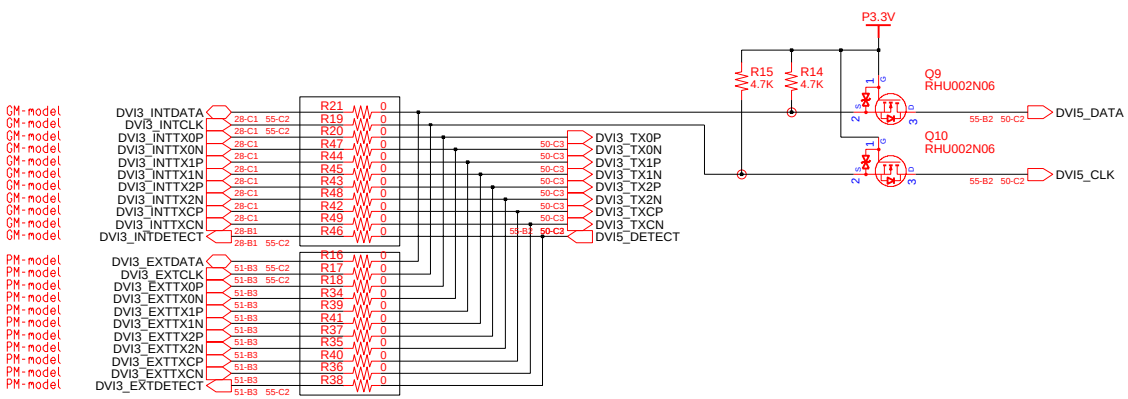


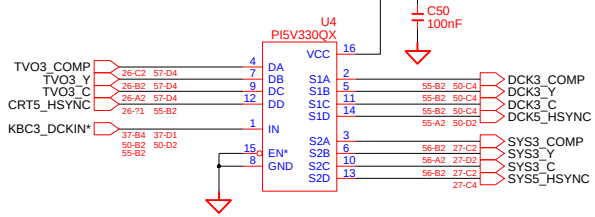




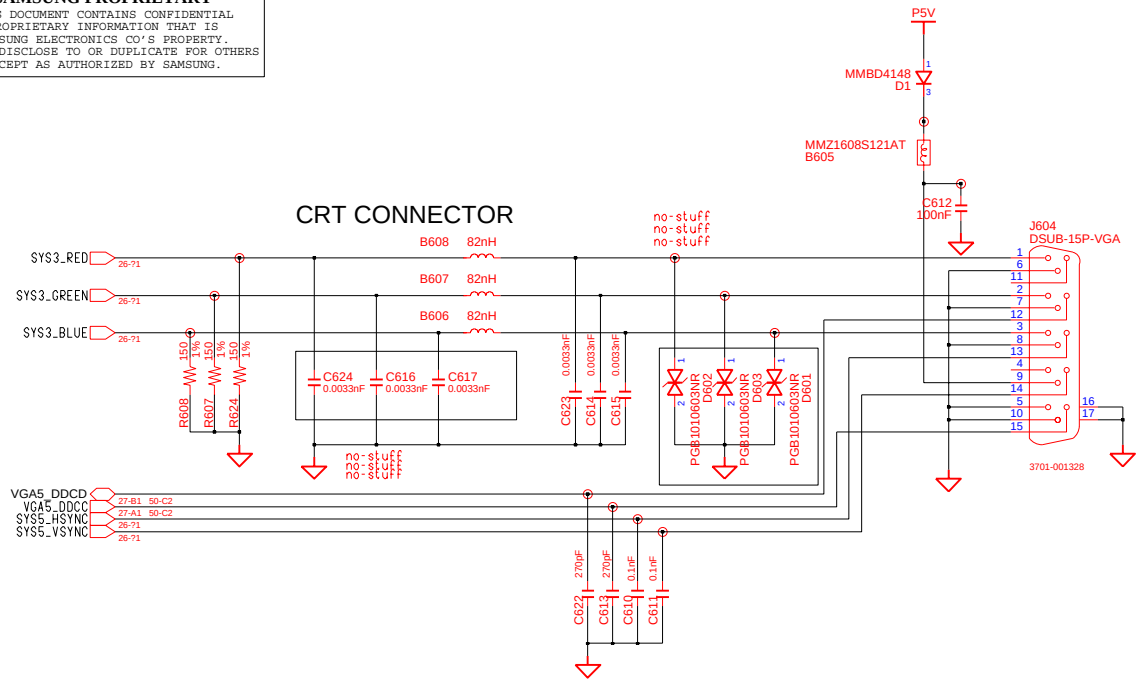




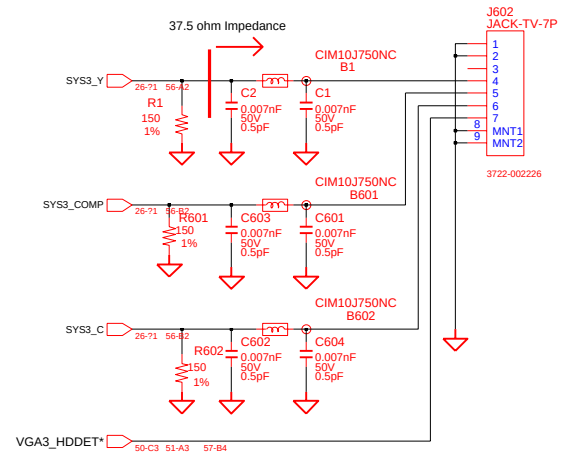


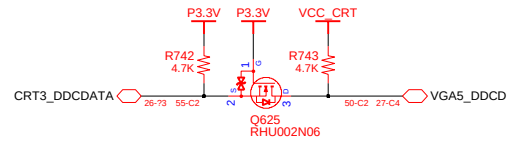


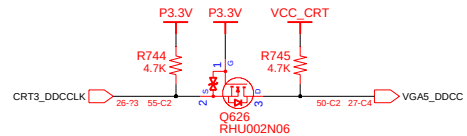
CRT CONNECTOR

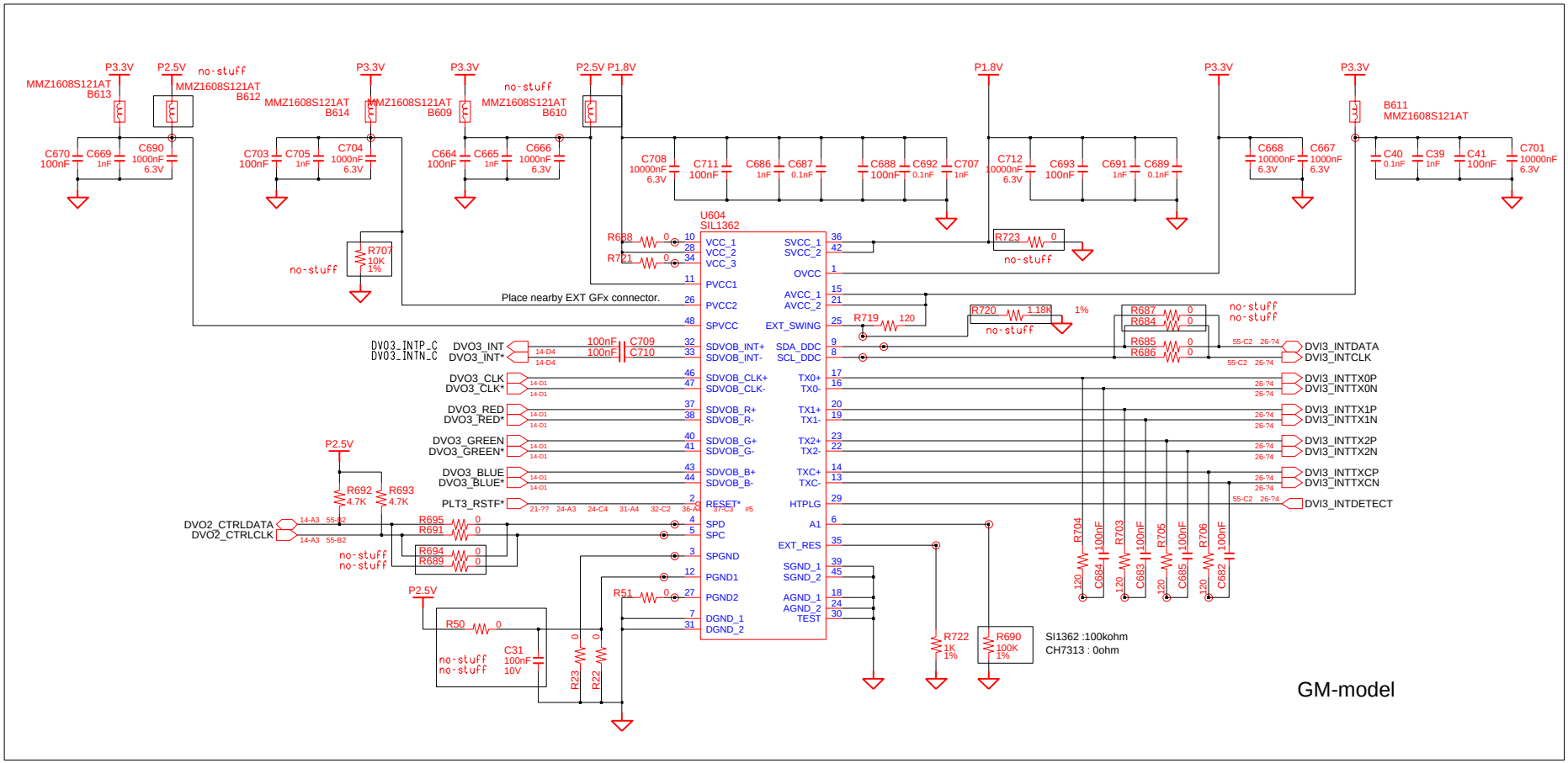


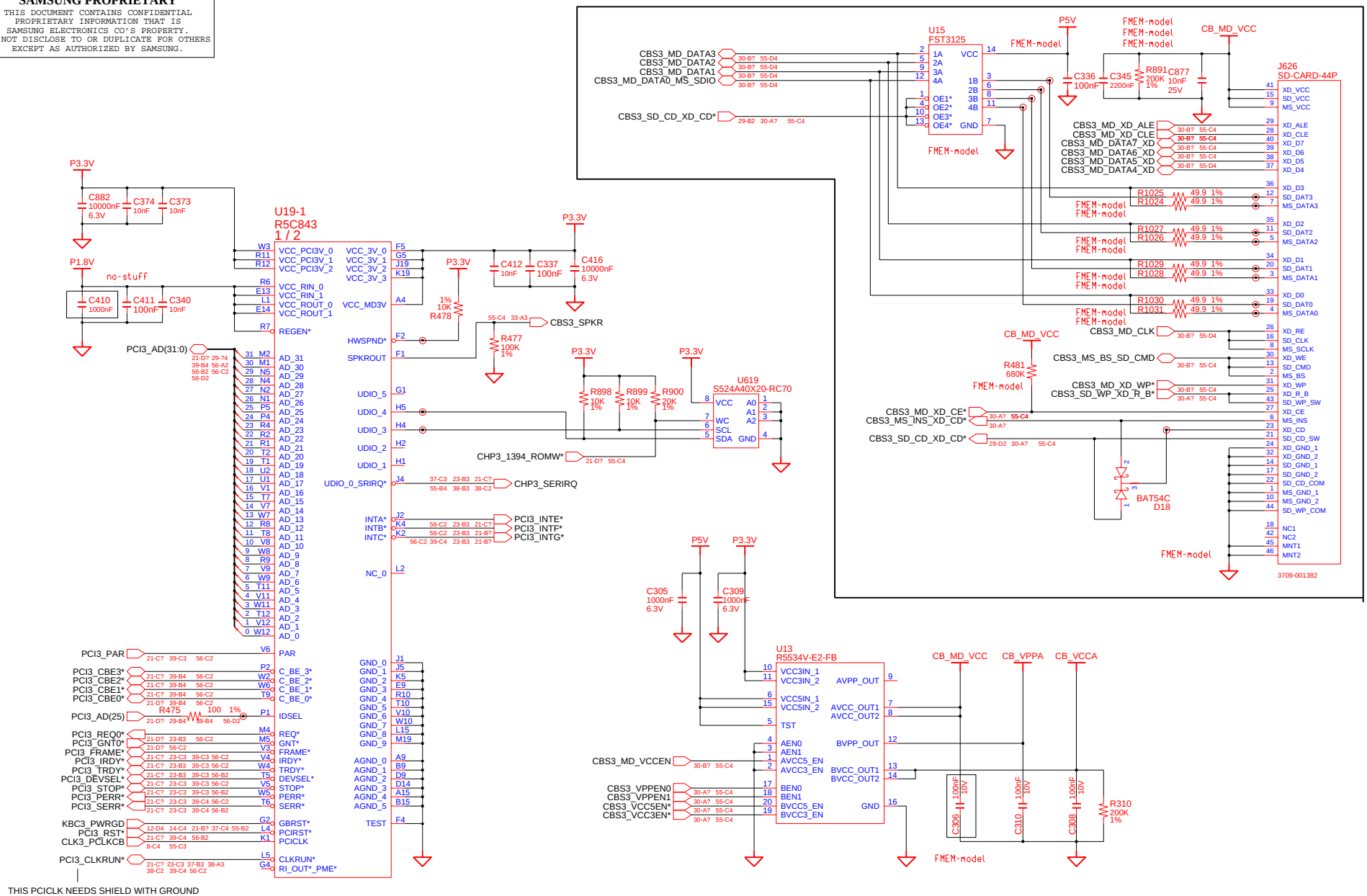
TV-OUT(S-VHS,COMPONENT)











U19-2
R5C843
2 / 2

CBS3_CAD(31:0)

CAD_31_CDATA_10 CAD_30_CDATA_9 CAD_29_CDATA_1 CAD_28_CDATA_8 CAD_27_CDATA_0 CAD_26_CADR_0 CAD_25_CADR_1 CAD_24_CADR_2 CAD_23_CADR_3 CAD_22_CADR_4 CAD_21_CADR_5 CAD_20_CADR_6 CAD_19_CADR_25 CAD_18_CADR_7 CAD_17_CADR_24 CAD_16_CADR_17 CAD_15_IOWR*_USBD- CAD_14_CADR_9 CAD_13_IORD*_USBD+ CAD_12_CADR_11 CAD_11_OE* CAD_10_CE_2* CAD_9_CADR_10 CAD_8_CDATA_15 CAD_7_CDATA_7 CAD_6_CDATA_13 CAD_5_CDATA_6 CAD_4_CDATA_12 CAD_3_CDATA_5 CAD_2_CDATA_11 CAD_1_CDATA_4 CAD_0_CDATA_3

CC_BE_3*_REG* CC_BE_2*_CADR_12 CC_BE_1*_CADR_8 CC_BE_0*_CE_1*

CPAR_CADR13 CAUDIO_BVD_2 CCD_1*_CD_1*_CCD_1* CCD_2*_CD_2*_CCD_2* CDEVSEL*_CADR_21 CFRAME*_CADR_23 CGNT*_WE* CINT*_RDY_IREQ* CIRDY*_CADR_15 CPERR*_CADR_14 CREQ*_INPACK* CSERR*_WAIT* CSTOP*_CADR_20 CSTSCHG_BVD_1 CTRDY*_CADR_22_CPUSB* CVS_1_VS_1*_CVS_1 CVS_2_VS_2*_CVS_2

A_CCLK_CADR_16 A_CCLKRUN*_WP_IOIS16* A_CRST*_RESET

CADR_19 CADR_18 CDATA_14 CDATA_2_PERST*

VCC5EN* VCC3EN* VPPEN_0 VPPEN_1 USBDP USBDM

AVCC_PHY_0 AVCC_PHY_1 AVCC_PHY_2 AVCC_PHY_3 CPS FIL0 REXT VREF TPBIAS_0 TPBN_0 TPBP_0 TPAN_0 TPAP_0 TPBIAS_1 TPBN_1 TPBP_1 TPAN_1 TPAP_1 XI XO NC_8

MDIO_13_MSCDAT_3_SDCDAT_3 MDIO_12_MSCDAT_2_SDCDAT_2 MDIO_11_MSCDAT_1_SDCDAT_1 MDIO_10_MSCDAT_0_SDCDAT_0 MDIO_9_MSCCLK_SDCCLK MDIO_8_MSBS_SDCCMD MDIO_7_MSEXTCK_SDEXTCK MDIO_6_MSLED*_SDLED* MDIO_5_SDPWR_1 MDIO_4_MSPWR_SDPWR_0 MDIO_3_SDWP* MDIO_2 MDIO_1_MSCD* MDIO_0_SDCD*

NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7

MDIO_19 MDIO_18 MDIO_17 MDIO_16 MDIO_15 MDIO_14

CBS3_MD_XD_ALE CBS3_MD_XD_CLE CBS3_MD_DATA7_XD CBS3_MD_DATA6_XD CBS3_MD_DATA5_XD CBS3_MD_DATA4_XD CBS3_MD_DATA3 CBS3_MD_DATA2 CBS3_MD_DATA1 CBS3_MD_DATA0_MS_SDIO

CBS3_MD_CLK CBS3_MS_BS_SD_CMD CLK3_FM48 CBS3_MD_XD_WP* CBS3_MD_VCCEN CBS3_SD_WP_XD_R_B* CBS3_MD_XD_CE* CBS3_MS_INS_XD_CD* CBS3_SD_CD_XD_CD*

P3.3V

B30 MMZ1608S121AT

C376 10nF, C382 10000nF 6.3V, C375 100nF, C372 1nF, C338 100nF, C339 1nF

C341 10nF 25V, R384 10K 1%, C414 10nF 25V

SHIELD WITH GROUND

PLACE THESE COMPONENTS TO R5C841 AS CLOSE AS POSSIBLE

1394_TPB- 1394_TPB+ 1394_TPA- 1394_TPA+

R435 56.2 1%, R434 56.2 1%, R385 56.2 1%, R386 56.2 1%

C381 10nF 25V, C379 330nF 10V, R387 5.11K 1%, C344 270pF

1394_TPB_R 1394_TPA_R

CBS_1394_TPB- CBS_1394_TPB+ CBS_1394_TPA- CBS_1394_TPA+

SHIELD WITH GROUND

Y3 24.576MHz

C342 0.01nF 0.5pF, C343 0.01nF 0.5pF

R437 56.2 1%, R436 56.2 1%, R439 56.2 1%, R440 56.2 1%

C378 10nF 25V, C380 330nF 10V, R441 5.11K 1%, C383 270pF

CBS_1394_TPB_R CBS_1394_TPA_R

R480 22.6 1%, R890 49.9 1%

R479 0 no-stuff

C415 0.01nF 0.5pF

**Note
CB3_MD_CLK NEEDS SHIELD WITH GROUND AND 22.6 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C843

R383 49.9 1%

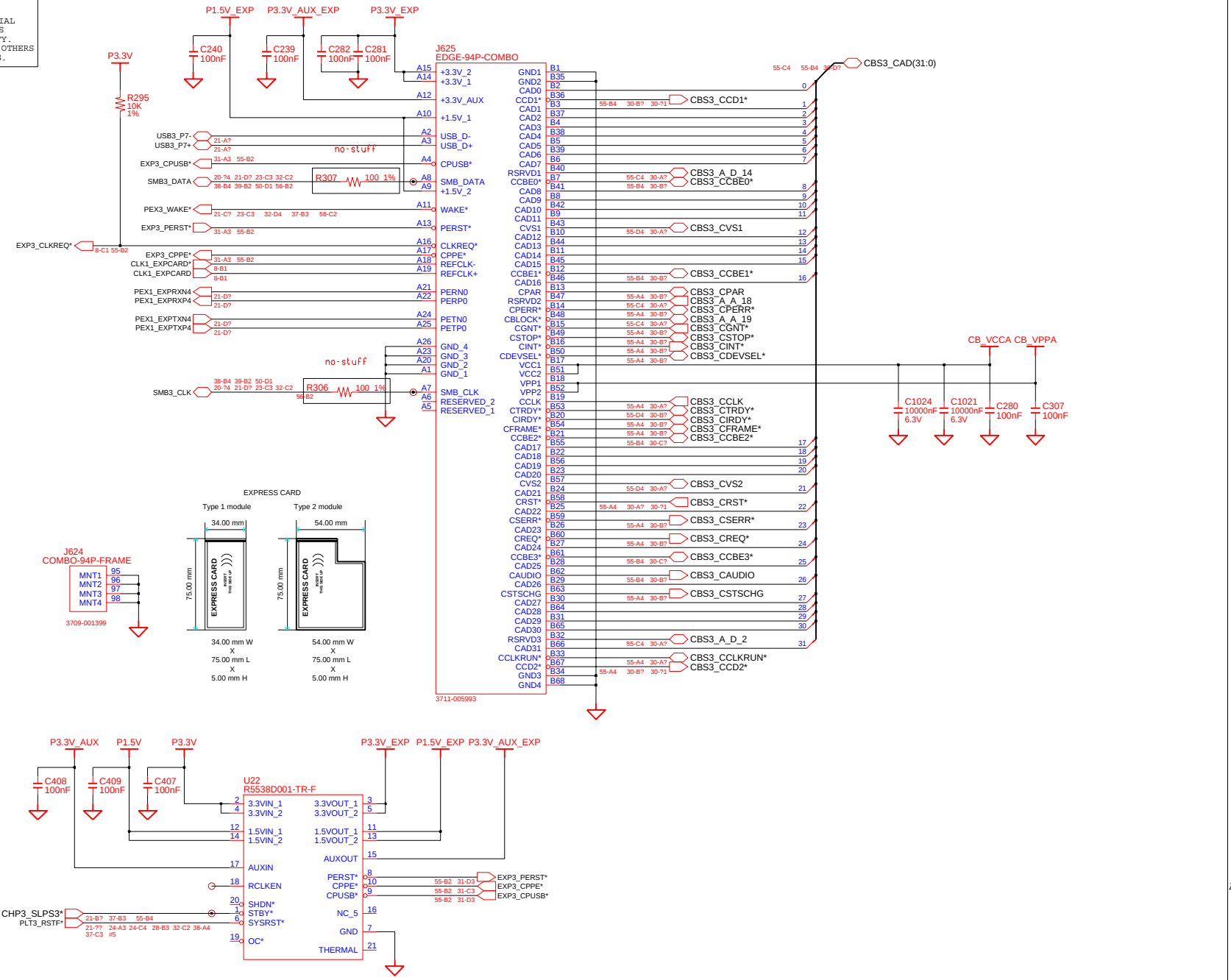
P3.3V

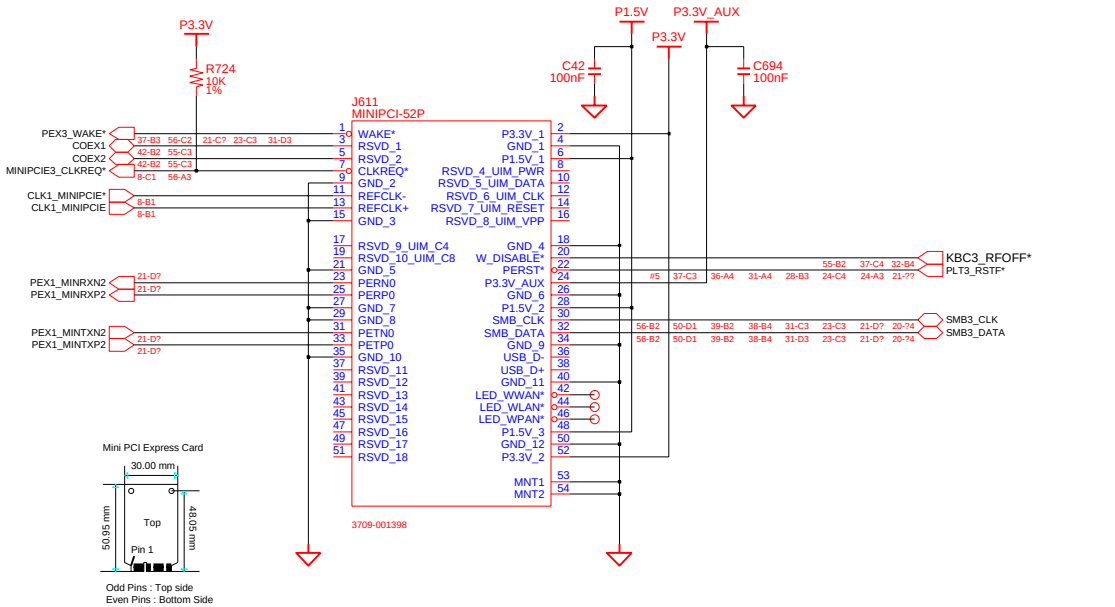
R334 100K 1%

**Note
CB3_CLK NEEDS SHIELD WITH GROUND AND 47 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C843

C880 10nF 25V, C241 270pF, C372 270pF

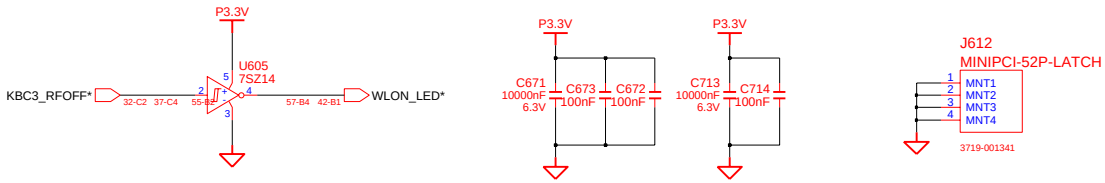
CBS3_CRST* CBS3_CCD1* CBS3_CCD2*





Mini PCI Express

PCI Express Mini Card ElectroMechanical Spec. 1.0



1.AGND_AUD IS AUDIO GROUND
2. GND IS DIGITAL GROUND
3.AGND_MIC IS MIC GROUND
4.AGND_CHS IS CHASS GROUND

ALL TYPE IS 1608

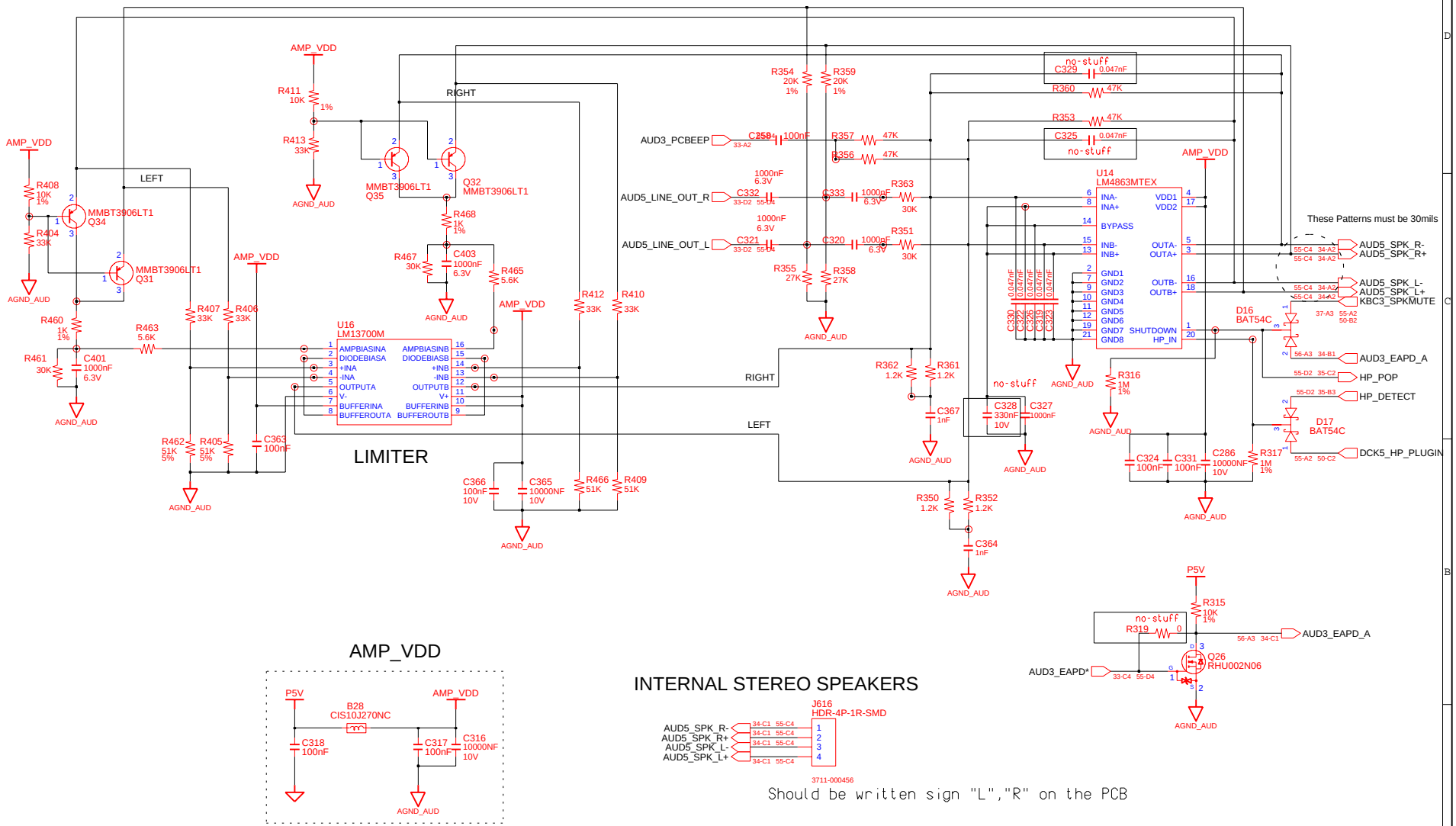
U8
AD1986AAJSTZ_R0.2

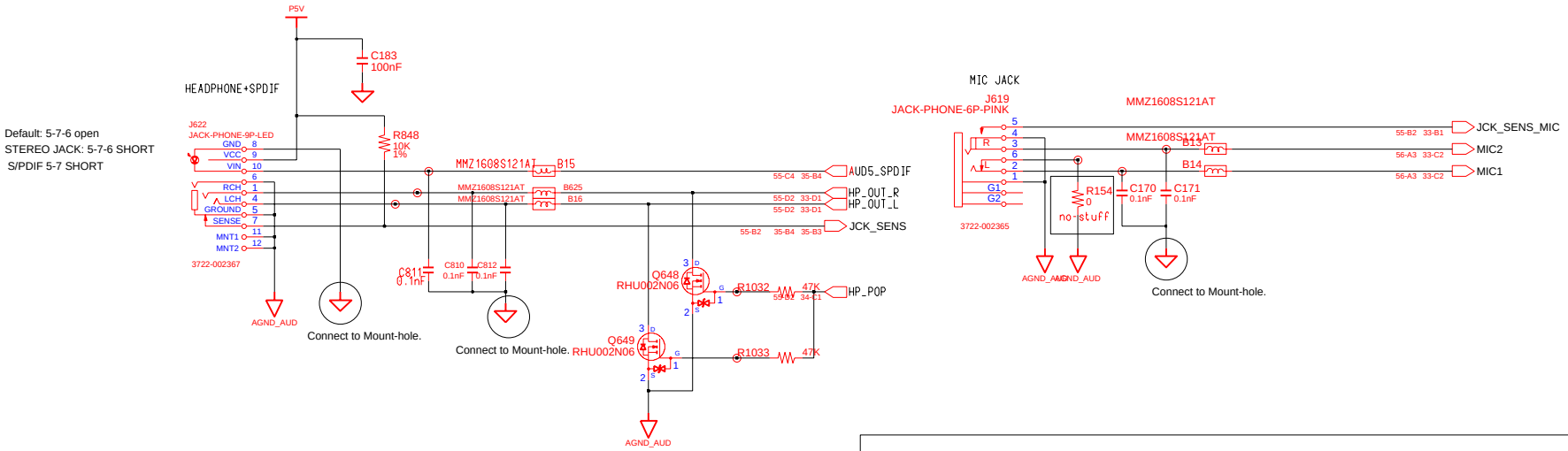
U10
TPS793475DBVR

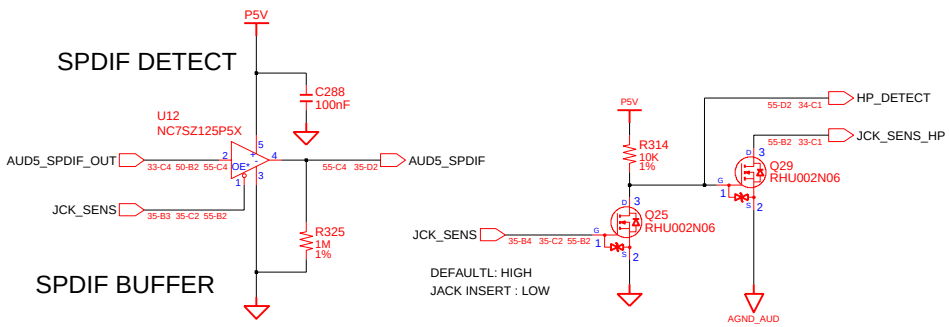
LDO

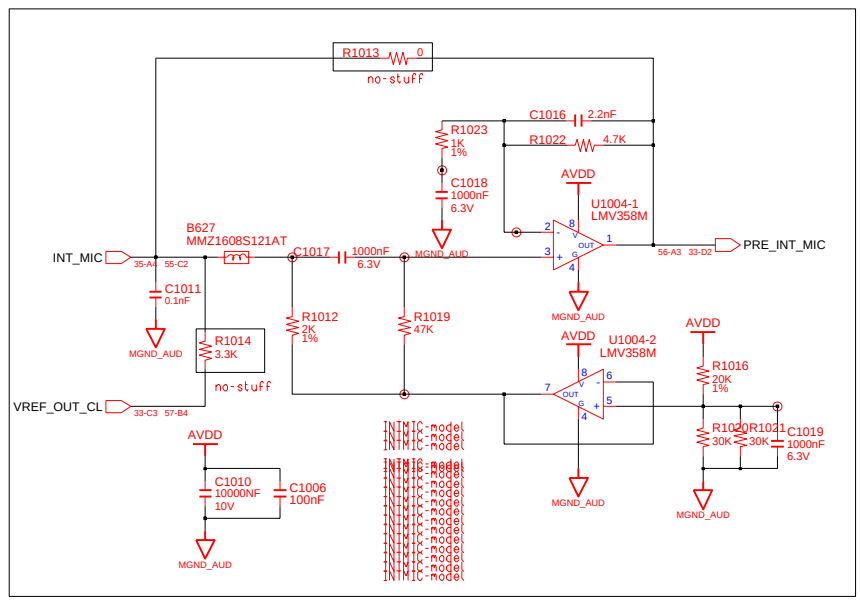
PC BEEP

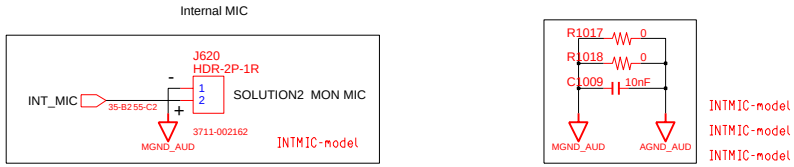
LINE OUT



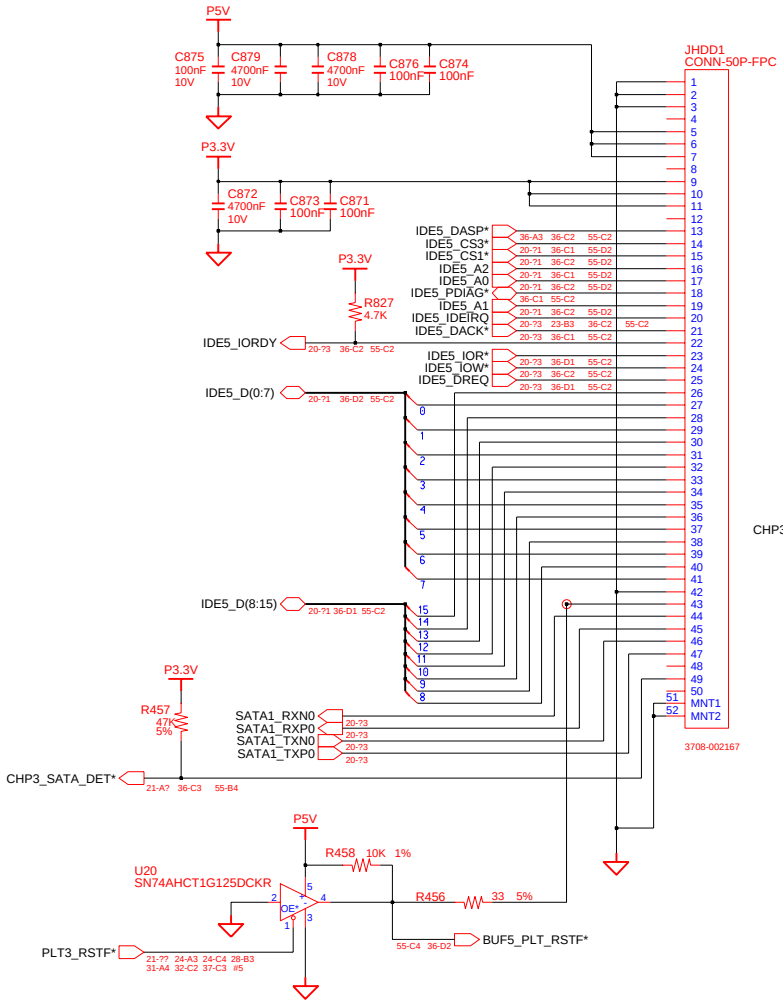




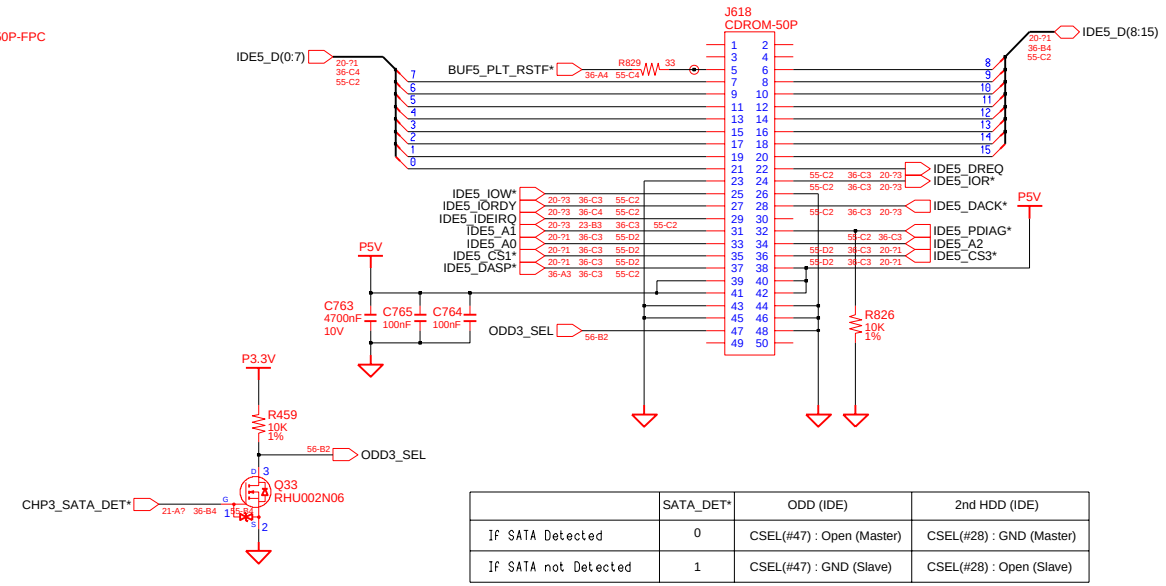




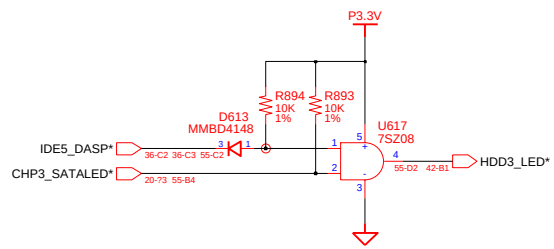
Main to HDD

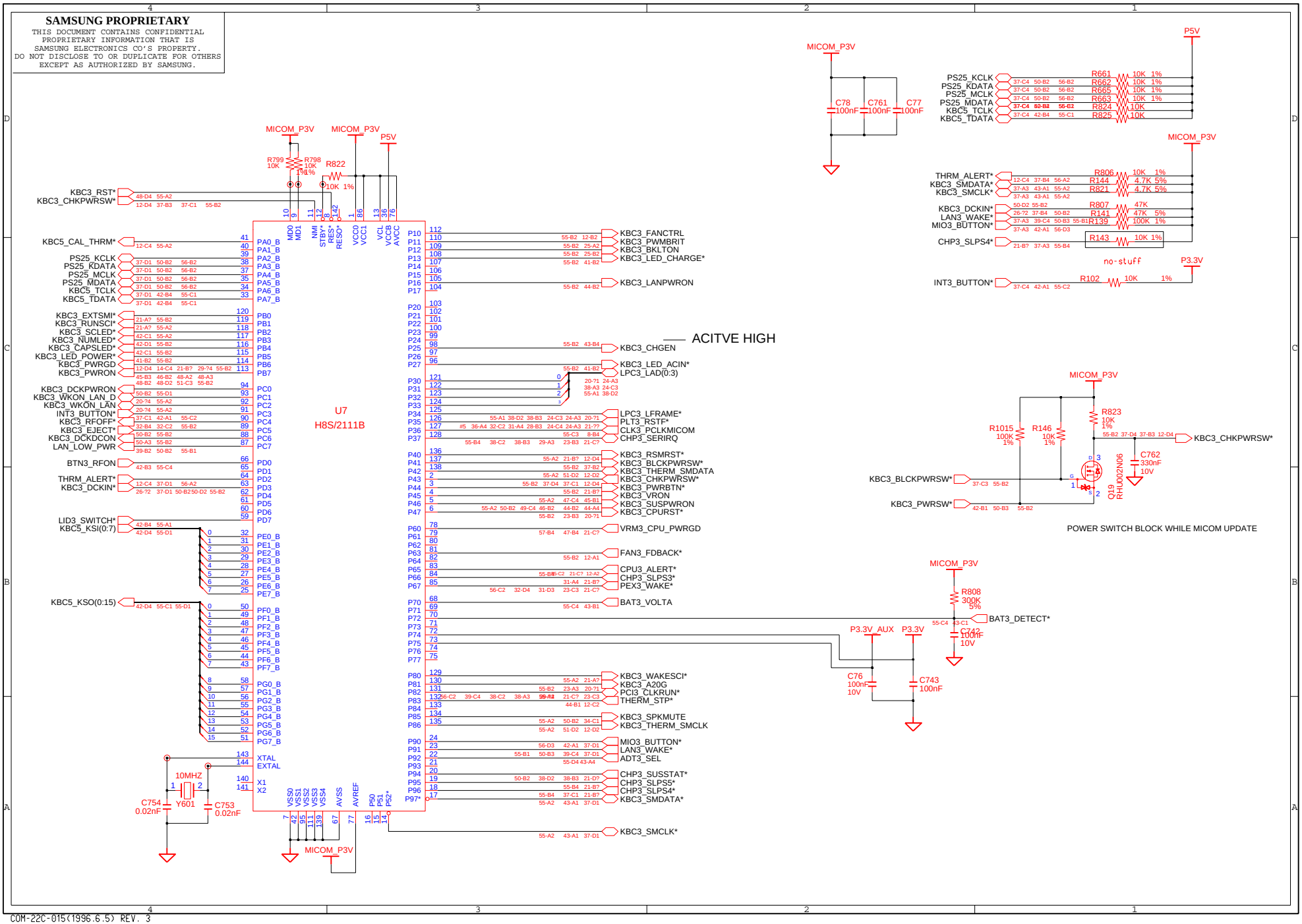


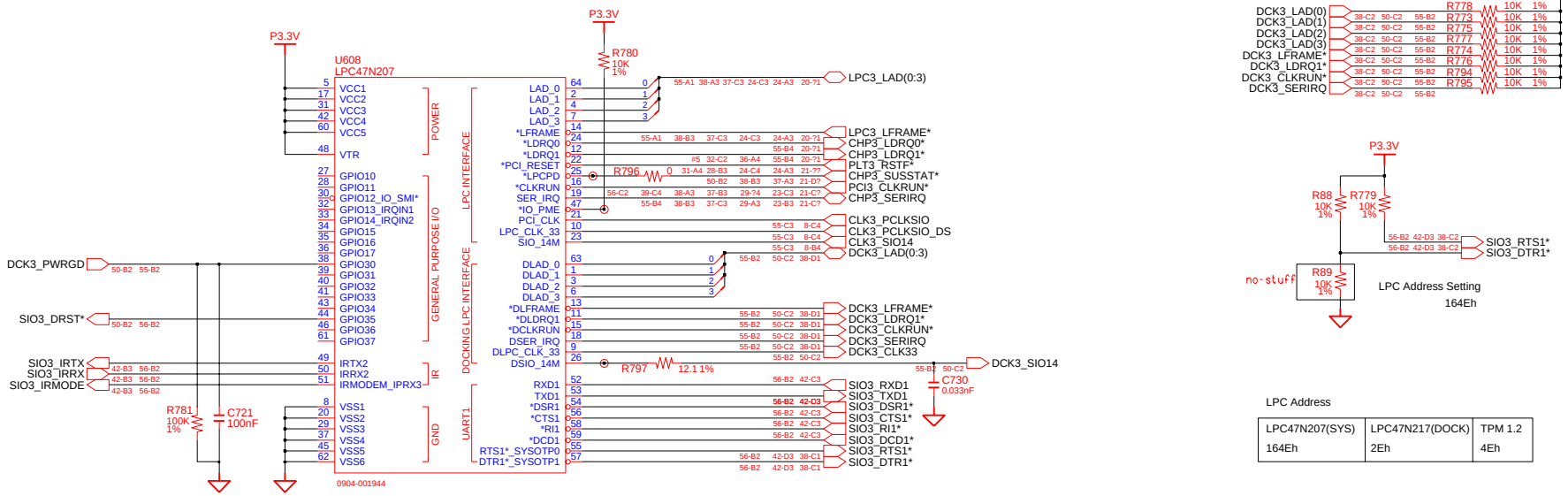
Main to Swap B'd

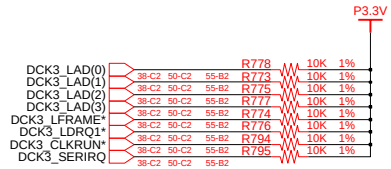


	SATA_DET*	ODD (IDE)	2nd HDD (IDE)
If SATA Detected	0	CSEL(#47) : Open (Master)	CSEL(#28) : GND (Master)
If SATA not Detected	1	CSEL(#47) : GND (Slave)	CSEL(#28) : Open (Slave)



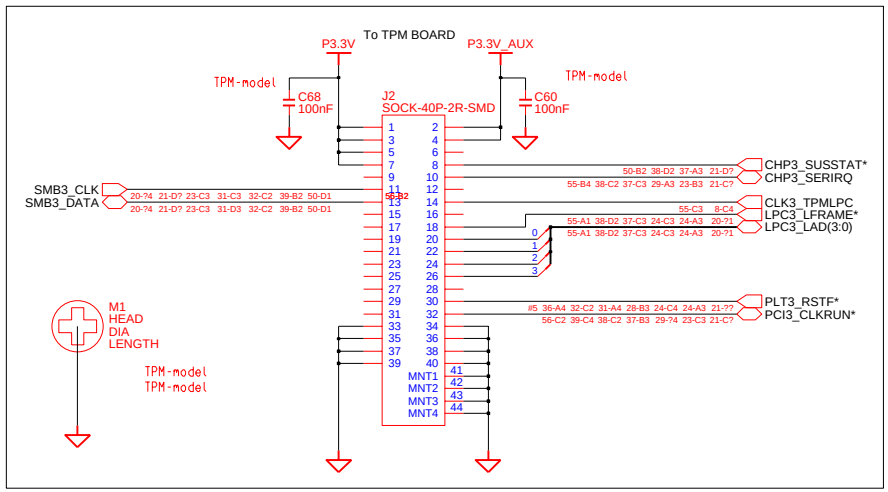


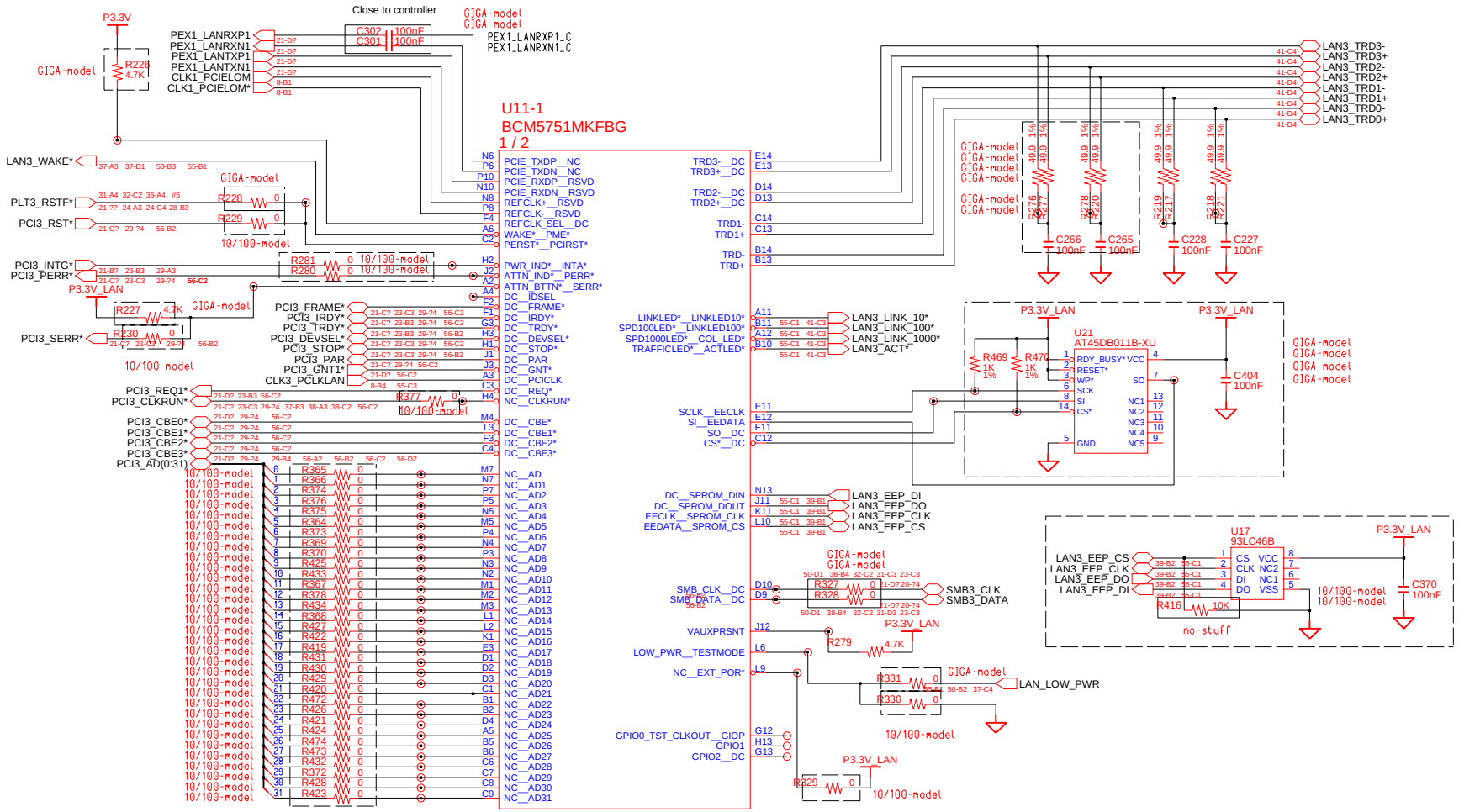


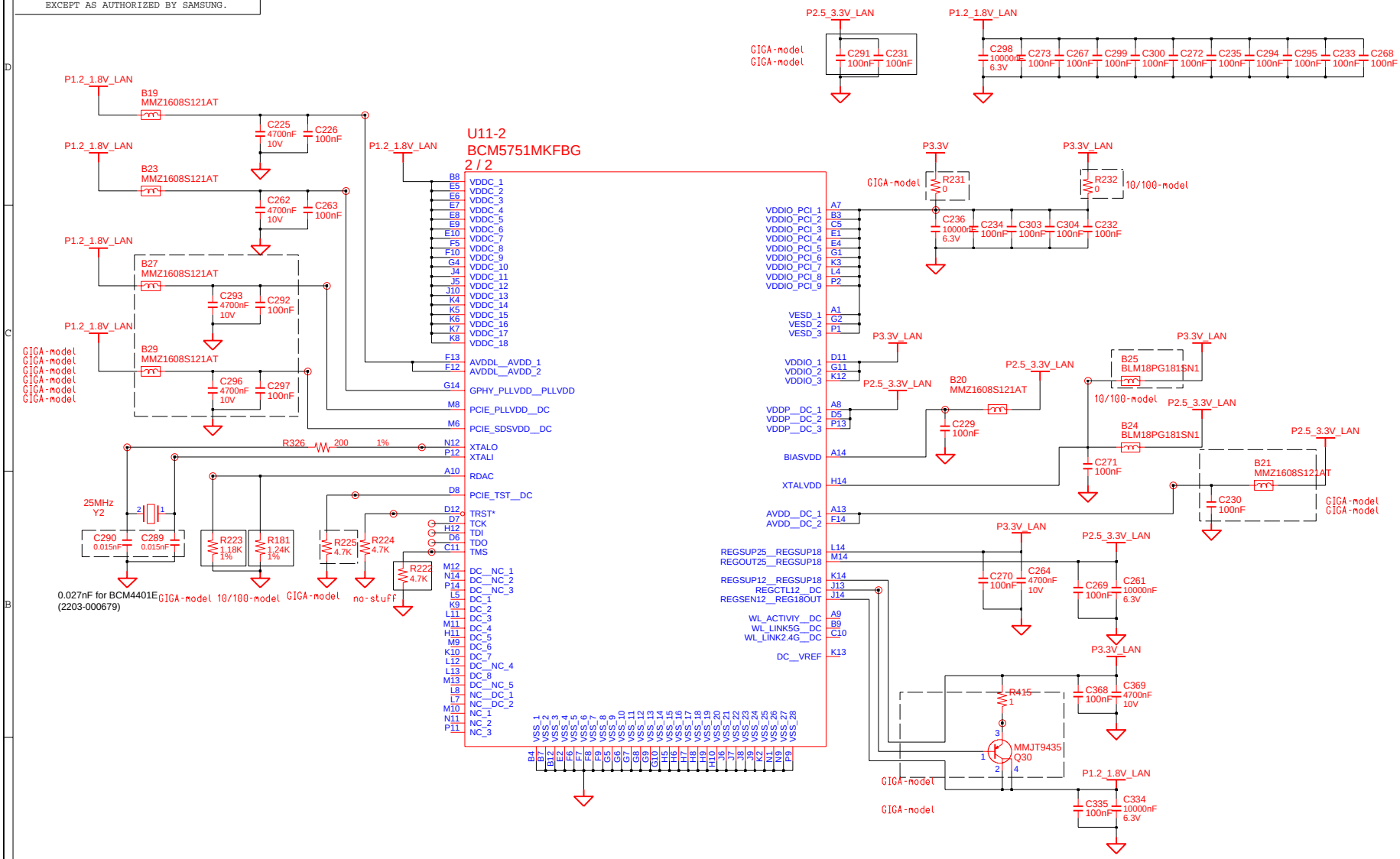


LPC Address

LPC47N207(SYS)	LPC47N217(DOCK)	TPM 1.2
164Eh	2Eh	4Eh

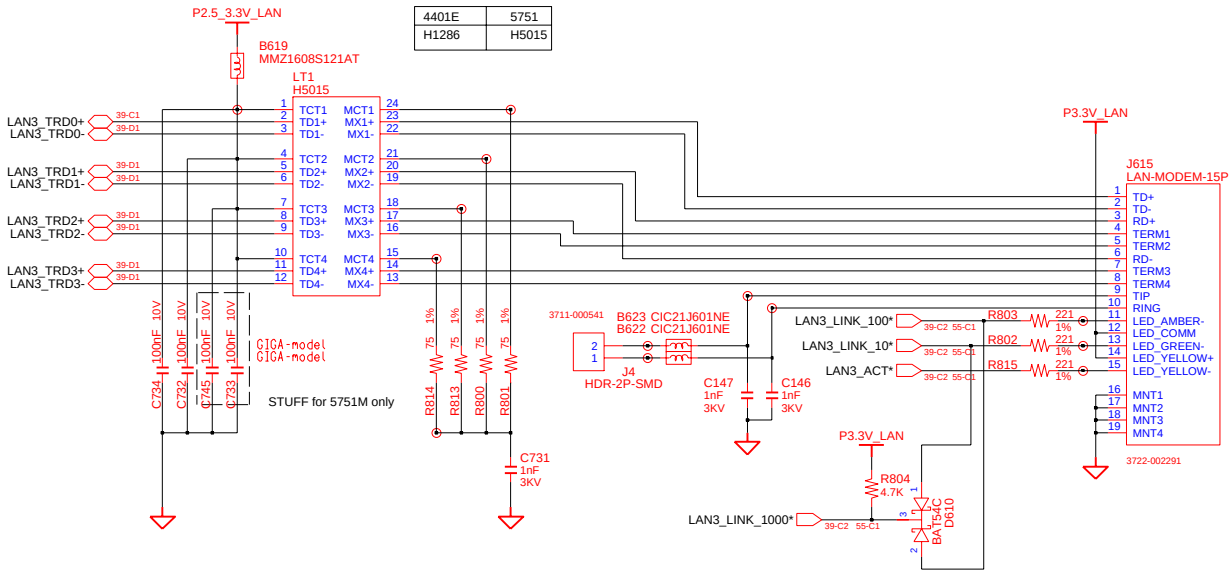




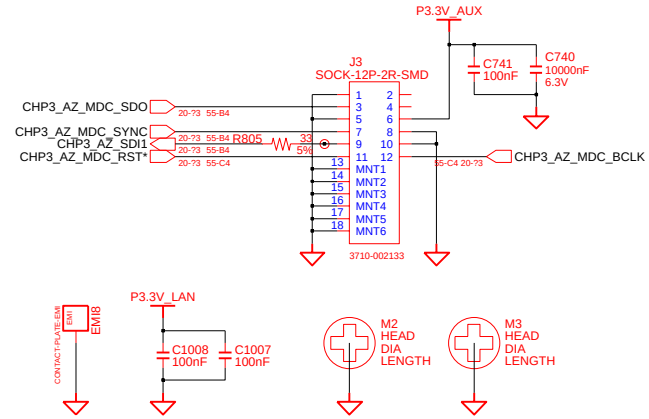


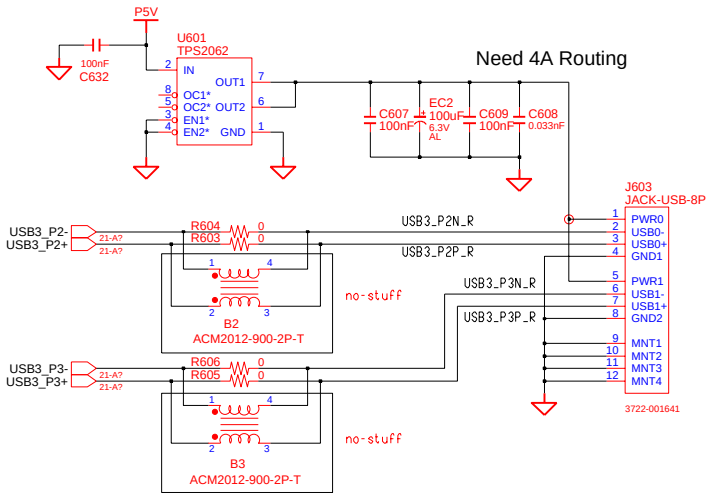
LAN Connector

4401E	5751
H1286	H5015

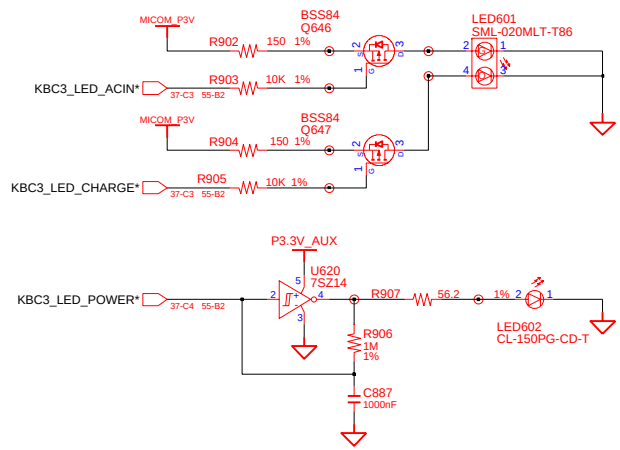


MDC Connecter

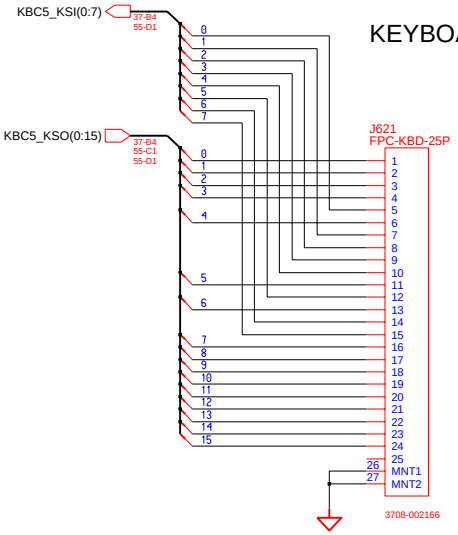




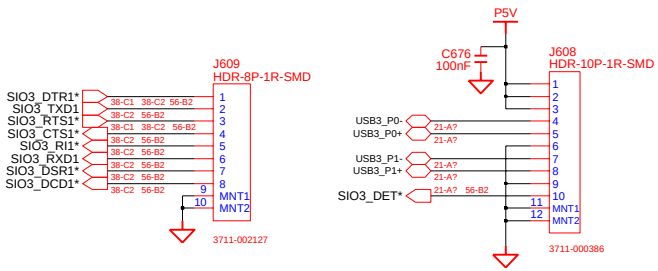
ADAPTERIN/CHARGING LED



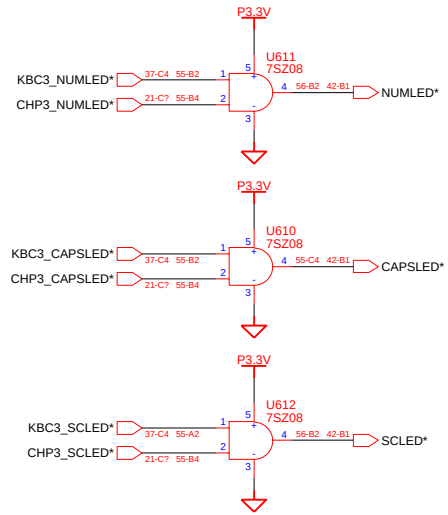
KEYBOARD



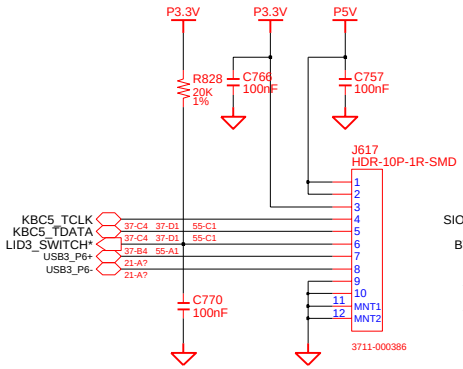
USB_SIO BOARD



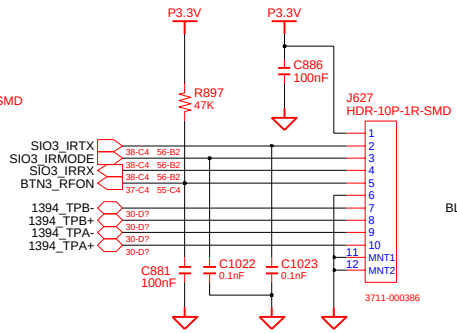
LED BOARD



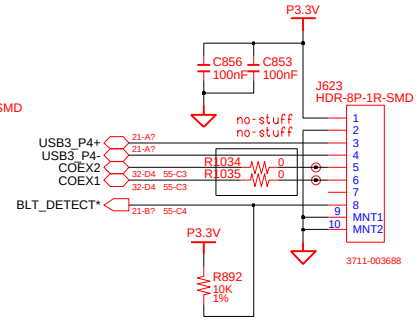
TOUCHPAD

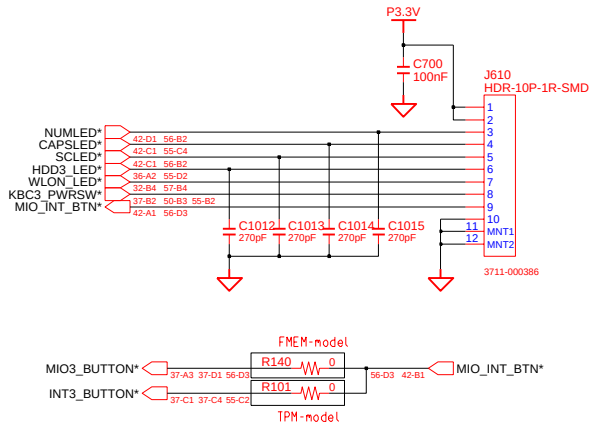


1394_IR BOARD

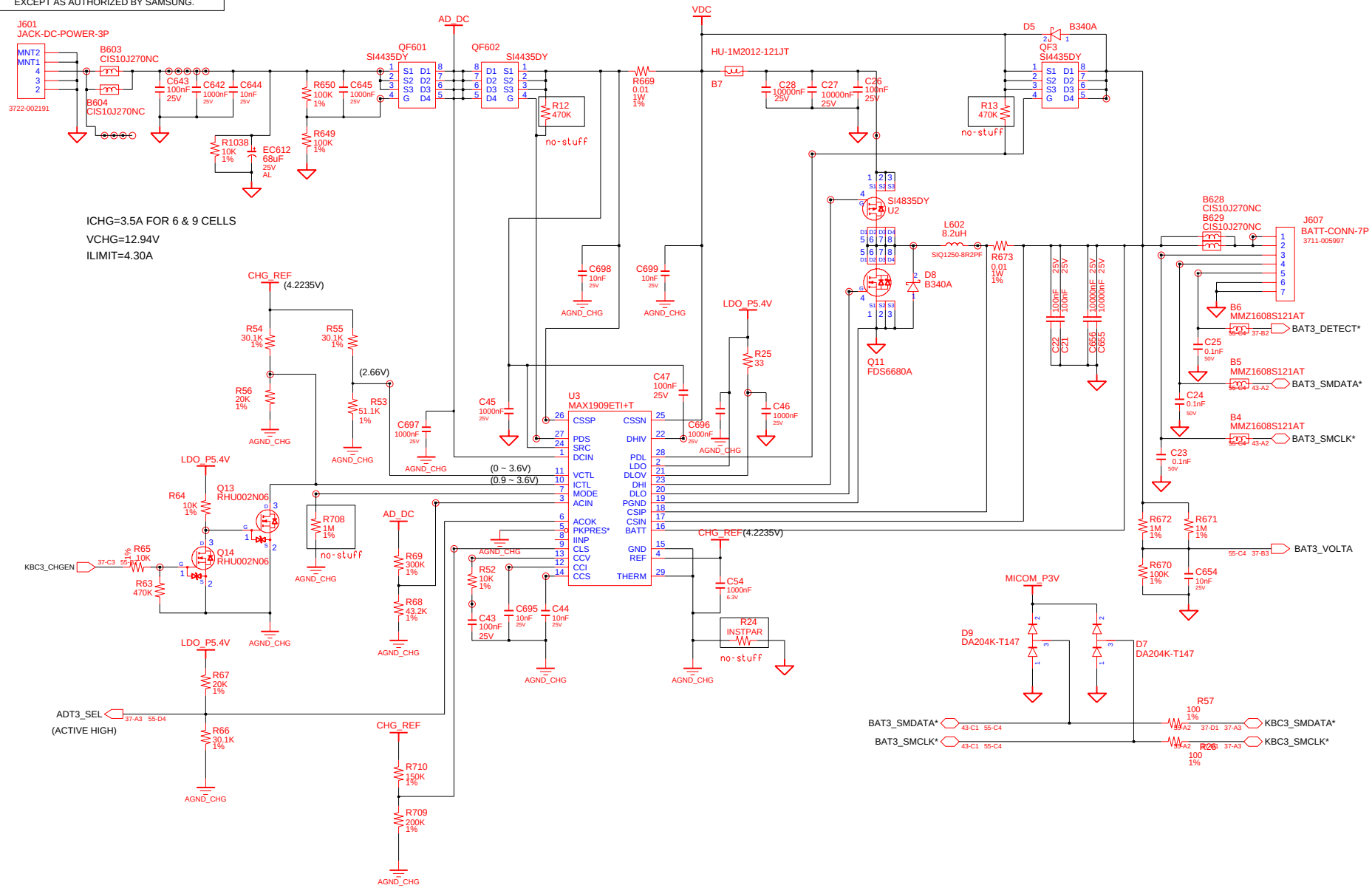


Bluetooth Interface

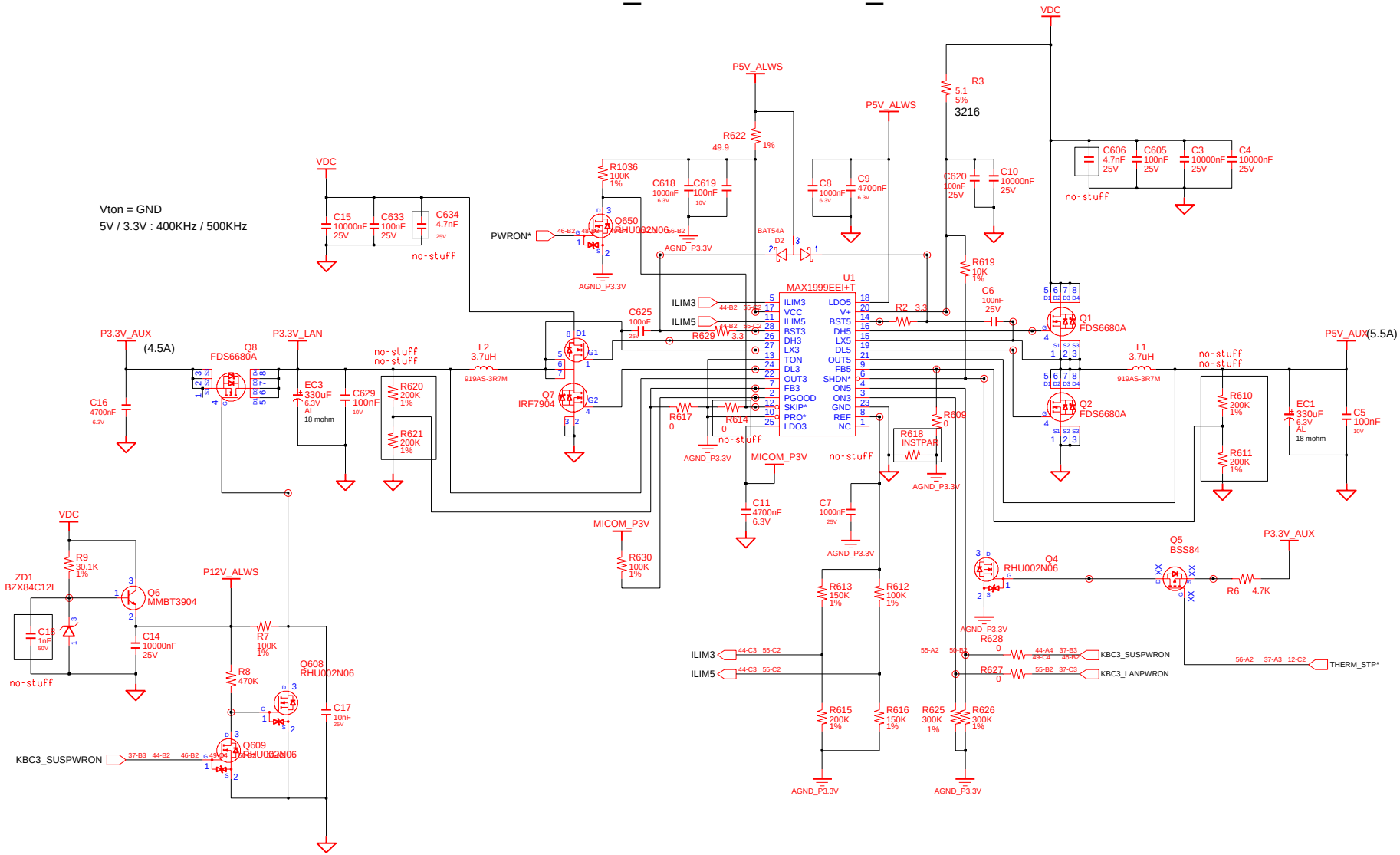




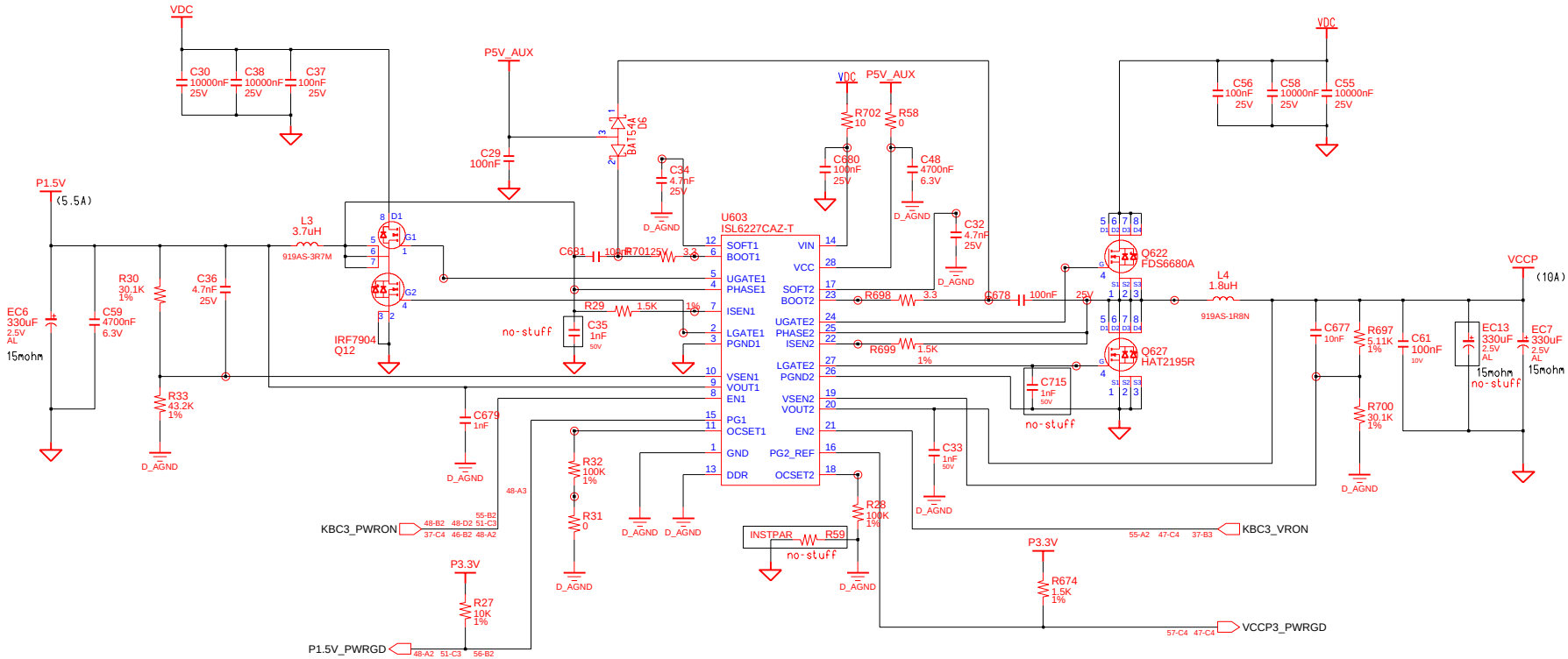
CHARGER & POWER MANAGEMENT



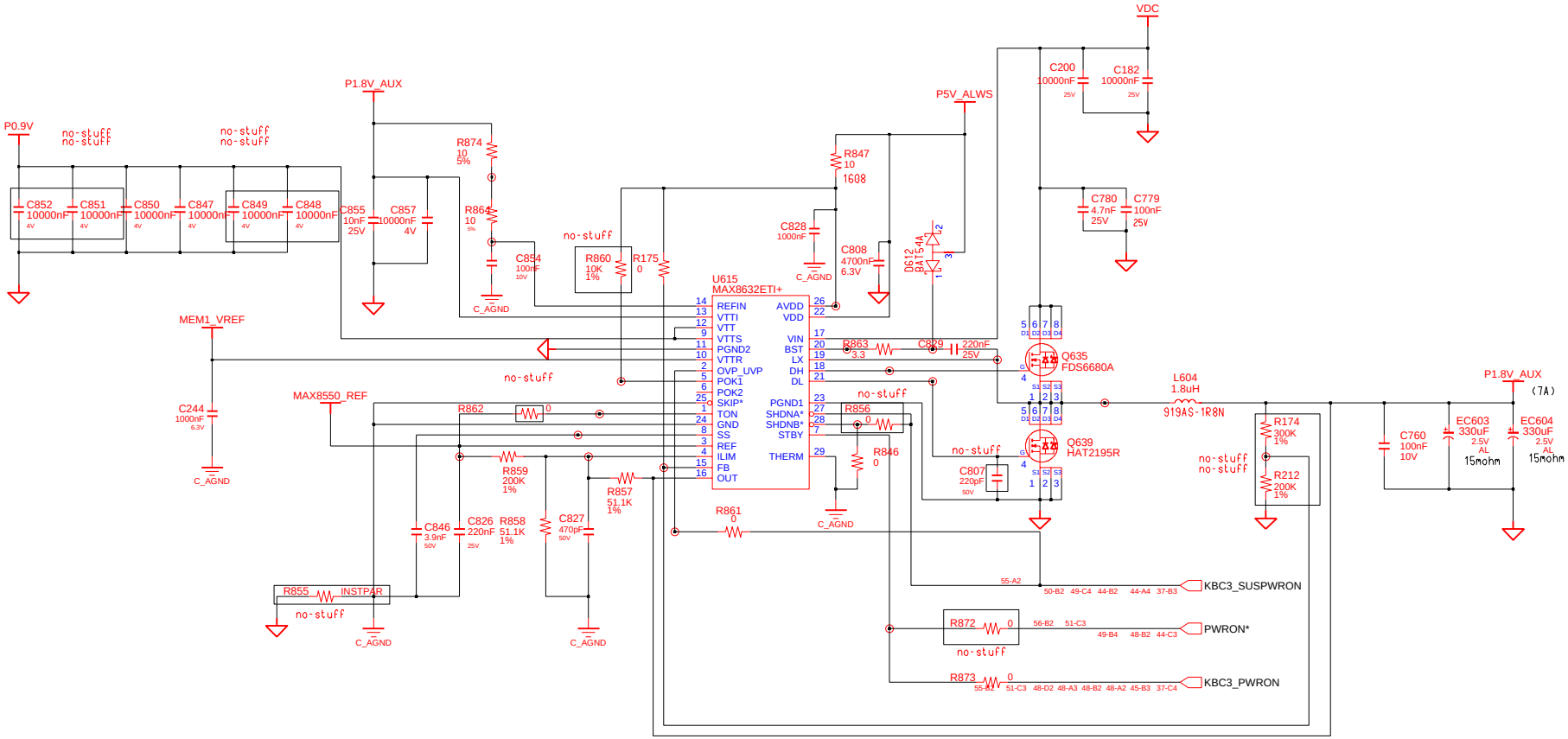
P3.3V_LAN/AUX & P5V_AUX



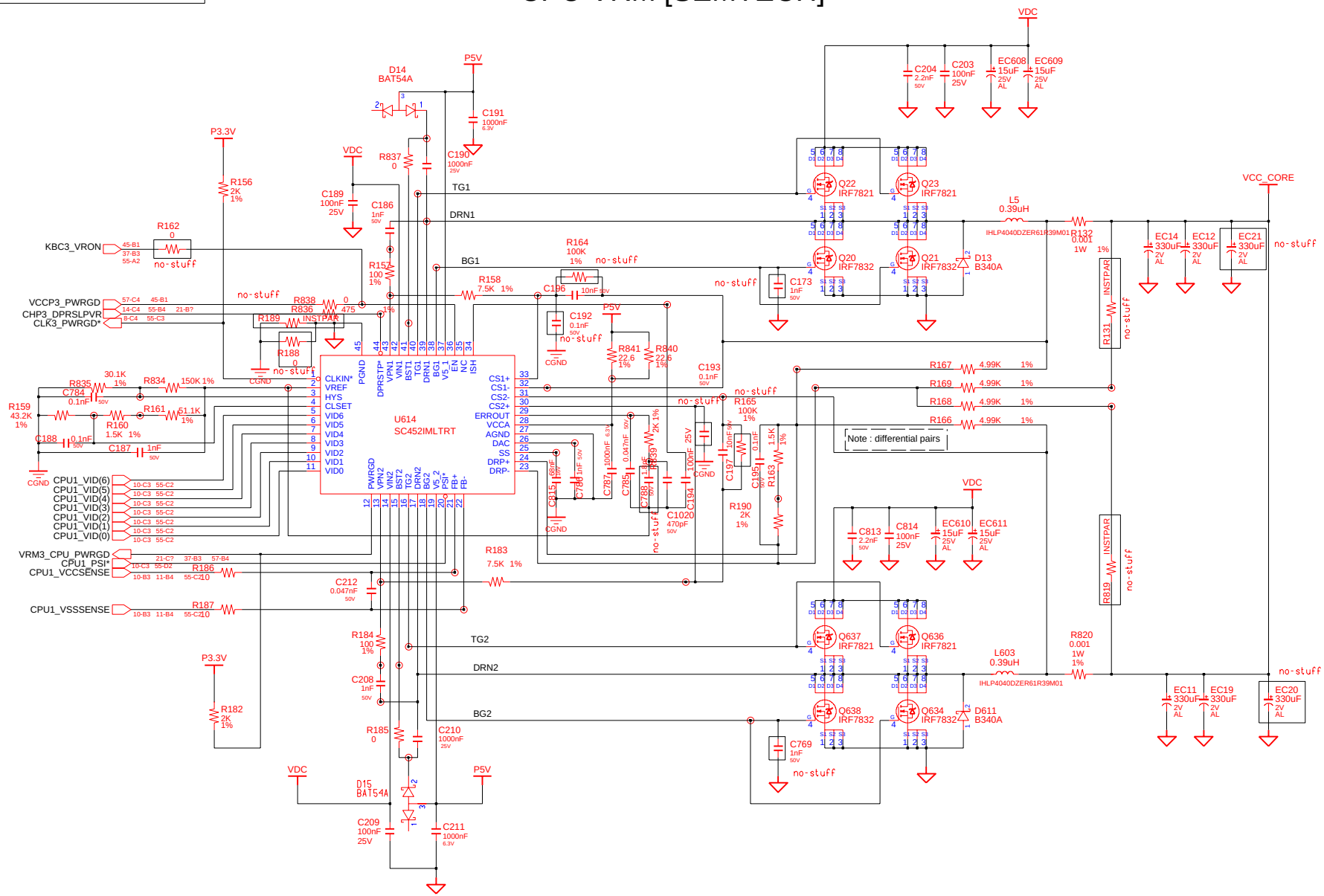
P1.5V & VCCP (1.05V)



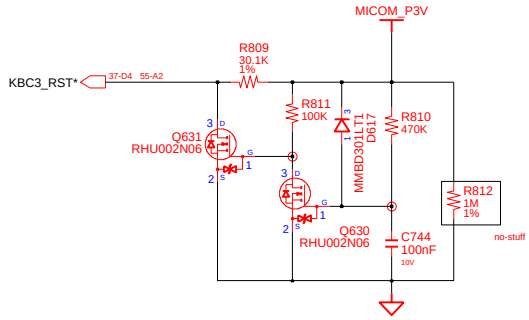
DDR2 Power



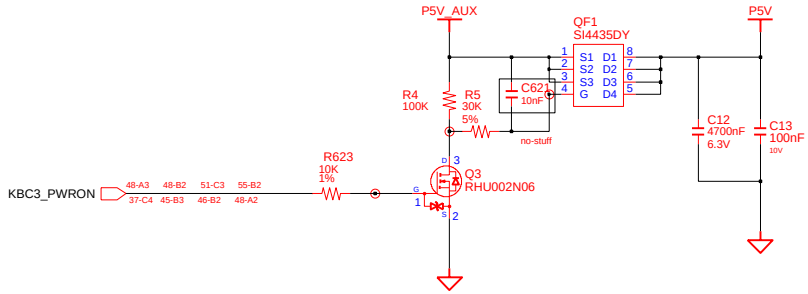
CPU VRM [SEMTECH]



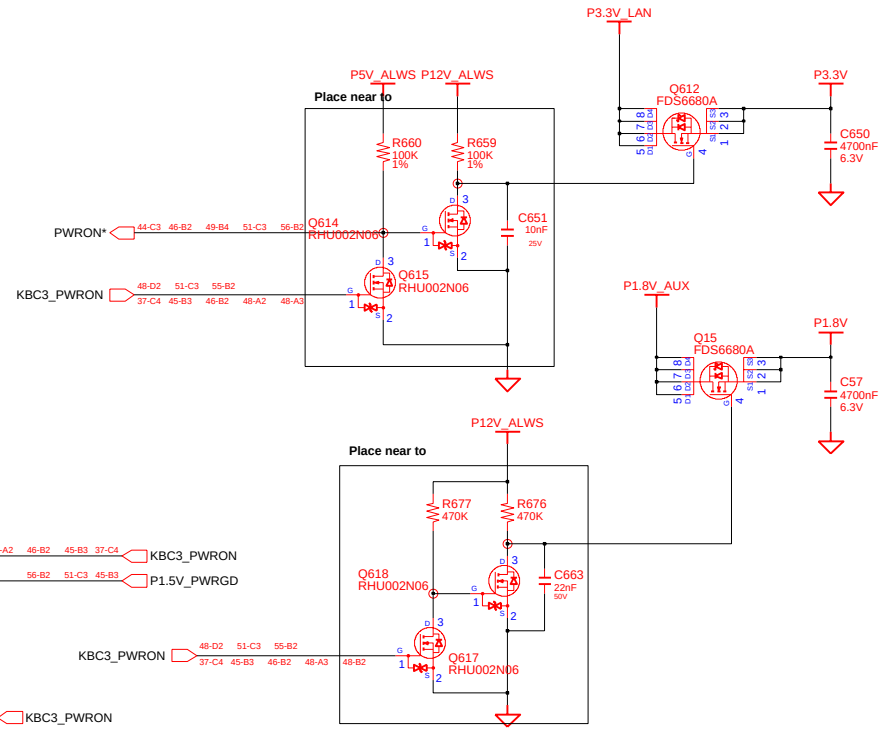
MICOM RESET



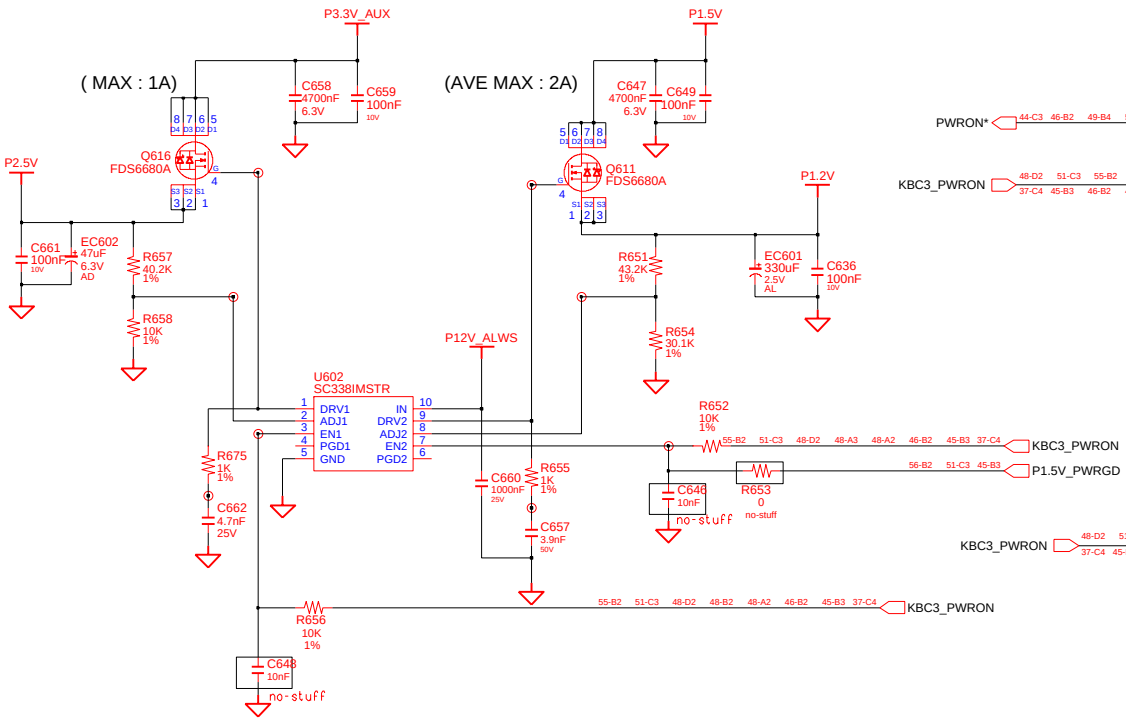
Switched Power On (P5V)

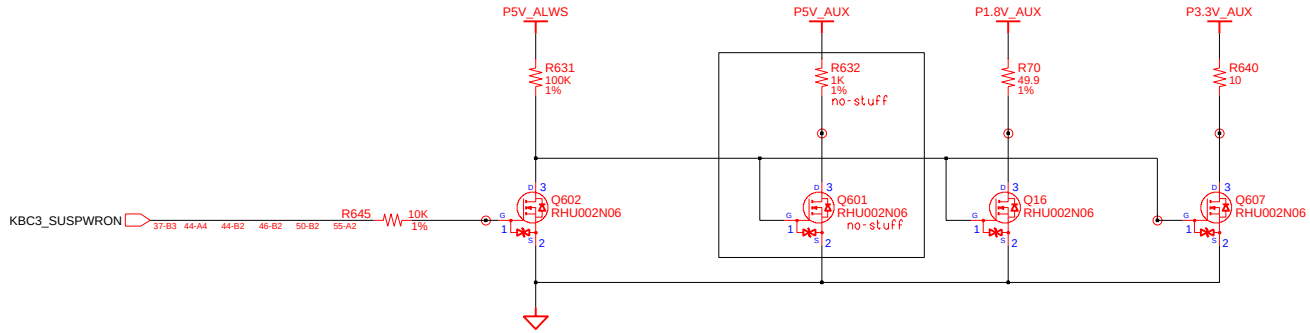


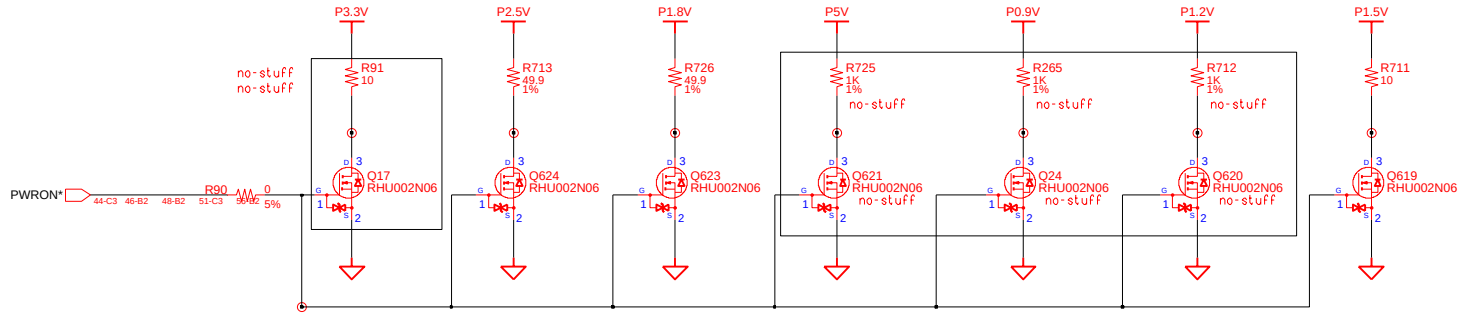
Switched Power On (P3.3V & 1.8V)



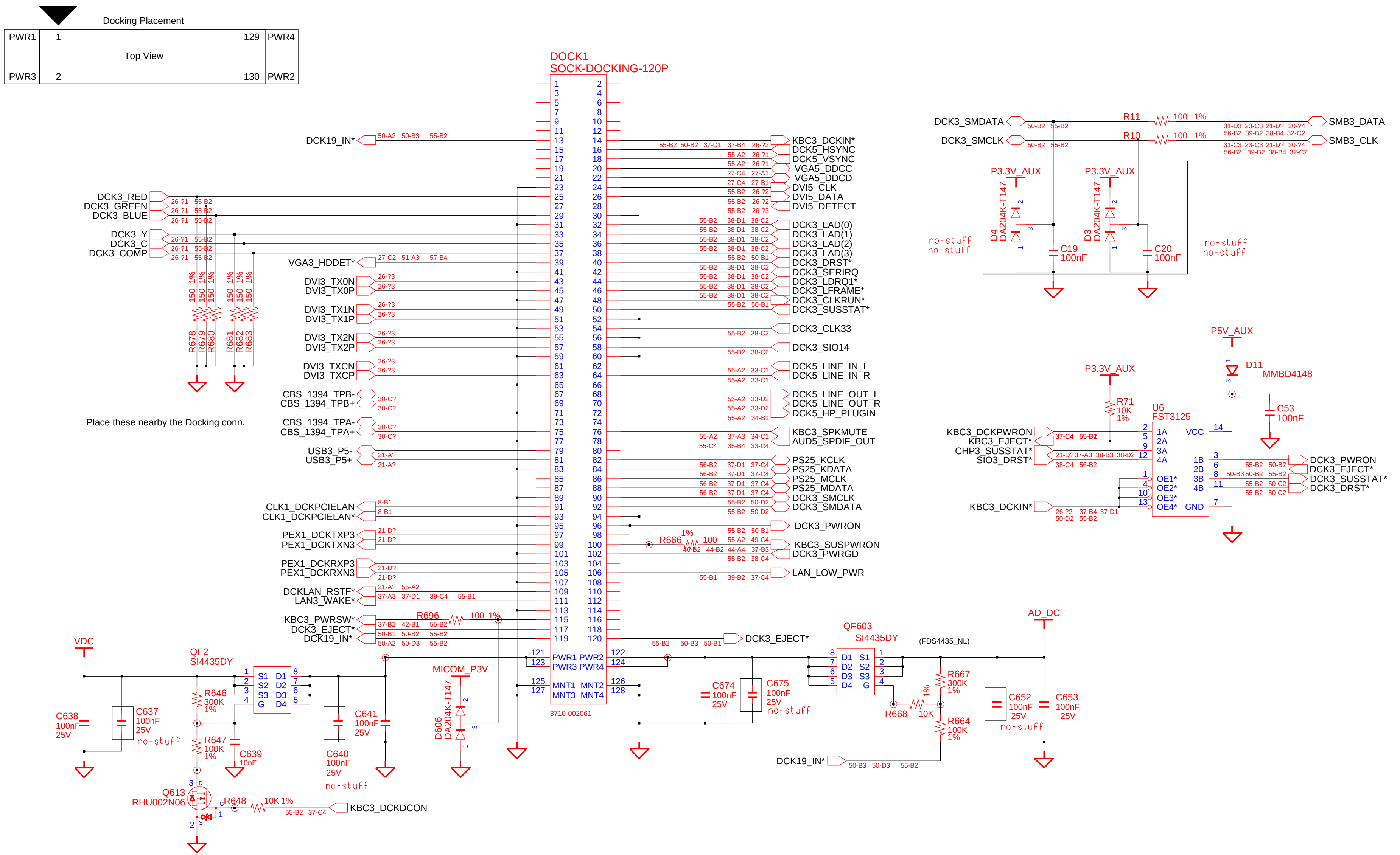
P1.2V / P2.5V POWER

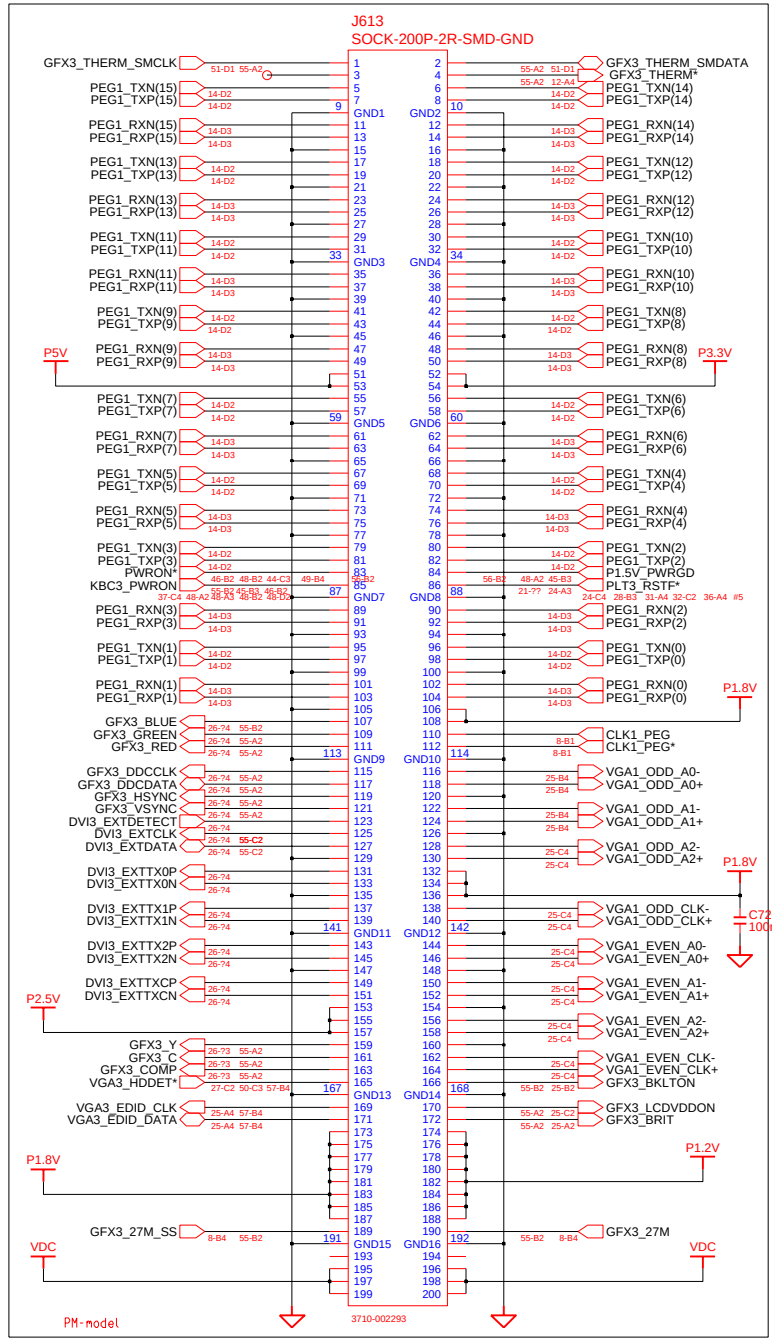


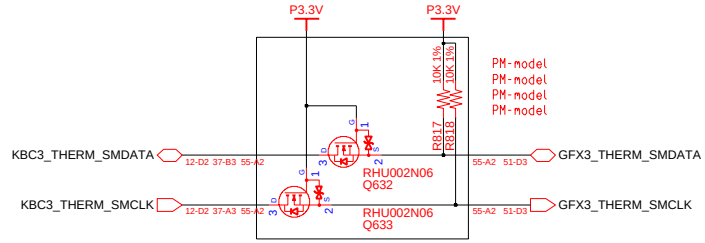


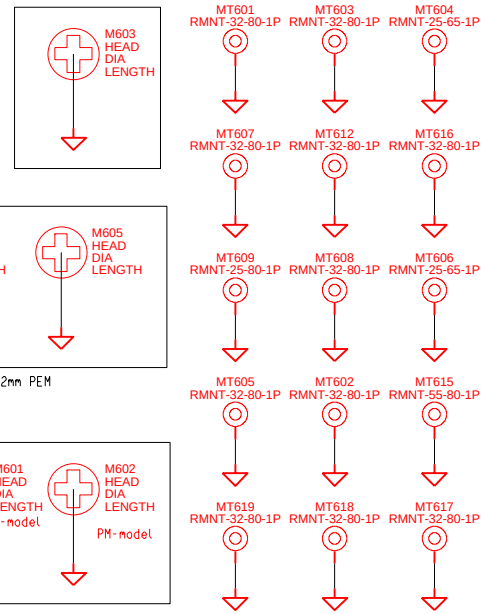


DOCKING CONNECTOR (130PIN)

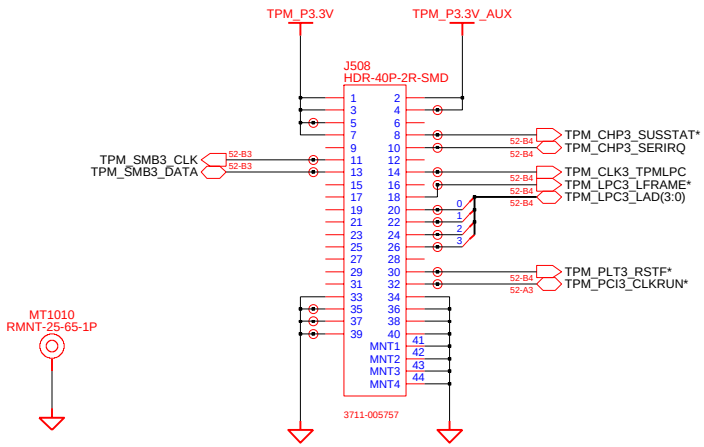




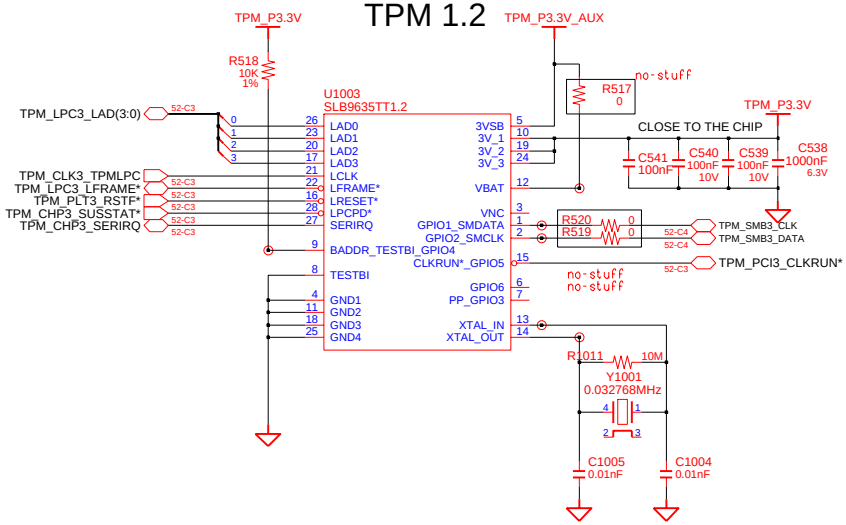




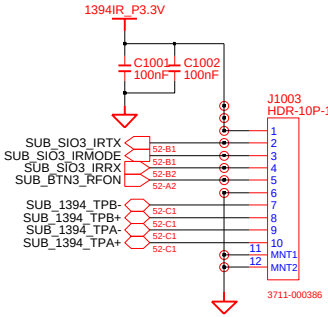
TPM BOARD

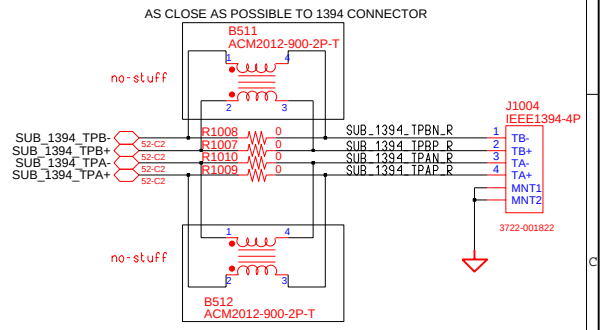


TPM 1.2

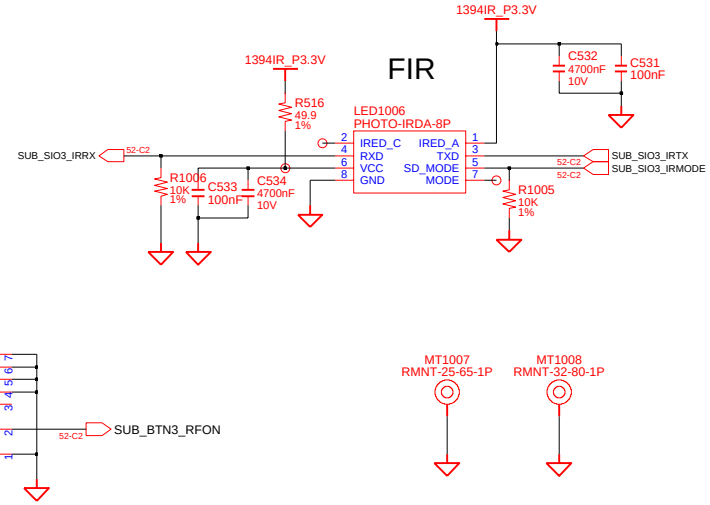


1394_IR BOARD

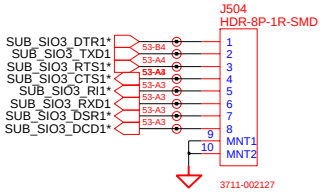


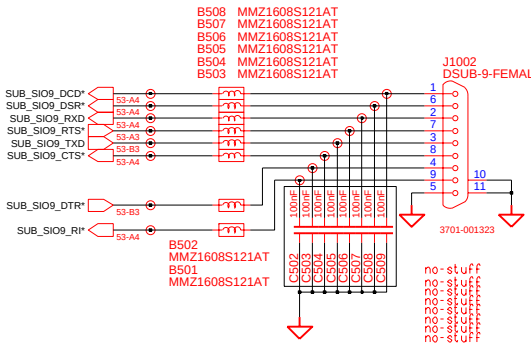


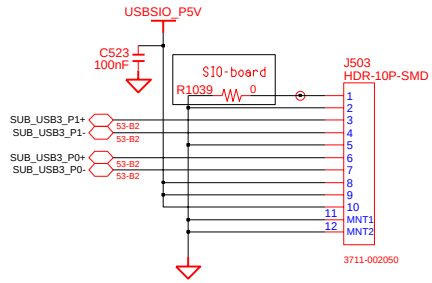
FIR

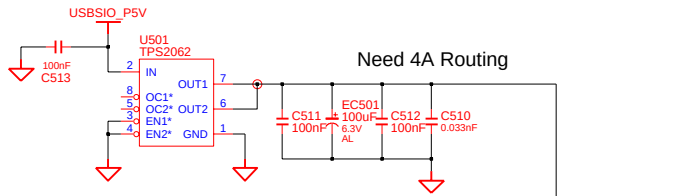


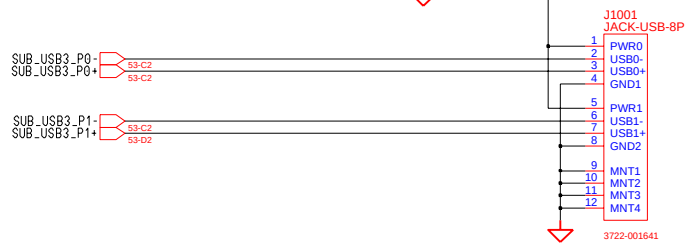
USB_SIO BOARD

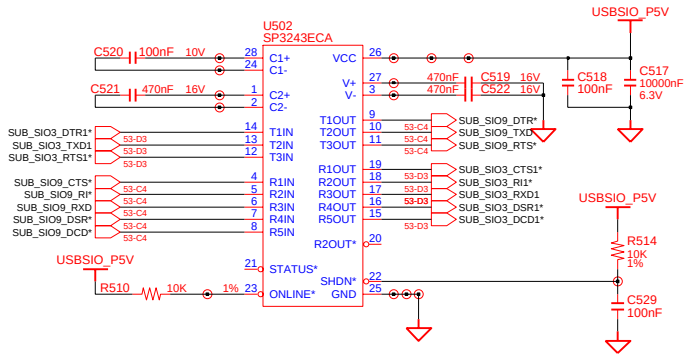


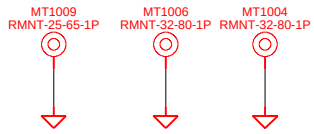




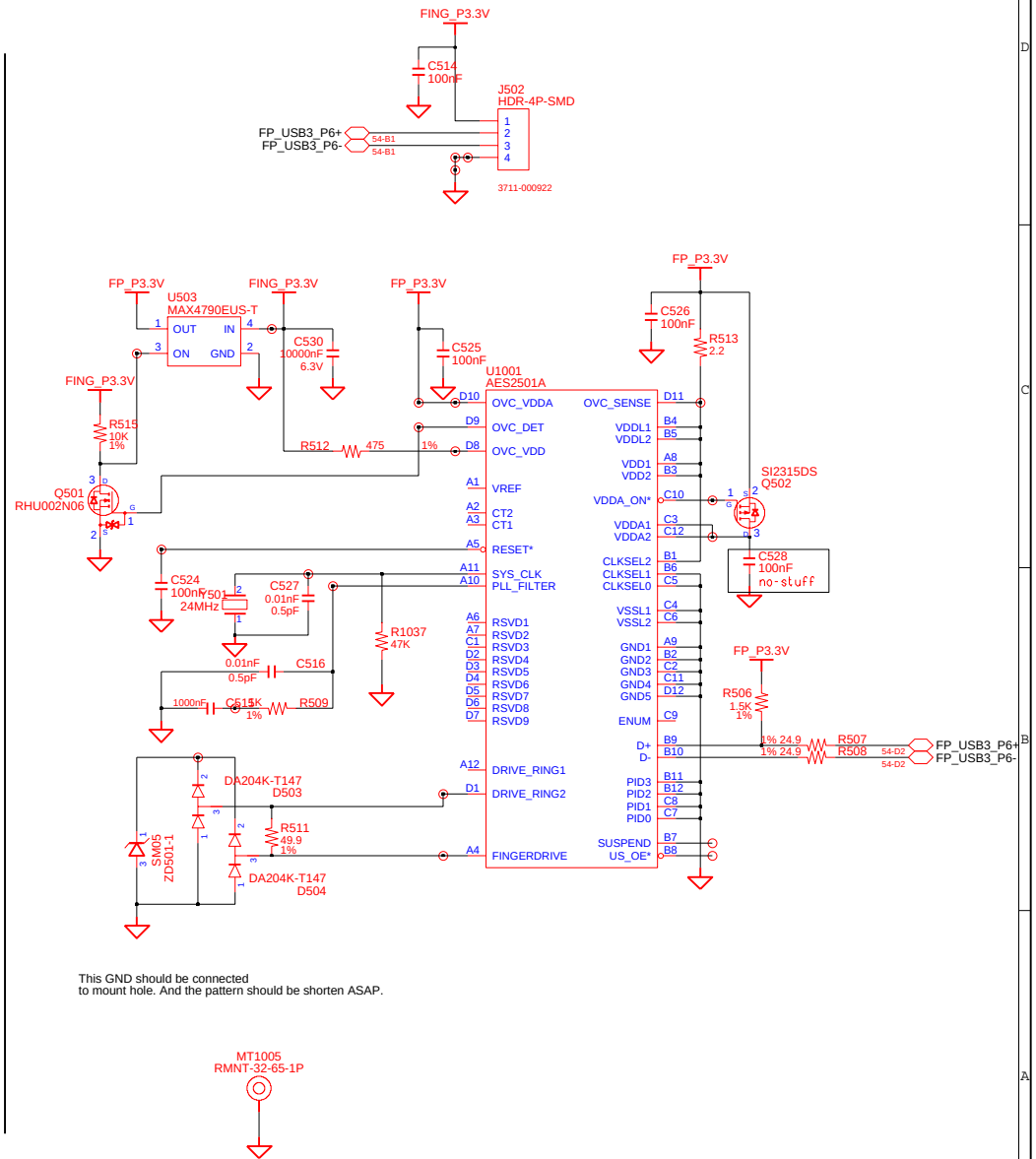








Finger Printer board



- ADT3_SEL
- AUD3_EAPD*
- AUD3_PCBEEP
- AUD5_LINE_OUT_L
- AUD5_LINE_OUT_R
- AUD5_SPDIF
- AUD5_SPDIF_OUT
- AUD5_SPK_L+
- AUD5_SPK_L-
- AUD5_SPK_R+
- AUD5_SPK_R-
- BAT3_DETECT*
- BAT3_SMCLK*
- BAT3_SMDATA*
- BAT3_VOLTA
- BLT_DETECT*
- BTN3_RFON
- BUF5_PLT_RSTF*
- CAPSLED*
- CBS3_A_A_18
- CBS3_A_A_19
- CBS3_A_D_14
- CBS3_A_D_2
- CBS3_CAD(0)
- CBS3_CAD(1)
- CBS3_CAD(10)
- CBS3_CAD(11)
- CBS3_CAD(12)
- CBS3_CAD(13)
- CBS3_CAD(14)
- CBS3_CAD(15)
- CBS3_CAD(16)
- CBS3_CAD(17)
- CBS3_CAD(18)
- CBS3_CAD(19)
- CBS3_CAD(2)
- CBS3_CAD(20)
- CBS3_CAD(21)
- CBS3_CAD(22)
- CBS3_CAD(23)
- CBS3_CAD(24)
- CBS3_CAD(25)
- CBS3_CAD(26)
- CBS3_CAD(27)
- CBS3_CAD(28)
- CBS3_CAD(29)
- CBS3_CAD(3)
- CBS3_CAD(30)
- CBS3_CAD(31)
- CBS3_CAD(4)
- CBS3_CAD(5)
- CBS3_CAD(6)
- CBS3_CAD(7)
- CBS3_CAD(8)
- CBS3_CAD(9)
- CBS3_CAUDIO
- CBS3_CCBE0*
- CBS3_CCBE1*
- CBS3_CCBE2*
- CBS3_CCBE3*
- CBS3_CCD1*
- CBS3_CCD2*
- CBS3_CCLK
- CBS3_CCLKRUN*
- CBS3_CDEVSEL*
- CBS3_CFRAME*
- CBS3_CGNT*
- CBS3_CINT*
- CBS3_CIRDY*
- CBS3_CPAR
- CBS3_CPERR*
- CBS3_CREQ*
- CBS3_CRST*
- CBS3_CSERR*
- CBS3_CSTOP*
- CBS3_CSTSCHG
- CBS3_CTRDY*
- CBS3_CVS1
- CBS3_CVS2
- CBS3_MD_CLK
- CBS3_MD_DATA0_MS_SDIO
- CBS3_MD_DATA1
- CBS3_MD_DATA2
- CBS3_MD_DATA3
- CBS3_MD_DATA4_XD
- CBS3_MD_DATA5_XD
- CBS3_MD_DATA6_XD
- CBS3_MD_DATA7_XD
- CBS3_MD_VCCEN
- CBS3_MD_XD_ALE
- CBS3_MD_XD_CE*
- CBS3_MD_XD_CLE
- CBS3_MD_XD_WP*
- CBS3_MS_BS_SD_CMD
- CBS3_MS_INS_XD_CD*
- CBS3_SD_CD_XD_CD*
- CBS3_SD_WP_XD_R_B*
- CBS3_SPKR
- CBS3_VCC3EN*
- CBS3_VCCGEN*
- CBS3_VPPEN0
- CBS3_VPPEN1
- CHP3_1394_ROMW*
- CHP3_AZ_AUD_BCLK
- CHP3_AZ_AUD_RST*
- CHP3_AZ_AUD_SDO
- CHP3_AZ_AUD_SYNC
- CHP3_AZ_MDC_BCLK
- CHP3_AZ_MDC_RST*
- CHP3_AZ_MDC_SDO
- CHP3_AZ_MDC_SYNC
- CHP3_AZ_SDI0
- CHP3_AZ_SDI1
- CHP3_BIOSTBL*
- CHP3_BIOSWP*
- CHP3_CAPSLED*
- CHP3_DPRSLPVR
- CHP3_INTRUDER*
- CHP3_LDRQ0*
- CHP3_LDRQ1*
- CHP3_NUMLED*
- CHP3_PCISTP*
- CHP3_SATACLKREQ*
- CHP3_SATALED*
- CHP3_SATA_DET*
- CHP3_SCLED*
- CHP3_SERIRQ
- CHP3_SLPS3*
- CHP3_SLPS4*
- CHP3_SLPS5*
- CHP3_SMLINK0
- CHP3_SMLINK1
- CHP3_SPKR
- CHP3_WKON_LAN_D
- CLK3_DBGLPC
- CLK3_FM48
- CLK3_ICH14
- CLK3_PCLKCB
- CLK3_PCLKFWH
- CLK3_PCLKICH
- CLK3_PCLKLAN
- CLK3_PCLKMICOM
- CLK3_PCLKSIO
- CLK3_PCLKSIO_DS
- CLK3_PWRGD*
- CLK3_SIO14
- CLK3_SMBCLK
- CLK3_SMBDATA
- CLK3_TPMLPC
- CLK3_USB48
- COEX1
- COEX2
- CPU1_A20M*
- CPU1_BSEL0
- CPU1_BSEL1
- CPU1_BSEL2
- CPU1_CPURST*
- CPU1_FERR*
- CPU1_IGNNE*
- CPU1_INIT*
- CPU1_NMI
- CPU1_PROCHOT*
- CPU1_PSI*
- CPU1_PWRGDCPU
- CPU1_SLP*
- CPU1_SMI*
- CPU1_TCK
- CPU1_TDI
- CPU1_THRMTRIP*
- CPU1_TMS
- CPU1_TRST*
- CPU1_VCCSENSE
- CPU1_VID(0)
- CPU1_VID(1)
- CPU1_VID(2)
- CPU1_VID(3)
- CPU1_VID(4)
- CPU1_VID(5)
- CPU1_VID(6)
- CPU1_VSSSENSE
- CPU2_THERMDA
- CPU2_THERMDC
- CPU3_ALERT*
- CPU3_THRMTRIP*
- CRT3_BLUE
- CRT3_DDCCLK
- CRT3_DDCDATA
- CRT3_GREEN
- CRT3_HSYNC
- CRT3_RED
- CRT3_VSYNC
- CRT5_HSYNC
- CRT5_VSYNC
- DCK19_IN*
- DCK3_BLUE
- DCK3_C
- DCK3_CLK33
- DCK3_CLKRUN*
- DCK3_COMP
- DCK3_DRST*
- DCK3_EJECT*
- DCK3_GREEN
- DCK3_LAD(0)
- DCK3_LAD(1)
- DCK3_LAD(2)
- DCK3_LAD(3)
- DCK3_LDRQ1*
- DCK3_LFRAME*
- DCK3_PWRGD
- DCK3_PWRON
- DCK3_RED
- DCK3_SERIRQ
- DCK3_SIO14
- DCK3_SMCLK
- DCK3_SMDATA
- DCK3_SUSSTAT*
- DCK3_Y
- DCK5_HP_PLUGIN
- DCK5_HSYNC
- DCK5_LINE_IN_L
- DCK5_LINE_IN_R
- DCK5_LINE_OUT_L
- DCK5_LINE_OUT_R
- DCK5_VSYNC
- DCKLAN_RSTF*
- DVI3_EXTCLK
- DVI3_EXTDATA
- DVI3_EXTDETECT
- DVI3_INTCLK
- DVI3_INTDATA
- DVI3_INTDETECT
- DVI5_CLK
- DVI5_DATA
- DVI5_DETECT
- DVO2_CTRLCLK
- DVO2_CTRLDATA
- EXP3_CLKREQ*
- EXP3_CPPE*
- EXP3_CPUSB*
- EXP3_PERST*
- FAN3_FDBACK*
- FWH3_INIT*
- GFX3_27M
- GFX3_27M_SS
- GFX3_BKLTON
- GFX3_BLUE
- GFX3_BRIT
- GFX3_C
- GFX3_COMP
- GFX3_DDCCLK
- GFX3_DDCDATA
- GFX3_GREEN
- GFX3_HSYNC
- GFX3_LCDVDDON
- GFX3_RED
- GFX3_THERM*
- GFX3_THERM_SMCLK
- GFX3_THERM_SMDATA
- GFX3_THRMTRIP*
- GFX3_VSYNC
- GFX3_Y
- HDD3_LED*
- HP_DETECT
- HP_OUT_L
- HP_OUT_R
- HP_POP
- IDE5_A0
- IDE5_A1
- IDE5_A2
- IDE5_CS1*
- IDE5_CS3*
- IDE5_D(0)
- IDE5_D(1)
- IDE5_D(10)
- IDE5_D(11)
- IDE5_D(12)
- IDE5_D(13)
- IDE5_D(14)
- IDE5_D(15)
- IDE5_D(2)
- IDE5_D(3)
- IDE5_D(4)
- IDE5_D(5)
- IDE5_D(6)
- IDE5_D(7)
- IDE5_D(8)
- IDE5_D(9)
- IDE5_DACK*
- IDE5_DASP*
- IDE5_DREQ
- IDE5_IDEIRQ
- IDE5_IOR*
- IDE5_IORDY
- IDE5_IOW*
- IDE5_PDIAG*
- ILIM3
- ILIM5
- INT3_BUTTON*
- INT_MIC
- ITP3_SYSRST*
- JCK_SENS
- JCK_SENS_HP
- JCK_SENS_MIC
- KBC3_A20G
- KBC3_BKLTON
- KBC3_BLKEXPWRSW*
- KBC3_CAPSLED*
- KBC3_CHGEN
- KBC3_CHKPWRSW*
- KBC3_CPURST*
- KBC3_DCKDCON
- KBC3_DCKIN*
- KBC3_EJECT*
- KBC3_EXTSMI*
- KBC3_FANCTRL
- KBC3_LANPWRON
- KBC3_LED_ACIN*
- KBC3_LED_CHARGE*
- KBC3_LED_POWER*
- KBC3_NUMLED*
- KBC3_PWMBRIT
- KBC3_PWRBTN*
- KBC3_PWRGD
- KBC3_PWRON
- KBC3_PWRSW*
- KBC3_RFOFF*
- KBC3_RSMRST*
- KBC3_RST*
- KBC3_RUNSCI*
- KBC3_SCLED*
- KBC3_SMCLK*
- KBC3_SMDATA*
- KBC3_SPKMUTE
- KBC3_SUSPWRON
- KBC3_THERM_SMCLK
- KBC3_THERM_SMDATA
- KBC3_VRON
- KBC3_WAKESCI*
- KBC3_WKON_LAN
- KBC3_WKON_LAN_D
- KBC5_CAL_THRM*
- KBC3_DCKPWRON
- KBC5_KSI(0)
- KBC5_KSI(1)
- KBC5_KSI(2)
- KBC5_KSI(3)
- KBC5_KSI(4)
- KBC5_KSI(5)
- KBC5_KSI(6)
- KBC5_KSI(7)
- KBC5_KSO(0)
- KBC5_KSO(1)
- KBC5_KSO(10)
- KBC5_KSO(11)
- KBC5_KSO(12)
- KBC5_KSO(13)
- KBC5_KSO(14)
- KBC5_KSO(15)
- KBC5_KSO(2)
- KBC5_KSO(3)
- KBC5_KSO(4)
- KBC5_KSO(5)
- KBC5_KSO(6)
- KBC5_KSO(7)
- KBC5_KSO(8)
- KBC5_KSO(9)
- KBC5_TCLK
- KBC5_TDATA
- LAN3_ACT*
- LAN3_EEP_CLK
- LAN3_EEP_CS
- LAN3_EEP_DI
- LAN3_EEP_DO
- LAN3_LINK_10*
- LAN3_LINK_100*
- LAN3_LINK_1000*
- LAN3_WAKE*
- LAN_LOW_PWR
- LCD3_BKLTCTRL
- LCD3_BKLTEN
- LCD3_BKLTON
- LCD3_BRIT
- LCD3_EDID_C
- LCD3_EDID_CLK
- LCD3_EDID_D
- LCD3_EDID_DATA
- LCD3_VDDEN
- LID3_SWITCH*
- LPC3_LAD(0)
- LPC3_LAD(1)
- LPC3_LAD(2)
- LPC3_LAD(3)
- LPC3_LFRAME*
- MCH1_HXSWING
- MCH1_HYSWING
- MCH3_BMBUSY*
- MCH3_CFG(10)
- MCH3_CFG(11)

MCH3_CFG(12)
MCH3_CFG(13)
MCH3_CFG(16)
MCH3_CFG(19)
MCH3_CFG(20)
MCH3_CFG(5)
MCH3_CFG(9)
MCH3_CLKREQ*
MCH3_ICHSYNC*

MIO3_BUTTON*
MIO_INT_BTN*

PCI3_AD(22)
PCI3_AD(23)
PCI3_AD(24)
PCI3_AD(25)
PCI3_AD(26)
PCI3_AD(27)
PCI3_AD(28)
PCI3_AD(29)
PCI3_AD(3)
PCI3_AD(30)
PCI3_AD(31)
PCI3_AD(4)
PCI3_AD(5)
PCI3_AD(6)
PCI3_AD(7)
PCI3_AD(8)
PCI3_AD(9)
PCI3_CBE0*
PCI3_CBE1*
PCI3_CBE2*
PCI3_CBE3*
PCI3_CLKRUN*
PCI3_DEVSEL*
PCI3_FRAME*
PCI3_GNT0*
PCI3_GNT1*
PCI3_INTA*
PCI3_INTB*
PCI3_INTC*
PCI3_INTD*
PCI3_INTE*
PCI3_INTF*
PCI3_INTG*
PCI3_INTH*
PCI3_IRDY*
PCI3_PAR
PCI3_PERR*
PCI3_PLOCK*
PCI3_REQ0*
PCI3_REQ1*
PCI3_REQ2*
PCI3_REQ3*
PCI3_RST*
PCI3_SERR*
PCI3_STOP*
PCI3_TRDY*

PEX3_WAKE*
PLT3_RST*
PLT3_RSTF*
PS25_KCLK
PS25_KDATA
PS25_MCLK
PS25_MDATA
PWRON*

SCLED*

SIO3_DET*
SIO3_CTS1*
SIO3_DCD1*
SIO3_DRST*
SIO3_DSR1*
SIO3_DTR1*
SIO3_IRMODE
SIO3_IRRX
SIO3_IRTX
SIO3_RI1*
SIO3_RTS1*
SIO3_RXD1
SIO3_TXD1
SMB3_ALERT*
SMB3_CLK
SMB3_DATA
SMB3_LINKALERT*
SYS3_C
SYS3_COMP
SYS3_Y
THERM_STP*
THRM_ALERT*

NUMLED*
ODD3_SEL
P1.5V_PWRGD
PCI3_AD(0)
PCI3_AD(1)
PCI3_AD(10)
PCI3_AD(11)
PCI3_AD(12)
PCI3_AD(13)
PCI3_AD(14)
PCI3_AD(15)
PCI3_AD(16)
PCI3_AD(17)
PCI3_AD(18)
PCI3_AD(19)
PCI3_AD(2)
PCI3_AD(20)
PCI3_AD(21)

MIC1
MIC2
MINIPCIE3_CLKREQ*

MCH3_EXTTS0*

AUD3_EAPD_A

PRE_INT_MIC

TV03_C
TV03_COMP
TV03_COMP_INT
TV03_C_INT
TV03_Y
TV03_Y_INT

VCCP3_PWRGD

VGA3_BLUE_INT
VGA3_DDCCLK
VGA3_DDCDATA
VGA3_EDID_CLK
VGA3_EDID_DATA
VGA3_GREEN_INT
VGA3_HDDET*
VGA3_HSYNC
VGA3_RED_INT
VGA3_VSYNC
VRM3_CPU_PWRGD
WLON_LED*
VREF_OUT_CL

AD_DC
AD_DC
AD_DC
AD_DC
AD_DC
AGND_AUD
AGND_AUD
AGND_AUD
AGND_AUD
AGND_AUD
AGND_CHG
AGND_CHG

AGND_P3.3V

AMP_VDD

AVDD
AVDD

CB_MD_VCC

CB_VCCA

CB_VPPA

CGND

CHG_REF

C_AGND

D_AGND

GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
INV_VDC

MGND_AUD

LCD_VDD3V

LDO_P5.4V

MEM1_VREF

MICOM_P3V

P0.9V
P0.9V
P0.9V
P0.9V
P0.9V
P1.2V
P1.2V

P1.2V
P1.2V
P1.2V
P1.2_1.8V_LAN
P1.2_1.8V_LAN
P1.2_1.8V_LAN
P1.2_1.8V_LAN
P1.2_1.8V_LAN
P1.5V
P1.5V
P1.5V
P1.5V
P1.5V
P1.5V_EXP
P1.5V_EXP

P1.5V_PCIE
P1.5V_PCIE

P1.8V
P1.8V
P1.8V
P1.8V
P1.8V
P1.8V_AUX
P1.8V_AUX
P1.8V_AUX
P1.8V_AUX
P1.8V_AUX
P12V_ALWS
P12V_ALWS

P2.5V
P2.5V
P2.5V
P2.5V
P2.5V
P2.5_3.3V_LAN
P2.5_3.3V_LAN
P2.5_3.3V_LAN
P2.5_3.3V_LAN
P2.5_3.3V_LAN
P3.3V
P3.3V
P3.3V
P3.3V
P3.3V
P3.3V_AUX
P3.3V_AUX
P3.3V_AUX
P3.3V_AUX
P3.3V_AUX
P3.3V_AUX_EXP
P3.3V_AUX_EXP

P3.3V_EXP
P3.3V_EXP

P3.3V_LAN
P3.3V_LAN
P3.3V_LAN
P3.3V_LAN
P3.3V_LAN
P5V
P5V
P5V
P5V
P5V

P5V_ALWS
P5V_ALWS

P5V_AUX
P5V_AUX
P5V_AUX
P5V_AUX
P5V_AUX
PRTC_BAT

VCCP
VCCP
VCCP
VCCP
VCCP
VCC_CORE
VCC_CORE
VCC_CORE
VCC_CORE
VCC_CORE
VCC_CRT

VDC
VDC
VDC
VDC
VDC

MGND_AUD
MGND_AUD
MGND_AUD

C1035 0.0033nF
C1031 0.015nF
C1033 0.02nF
C1037 0.033nF
C1027 0.047nF
C1025 0.1nF
C1039 0.01nF 0.5pF
C1029 0.007nF 50V 0.5pF

C1036 0.0033nF
C1032 0.015nF
C1034 0.02nF
C1038 0.033nF
C1028 0.047nF
C1026 0.1nF
C1040 0.01nF 0.5pF
C1030 0.007nF 50V 0.5pF

REV601
1
2
3

PCB REVISION CONTROL (ICT)

NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

EXT GFx

CPU :
Chip Set : NVIDIA 7X series
Remarks :

Model Name	:	HABANA EXT GFx
PBA Name	:	
PCB Code	:	
Dev. Step	:	MP
Revision	:	1.0
T.R. Date	:	2005.11.14

DRAW	CHECK	APPROVAL
SE LEE	ES CHO	BL LEE

J501
HEAD-200P-2R-SMD-GND

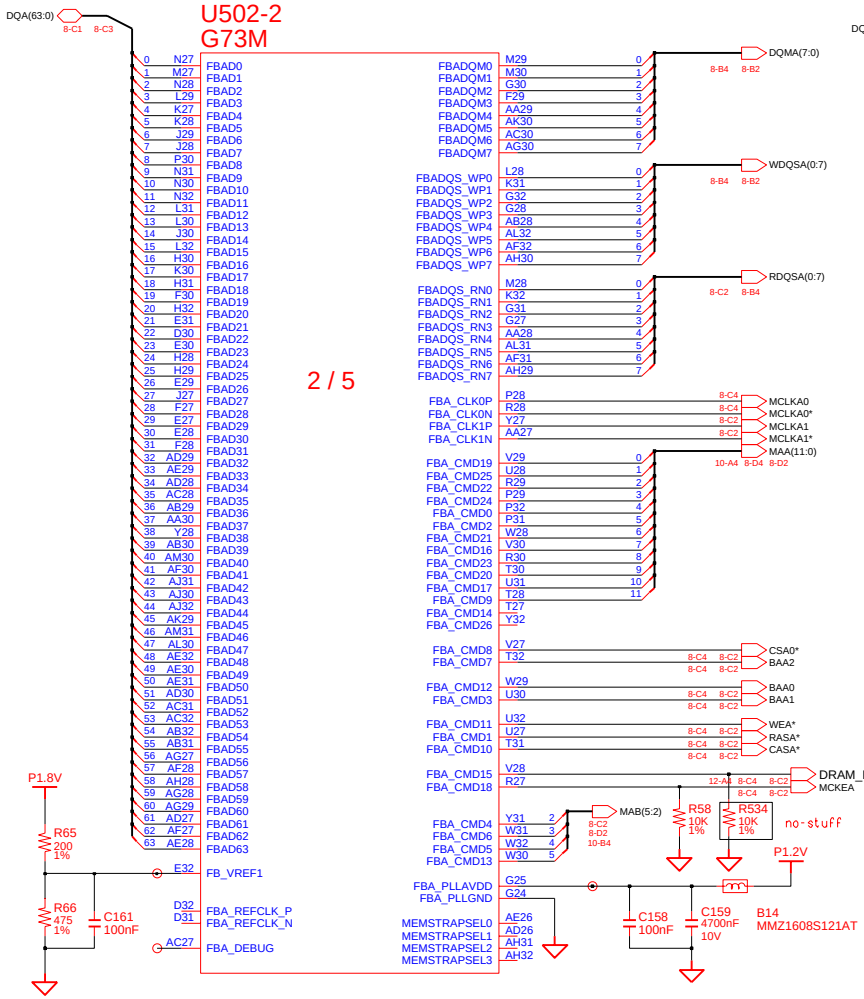
THERM_SMCLK
PEG1_TXN(15)
PEG1_TXP(15)
PEG1_RXN(15)
PEG1_RXP(15)
PEG1_TXN(13)
PEG1_TXP(13)
PEG1_RXN(13)
PEG1_RXP(13)
PEG1_TXN(11)
PEG1_TXP(11)
PEG1_RXN(11)
PEG1_RXP(11)
PEG1_TXN(9)
PEG1_TXP(9)
PEG1_RXN(9)
PEG1_RXP(9)
PEG1_TXN(7)
PEG1_TXP(7)
PEG1_RXN(7)
PEG1_RXP(7)
PEG1_TXN(5)
PEG1_TXP(5)
PEG1_RXN(5)
PEG1_RXP(5)
PEG1_TXN(3)
PEG1_TXP(3)
PWRON*
KBC3_PWRON
PEG1_RXN(3)
PEG1_RXP(3)
PEG1_TXN(1)
PEG1_TXP(1)
PEG1_RXN(1)
PEG1_RXP(1)
GFX3_BLUE
GFX3_GREEN
GFX3_RED
GFX3_DDCCLK
GFX3_DDCDATA
GFX3_HSYNC
GFX3_VSYNC
GFX3_HTPLG
GFX3_DVICLK
GFX3_DVIDATA
GFX3_TX0P
GFX3_TX0N
GFX3_TX1P
GFX3_TX1N
GFX3_TX2P
GFX3_TX2N
GFX3_TXCP
GFX3_TXCN
GFX3_Y
GFX3_C
GFX3_COMP
HDDECT*
EDID_CLK
EDID_DATA
GFX3_27M_SS
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
GND16
THERM_SMDATA
GFX3_THERM*
PEG1_TXN(14)
PEG1_TXP(14)
PEG1_RXN(14)
PEG1_RXP(14)
PEG1_TXN(12)
PEG1_TXP(12)
PEG1_RXN(12)
PEG1_RXP(12)
PEG1_TXN(10)
PEG1_TXP(10)
PEG1_RXN(10)
PEG1_RXP(10)
PEG1_TXN(8)
PEG1_TXP(8)
PEG1_RXN(8)
PEG1_RXP(8)
PEG1_TXN(6)
PEG1_TXP(6)
PEG1_RXN(6)
PEG1_RXP(6)
PEG1_TXN(4)
PEG1_TXP(4)
PEG1_RXN(4)
PEG1_RXP(4)
PEG1_TXN(2)
PEG1_TXP(2)
P1.5V_PWRGD
PLT3_RSTF*
PEG1_RXN(2)
PEG1_RXP(2)
PEG1_TXN(0)
PEG1_TXP(0)
PEG1_RXN(0)
PEG1_RXP(0)
CLK1_PEG
CLK1_PEG*
VGA1_ODD_A0-
VGA1_ODD_A0+
VGA1_ODD_A1-
VGA1_ODD_A1+
VGA1_ODD_A2-
VGA1_ODD_A2+
VGA1_ODD_CLK-
VGA1_ODD_CLK+
VGA1_EVEN_A0-
VGA1_EVEN_A0+
VGA1_EVEN_A1-
VGA1_EVEN_A1+
VGA1_EVEN_A2-
VGA1_EVEN_A2+
VGA1_EVEN_CLK-
VGA1_EVEN_CLK+
GFX3_BLON
GFX3_LCDVDDON
GFX3_BRIT
GFX3_27M
P5V
P3.3V
P2.5V
P1.8V
P1.8V
P1.2V
VDC
VDC
C7 100nF
C8 100nF
C6 100nF
C5 100nF
C4 100nF
C3 100nF
C13 100nF
C2 100nF 25V
C1 100nF 25V
no-stuff
R1
3711-006000

MT4 RMNT-28-45-1P
MT8 RMNT-28-45-1P
MT7 RMNT-28-45-1P
MT6 RMNT-28-45-1P
MT2 RMNT-28-45-1P
MT9 RMNT-28-45-1P
MT1 RMNT-28-45-1P
MT3 RMNT-28-45-1P
MT5 RMNT-25-45-1P
EM1 CONTACT-PLATE-EMI SMI

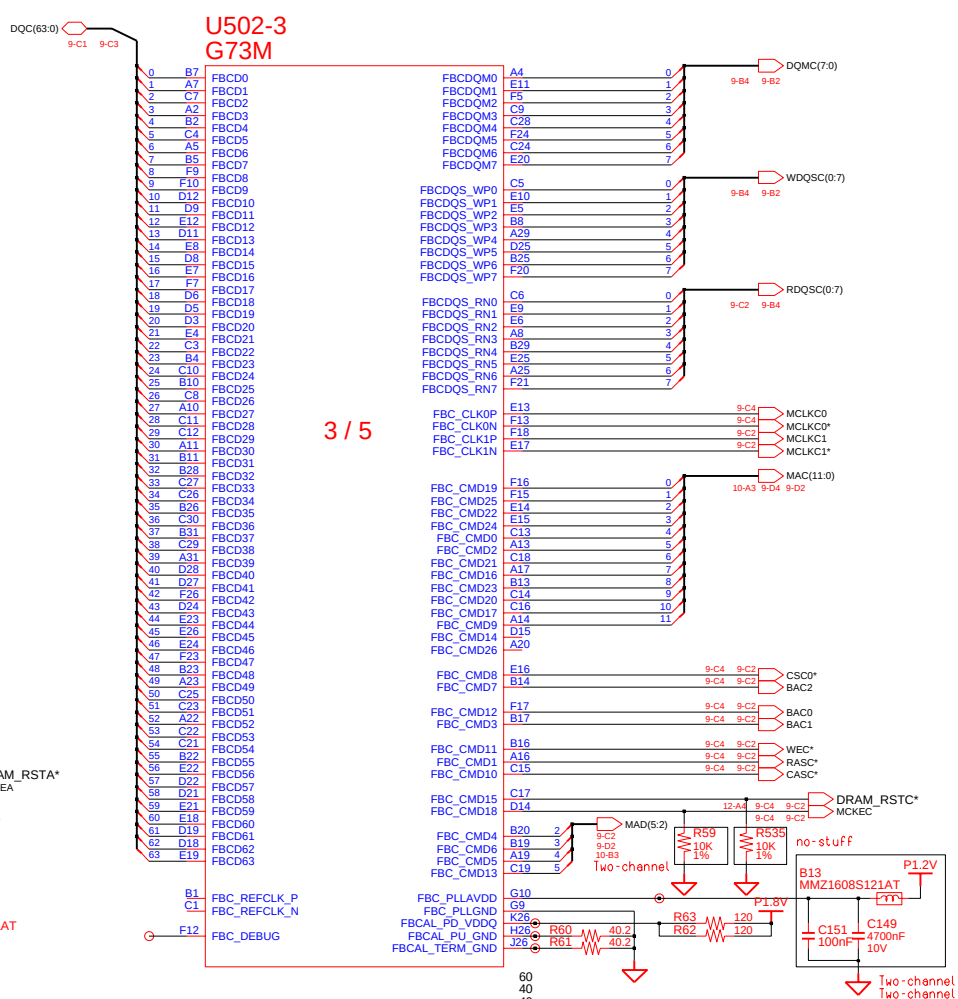
U502-1
G73M
1 / 5

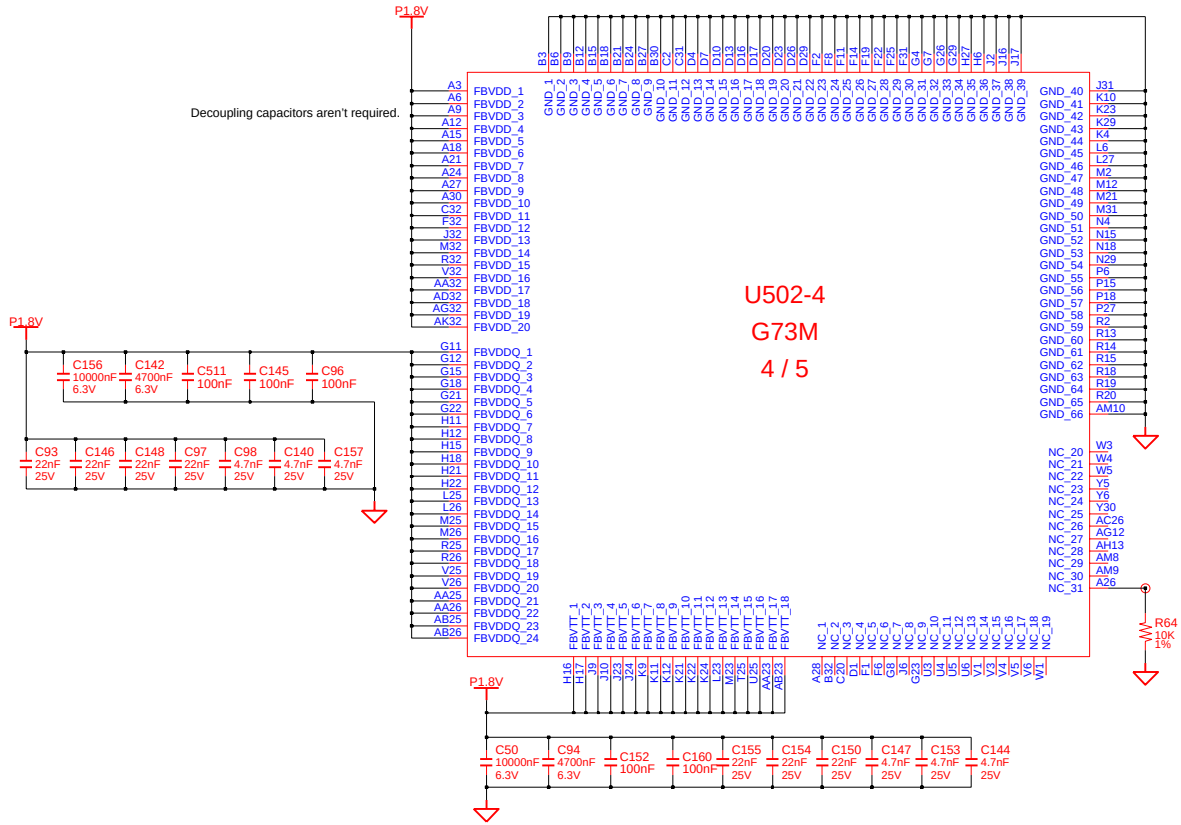
Pin	Description	Activate
GPIO(0)	DVI detect	High
GPIO(1)	TV detect	Low
GPIO(2)	PWM Brigtness control	High
GPIO(3)	LCD VDD on enable	High
GPIO(4)	Backlight on/off	High
GPIO(5)	GPU voltage ID0	High = 1.0V, Low = 1.1V
GPIO(6)	GPU Voltage ID1	NC
GPIO(7)	GPU voltage ID2	NC
GPIO(8)	Thermal diode Alert	Low
GPIO(9)	Fan control	NC
GPIO(10)	TBD	NC
GPIO(11)	HDTV enable	High
GPIO(12)	HDTV DET	NC

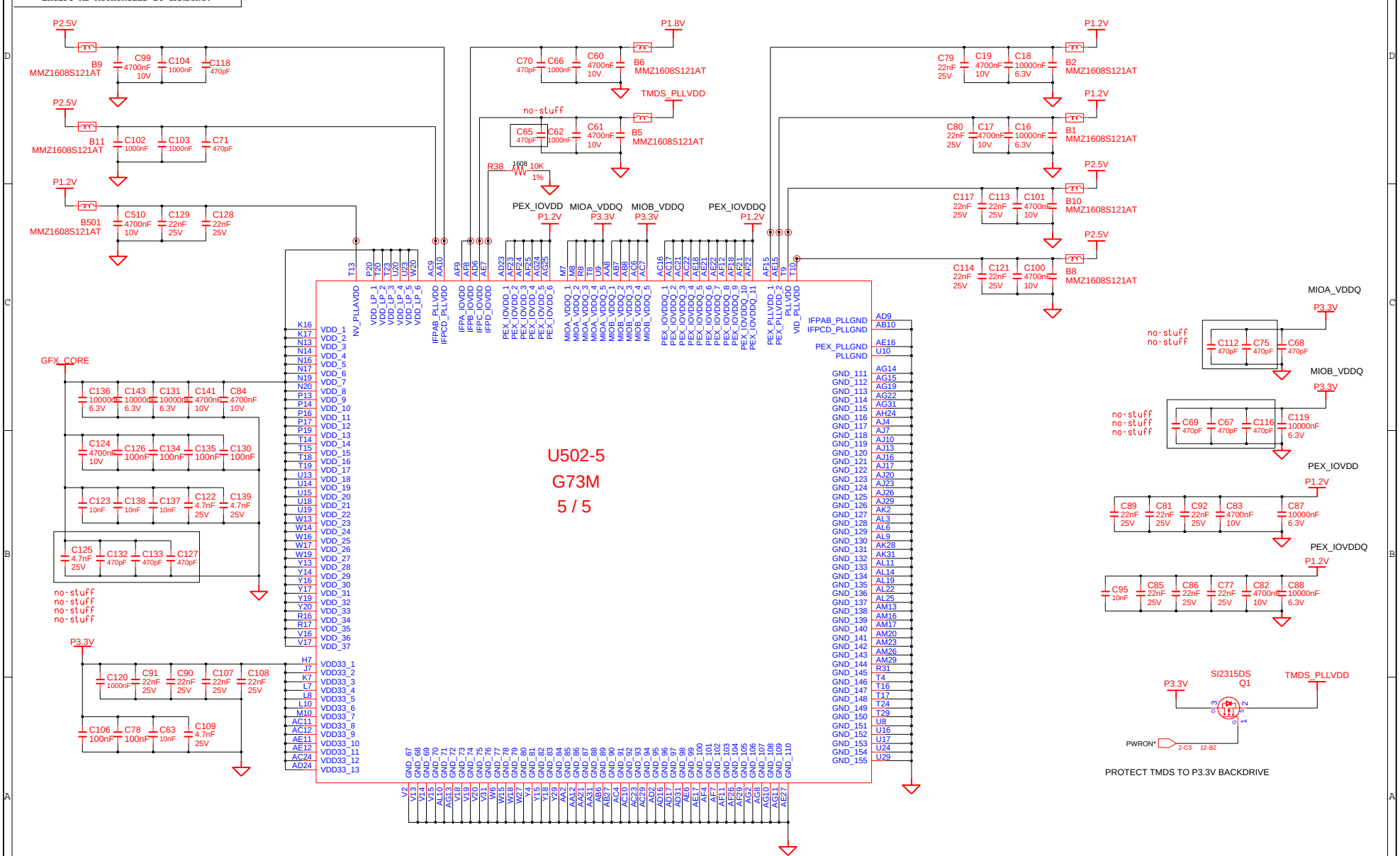
Graphic Memory I/F (Using FBA Channel)



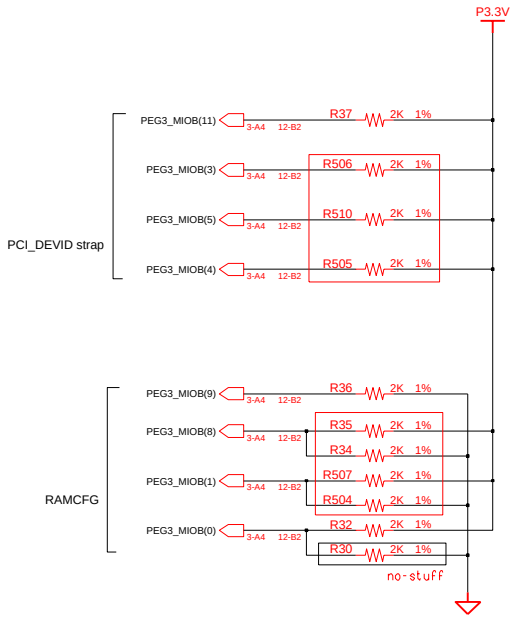
Graphic Memory I/F (Using FBC Channel)







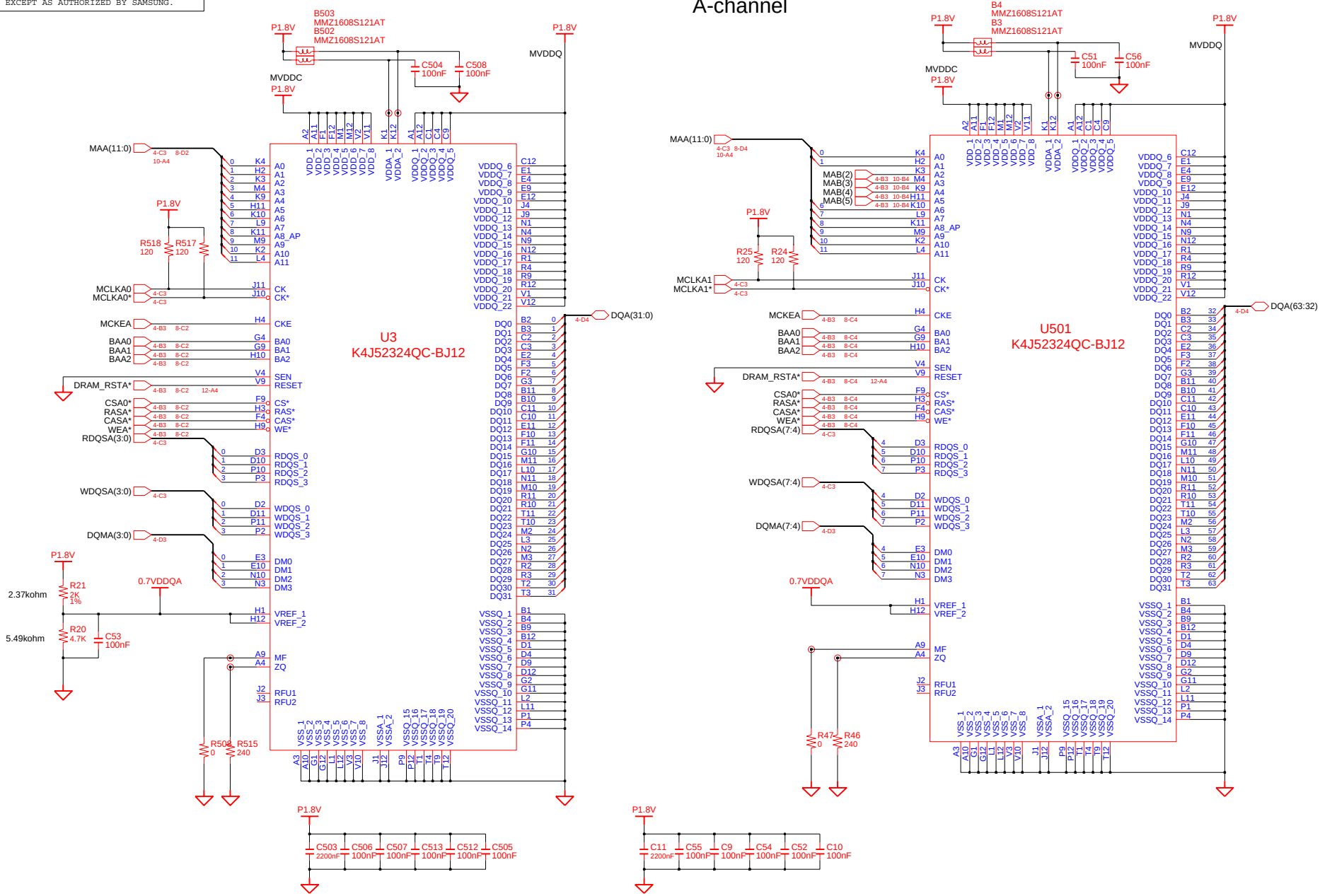
	R37	R506	R510	R505
72M-V	no-stuff	stuff	stuff	stuff
72M	stuff	no-stuff	no-stuff	no-stuff
73M	stuff	no-stuff	no-stuff	no-stuff



	R35	R34	R507	R504
SS 256Mb	stuff	no-stuff	stuff	no-stuff
INF 256Mb	stuff	no-stuff	no-stuff	stuff
SS 512Mb	no-stuff	stuff	stuff	no-stuff
INF 512Mb	no-stuff	stuff	no-stuff	stuff

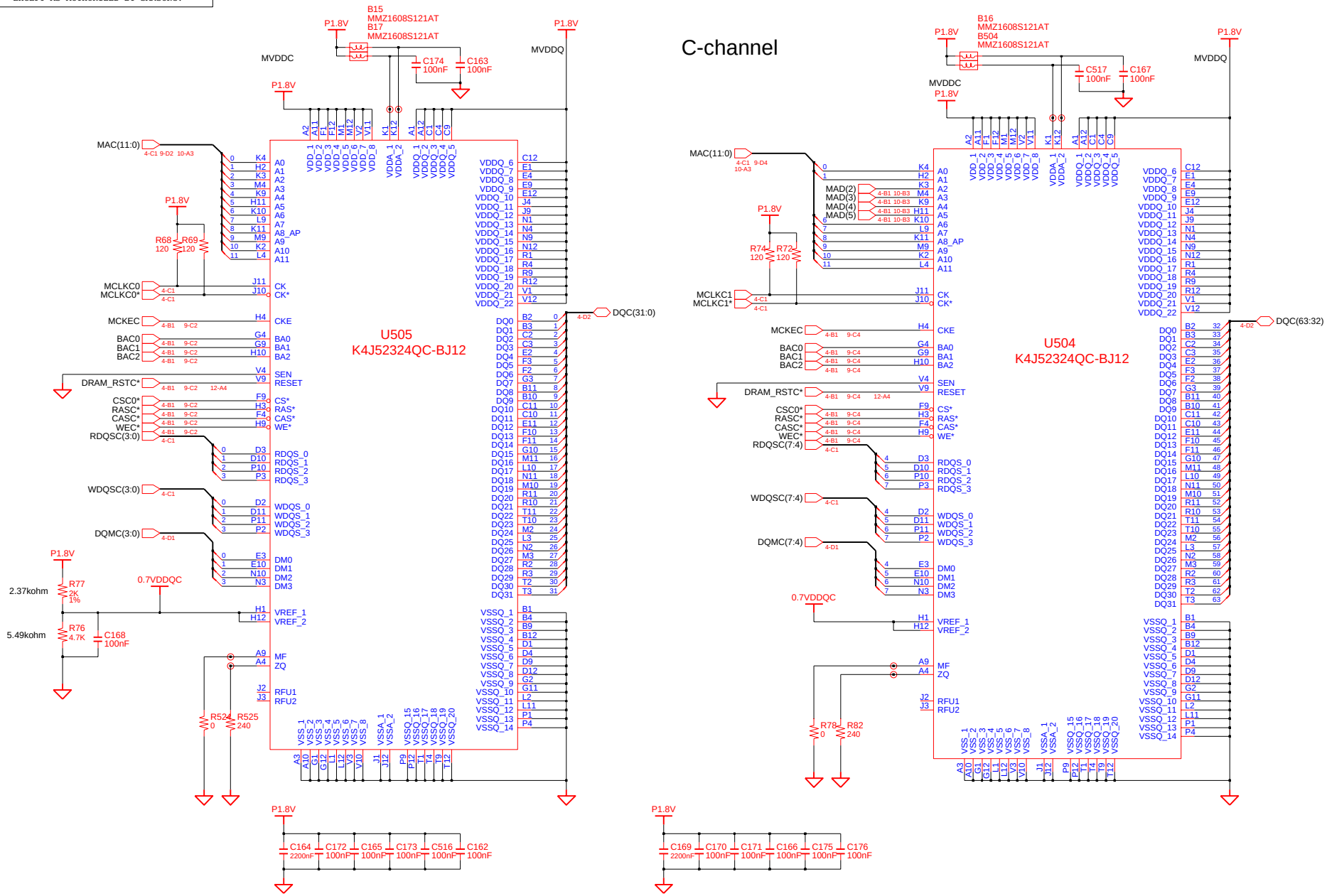
Straps	Pin # (Rev.A02)	Descriptions
SUB_VENDOR	MIOAD(1)	0 : No BIOS 1 : Read from BIOS(Default)
RAMCFG(3:0) [9,8,1,0]	MIOB(9) MIOB(8) MIOB(1) MIOB(0)	0111 : samsung GDDR3 256Mbit 0101 : infineon GDDR3 256Mbit 0011 : samsung GDDR3 512Mbit 0001 : infineon GDDR3 512Mbit
CRYSTAL(1:0)	MIOB(2) MIOB(6)	01 : 14.318 MHz 10 : 27 MHz (Default) 11 : Unknown 00 : 13.5 MHz
TV_MODE(1:0)	MIOAD(7) MIOAD(10)	00 : SECAM 01 : NTSC (Default) 10 : PAL 11 : CRT
PCI_DEVID(3:0) [11,3,5,4]	MIOB(11) MIOB(3) MIOB(5) MIOB(4)	72M : 0X01D8 72M-V : 0X01D7 73M : 0X0398
ROM_TYPE(1:0)	MIOB(10) MIOBVSYNC	No ROM (NC)
USER STRAP	MIOAD(2:5)	EDID

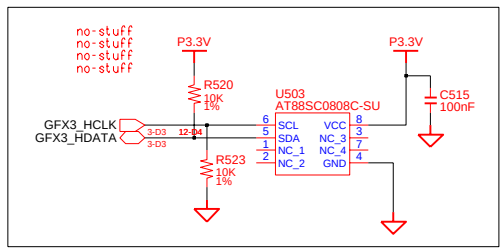
A-channel

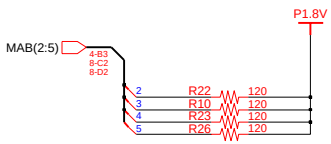


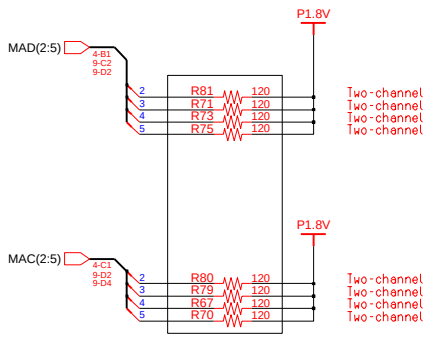
This page is for "2channel-model".

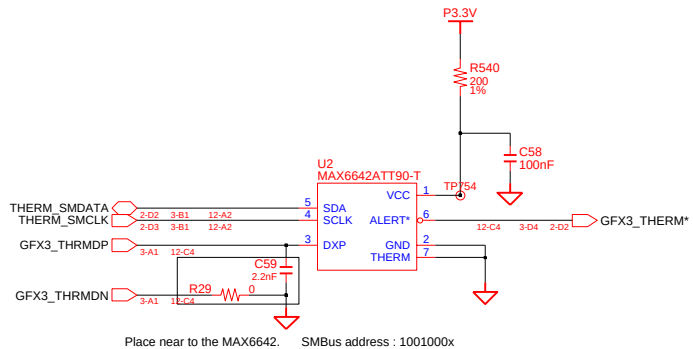
C-channel





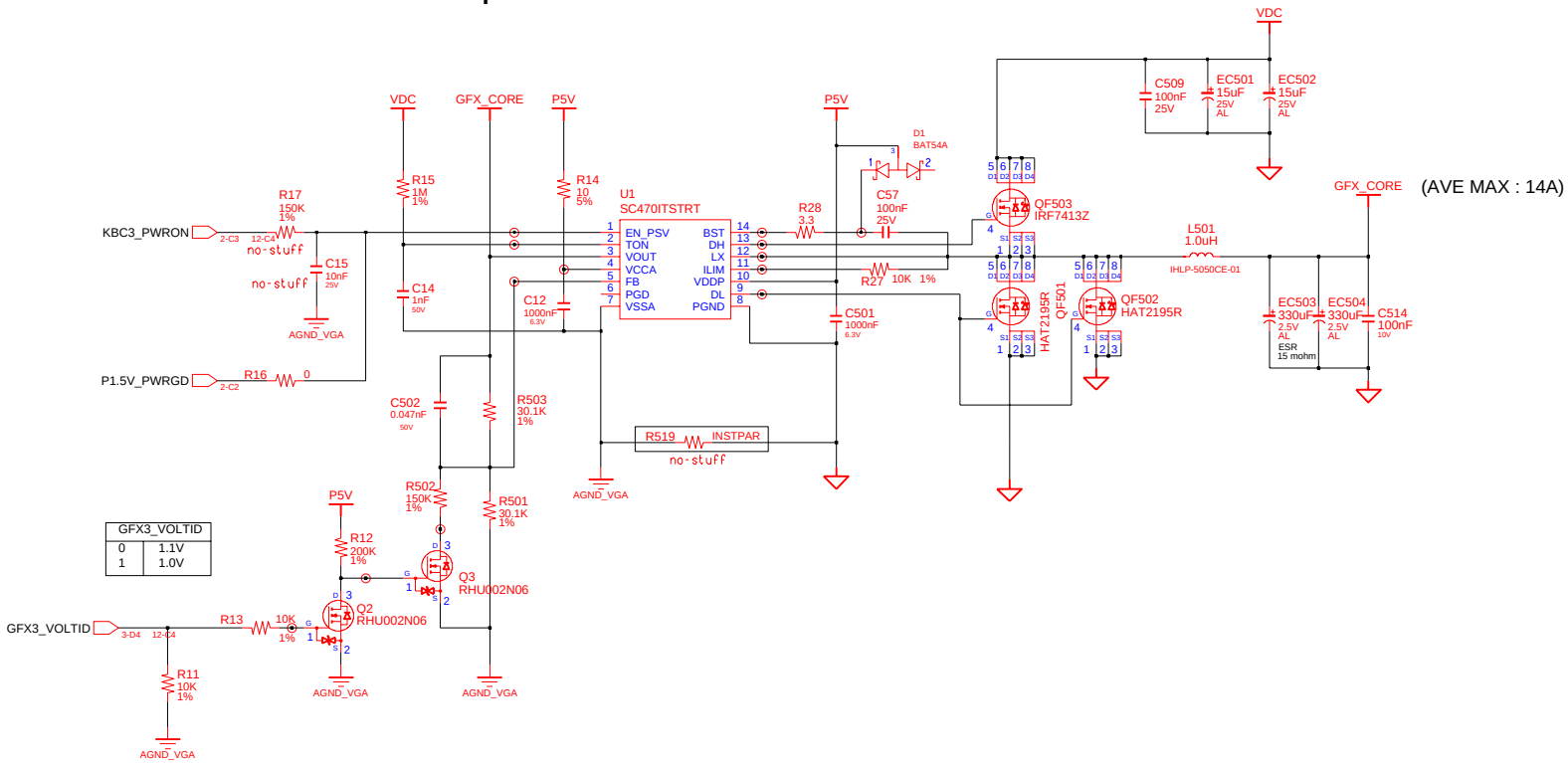






Place near to the MAX6642. SMBus address : 1001000x

Graphic Core Power



GFX3_27M
GFX3_27M_SS
GFX3_BLON
GFX3_BLUE
GFX3_BRIT
GFX3_C
GFX3_COMP
GFX3_DDCCLK
GFX3_DDCDATA
GFX3_DVICLK
GFX3_DVIDATA

GFX3_GREEN
GFX3_HCLK
GFX3_HDATA
GFX3_HSYNC
GFX3_HTPLG
GFX3_LCDVDDON
GFX3_RED
GFX3_THERM*
GFX3_THRMDN
GFX3_THRMDP

GFX3_VOLTID
GFX3_VSYNC
GFX3_Y
HDDET*
KBC3_PWRON

DRAM_RST#
DRAM_RST*
EDID_CLK
EDID_DATA

P5V
P5V
P5V
P5V
TMDS_PLLVDD
TMDS_PLLVDD

VDC
VDC
VDC
VDC
VDC

0.7VDDQA
0.7VDDQA

0.7VDDQC
0.7VDDQC

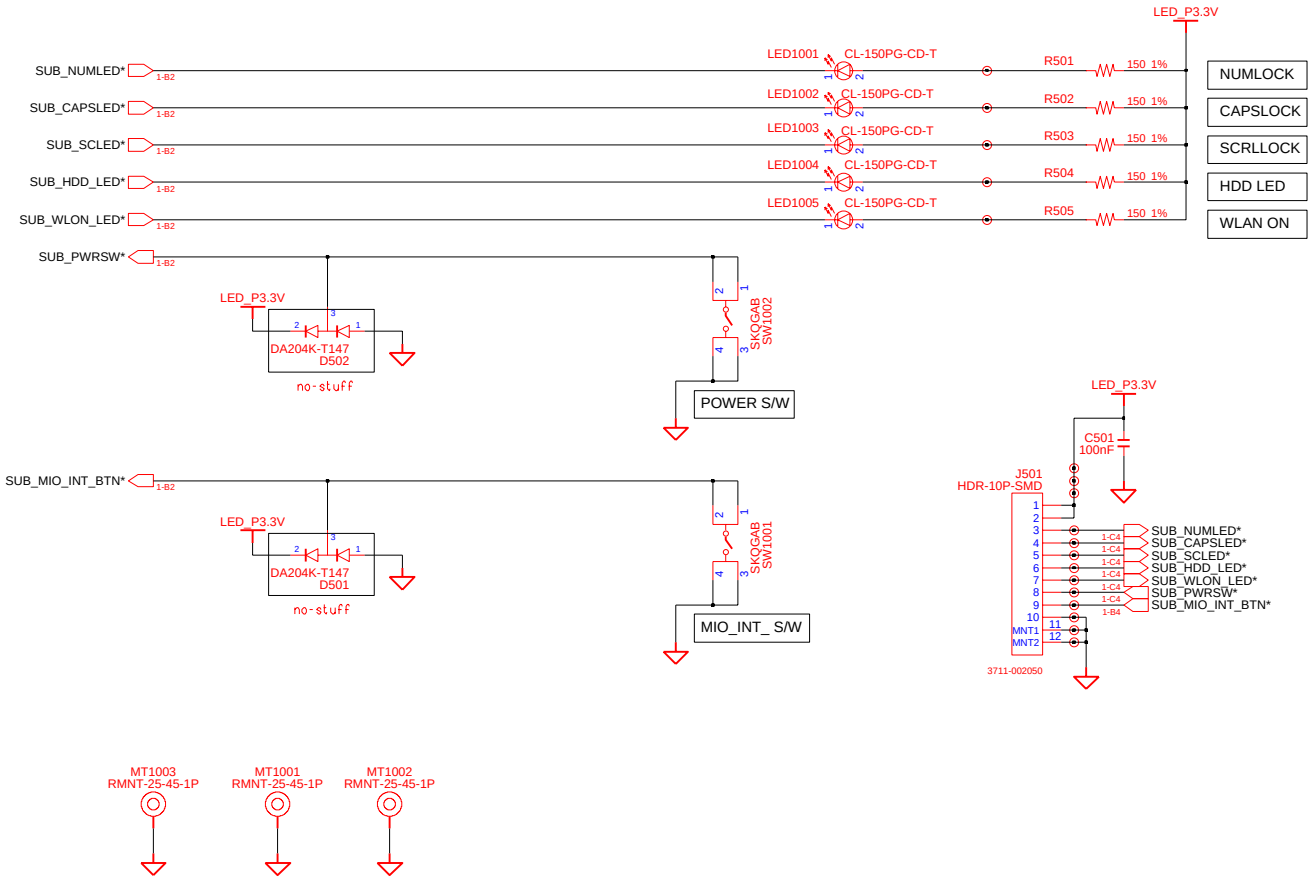
AGND_VGA
AGND_VGA

PEG3_MIOB(0)
PEG3_MIOB(1)
PEG3_MIOB(11)
PEG3_MIOB(3)
PEG3_MIOB(4)
PEG3_MIOB(5)
PEG3_MIOB(8)
PEG3_MIOB(9)
PLT3_RST#
PWRON*

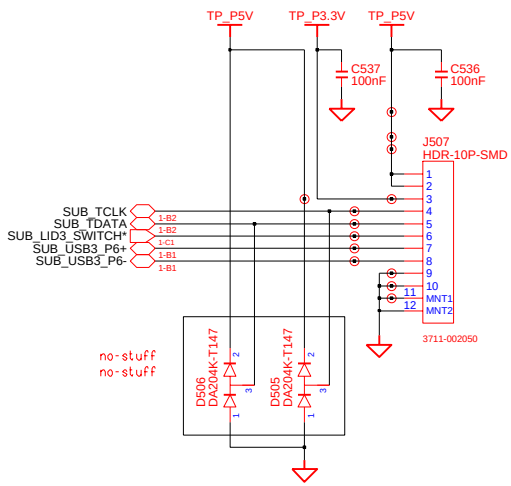
GFX_CORE
GFX_CORE
GFX_CORE
GFX_CORE
GFX_CORE
GROUND
GROUND
GROUND
GROUND
GROUND
P1.2V
P1.2V
P1.2V
P1.2V
P1.2V
P1.8V
P1.8V
P1.8V
P1.8V
P1.8V
P1.8V
P2.5V
P2.5V
P2.5V
P2.5V
P2.5V
P2.5V
P3.3V
P3.3V
P3.3V
P3.3V
P3.3V
P5V

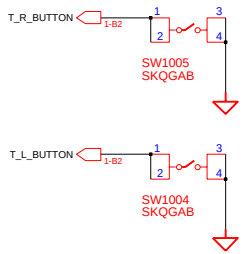
THERM_SMCLK
THERM_SMDATA

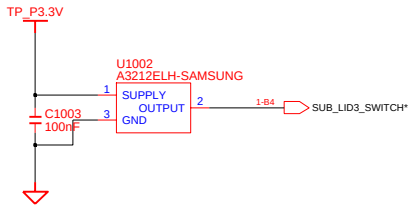
On-Top Board



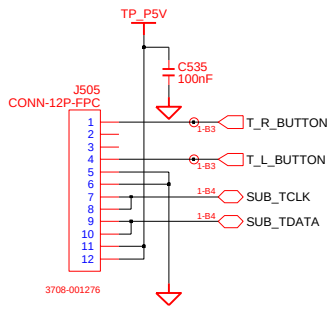
TOUCHPAD BOARD







To Touchpad



To Finger Printer