HAINAN C

CPU : Intel Yonah/Merom
Chip Set : Intel Calistoga & ICH7-M
Remarks : Mobility Platform

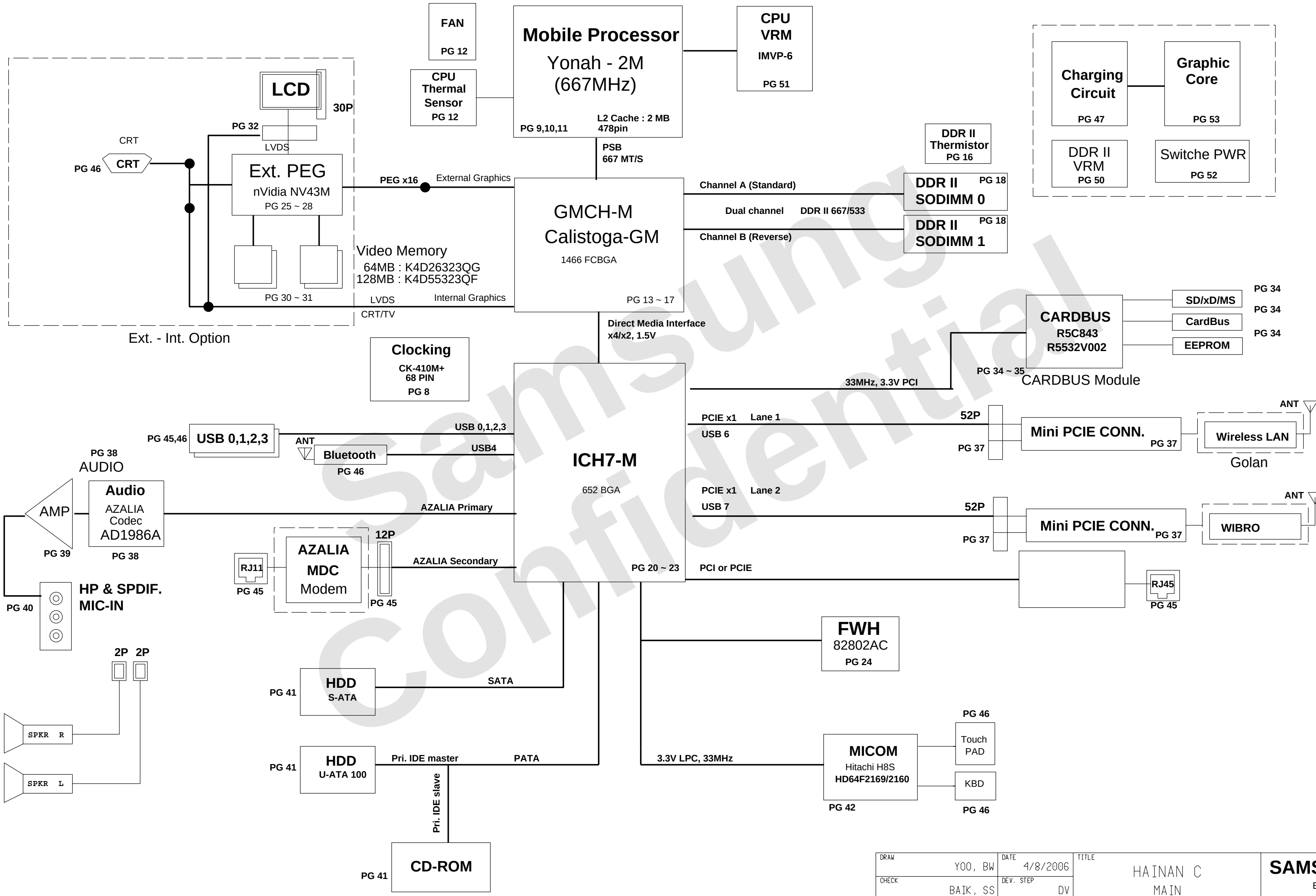
Model Name : HAINAN C
PBA Name : MAIN
PCB Code : BA41-00694A GCE
BA41-00695A TPT
Dev. Step : MP
Revision : 1.0
T.R. Date : 2006.07.17

DRAW	CHECK	APPROVAL
BW YOO	SS BAIK	KK BIN

■ ***Owner : SEC Mobile R & D*** ***Signature :*** ***X***

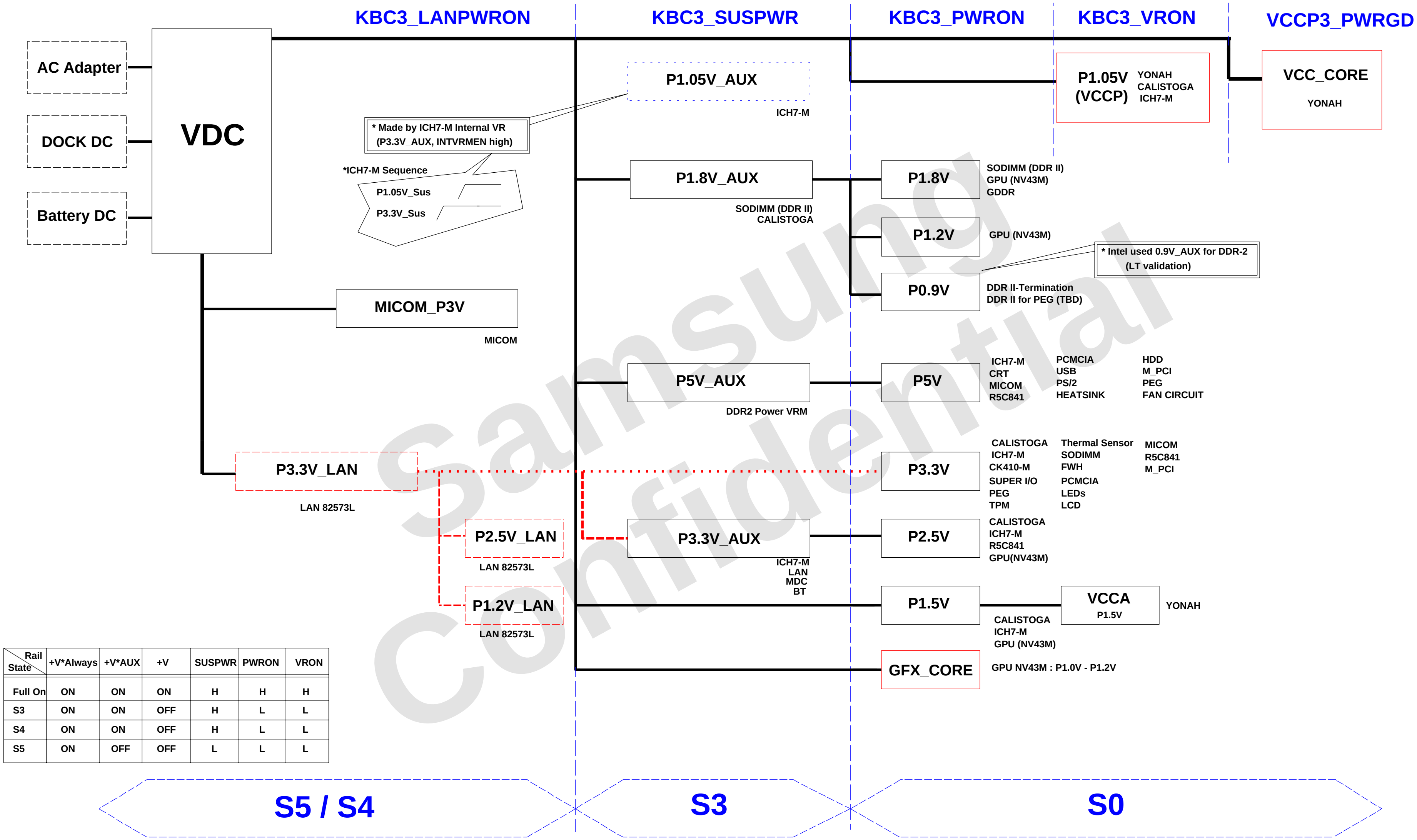
Table of Contents

DRAW	YOO, BW	DATE	4/8/2006	TITLE HAINAN C COVER	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV		
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:00:28 PM	PAGE 1 OF 50	



DRAW	YOO, BW	DATE	4/8/2006	TITLE	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	HAINAN C MAIN OPERATION BLOCK DIAGRAM	
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:00:42 PM		PAGE 2 OF 50

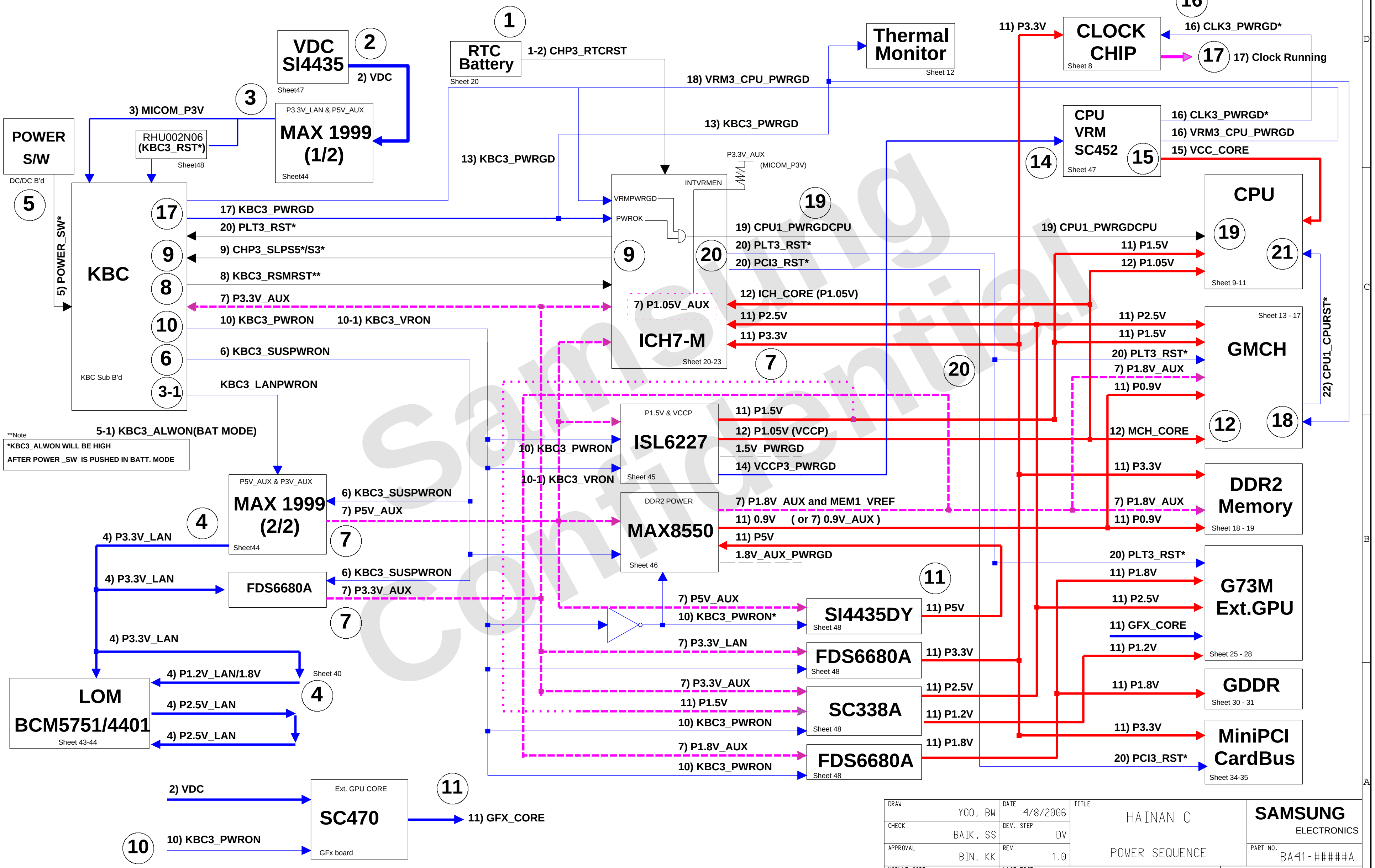
Power Diagram



Rail / State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

DRAW	YOO, BW	DATE	4/8/2006	TITLE	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	HAINAN C MAIN POWER DIAGRAM	
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:00:55 PM		PAGE 3 OF 50

POWER SEQUENCE Rev. 0.8



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CHECK	BAIK, SS	DEV. STEP	DV		POWER SEQUENCE
APPROVAL	BIN, KK	REV	1.0	PART NO.	BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:01:27 PM	PAGE	4 OF 50

SAMSUNG ELECTRONICS

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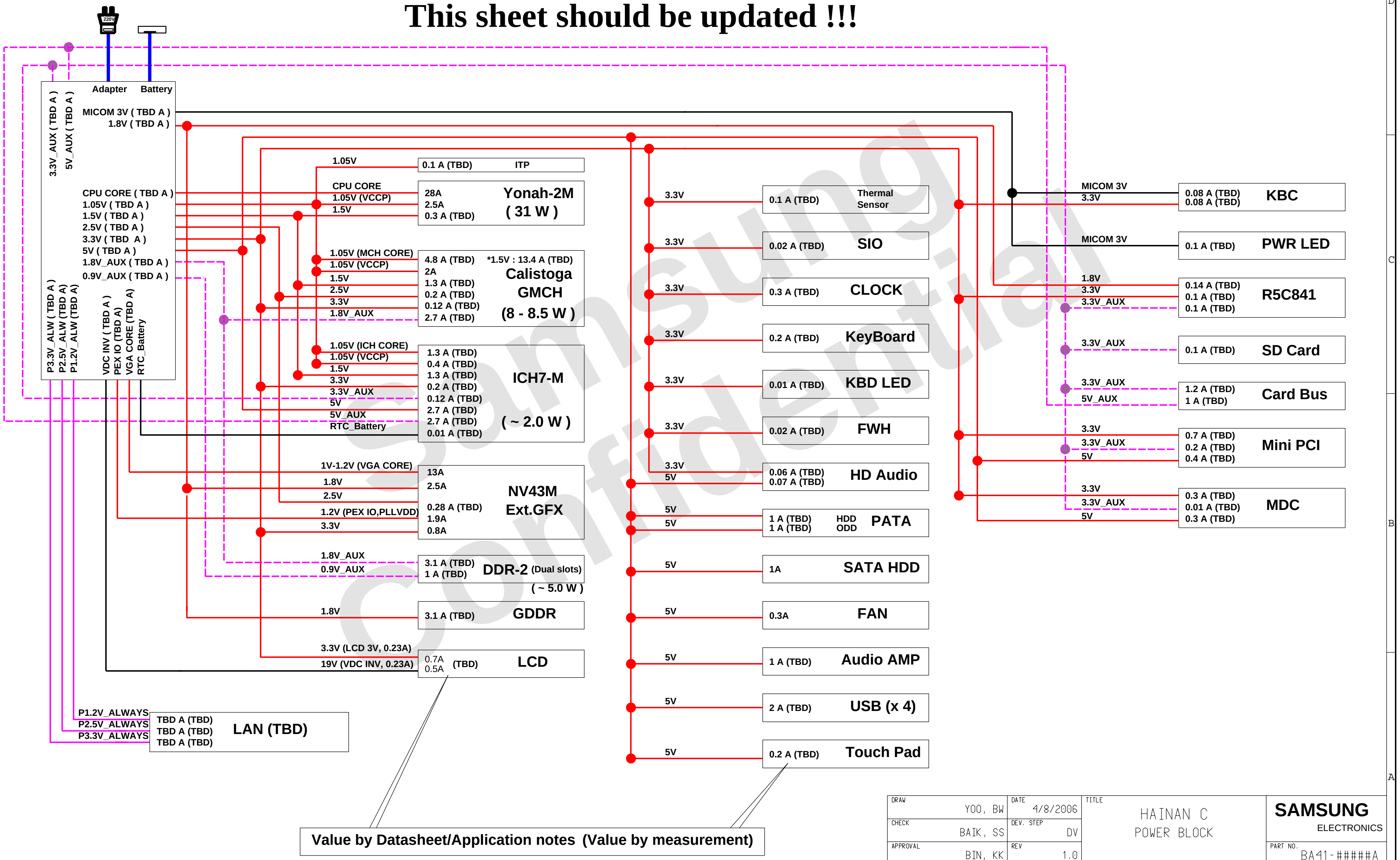
POWER RAILS ANALYSIS Rev. 0.8

(solid line)	S0 - S5
(dashed line)	S0 - S3
(thin line)	OFF IN S3 - S5

This sheet should be updated !!!



DRAW YOO, BW	DATE 4/8/2006	TITLE HAINAN C POWER BLOCK		SAMSUNG ELECTRONICS	
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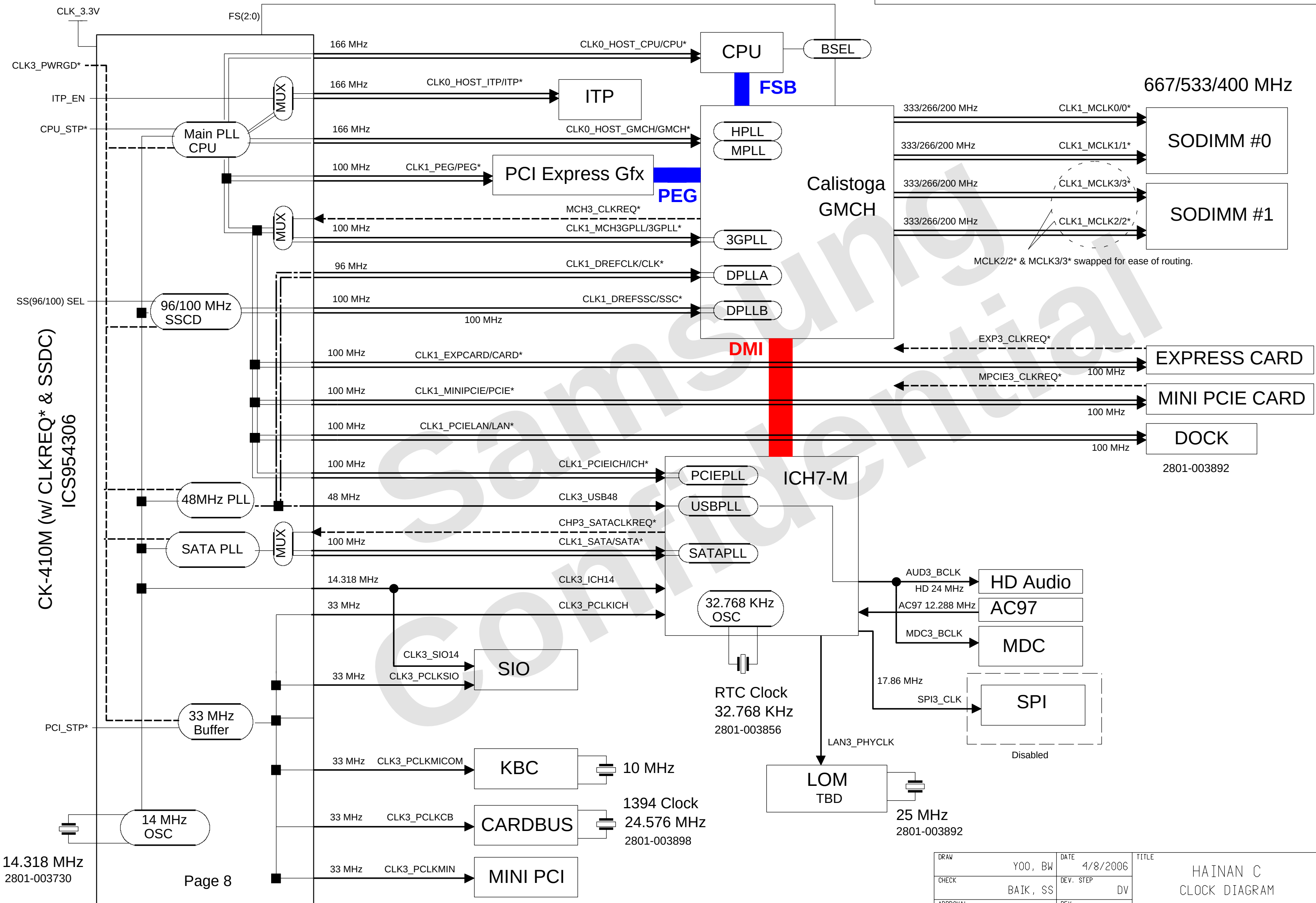
APPROVAL BIN, KK	REV 1.0			PART NO. BA41-#####A	
MODULE CODE undefined	LAST EDIT April, 13, 2006 5:01:42 PM			PAGE 5	OF 50

CLOCK DISTRIBUTION Rev. 0.7



DRAW	YOO, BW	DATE	4/8/2006	TITLE	HAINAN C CLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	1.0			PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:05:19 PM			PAGE 6 OF 50

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	E,F,G
LAN	AD21	1	G
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308~1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P3.3V_DTV	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_ALWS	3.3V power rail (Always On)
P2.5V_ALWS	2.5V power rail (Always On)
P1.2V_ALWS	1.2V power rail (Always On)

I^2C / SMB Address

Devices	Address	Hex	Bus
ICH7	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A4h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0,1	SYSTEM PORT A, B
2	RESERVED
3	RESERVED
4	BLUETOOTH
5	RESERVED
6	MINI PCIE EXPRESS CARD
7	RESERVED

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other criticial subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.

CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH7-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	Intel LAN

CPU Core Voltage Table IMVP-6

Active Mode

VID(6:0)							Voltage
0	0	0	0	0	0	0	1.5000 V
0	0	0	0	0	0	1	1.4875 V
0	0	0	0	0	1	0	1.4750 V
0	0	0	0	0	1	1	1.4625 V
0	0	0	0	1	0	0	1.4500 V
0	0	0	0	1	0	1	1.4375 V
0	0	0	0	1	1	0	1.4250 V
0	0	0	0	1	1	1	1.4125 V
0	0	0	1	0	0	0	1.4000 V
0	0	0	1	0	0	1	1.3875 V
0	0	0	1	0	1	0	1.3750 V
0	0	0	1	0	1	1	1.3625 V
0	0	0	1	1	0	0	1.3500 V
0	0	0	1	1	0	1	1.3375 V
0	0	0	1	1	1	0	1.3250 V
0	0	0	1	1	1	1	1.3125 V
0	0	1	0	0	0	0	1.3000 V
0	0	1	0	0	0	1	1.2875 V
0	0	1	0	0	1	0	1.2750 V
0	0	1	0	0	1	1	1.2625 V
0	0	1	0	1	0	0	1.2500 V
0	0	1	0	1	0	1	1.2375 V
0	0	1	0	1	1	0	1.2250 V
0	0	1	0	1	1	1	1.2125 V
0	0	1	1	0	0	0	1.2000 V
0	0	1	1	0	0	1	1.1875 V
0	0	1	1	0	1	0	1.1750 V
0	0	1	1	0	1	1	1.1625 V
0	0	1	1	1	0	0	1.1500 V
0	0	1	1	1	0	1	1.1375 V
0	0	1	1	1	1	0	1.1250 V
0	0	1	1	1	1	1	1.1125 V
0	1	0	0	0	0	0	1.1000 V
0	1	0	0	0	0	1	1.0875 V
0	1	0	0	0	1	0	1.0750 V
0	1	0	0	0	1	1	1.0625 V
0	1	0	0	1	0	0	1.0500 V
0	1	0	0	1	0	1	1.0375 V
0	1	0	0	1	1	0	1.0250 V
0	1	0	0	1	1	1	1.0125 V

Active
DPRSLPVR 0
DPRSTP* 1
PSI2* 0 or 1

Active/Deeper Sleep Dual Mode Region

VID(6:0)							Voltage
0	1	0	1	0	0	0	1.0000 V
0	1	0	1	0	0	1	0.9875 V
0	1	0	1	0	1	0	0.9750 V
0	1	0	1	0	1	1	0.9625 V
0	1	0	1	1	0	0	0.9500 V
0	1	0	1	1	0	1	0.9375 V
0	1	0	1	1	1	0	0.9250 V
0	1	0	1	1	1	1	0.9125 V
0	1	1	0	0	0	0	0.9000 V
0	1	1	0	0	0	1	0.8875 V
0	1	1	0	0	1	0	0.8750 V
0	1	1	0	0	1	1	0.8625 V
0	1	1	0	1	0	0	0.8500 V
0	1	1	0	1	0	1	0.8375 V
0	1	1	0	1	1	0	0.8250 V
0	1	1	0	1	1	1	0.8125 V
0	1	1	1	0	0	0	0.8000 V
0	1	1	1	0	0	1	0.7875 V
0	1	1	1	0	1	0	0.7750 V
0	1	1	1	0	1	1	0.7625 V
0	1	1	1	1	0	0	0.7500 V
0	1	1	1	1	0	1	0.7375 V
0	1	1	1	1	1	0	0.7250 V
0	1	1	1	1	1	1	0.7125 V
1	0	0	0	0	0	0	0.7000 V
1	0	0	0	0	0	1	0.6875 V
1	0	0	0	0	1	0	0.6750 V
1	0	0	0	0	1	1	0.6625 V
1	0	0	0	1	0	0	0.6500 V
1	0	0	0	1	0	1	0.6375 V
1	0	0	0	1	1	0	0.6250 V
1	0	0	0	1	1	1	0.6125 V
1	0	0	1	0	0	0	0.6000 V
1	0	0	1	0	0	1	0.5875 V
1	0	0	1	0	1	0	0.5750 V
1	0	0	1	0	1	1	0.5625 V
1	0	0	1	1	0	0	0.5500 V
1	0	0	1	1	0	1	0.5375 V
1	0	0	1	1	1	0	0.5250 V
1	0	0	1	1	1	1	0.5125 V
1	0	1	0	0	0	0	0.5000 V

Deeper Slp
DPRSLPVR 1
DPRSTP* 0
PSI2* 0 or 1

Deeper Sleep/Extended Deeper Sleep Dual Mode Region

VID(6:0)							Voltage
1	0	1	0	0	0	1	0.4875 V
1	0	1	0	0	1	0	0.4750 V
1	0	1	0	0	1	1	0.4625 V
1	0	1	0	1	0	0	0.4500 V
1	0	1	0	1	0	1	0.4375 V
1	0	1	0	1	1	0	0.4250 V
1	0	1	0	1	1	1	0.4125 V
1	0	1	1	0	0	0	0.4000 V
1	0	1	1	0	0	1	0.3875 V
1	0	1	1	0	1	0	0.3750 V
1	0	1	1	0	1	1	0.3625 V
1	0	1	1	1	0	0	0.3500 V
1	0	1	1	1	0	1	0.3375 V
1	0	1	1	1	1	0	0.3250 V
1	0	1	1	1	1	1	0.3125 V
1	1	0	0	0	0	0	0.3000 V
1	1	0	0	0	0	1	0.2875 V
1	1	0	0	0	1	0	0.2750 V
1	1	0	0	0	1	1	0.2625 V
1	1	0	0	1	0	0	0.2500 V
1	1	0	0	1	0	1	0.2375 V
1	1	0	0	1	1	0	0.2250 V
1	1	0	0	1	1	1	0.2125 V
1	1	0	1	0	0	0	0.2000 V
1	1	0	1	0	0	1	0.1875 V
1	1	0	1	0	1	0	0.1750 V
1	1	0	1	0	1	1	0.1625 V
1	1	0	1	1	0	0	0.1500 V
1	1	0	1	1	0	1	0.1375 V
1	1	0	1	1	1	0	0.1250 V
1	1	0	1	1	1	1	0.1125 V
1	1	1	0	0	0	0	0.1000 V
1	1	1	0	0	0	1	0.0875 V
1	1	1	0	0	1	0	0.0750 V
1	1	1	0	0	1	1	0.0625 V
1	1	1	0	1	0	0	0.0500 V
1	1	1	0	1	0	1	0.0375 V
1	1	1	0	1	1	0	0.0250 V
1	1	1	0	1	1	1	0.0125 V
1	1	1	1	0	0	0	0.0000 V
1	1	1	1	0	0	1	0.0000 V
1	1	1	1	0	1	0	0.0000 V
1	1	1	1	0	1	1	0.0000 V
1	1	1	1	1	0	0	0.0000 V
1	1	1	1	1	0	1	0.0000 V
1	1	1	1	1	1	0	0.0000 V
1	1	1	1	1	1	1	0.0000 V

*"1111111" : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW	YOO, BW	DATE	4/8/2006	TITLE HAINAN C MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV		
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:06:18 PM		PAGE 7 OF 50

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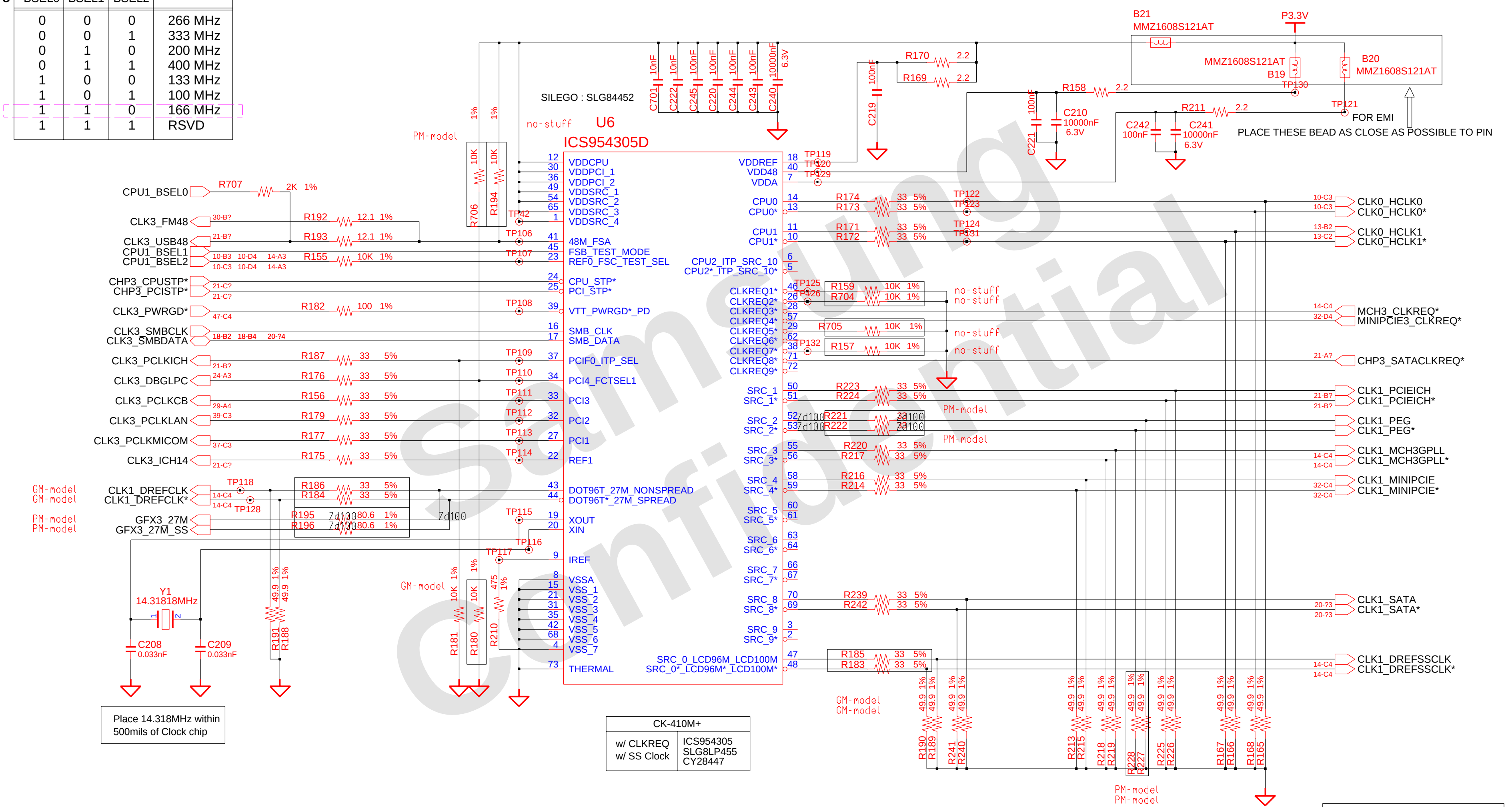
CPU	FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD

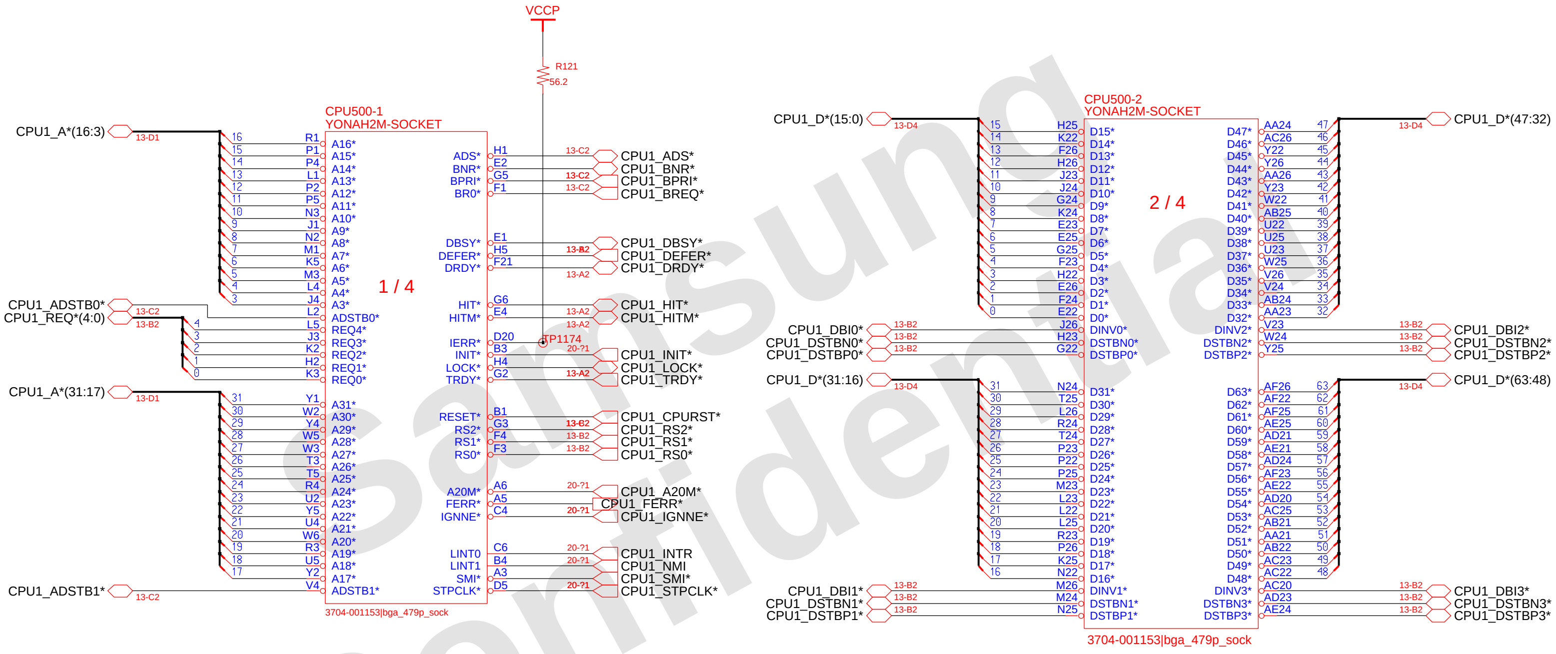
PCI4_FCTSEL1(PIN34)	PIN 43, 44	PIN 47, 48
0	DOT96	LCD96/100
1	27MHZ	SRC0



Place 14.318MHz within 500mils of Clock chip

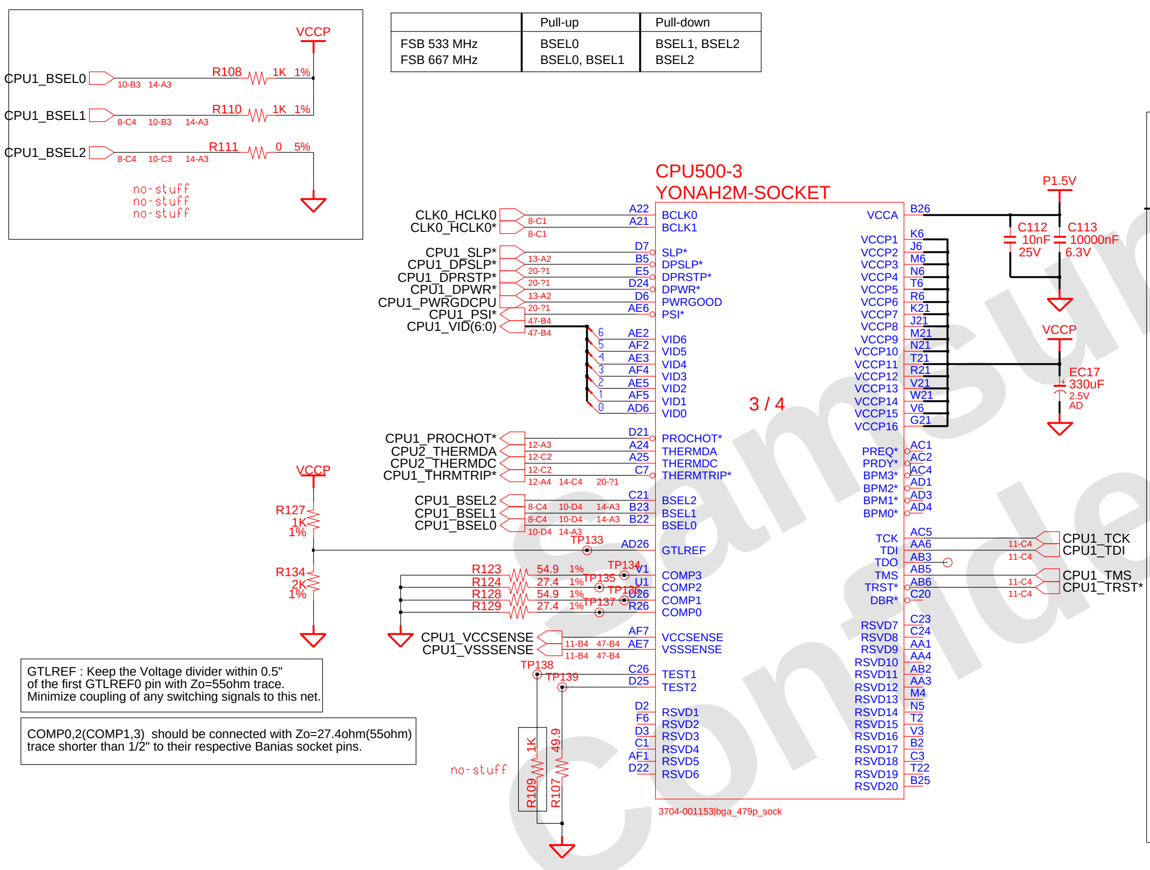
CK-410M+	
w/ CLKREQ w/ SS Clock	ICS954305 SLG8LP455 CY28447

DRAW: YOO, BW	DATE: 4/8/2006	TITLE: HAINAN C MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
CHECK: BAIK, SS	DEV. STEP: DV		
APPROVAL: BIN, KK	REV: 1.0		PART NO. BA41-#####A
MODULE CODE: undefined	LAST EDIT: April, 13, 2006 5:07:53 PM		PAGE 8 OF 50



DRAW	YOO, BW	DATE	4/8/2006	TITLE HAINAN C MAIN YONAH CPU (1/3)	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV		
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:08:17 PM		PAGE 9 OF 50

	Pull-up	Pull-down
FSB 533 MHz	BSEL0	BSEL1, BSEL2
FSB 667 MHz	BSEL0, BSEL1	BSEL2



GTLREF : Keep the Voltage divider within 0.5"
of the first GTLREF0 pin with Zo=55ohm trace.
Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm)
trace shorter than 1/2" to their respective Banias socket pins.

CPU Core Voltage Table IMVP-6

Active Mode

VID(6:0)							Voltage
0	0	0	0	0	0	0	1.5000 V
0	0	0	0	0	0	1	1.4875 V
0	0	0	0	0	1	0	1.4750 V
0	0	0	0	0	1	1	1.4625 V
0	0	0	0	1	0	0	1.4500 V
0	0	0	0	1	0	1	1.4375 V
0	0	0	0	1	1	0	1.4250 V
0	0	0	0	1	1	1	1.4125 V
0	0	0	1	0	0	0	1.4000 V
0	0	0	1	0	0	1	1.3875 V
0	0	0	1	0	1	0	1.3750 V
0	0	0	1	0	1	1	1.3625 V
0	0	0	1	1	0	0	1.3500 V
0	0	0	1	1	0	1	1.3375 V
0	0	0	1	1	1	0	1.3250 V
0	0	0	1	1	1	1	1.3125 V
0	0	1	0	0	0	0	1.3000 V
0	0	1	0	0	0	1	1.2875 V
0	0	1	0	0	1	0	1.2750 V
0	0	1	0	0	1	1	1.2625 V
0	0	1	0	1	0	0	1.2500 V
0	0	1	0	1	0	1	1.2375 V
0	0	1	0	1	1	0	1.2250 V
0	0	1	0	1	1	1	1.2125 V
0	0	1	1	0	0	0	1.2000 V
0	0	1	1	0	0	1	1.1875 V
0	0	1	1	0	1	0	1.1750 V
0	0	1	1	0	1	1	1.1625 V
0	0	1	1	1	0	0	1.1500 V
0	0	1	1	1	0	1	1.1375 V
0	0	1	1	1	1	0	1.1250 V
0	0	1	1	1	1	1	1.1125 V
0	1	0	0	0	0	0	1.1000 V
0	1	0	0	0	0	1	1.0875 V
0	1	0	0	0	1	0	1.0750 V
0	1	0	0	0	1	1	1.0625 V
0	1	0	0	1	0	0	1.0500 V
0	1	0	0	1	0	1	1.0375 V
0	1	0	0	1	1	0	1.0250 V
0	1	0	0	1	1	1	1.0125 V

Active

DPRSLPVR	0
DPRSTP*	1
PSI2*	0 or 1

Active/Deeper Sleep Dual Mode Region

VID(6:0)							Voltage
0	1	0	1	0	0	0	1.0000 V
0	1	0	1	0	0	1	0.9875 V
0	1	0	1	0	1	0	0.9750 V
0	1	0	1	0	1	1	0.9625 V
0	1	0	1	1	0	0	0.9500 V
0	1	0	1	1	0	1	0.9375 V
0	1	0	1	1	1	0	0.9250 V
0	1	0	1	1	1	1	0.9125 V
0	1	1	0	0	0	0	0.9000 V
0	1	1	0	0	0	1	0.8875 V
0	1	1	0	0	1	0	0.8750 V
0	1	1	0	0	1	1	0.8625 V
0	1	1	0	1	0	0	0.8500 V
0	1	1	0	1	0	1	0.8375 V
0	1	1	0	1	1	0	0.8250 V
0	1	1	0	1	1	1	0.8125 V
0	1	1	1	0	0	0	0.8000 V
0	1	1	1	0	0	1	0.7875 V
0	1	1	1	0	1	0	0.7750 V
0	1	1	1	0	1	1	0.7625 V
0	1	1	1	1	0	0	0.7500 V
0	1	1	1	1	0	1	0.7375 V
0	1	1	1	1	1	0	0.7250 V
0	1	1	1	1	1	1	0.7125 V
1	0	0	0	0	0	0	0.7000 V
1	0	0	0	0	0	1	0.6875 V
1	0	0	0	0	1	0	0.6750 V
1	0	0	0	0	1	1	0.6625 V
1	0	0	0	1	0	0	0.6500 V
1	0	0	0	1	0	1	0.6375 V
1	0	0	0	1	1	0	0.6250 V
1	0	0	0	1	1	1	0.6125 V
1	0	0	1	0	0	0	0.6000 V
1	0	0	1	0	0	1	0.5875 V
1	0	0	1	0	1	0	0.5750 V
1	0	0	1	0	1	1	0.5625 V
1	0	0	1	1	0	0	0.5500 V
1	0	0	1	1	0	1	0.5375 V
1	0	0	1	1	1	0	0.5250 V
1	0	0	1	1	1	1	0.5125 V
1	0	1	0	0	0	0	0.5000 V

Deeper Slp

DPRSLPVR	1
DPRSTP*	0
PSI2*	0 or 1

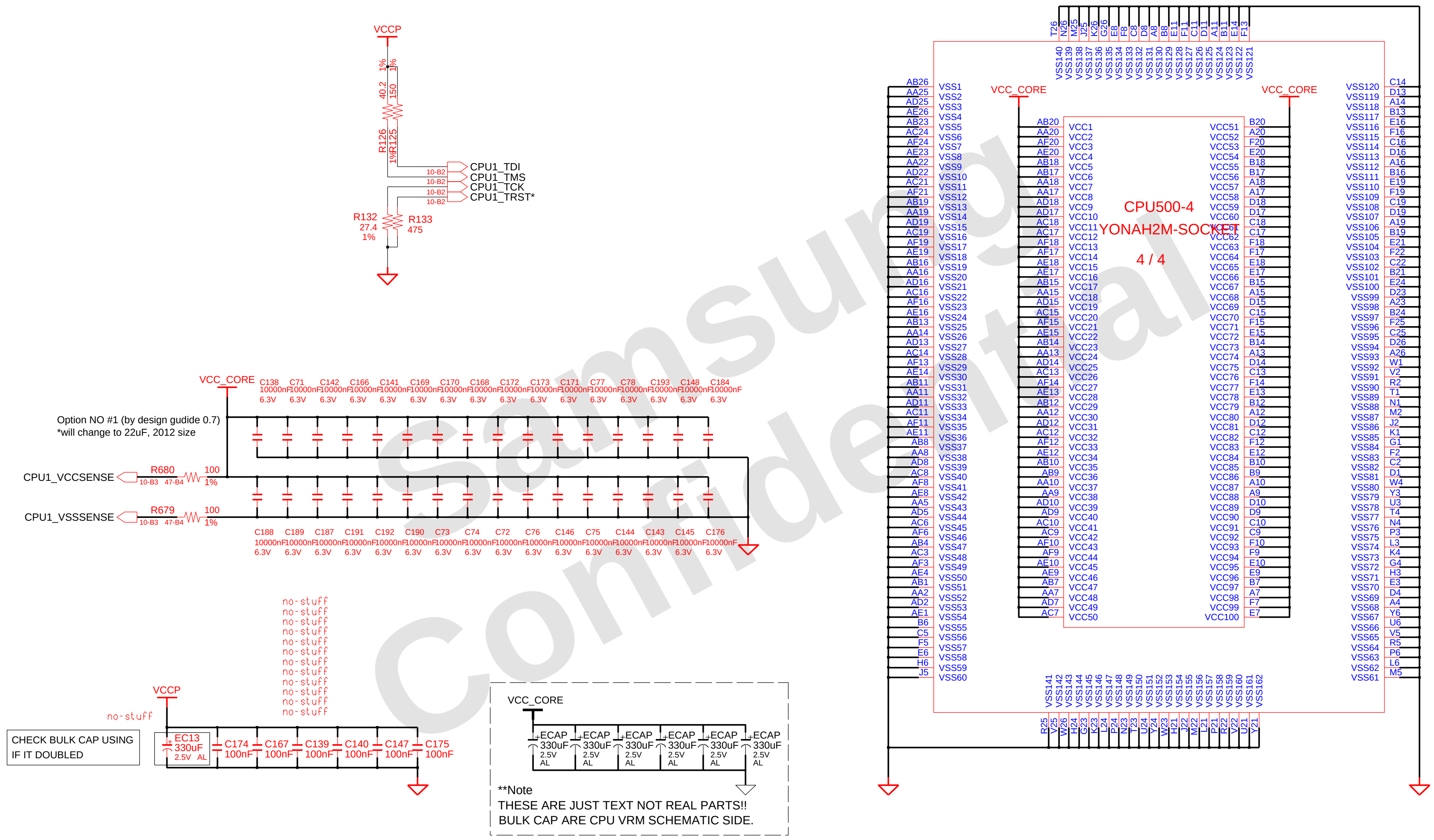
Deeper Sleep/Extended Deeper Sleep Dual Mode Region

VID(6:0)							Voltage
1	0	1	0	0	0	1	0.4875 V
1	0	1	0	0	1	0	0.4750 V
1	0	1	0	0	1	1	0.4625 V
1	0	1	0	1	0	0	0.4500 V
1	0	1	0	1	0	1	0.4375 V
1	0	1	0	1	1	0	0.4250 V
1	0	1	0	1	1	1	0.4125 V
1	0	1	1	0	0	0	0.4000 V
1	0	1	1	0	0	1	0.3875 V
1	0	1	1	0	1	0	0.3750 V
1	0	1	1	0	1	1	0.3625 V
1	0	1	1	1	0	0	0.3500 V
1	0	1	1	1	0	1	0.3375 V
1	0	1	1	1	1	0	0.3250 V
1	0	1	1	1	1	1	0.3125 V
1	1	0	0	0	0	0	0.3000 V
1	1	0	0	0	0	1	0.2875 V
1	1	0	0	0	1	0	0.2750 V
1	1	0	0	0	1	1	0.2625 V
1	1	0	0	1	0	0	0.2500 V
1	1	0	0	1	0	1	0.2375 V
1	1	0	0	1	1	0	0.2250 V
1	1	0	0	1	1	1	0.2125 V
1	1	0	1	0	0	0	0.2000 V
1	1	0	1	0	0	1	0.1875 V
1	1	0	1	0	1	0	0.1750 V
1	1	0	1	0	1	1	0.1625 V
1	1	0	1	1	0	0	0.1500 V
1	1	0	1	1	0	1	0.1375 V
1	1	0	1	1	1	0	0.1250 V
1	1	0	1	1	1	1	0.1125 V
1	1	1	0	0	0	0	0.1000 V
1	1	1	0	0	0	1	0.0875 V
1	1	1	0	0	1	0	0.0750 V
1	1	1	0	0	1	1	0.0625 V
1	1	1	0	1	0	0	0.0500 V
1	1	1	0	1	0	1	0.0375 V
1	1	1	0	1	1	0	0.0250 V
1	1	1	0	1	1	1	0.0125 V
1	1	1	1	0	0	0	0.0000 V
1	1	1	1	0	0	1	0.0000 V
1	1	1	1	0	1	0	0.0000 V
1	1	1	1	0	1	1	0.0000 V
1	1	1	1	1	0	0	0.0000 V
1	1	1	1	1	0	1	0.0000 V
1	1	1	1	1	1	0	0.0000 V
1	1	1	1	1	1	1	0.0000 V

*"1111111" : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW	YOO, BW	DATE	4/8/2006	TITLE	HAINAN C MAIN YONAH CPU(2/3)	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	1.0			PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:08:33 PM			PAGE 10 OF 50



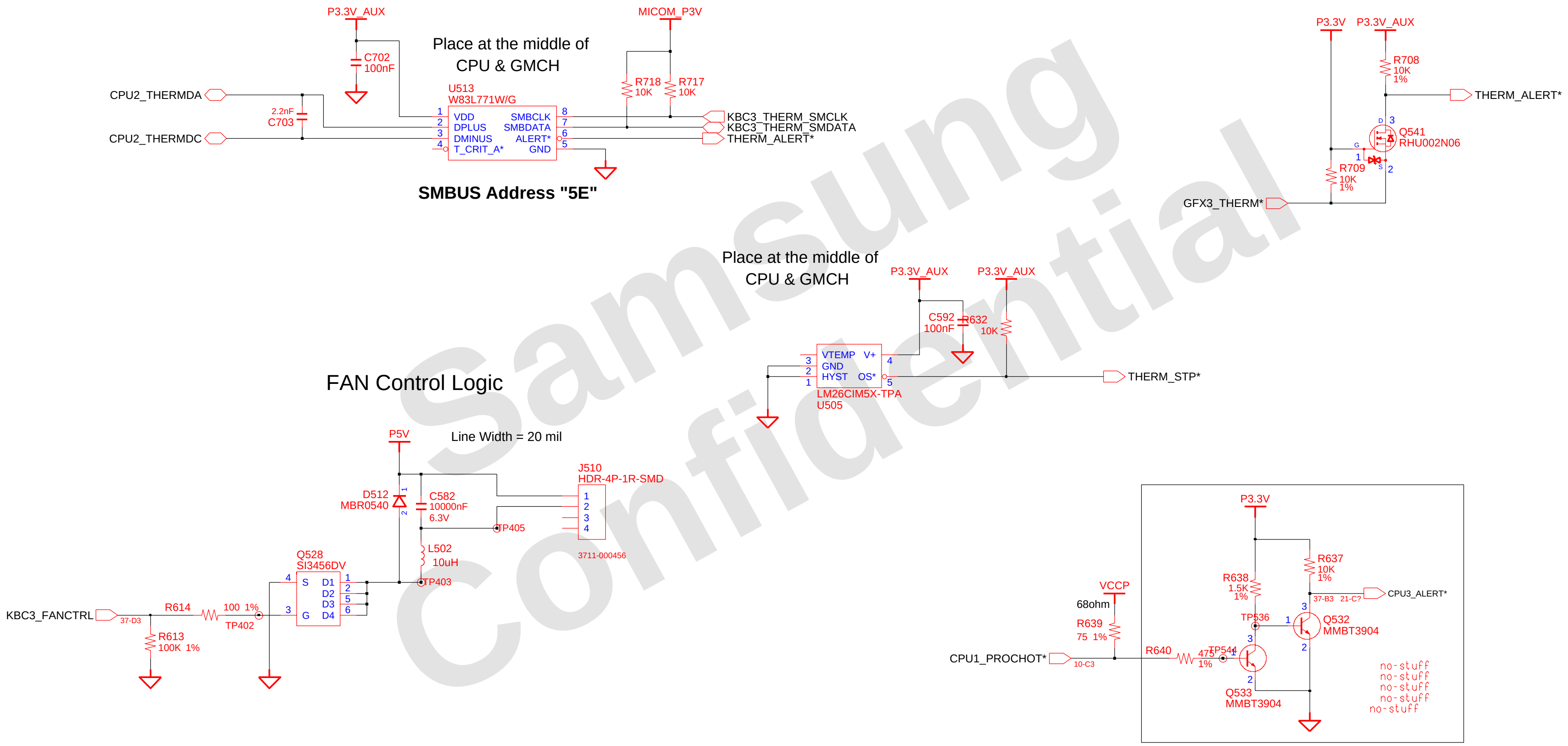
Samsung Confidential

DRAW: YOO, BW	DATE: 4/8/2006	TITLE: HAINAN C MAIN YONAH CPU(3/3)	SAMSUNG ELECTRONICS
CHECK: BAIK, SS	DEV. STEP: DV		
APPROVAL: BIN, KK	REV: 1.0		PART NO. BA41-#####A
MODULE CODE: undefined	LAST EDIT: April, 13, 2006 5:08:46 PM		PAGE 11 OF 50

Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

Thermal Monitor



Changed to Control Methode(EBL)

DRAW	YOO, BW	DATE	4/8/2006	TITLE HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN	
APPROVAL	BIN, KK	REV	1.0	THERMAL SENSOR/FAN Control	PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT		April, 13, 2006 5:09:14 PM	PAGE 12 OF 50

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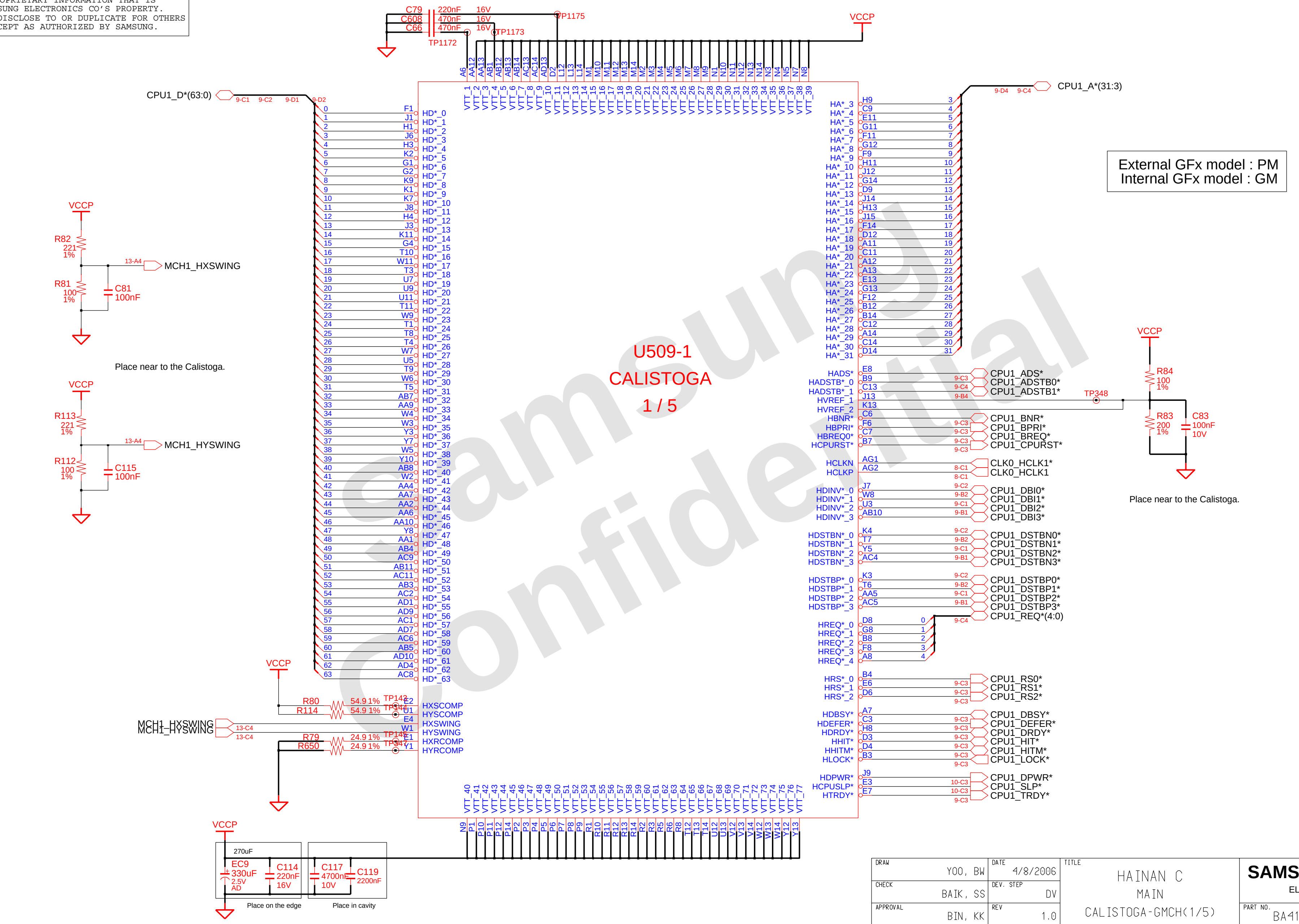

DRAW	YOO, BW	DATE	4/8/2006	TITLE	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	HAINAN C MAIN	
APPROVAL	BIN, KK	REV	1.0	CALISTOGA-GMCH(1/5)	PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:09:24 PM		PAGE 13 OF 50

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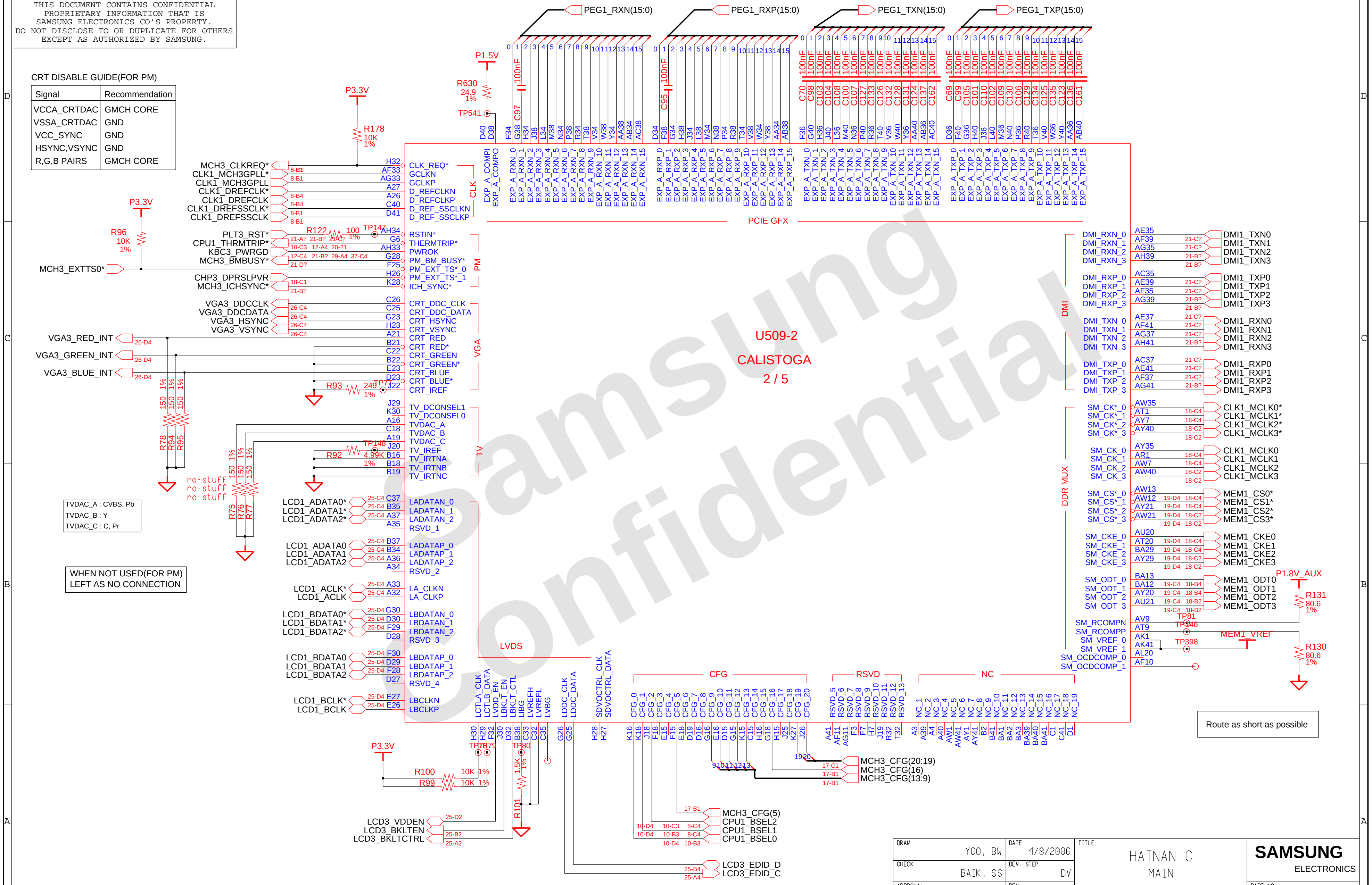
CRT DISABLE GUIDE(FOR PM)

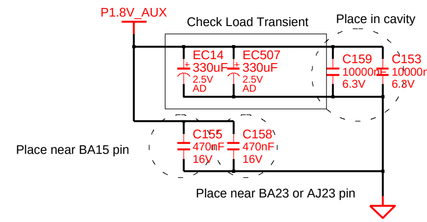
Signal	Recommendation
VCCA_CRTDAC	GMCH CORE
VSSA_CRTDAC	GND
VCC_SYNC	GND
HSYNC,VSYNC	GND
R,G,B PAIRS	GMCH CORE

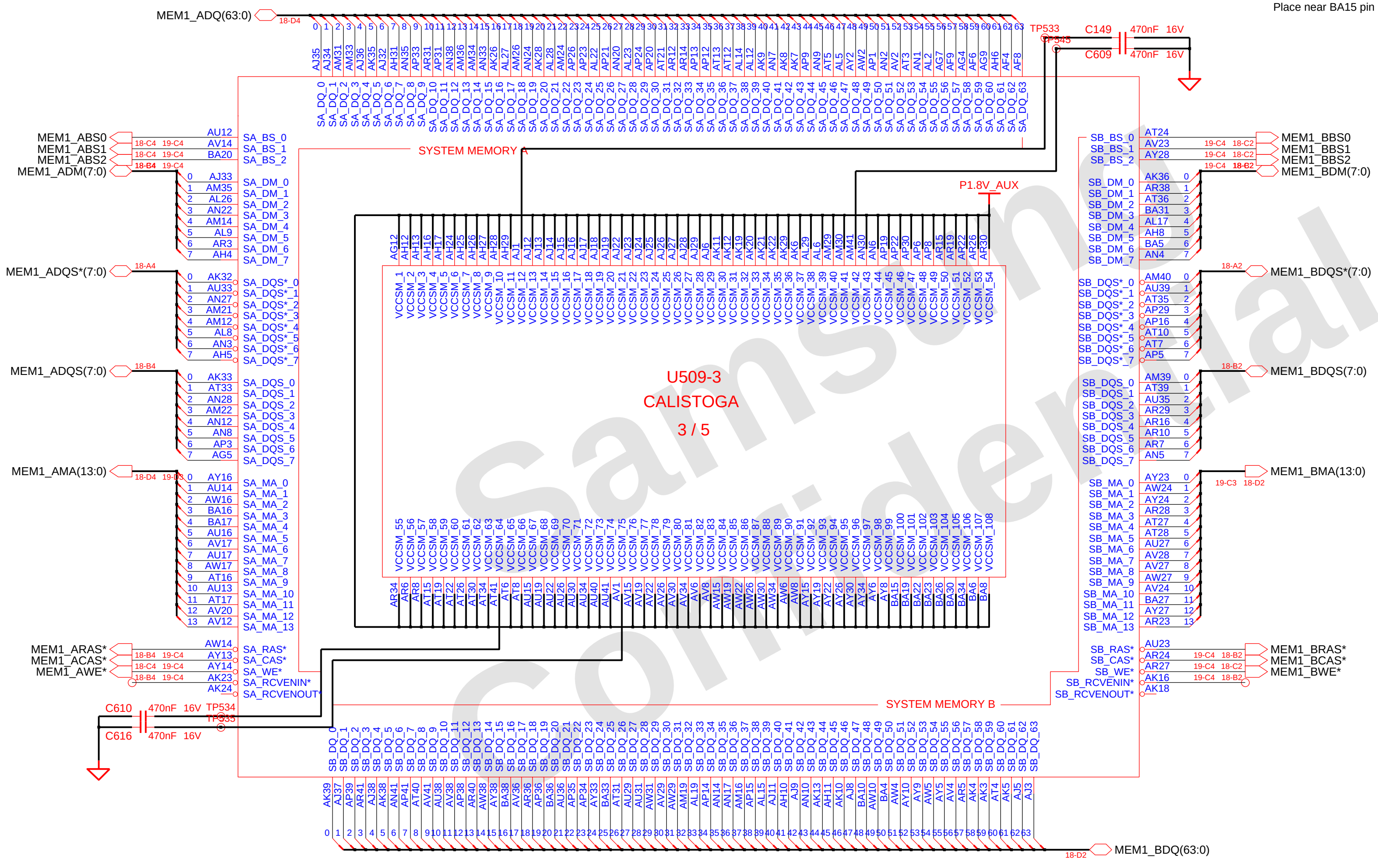


DRAW	YOO, BW	DATE 4/8/2006	TITLE HAINAN C MAIN CALISTOGA-GMCH(2/5)	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP DV		PART NO. BA41-#####A
APPROVAL	BIN, KK	REV 1.0		
MODULE CODE	undefined	LAST EDIT April, 13, 2006 5:09:34 PM		PAGE 14 OF 50

COM-22C-015(1996.6.5) REV. 3

d:/users/mobile20/mentor/hainan_c/hainan_c





Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)*	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)*	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOB_ALPHA*	
SDVOC_RED	EXP_TXP_4
SDVOB_ALPHA	
SDVOC_GREEN*	EXP_TXN_5
SDVOC_GREEN	EXP_TXP_5
SDVOC_BLUE*	EXP_TXN_6
SDVOC_BLUE	EXP_TXP_6
SDVOC_CLK*	EXP_TXN_7
SDVOC_CLK	EXP_TXP_7
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

DRAW YOO, BW	DATE 4/8/2006	TITLE HAINAN C MAIN CALISTOGA-GMCH(3/5)	SAMSUNG ELECTRONICS
CHECK BAIK, SS	DEV. STEP DV		PART NO. BA41-#####A
APPROVAL BIN, KK	REV 1.0		
MODULE CODE undefined	LAST EDIT April, 13, 2006 5:09:45 PM		PAGE 15 OF 50

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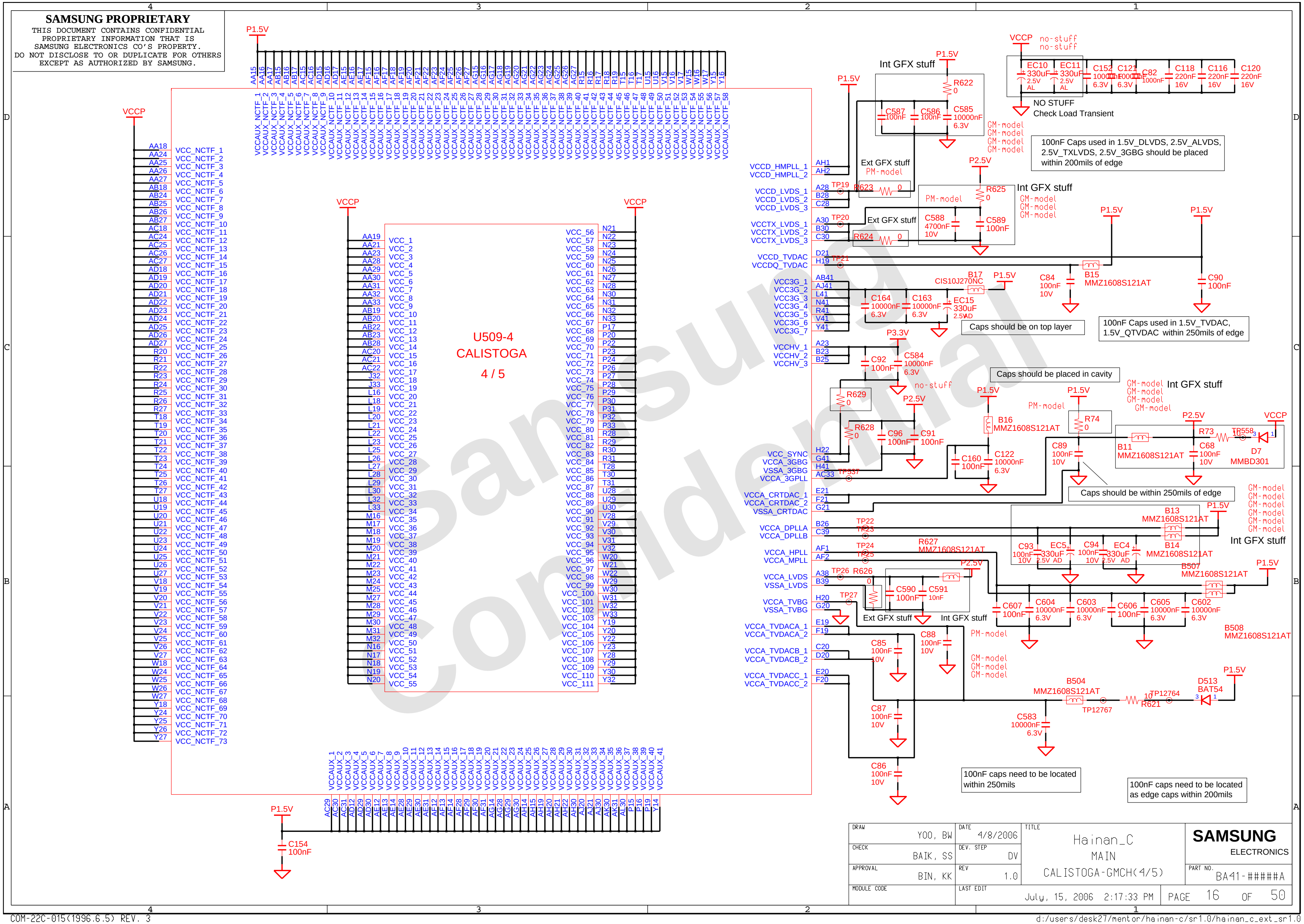
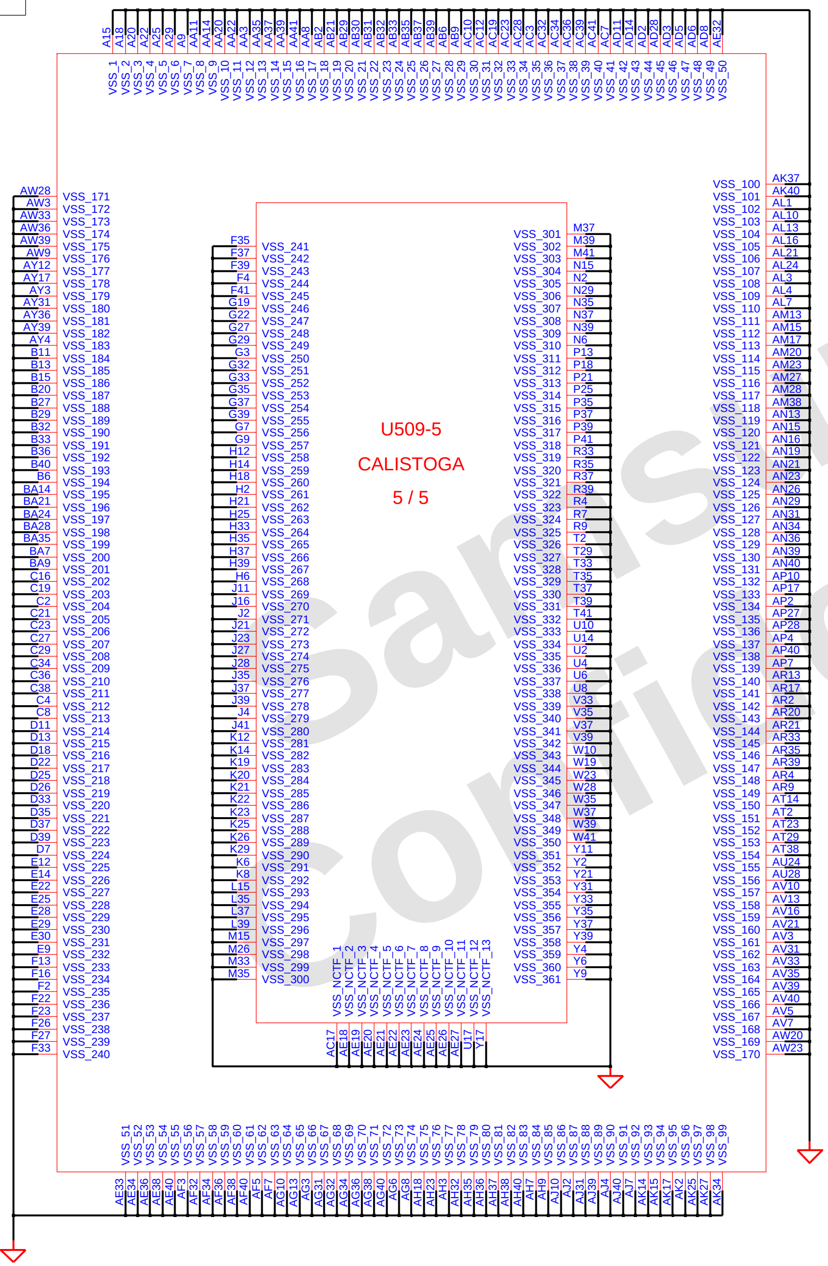
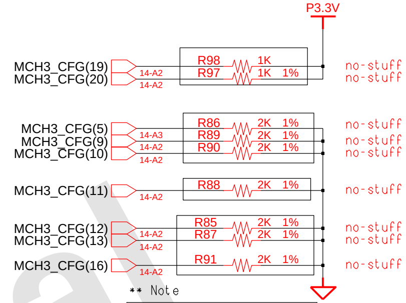


DRAW	YOO, BW	DATE	4/8/2006	TITLE	Hainan_C MAIN CALISTOGA-GMCH(4/5)	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV			PART NO. BA41-#####A
APPROVAL	BIN, KK	REV	1.0			
MODULE CODE		LAST EDIT	July, 15, 2006 2:17:33 PM		PAGE 16 OF 50	

COM-22C-015(1996.6.5) REV. 3

d:/users/desk27/mentor/hainan-c/sr1.0/hainan_c_ext_sr1.0





** Note

CFG(17:3)	Internal Pull-up
CFG(20:18)	Internal Pull-down

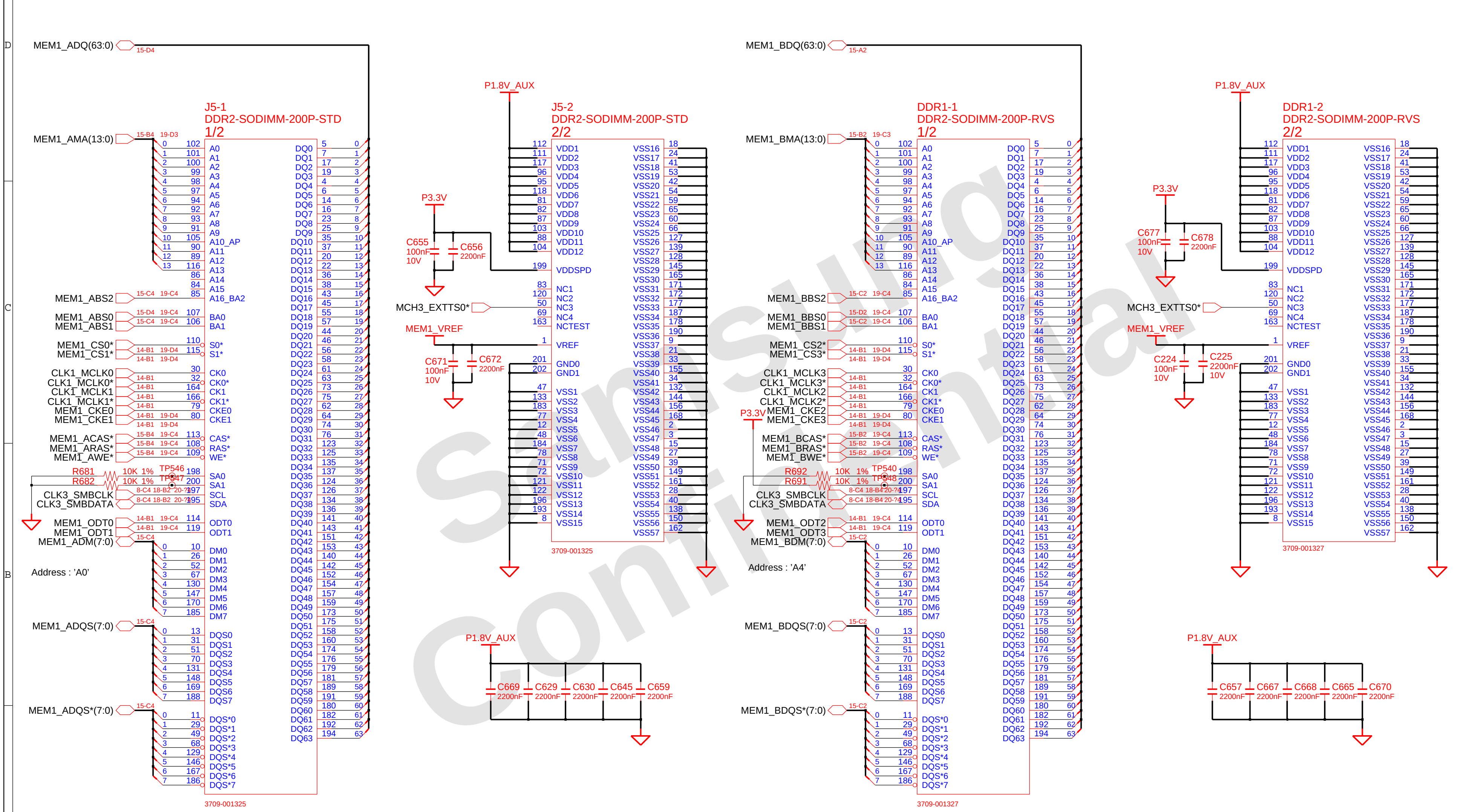
When CFG13:12 are pulled down to '00', certain clocks within Calistoga will become free-running clocks. This will lead to a rise in avg. power, but eliminates any possible clock-timing marginalities involbed in clockpower-up/power-down.
Intel strongly recommends leaving CFG13:12=NC (Internal PU to '11') to ensure low avg.

** Note *POCAFEB-10 Only (Remove in MP Model)*

Current Setting (def. : default Option)

CFG#	Low	High
CFG(5)	DMIx2	**DMIx4 (def.)**
CFG(6)	Reserved	**DDR-II (def.)**
CFG(7)	DT/Transportable	**Mobile CPU (def.)**
CFG(9)	PEG Reversal	**Normal**
CFG(16)	Dynamic ODT Disabled	**Dynamic ODT Enabled (def.)**
CFG(18)	**VCC 1.05V (def.)**	VCC 1.5V
CFG(19)	**DMI Lane Normal**	DMI Lane Reversal
CFG(20)	**SDVO or PCIE X1 Only(def.)**	SDVO and PCIE X1 Simultaneously

DRAW: YOO, BW	DATE: 4/8/2006	TITLE: HAINAN C MAIN CALISTOGA-GMCH(5/5)	**SAMSUNG** ELECTRONICS
CHECK: BAIK, SS	DEV. STEP: DV		
APPROVAL: BIN, KK	REV: 1.0		PART NO. BA41-#####A
MODULE CODE: undefined	LAST EDIT: April, 13, 2006 5:10:03 PM		PAGE 17 OF 50



DRAW YOO, BW	DATE 4/8/2006	TITLE HAINAN C MAIN DDR2 - SODIMM	SAMSUNG ELECTRONICS
CHECK BAIK, SS	DEV. STEP DV		
APPROVAL BIN, KK	REV 1.0		PART NO. BA41-#####A
MODULE CODE undefined	LAST EDIT April, 13, 2006 5:10:14 PM		PAGE 18 OF 50

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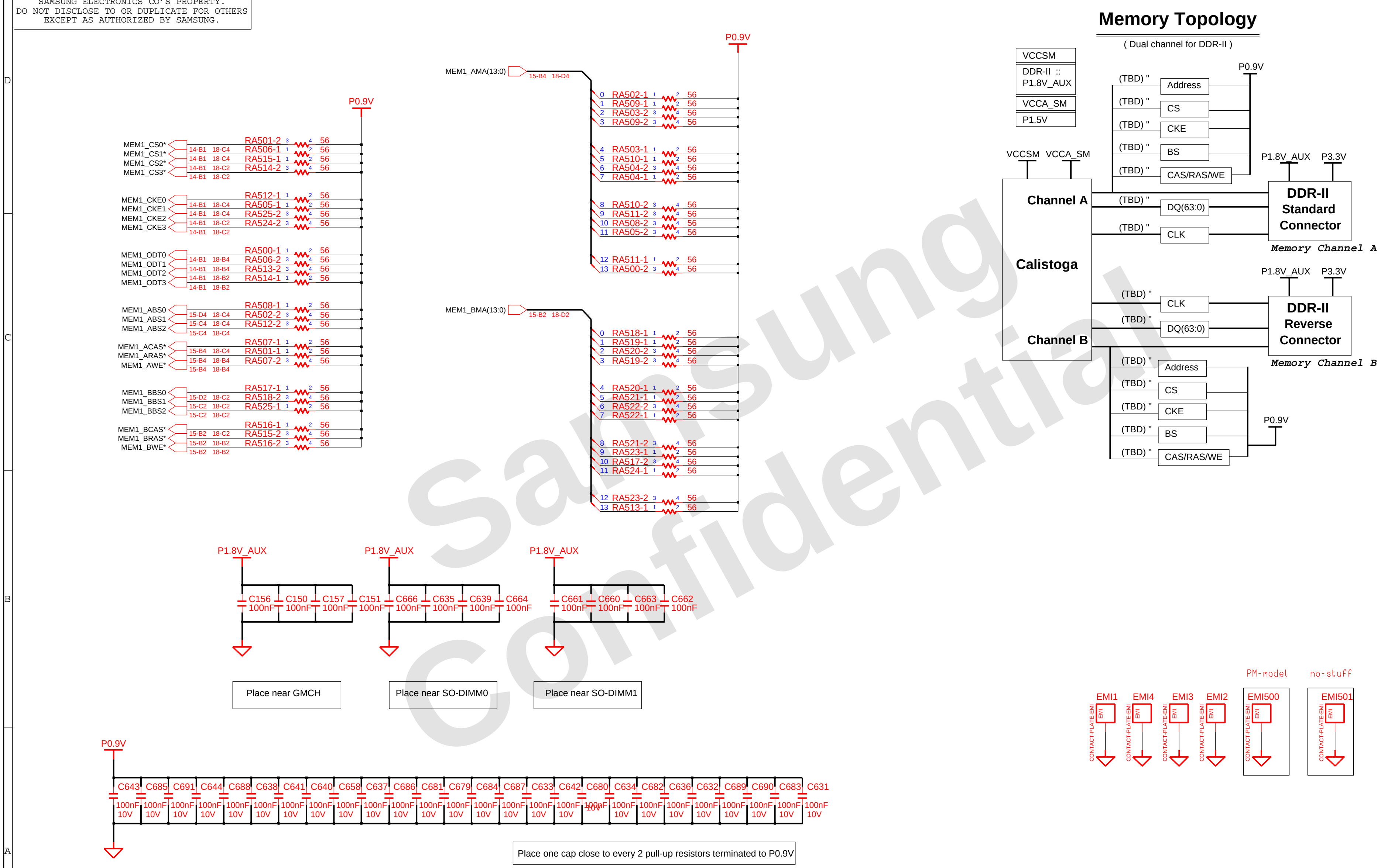

DRAW	YOO, BW	DATE	4/8/2006	TITLE	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	HAINAN C MAIN DDR2 - TERMINATION	
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:10:25 PM		PAGE 19 OF 50

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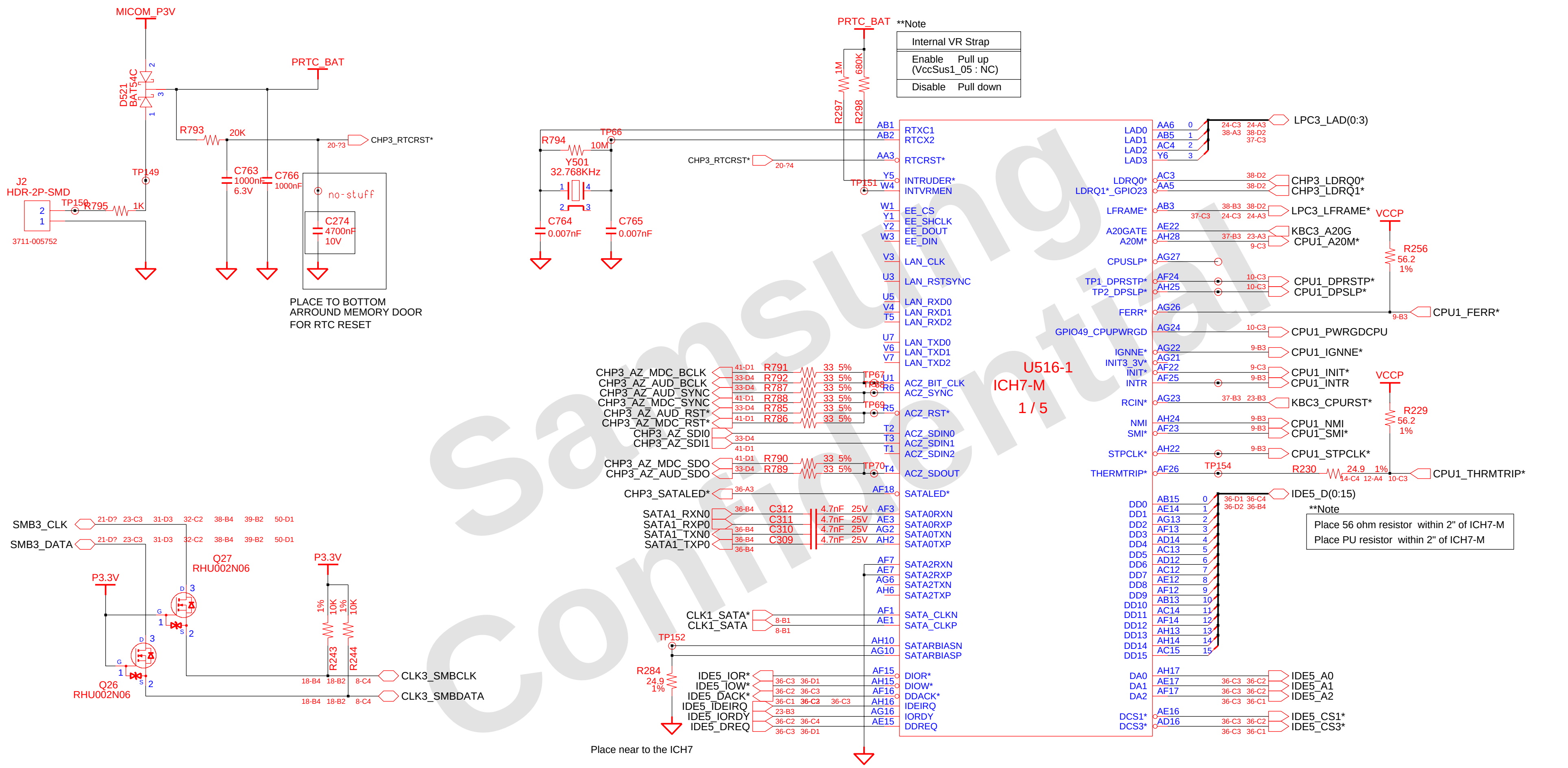
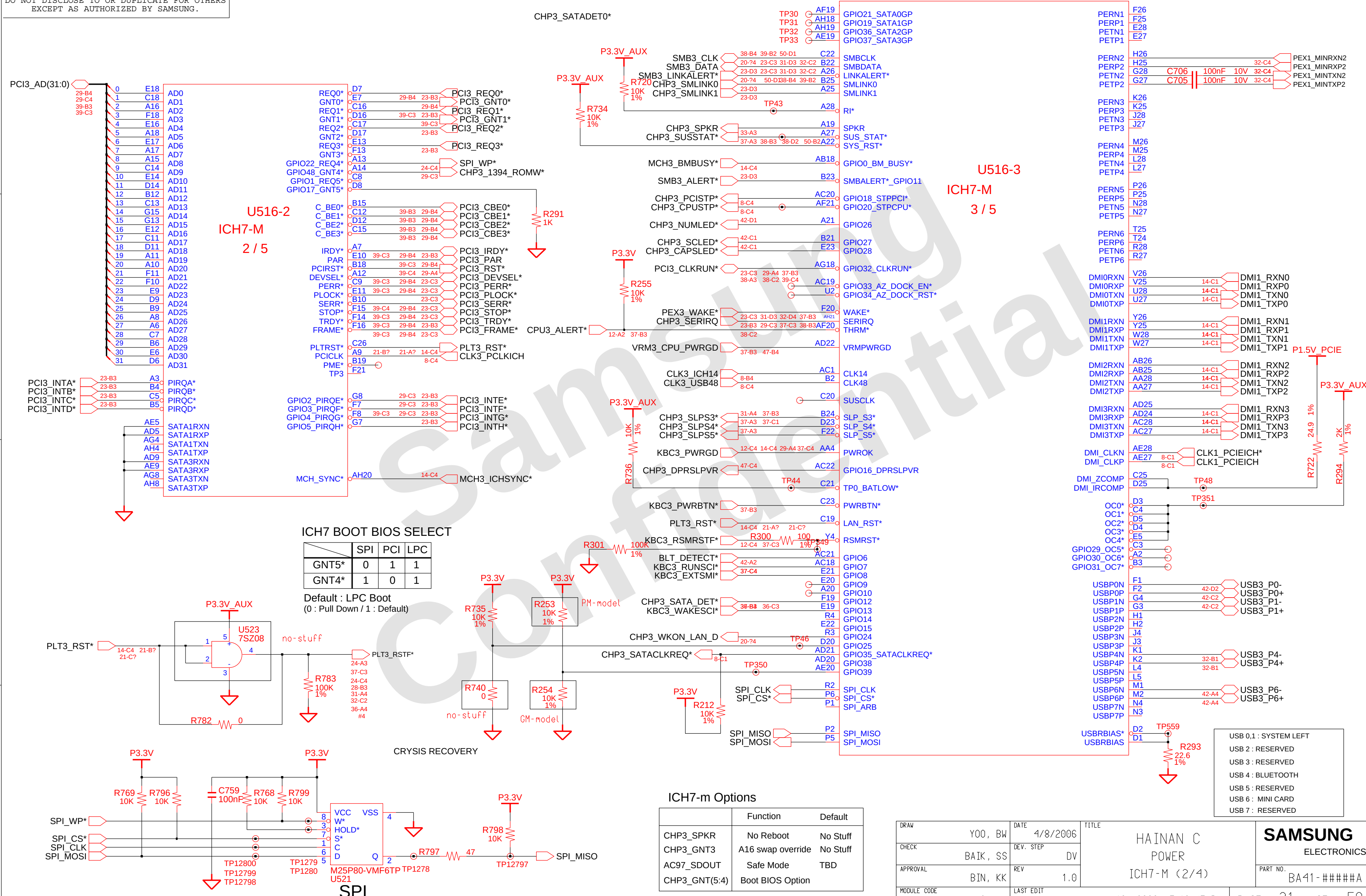


DRAW	YOO, BW	DATE	4/8/2006	TITLE	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	HAINAN C MAIN ICH7 - M(1/4)	
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:10:35 PM		PAGE 20 OF 50

AC caps : PCIE need to be within 250mils of the driver
Resistor for Test : Place Stuffing Option to minimize stubs



ICH7 BOOT BIOS SELECT

	SPI	PCI	LPC
GNT5*	0	1	1
GNT4*	1	0	1

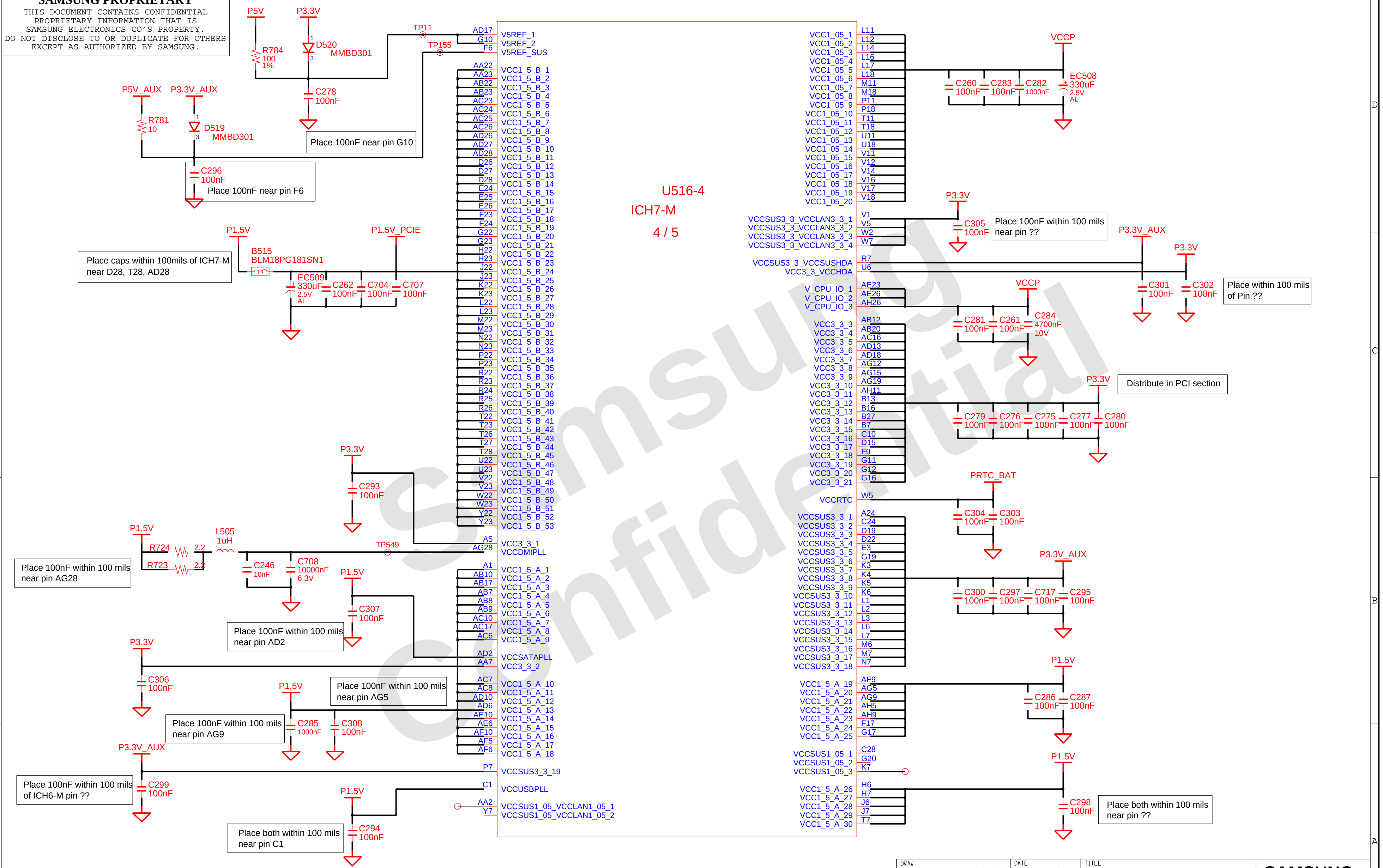
Default : LPC Boot
(0 : Pull Down / 1 : Default)

USB 0,1 : SYSTEM LEFT
USB 2 : RESERVED
USB 3 : RESERVED
USB 4 : BLUETOOTH
USB 5 : RESERVED
USB 6 : MINI CARD
USB 7 : RESERVED

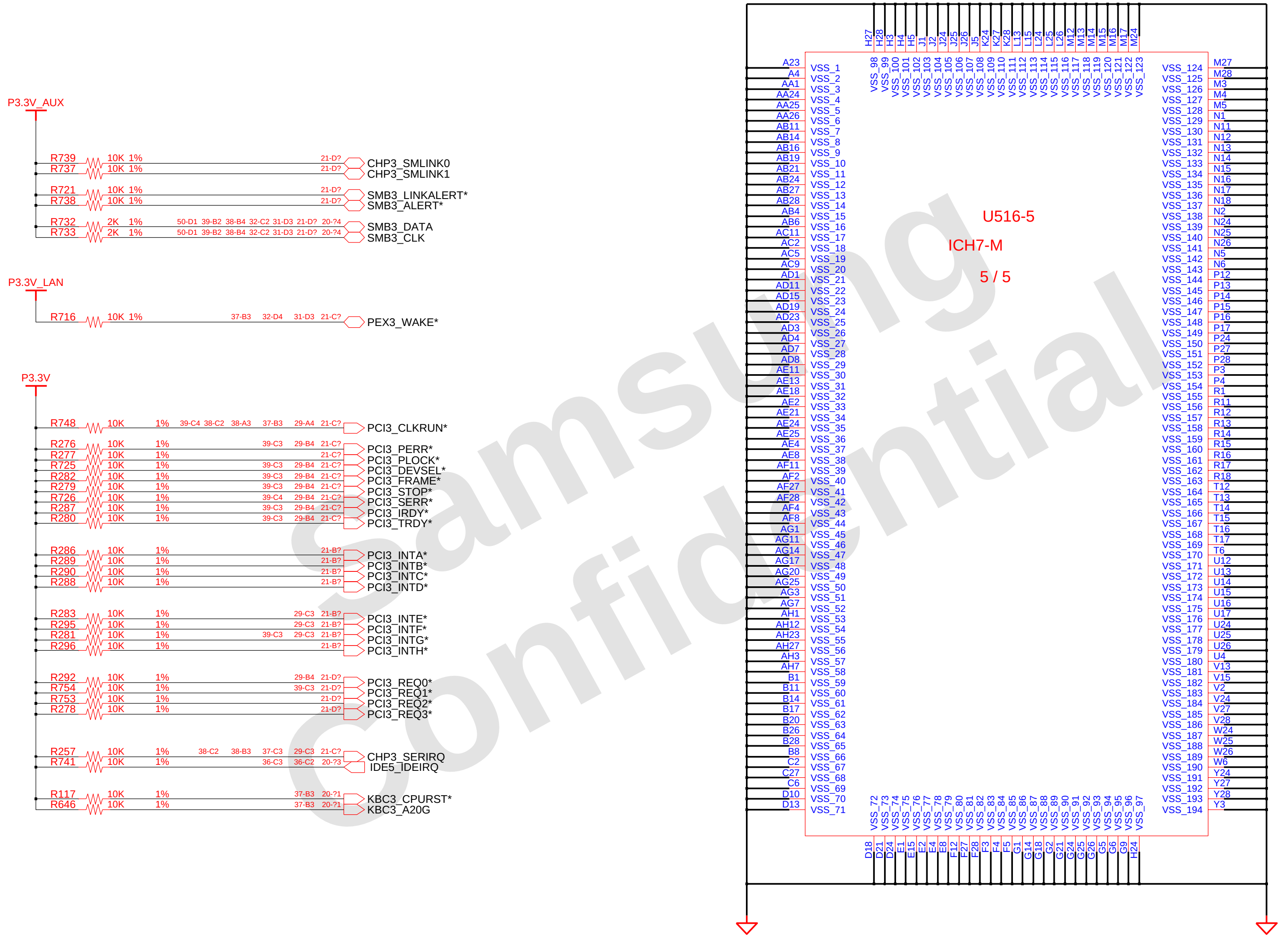
ICH7-m Options

	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_GNT3	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
CHP3_GNT(5:4)	Boot BIOS Option	

DRAW: YOO, BW	DATE: 4/8/2006	TITLE: HAINAN C POWER ICH7-M (2/4)	SAMSUNG ELECTRONICS
CHECK: BAIK, SS	DEV. STEP: DV		
APPROVAL: BIN, KK	REV: 1.0		PART NO. BA41-#####A
MODULE CODE: undefined	LAST EDIT: April, 13, 2006 5:10:45 PM		PAGE 21 OF 50



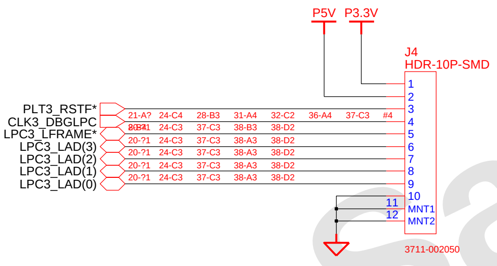
DRAW	YOO, BW	DATE	4/8/2006	TITLE	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	HAINAN C MAIN ICH7 - M(3/4)	
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:10:54 PM		PAGE 22 OF 50



DRAW	YOO, BW	DATE	4/8/2006	TITLE
CHECK	BAIK, SS	DEV. STEP	DV	HAINAN C MAIN ICH7 - M(4/4)
APPROVAL	BIN, KK	REV	1.0	
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:11:07 PM	PAGE 23 OF 50

SAMSUNG ELECTRONICS
PART NO. BA41-#####A

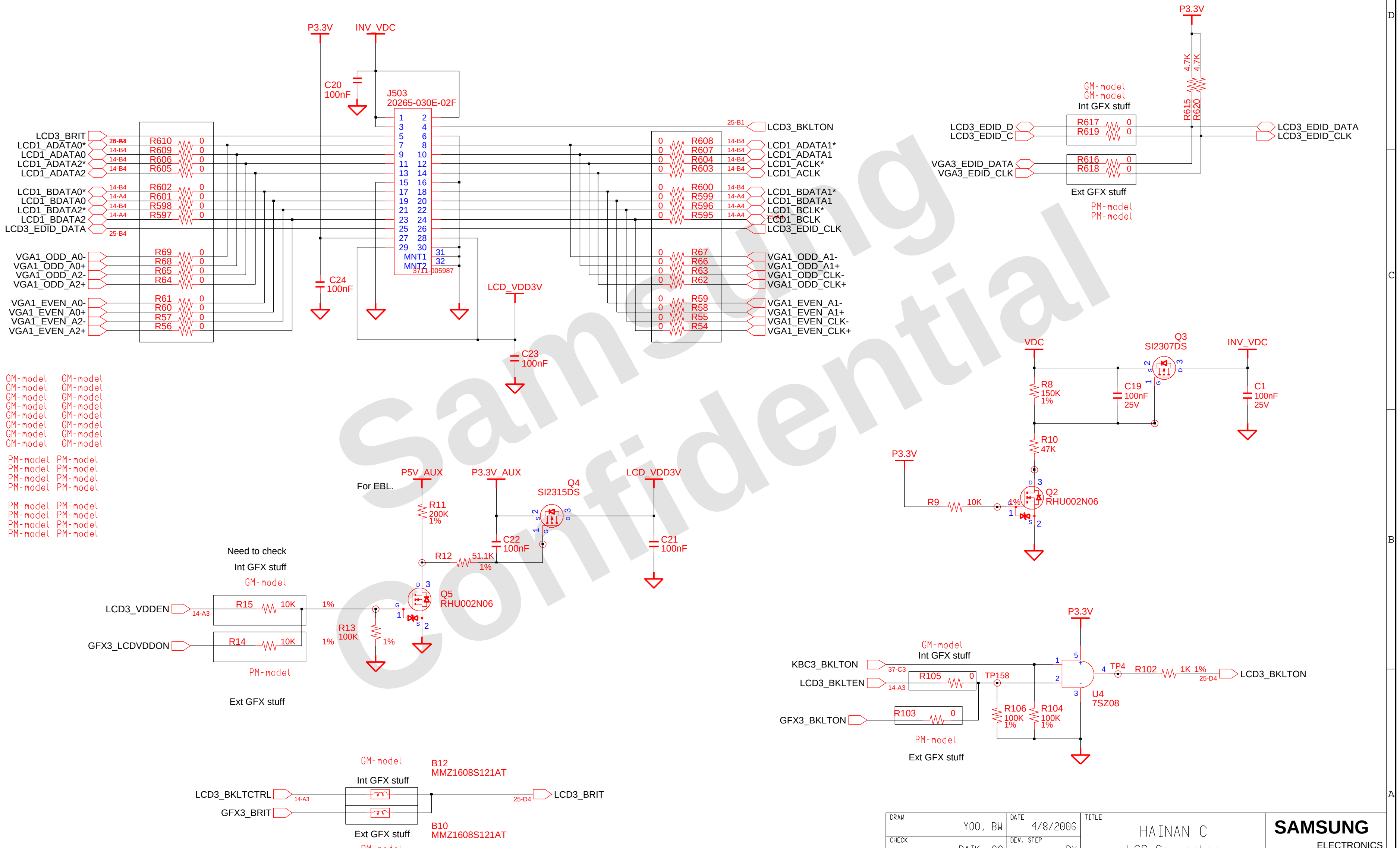
BIOS CODE



02 VERIFY REAL MODE
03 DISABLE NMI
04 GET CPU TYPE
06 INIT. SYSTEM H/W
08 INIT. CHIPSET REG.
09 SET IN POST FLAG
0A INIT CPU.REG
0B CPU CACHE ON
0C INIT.CACHE TO POST
OE INIT. I/O VALUE
0F ENABLE THE L-BUS IDE
10 INIT. POWER MANAGER
11 LOAD ALTERNATE REG.
13 PCI BUS MASTER RESET
WITH INITIAL POST VALUE
14 INIT. KEYBOARD CONTROLLER
16 CHECK CHECKSUM
18 8254 TIMER INIT.
1A 8237 DMA CONTROLLER INIT.
1C RESET INTERRUP CONTROLLER
20 TEST DRAM REFRESH
22 TEST 8742 KEYBOARD CONTROLLER
24 SET ES SEGMENT REG. TO 4GB
26 ENABLE A20
28 AUTO SIZING DRAM
32 COMPUTE THE CPU SPEED
34 TESET CMOS RAM
38 SHADOW SYSTEM BIOS ROM
3A AUTO SIZING CACHE
3C CONFIGURE ADVANCED CHIPSET REG.
3D LOAD ALTER REG. WITH CMOS VALUE
42 INIT. INTERRUPT VECTOR
44 INIT. BIOS INTERRUPT
46 CHECK ROM COPYRIGHT NOTICE
47 INIT. I20 SUPPORT IF INSTALLED
48 CHECK VIDEO CONFIGURE AGAINST CMOS
49 INIT. PCI BUS AND DEVICE
4A INIT. ALL VIDEO BIOS ROM
4C SHADOW VIDEO BIOS ROM
50 DISPLAY CPU TYPE AND SPEED
52 TEST KEYBOARD
54 SET KEYCLICK IF ENABLED
56 ENABLE KEYBOARD
58 TEST FOR UNEXPECTED INTERRUPTS
5A DISPLAY " PRESS ...... SETUP"
5C TEST RAM GETWEEN 512K AND 640K
60 TEST EXTENDED MEMORY
62 TEST EXTENDED MEMORY ADDRESS LINE
64 JUMP TO USER PATCH 1

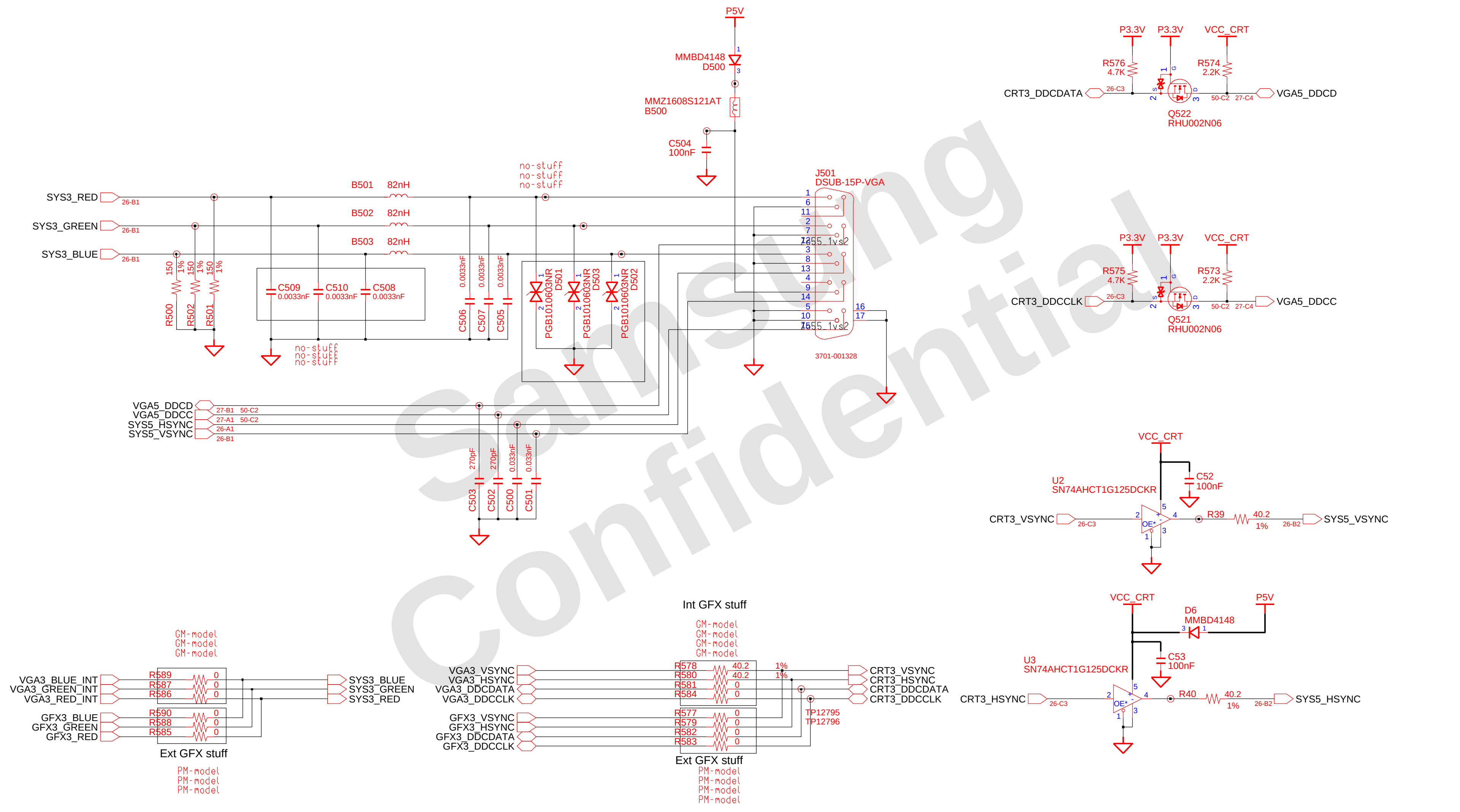
66 CONFIGURE ADVANCE CACHE REG.
6A DISPLAY EXTERNAL CACHE SIZE
6C DISPLAY SHADOW MESSAGE
6E DISPLAY NON-DISPOSABLE SEGMENT
70 DISPLAY ERROR MESSAGE
72 CHECK FOR CONFIGURATION ERROR
74 TEST REAL-TIME CLOCK
76 CHECK FOR KEYBOARD EERROR
7C SETUP HARDWARE INTERRUPT VECTOR
7E TEST COPROCESSER IF PRESENT
80 DISABLE ON-BOARD I/O PORT
82 DETECT AND INSTALL EXT.RS232C
84 DETECT AND INSTALL EXT.PARALLEL
86 RE-INIT. ON-BOARD I/O PORT
88 INIT. BIOS DATA ROM
8A INIT.EXTENDED BIOS DATA AREA
8C INIT. FDD CONTROLLER
9A SHADOW OPTION ROMS
9C SETUP POWER MANAGEMENT
9E ENABLE H/W INTERRUPT
A0 SET TIME OF DAY
A4 INIT. TYPEMATIC RATE
A8 ERASE F2 PROMPT
AA SCAN FOR F2 KEY STROKE
AC ENTER SETUP
AE CLEAR IN POST FLAG
B0 CHECK FOR ERRORS
B2 POST DONE-PREPARE TO BOOT O/S
B4 ONE BEEP
B6 CHECK PASSWORD (OPTION)
B7 ACPI INIT
BA DMI INIT
BE CLEAR SCREEN
C0 TRY BOOT WITH INT19
D0 INTERRUPT HANDLER ERROR
D2 UNKNOWN INTERRUPT ERROR
D4 PENDING INTERRUPT ERROR
D6 SHUTDOWN 5
D8 SHUTDOWN ERROR
DA EXTENDED BLOCK MOVE
DC SHUTDOWN 10
89 ENABLE NMI
90 INIT. HDD CONTROLLER
91 INIT. LOCAL BUS HDD CONTROLLER
92 JUMP TO USER PATCH 2
94 DISABLE A20 ADDRESS LINE
96 CLEAR HUGE ES SEGMENT REG.
98 SEARCH FOR OPTION ROMS

DRAW	YOO, BW	DATE	4/8/2006	TITLE: HAINAN C MAIN FIRMWARE HUB	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV		
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:15:06 PM		PAGE 24 OF 50



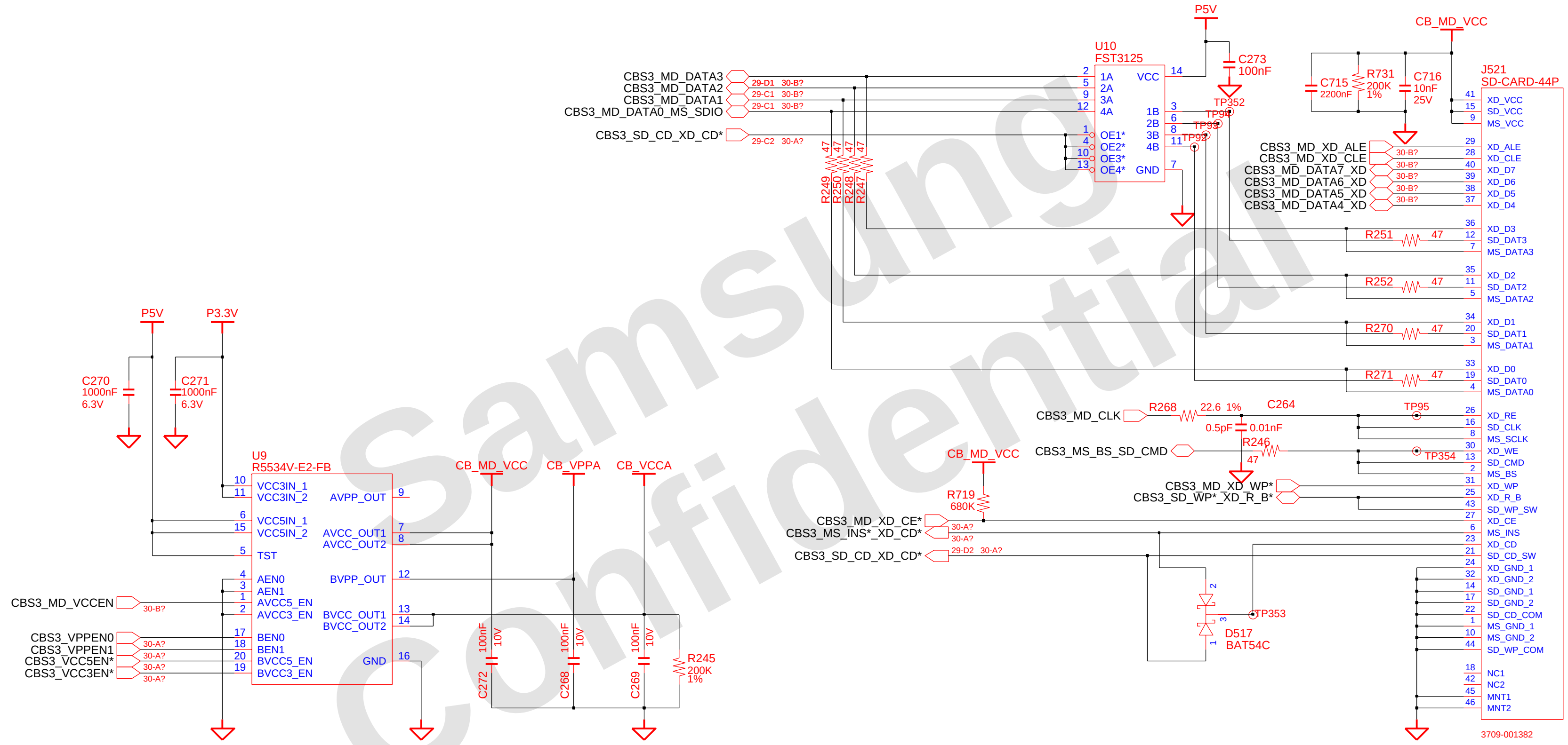
DRAW	YOO, BW	DATE	4/8/2006	TITLE	HAINAN C LCD Connector	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	1.0			PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:15:16 PM			PAGE 25 OF 50

CRT CONNECTOR



DRAW: YOO, BW	DATE: 4/8/2006	TITLE: HAINAN C POWER CRT connector		SAMSUNG ELECTRONICS
CHECK: BAIK, SS	DEV. STEP: DV			PART NO. BA41-#####A
APPROVAL: BIN, KK	REV: 1.0			
MODULE CODE: undefined	LAST EDIT: April, 13, 2006 5:15:34 PM			PAGE 26 OF 50

5in1 Socket



DRAW	YOO, BW	DATE	4/8/2006	TITLE	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	HAINAN C POWER CARDBUS Controller (1/2)	
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:15:45 PM	PAGE 27 OF 50	

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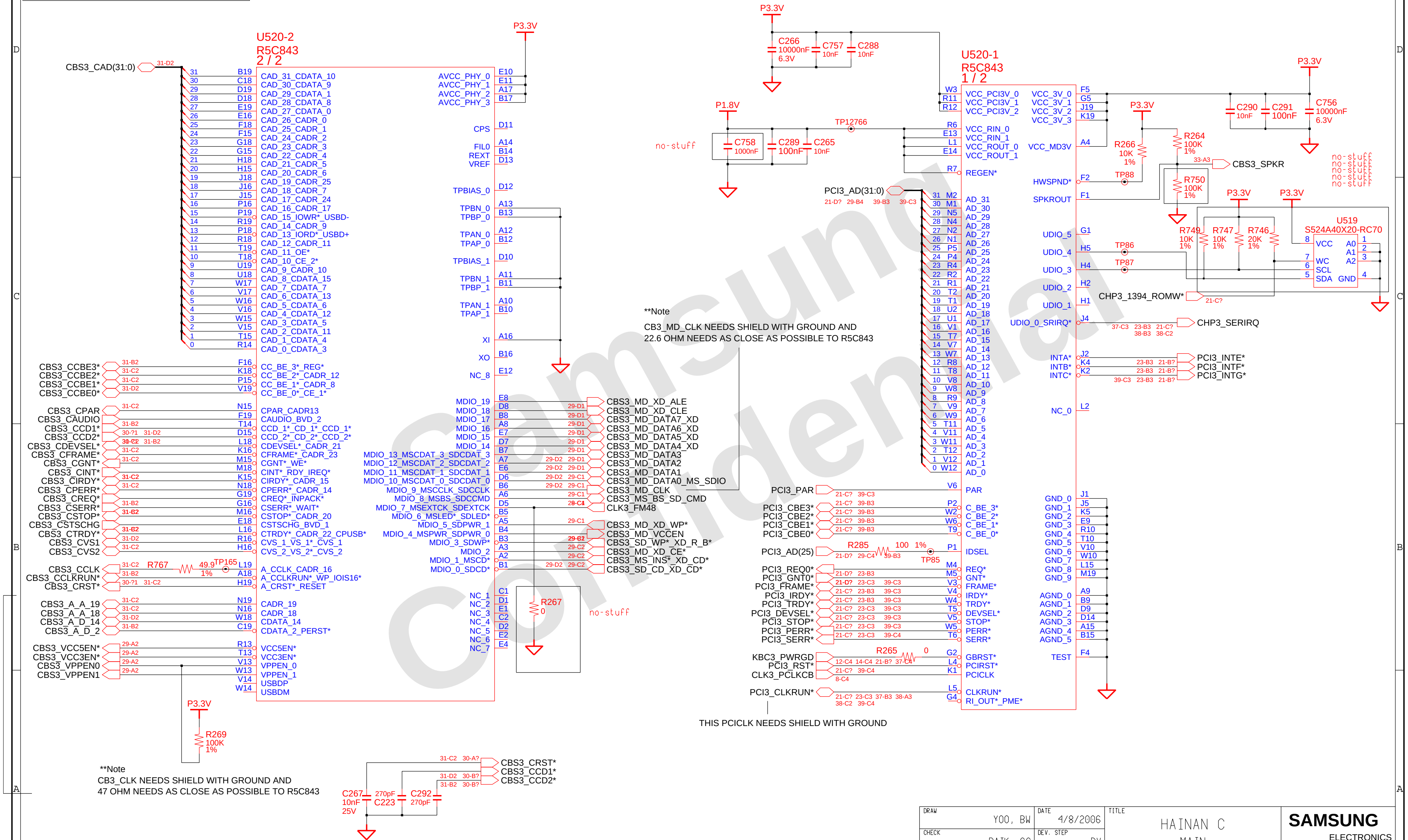
CARDBUS Controller



**Note

CB3_MD_CLK NEEDS SHIELD WITH GROUND AND 22.6 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C843

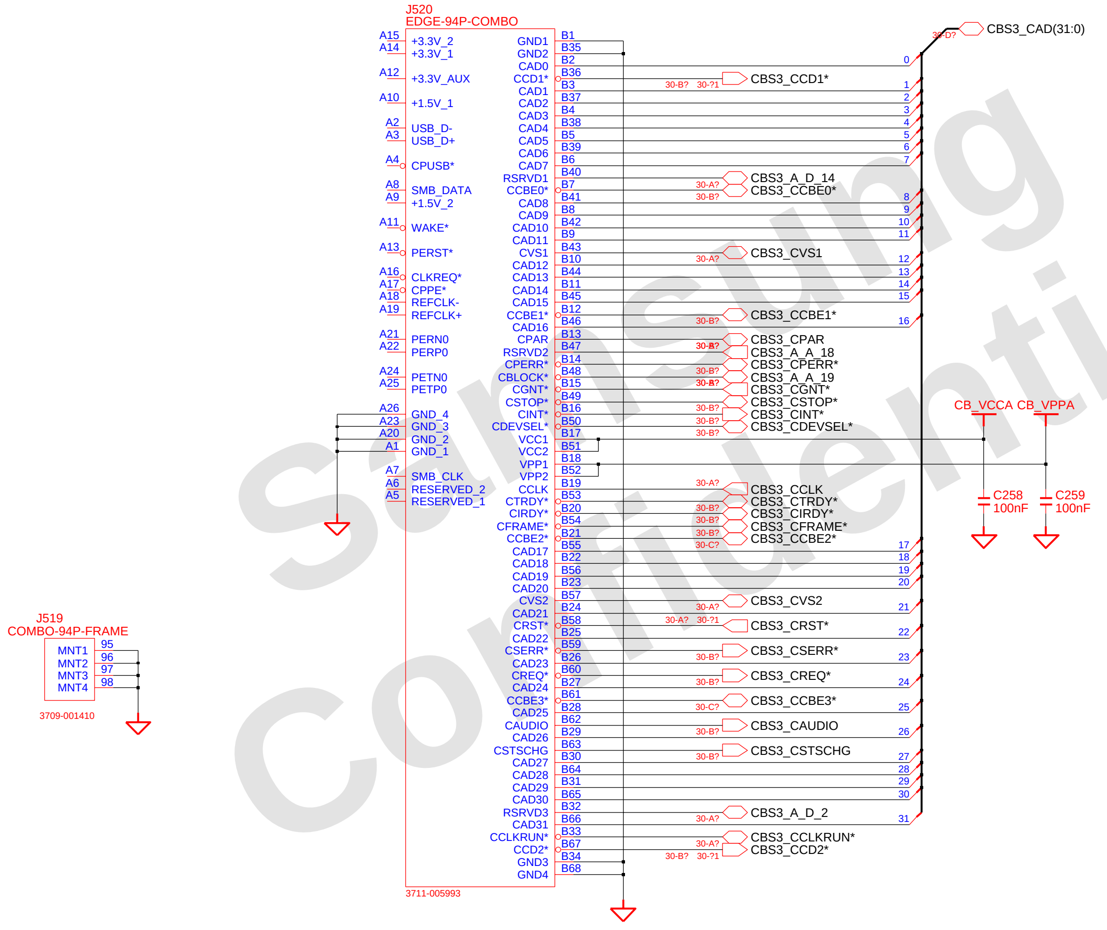
THIS PCICLK NEEDS SHIELD WITH GROUND

**Note

CB3_CLK NEEDS SHIELD WITH GROUND AND 47 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C843

DRAW: YOO, BW	DATE: 4/8/2006	TITLE: HAINAN C MAIN CARDBUS Controller (1/2)	SAMSUNG ELECTRONICS
CHECK: BAIK, SS	DEV. STEP: DV		PART NO. BA41-#####A
APPROVAL: BIN, KK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: April, 13, 2006 5:15:56 PM		PAGE 28 OF 50

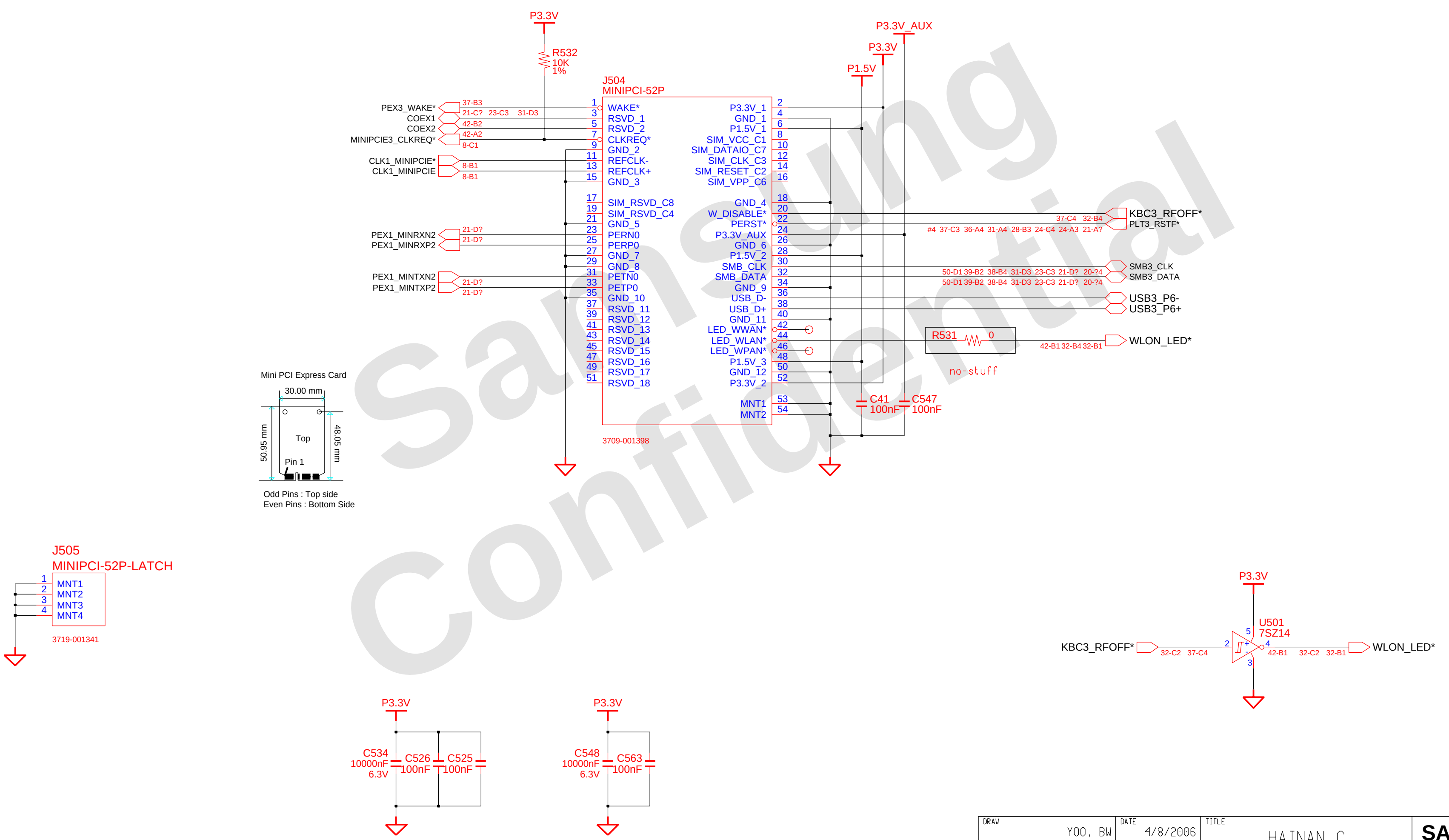
PCMCIA / EXPRESS CARD Connector



DRAW	YOO, BW	DATE	4/8/2006	TITLE	HAINAN C POWER PCMCIA/EXPRESS Connector
CHECK	BAIK, SS	DEV. STEP	DV	SAMSUNG ELECTRONICS	
APPROVAL	BIN, KK	REV	1.0	PART NO.	BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:16:07 PM	PAGE 29	OF 50

PCI Express Mini Card

PCI Express Mini Card ElectroMechanical Spec. 1.0



DRAW YOO, BW	DATE 4/8/2006	TITLE HAINAN C MAIN MINI Card (WLAN) & DMB	SAMSUNG ELECTRONICS
CHECK BAIK, SS	DEV. STEP DV		
APPROVAL BIN, KK	REV 1.0		PART NO. BA41-#####A
MODULE CODE undefined	LAST EDIT April, 13, 2006 5:17:05 PM		PAGE 31 OF 50

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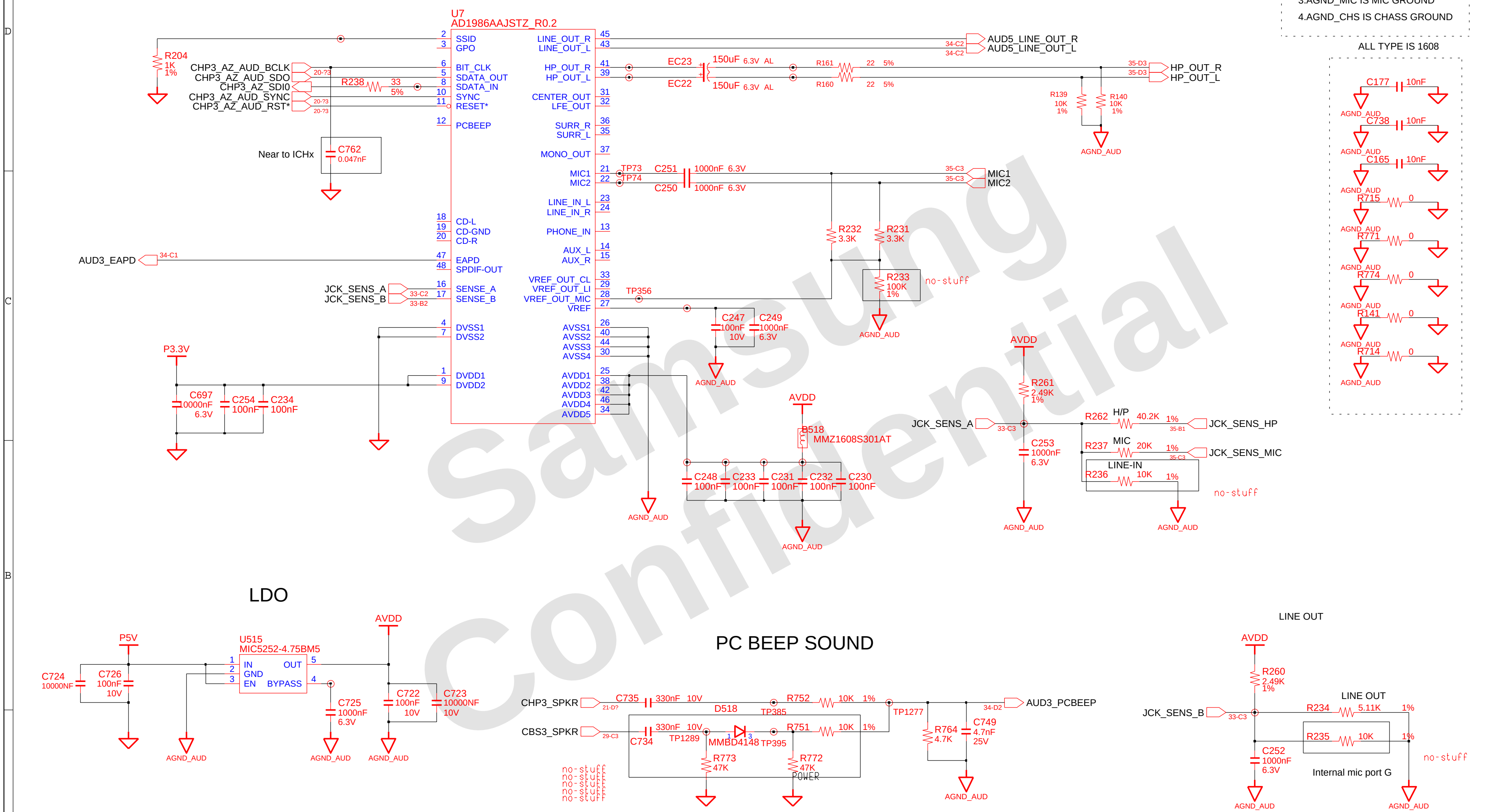
AUDIO CODEC

1.AGND_AUD IS AUDIO GROUND
2. GND IS DIGITAL GROUND
3.AGND_MIC IS MIC GROUND
4.AGND_CHS IS CHASS GROUND



DRAW	YOO, BW	DATE	4/8/2006	TITLE	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	HAINAN C MAIN AUDIO CODEC	
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:17:16 PM		PAGE 32 OF 50

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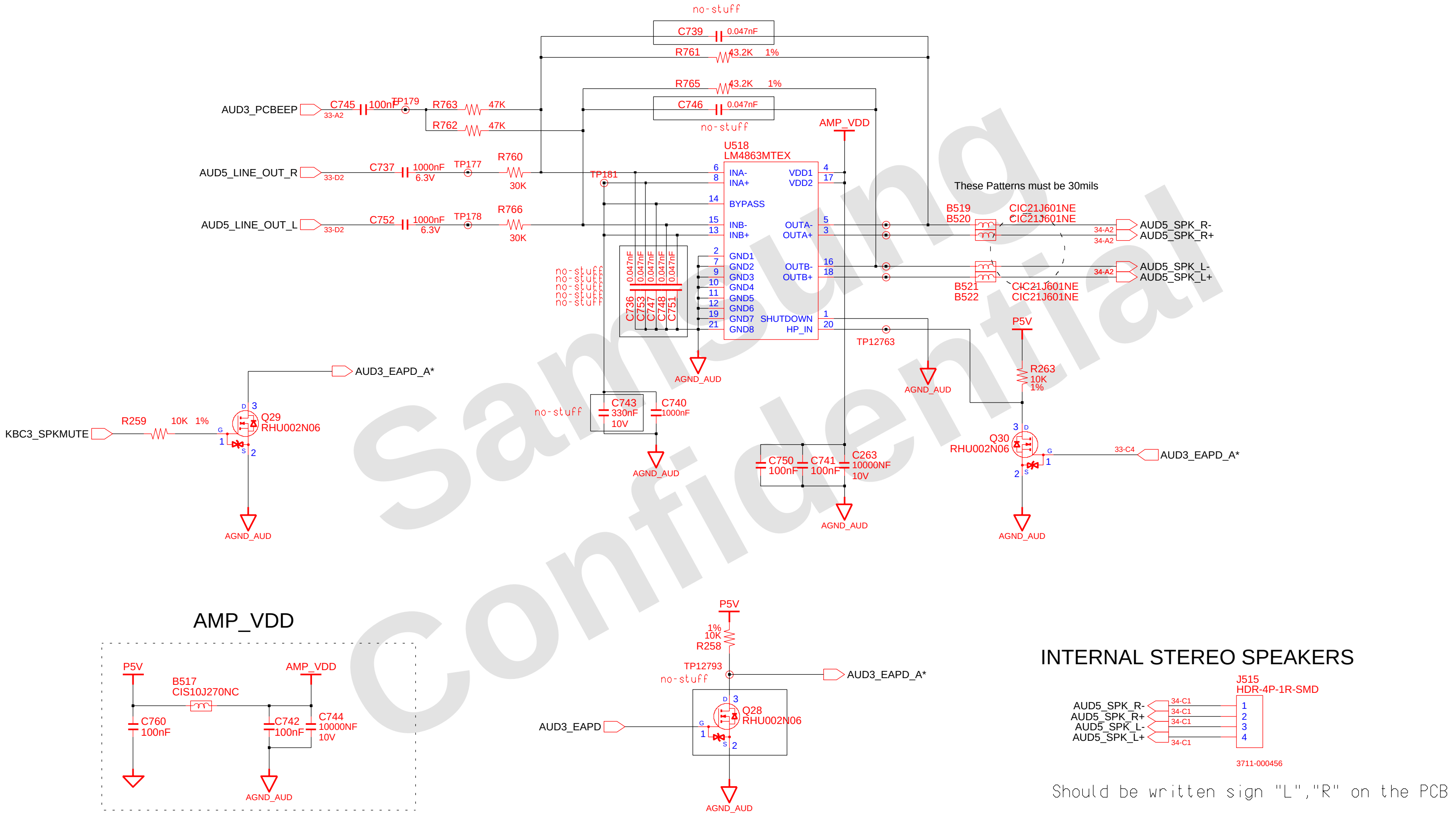
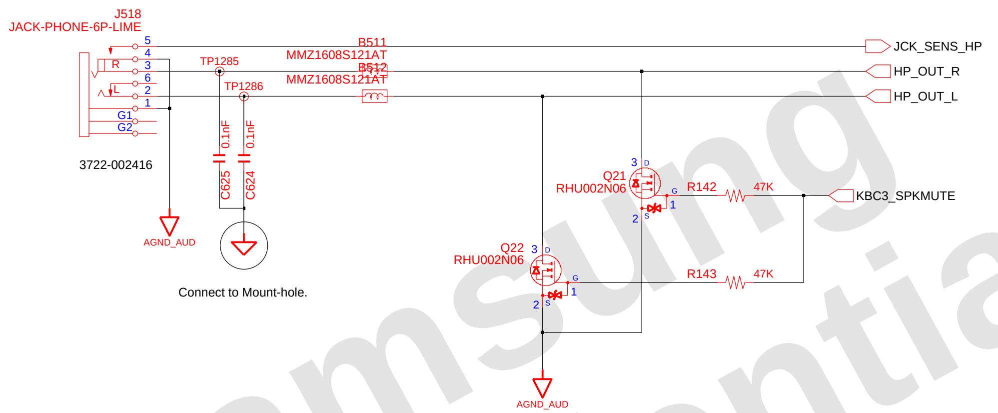
d:/users/mobile20/mentor/hainan_c/hainan_c

AUDIO AMP

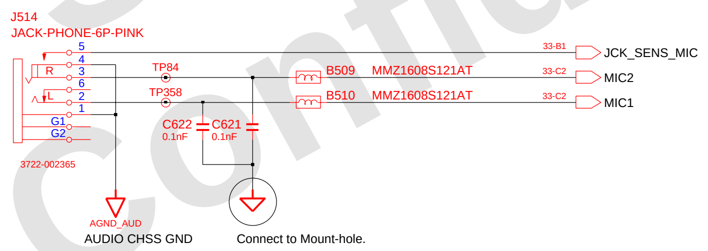


DRAW	YOO, BW	DATE	4/8/2006	TITLE	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	HAINAN C MAIN AUDIO AMP	
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:17:25 PM		PAGE 33 OF 50

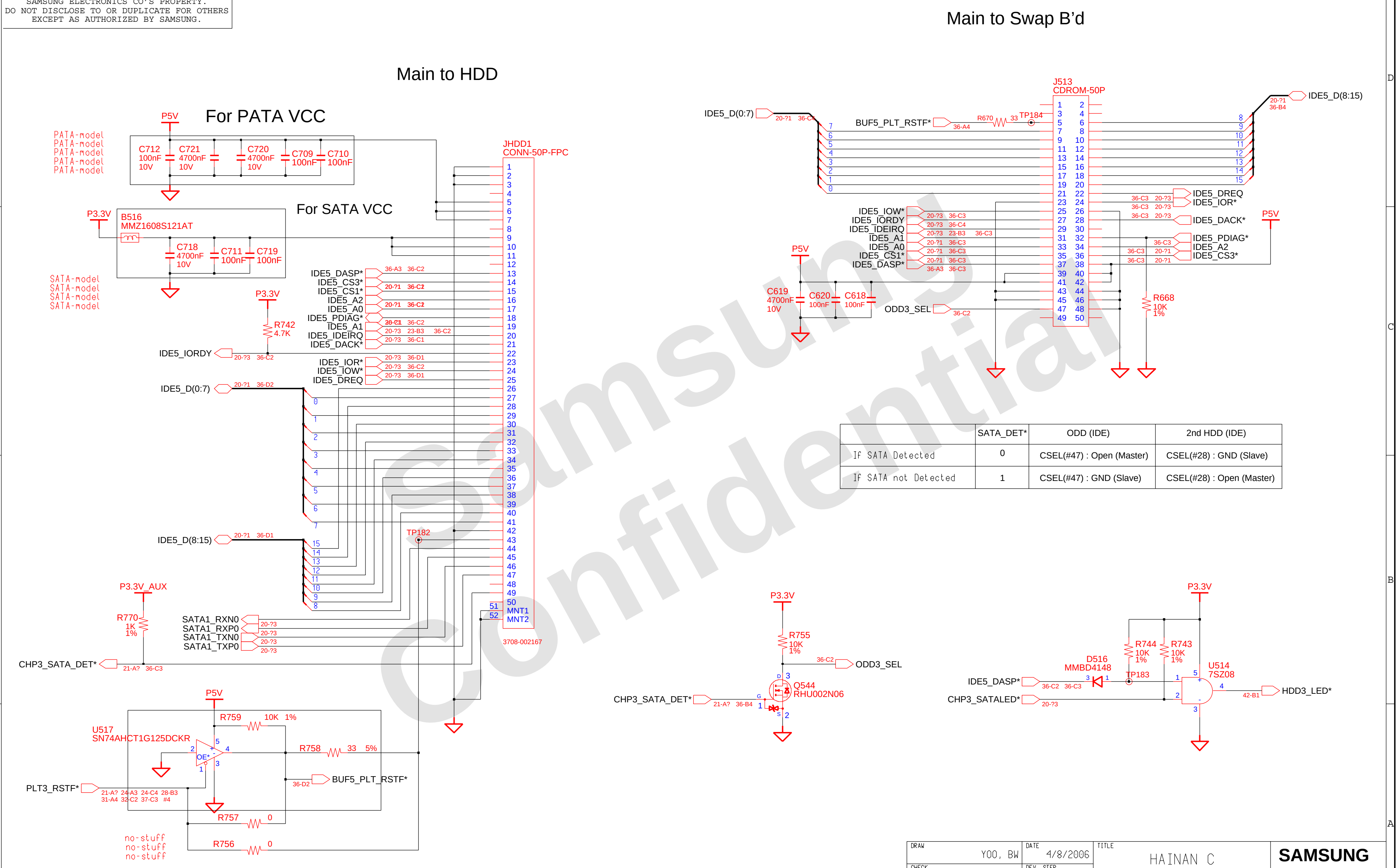
HEADPHONE



MIC JACK



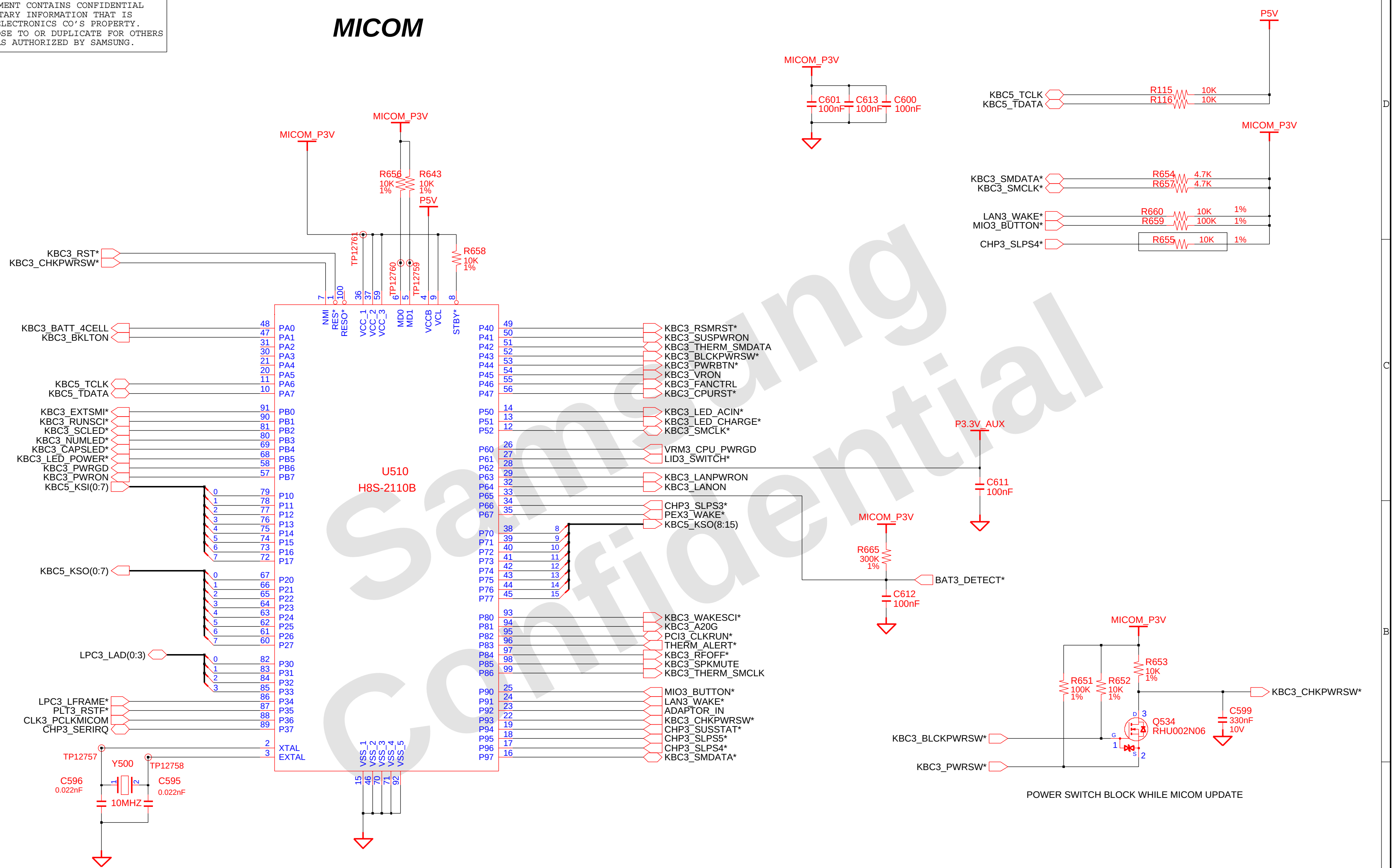
DRAW	YOO, BW	DATE	4/8/2006	TITLE: HAINAN C / MAIN / Headphone & MIC Jack	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV		
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:17:46 PM		PAGE 34 OF 50



	SATA_DET*	ODD (IDE)	2nd HDD (IDE)
If SATA Detected	0	CSEL(#47) : Open (Master)	CSEL(#28) : GND (Slave)
If SATA not Detected	1	CSEL(#47) : GND (Slave)	CSEL(#28) : Open (Master)

DRAW: YOO, BW	DATE: 4/8/2006	TITLE: HAINAN C MAIN HDD ODD CONNECTOR	SAMSUNG ELECTRONICS
CHECK: BAIK, SS	DEV. STEP: DV		
APPROVAL: BIN, KK	REV: 1.0		PART NO. BA41-#####A
MODULE CODE: undefined	LAST EDIT: April, 13, 2006 5:18:03 PM		PAGE 35 OF 50

MICOM



DRAW	YOO, BW	DATE 4/8/2006	TITLE HAINAN C MAIN MICOM	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP DV		
APPROVAL	BIN, KK	REV 1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:18:15 PM	PAGE 36 OF 50

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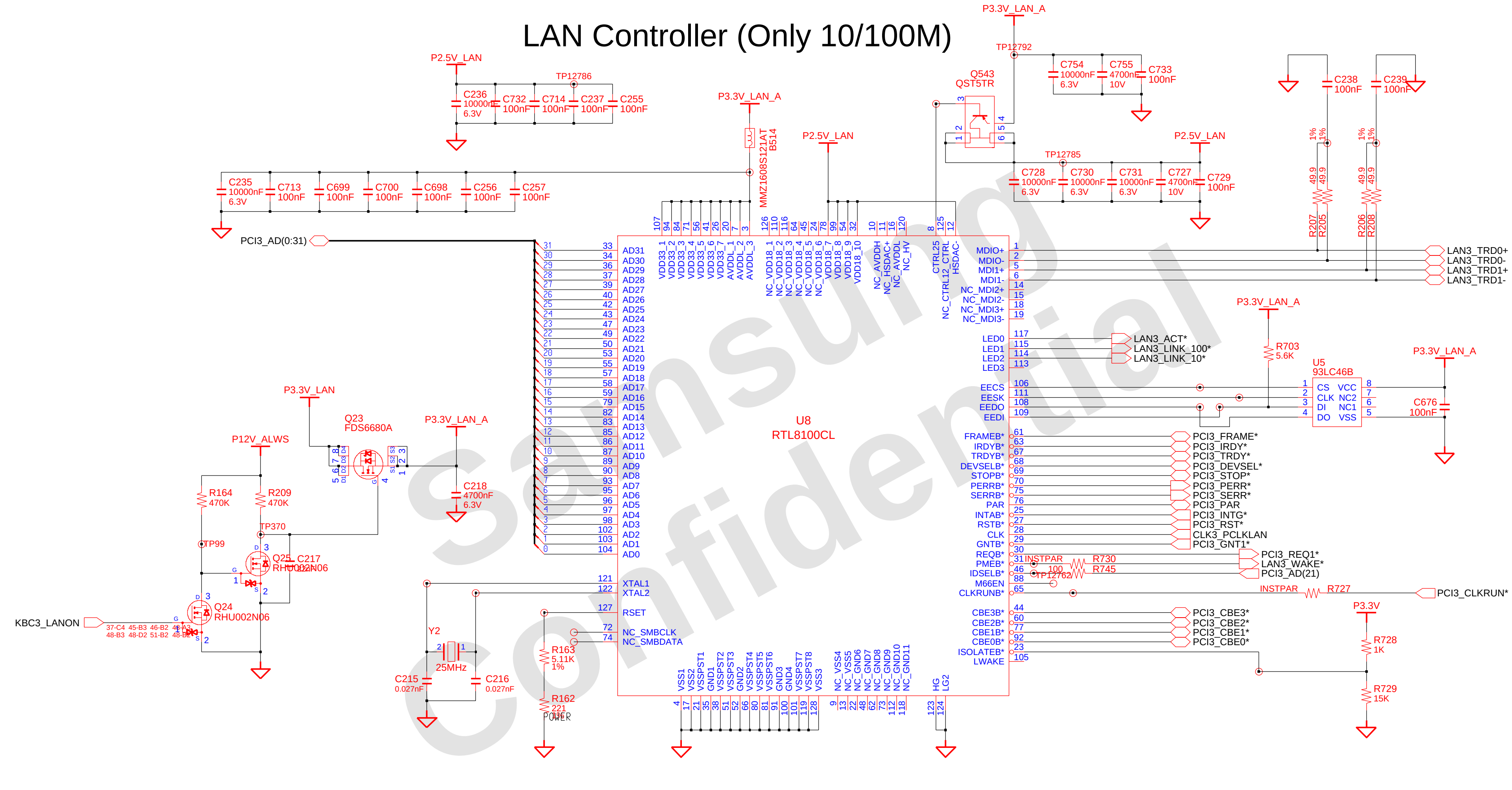
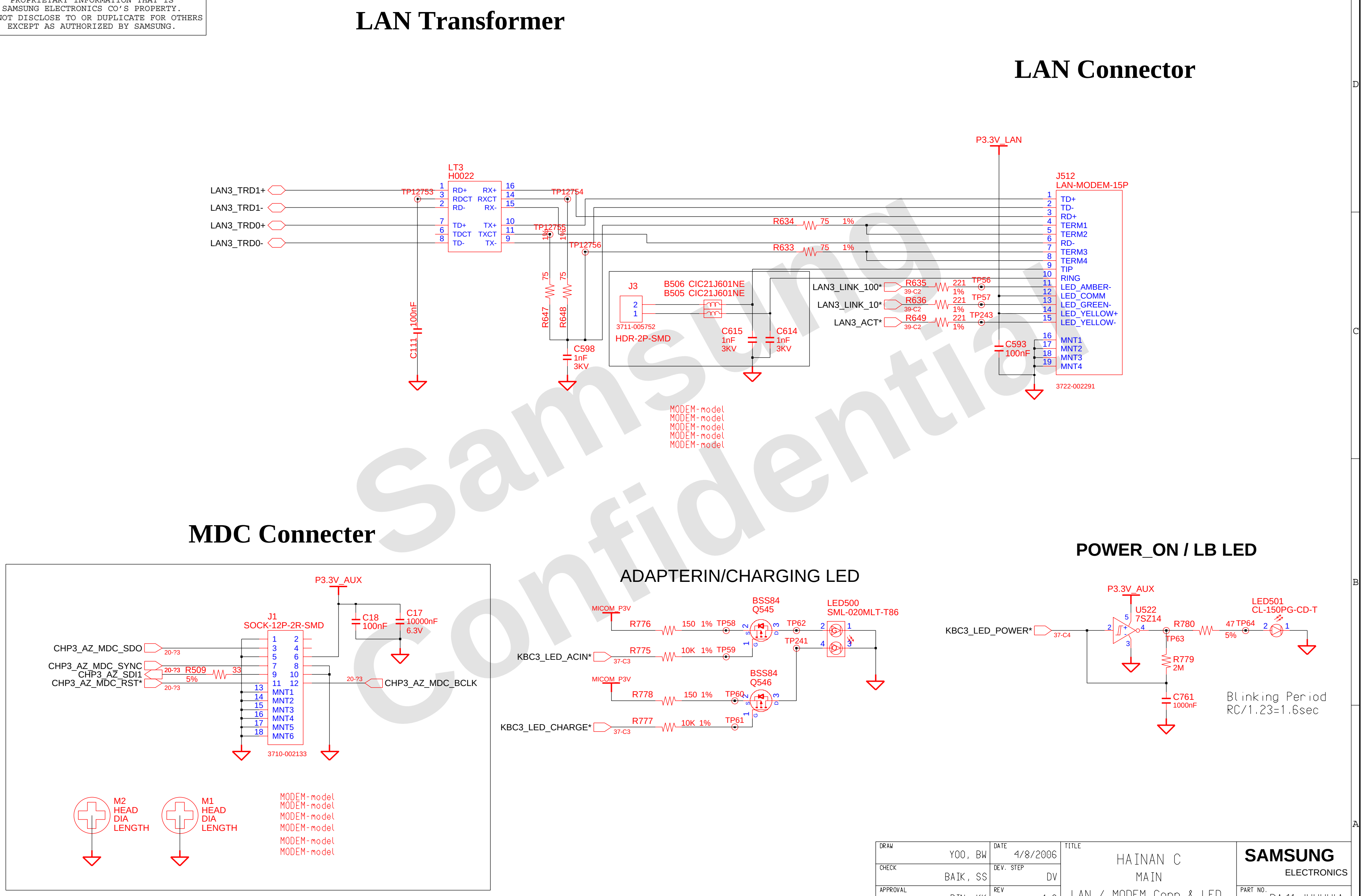
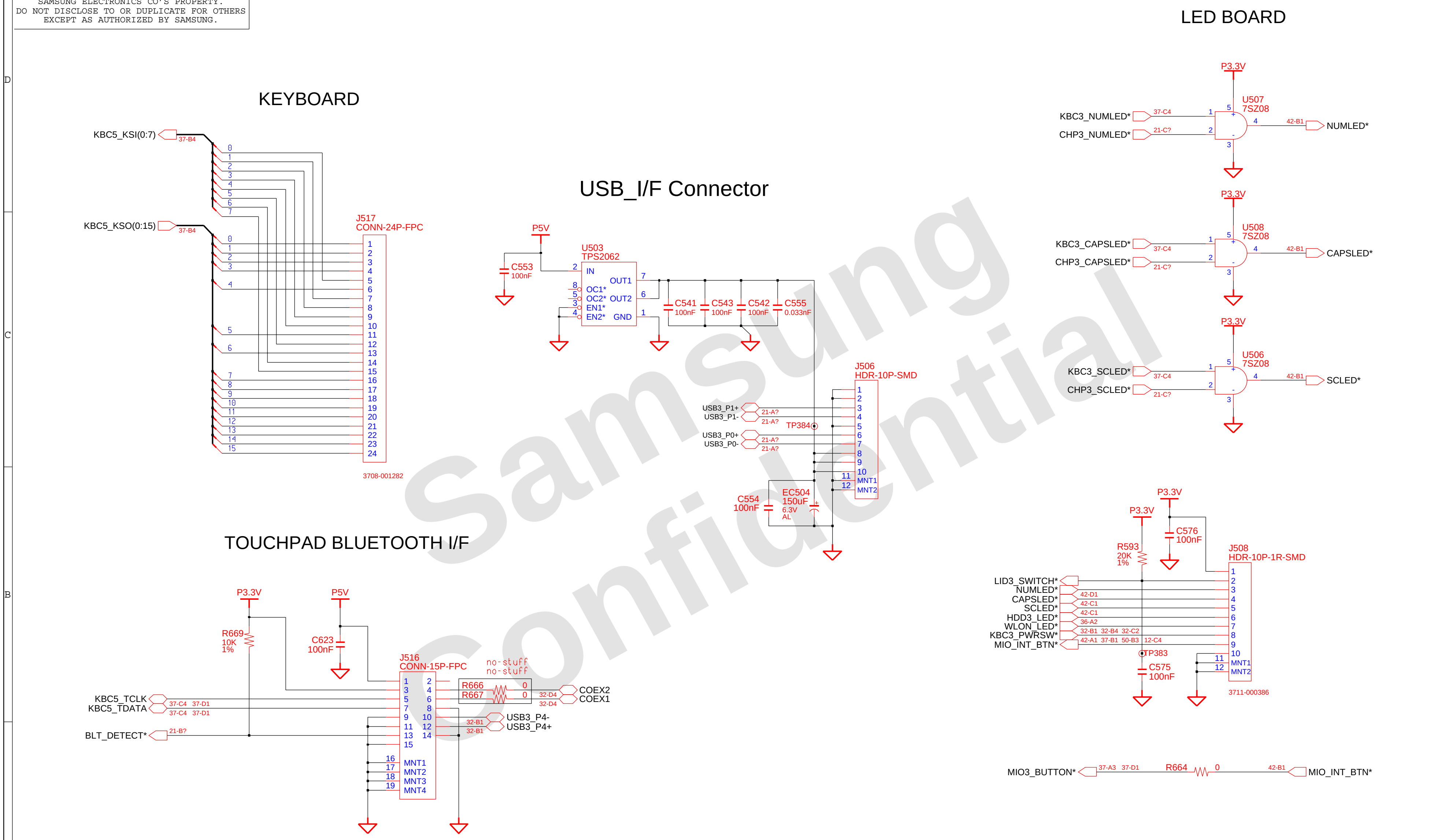
LAN Controller (Only 10/100M)



DRAW	YOO, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV		MAIN	
APPROVAL	BIN, KK	REV	1.0		BCM 5751/4401 (1/2)	PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:18:26 PM			PAGE 37 OF 50

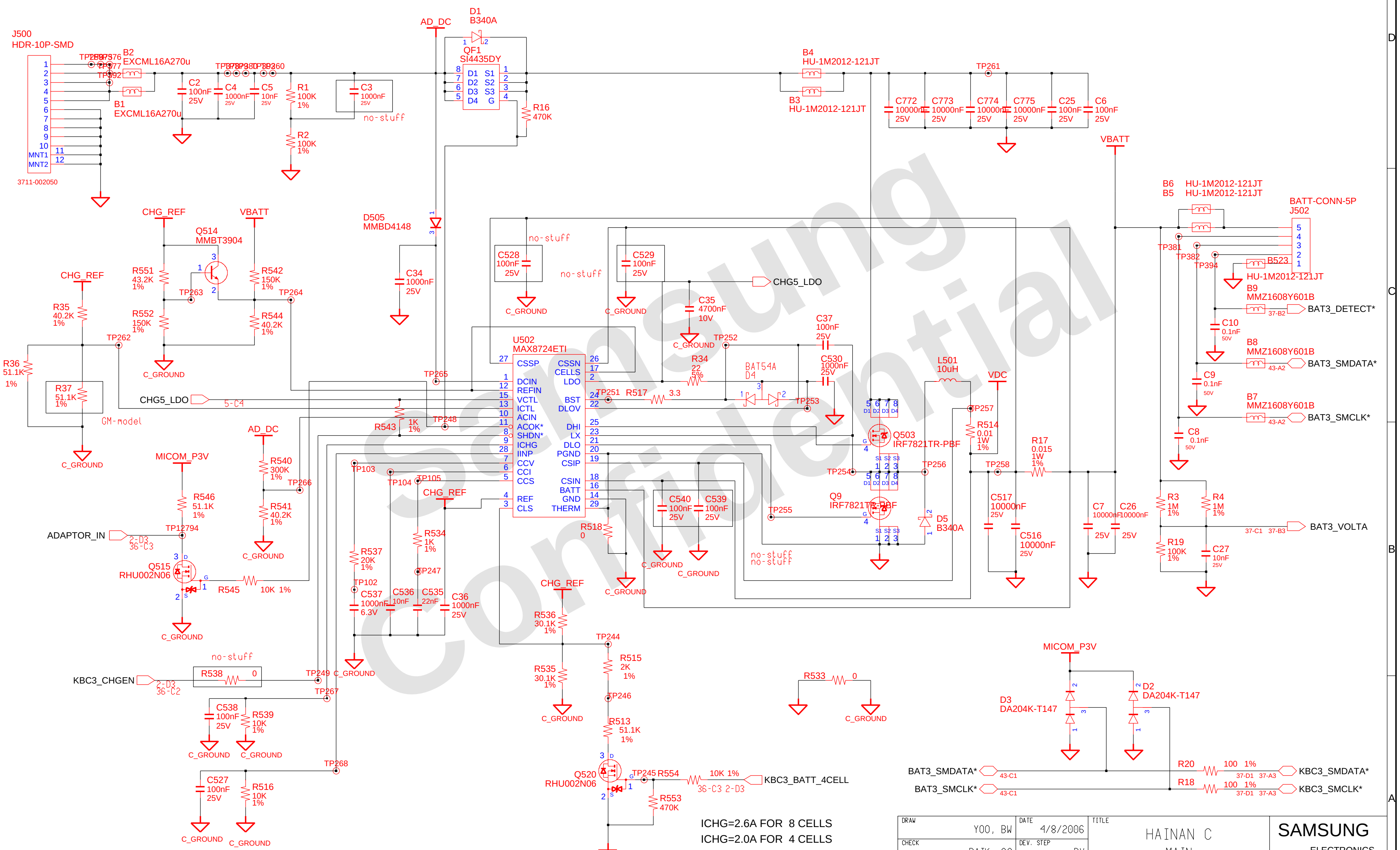


DRAW YOO, BW	DATE 4/8/2006	TITLE HAINAN C		SAMSUNG ELECTRONICS
CHECK BAIK, SS	DEV. STEP DV	MAIN		
APPROVAL BIN, KK	REV 1.0	LAN / MODEM Conn & LED.		PART NO. BA41-#####A
MODULE CODE undefined	LAST EDIT April, 13, 2006 5:18:39 PM		PAGE 38	OF 50



DRAW	YOO, BW	DATE	4/8/2006	TITLE	HAINAN C MAIN SUB B'D CONNECTOR
CHECK	BAIK, SS	DEV. STEP	DV		SAMSUNG ELECTRONICS
APPROVAL	BIN, KK	REV	1.0	PART NO.	BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:19:12 PM	PAGE 39	OF 50

CHARGER & POWER MANAGEMENT



ICHG=2.6A FOR 8 CELLS
ICHG=2.0A FOR 4 CELLS
VCHG=16.8V(4.2V*4)
ILIMIT=4.50A(85%x90W)

DRAW	YOO, BW	DATE	4/8/2006	TITLE	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	HAINAN C MAIN CHARGER	
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:19:26 PM		PAGE 40 OF 50

COM-22C-015(1996.6.5) REV. 3

d:/users/mobile20/mentor/hainan_c/hainan_c

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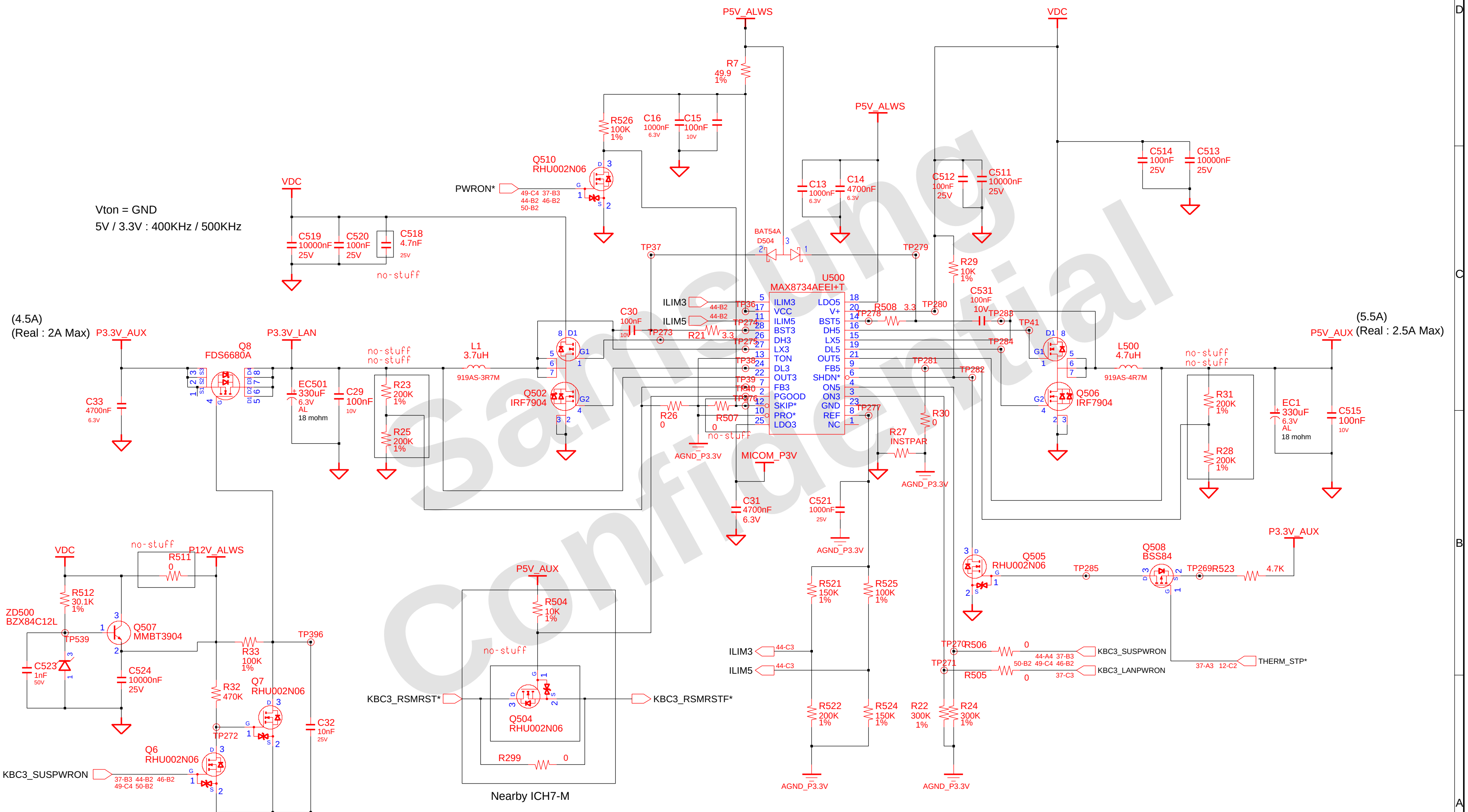
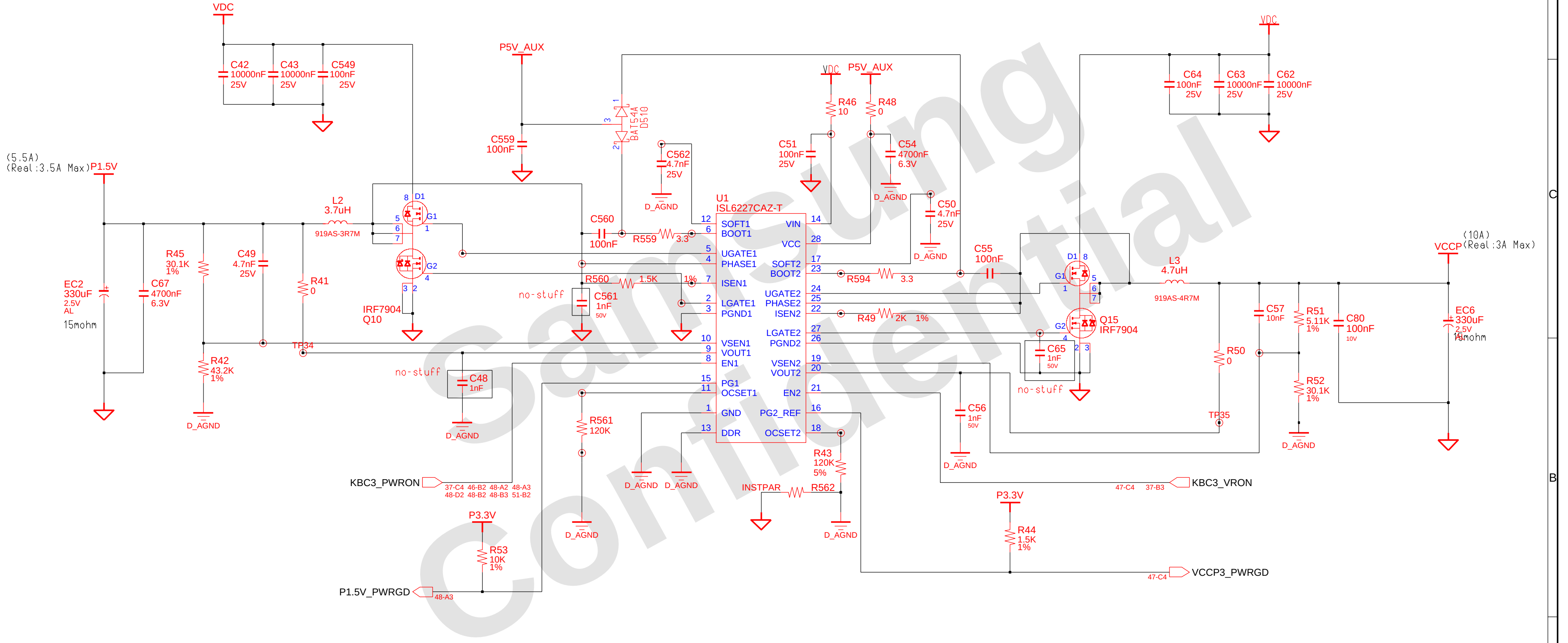
P3.3V_LAN/AUX & P5V_AUX



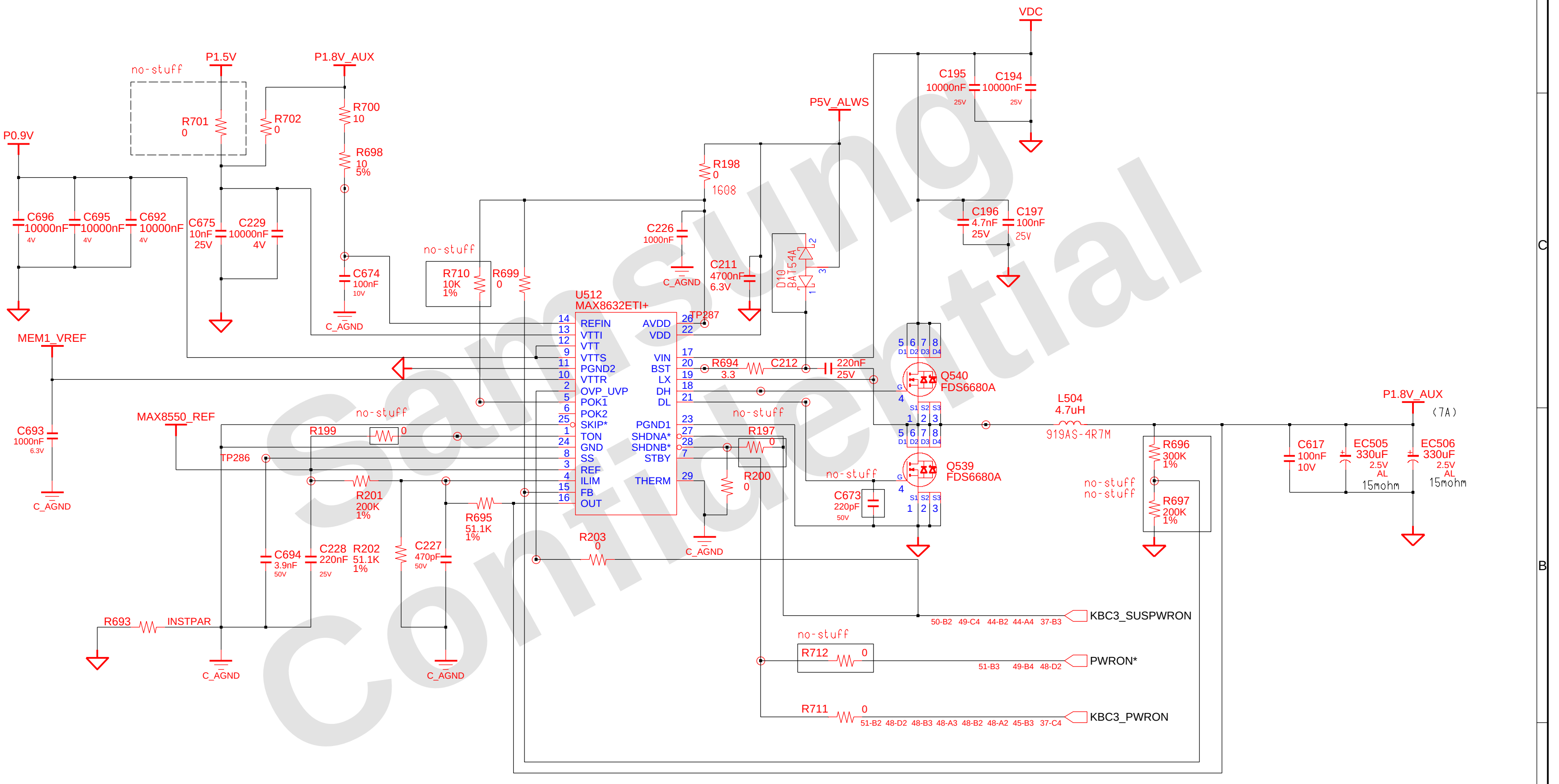
DRAW	YOO, BW	DATE	4/8/2006	TITLE	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	HAINAN C POWER P3.3V LAN & P5V_AUX	
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:19:38 PM	PAGE 41 OF 50	

P1.5V & VCCP (1.05V)



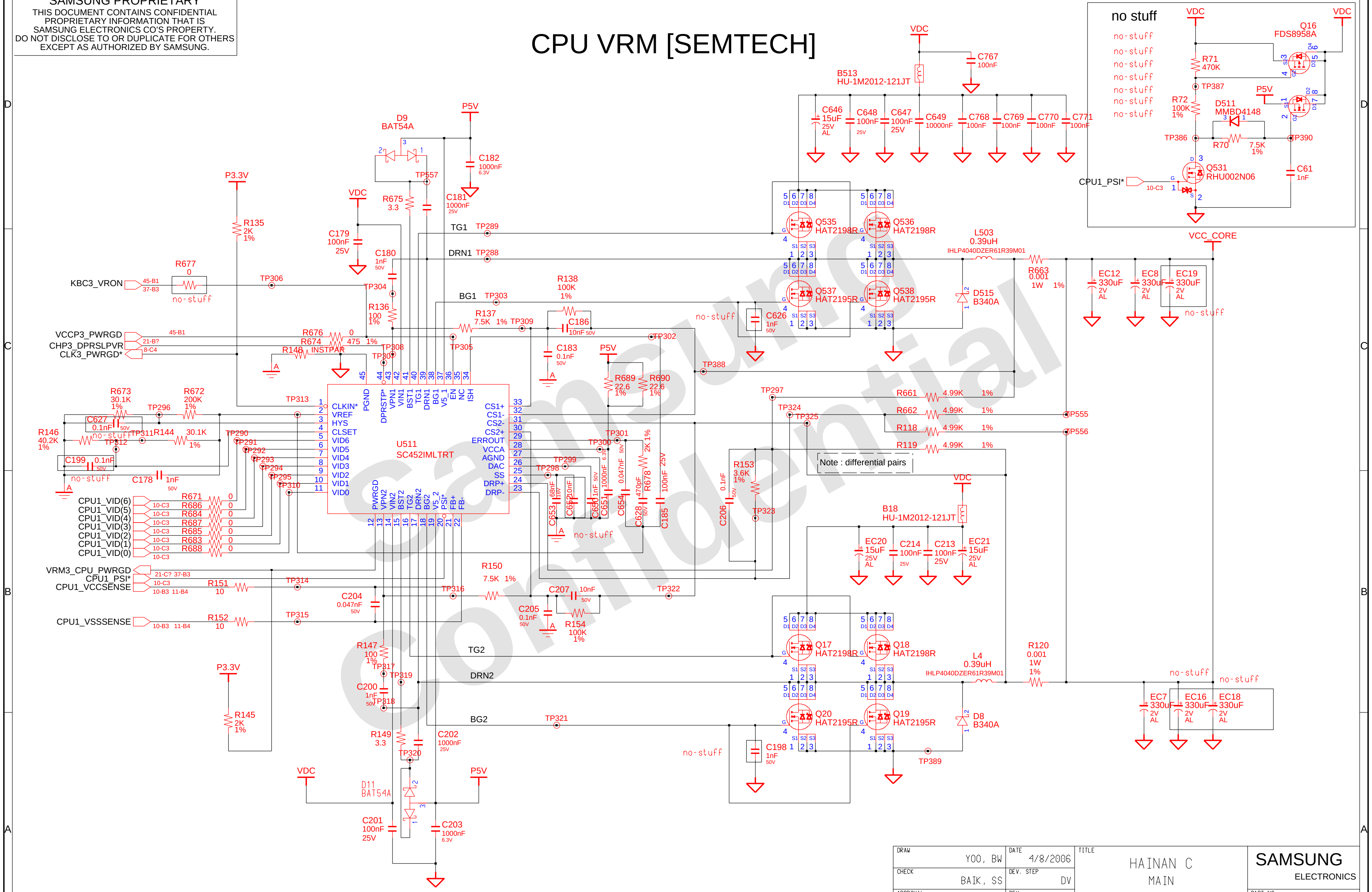
DRAW	YOO, BW	DATE	4/8/2006	TITLE	HAINAN C / POWER / P1.5V & VCCP	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV			PART NO. BA41-#####A
APPROVAL	BIN, KK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:19:58 PM			PAGE 42 OF 50

DDR2 Power



DRAW	YOO, BW	DATE	4/8/2006	TITLE: HAINAN C MAIN DDR2 POWER	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV		PART NO. BA41-#####A
APPROVAL	BIN, KK	REV	1.0		
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:20:19 PM	PAGE 43 OF 50	

CPU VRM [SEMTECH]



DRAW	YOO, BW	DATE	4/8/2006	TITLE	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	HAINAN C	
APPROVAL	BIN, KK	REV	1.0	MAIN	PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:20:30 PM	CPU POWER	PAGE 44 OF 50

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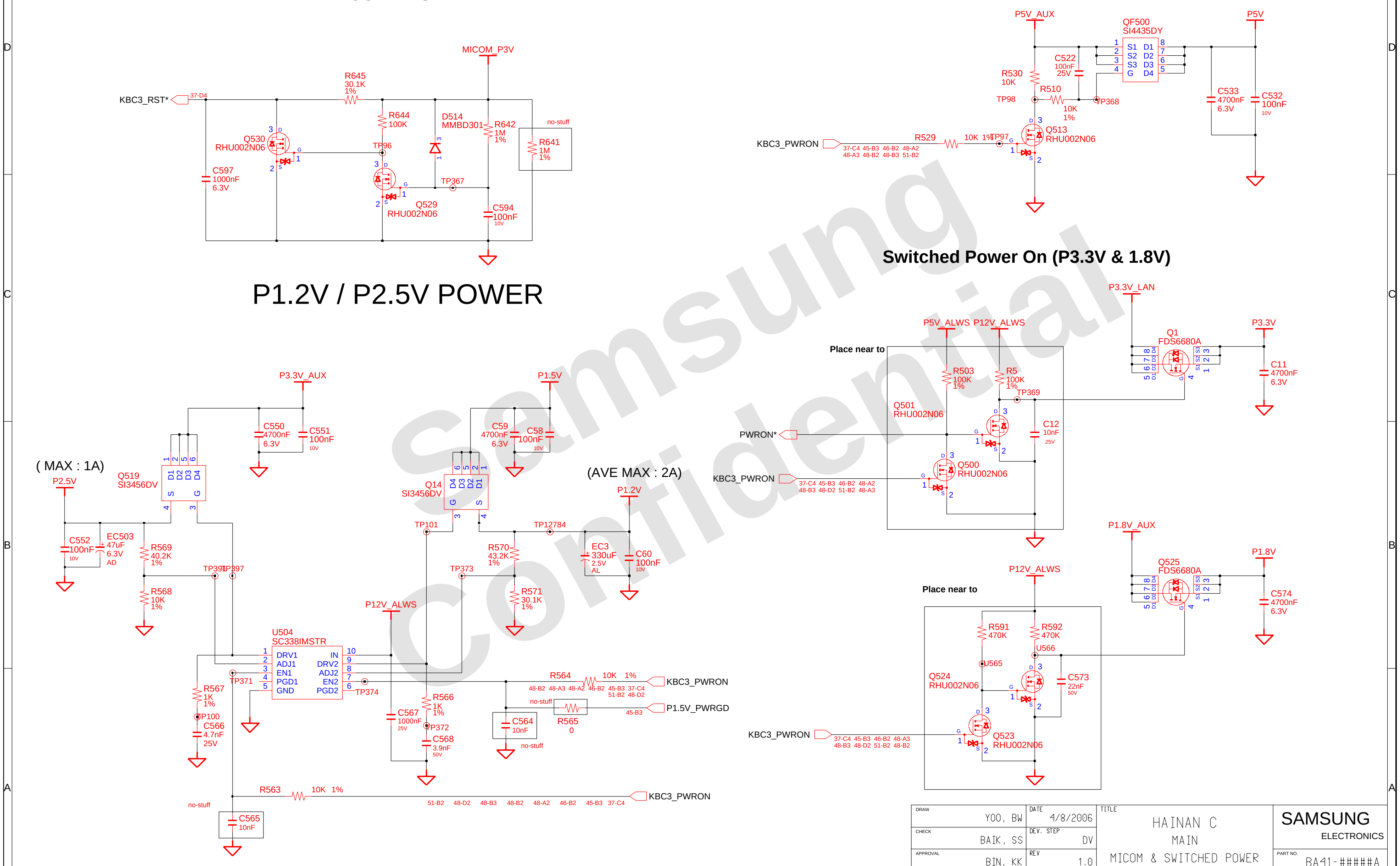
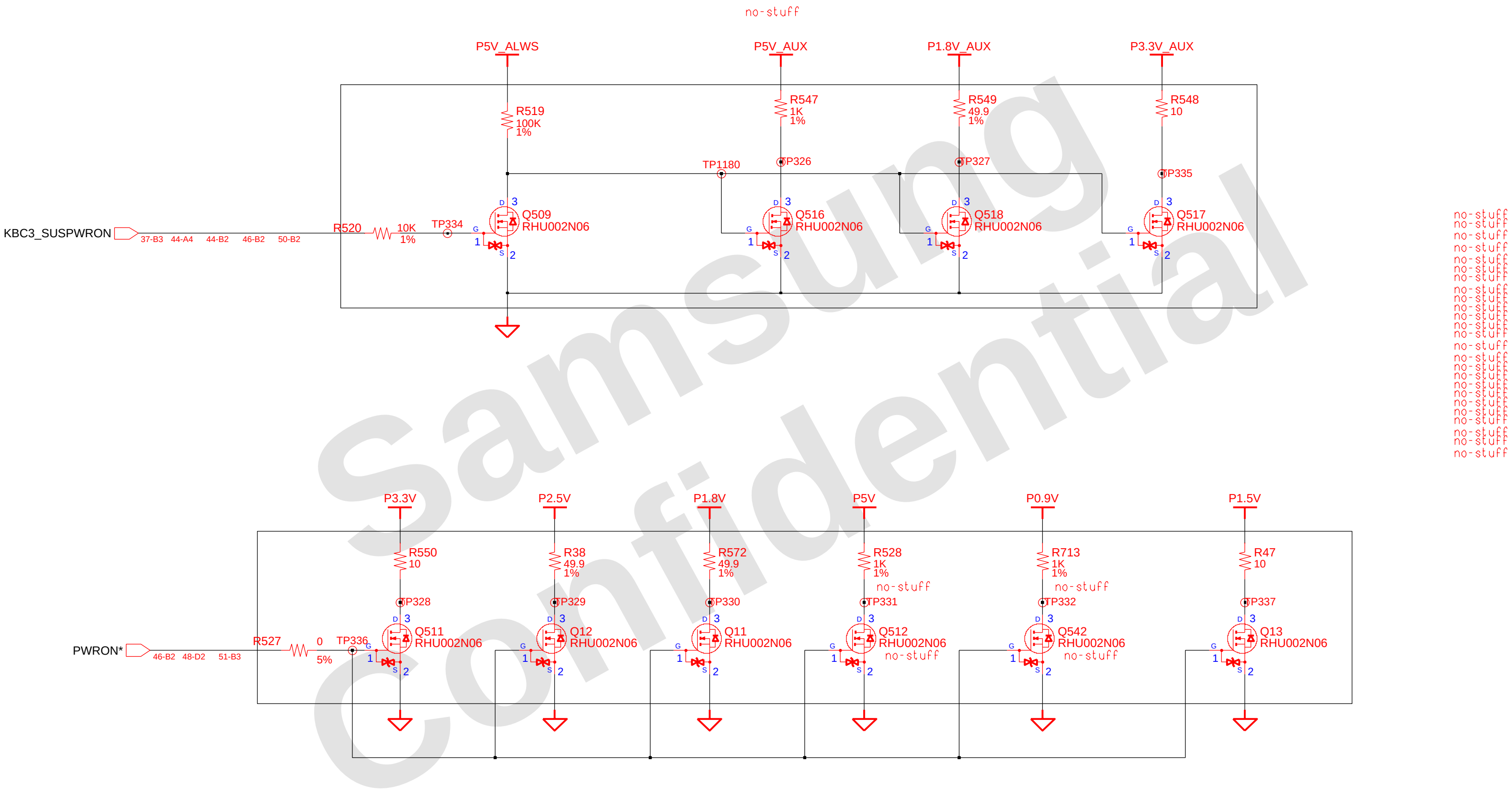


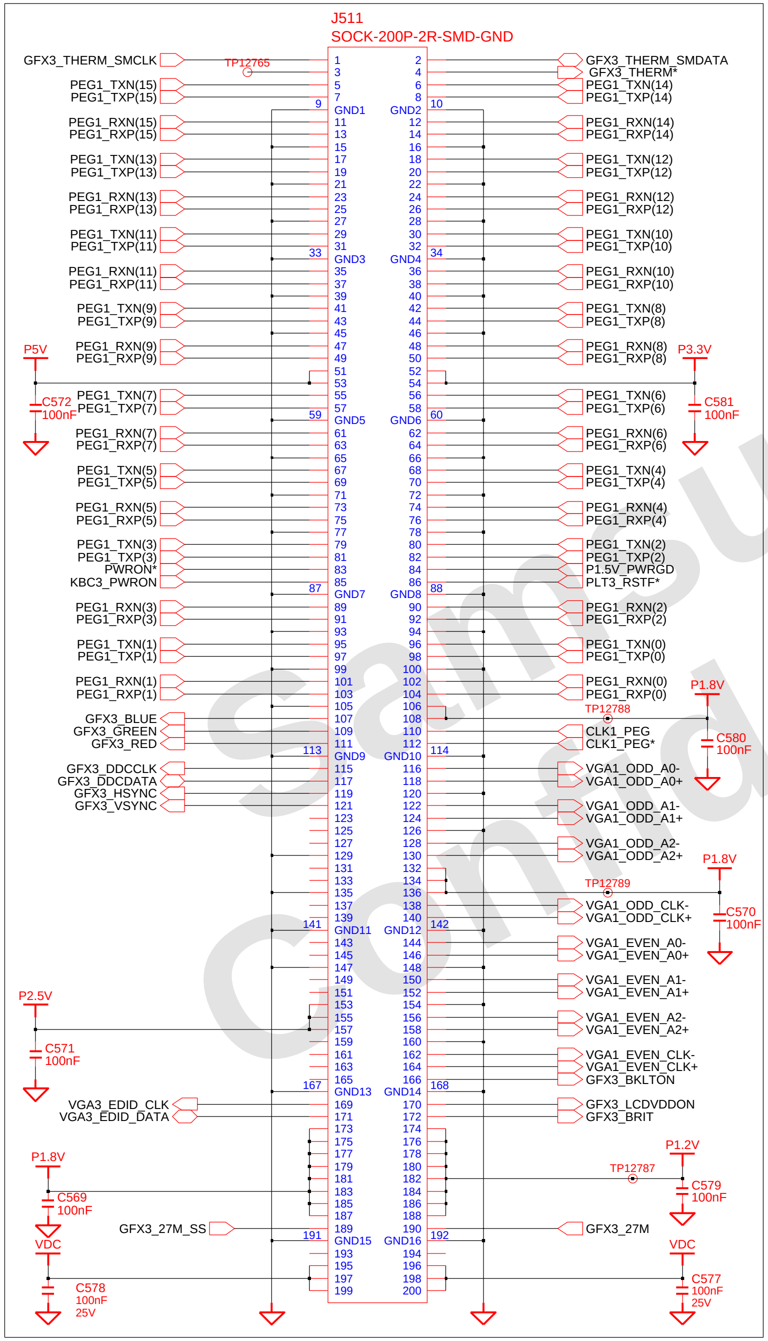
DRAW	YOO, BW	DATE	4/8/2006	TITLE
CHECK	BAIK, SS	DEV. STEP	DV	HAINAN C MAIN
APPROVAL	BIN, KK	REV	1.0	MICOM & SWITCHED POWER
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:20:41 PM	PAGE 45 OF 50

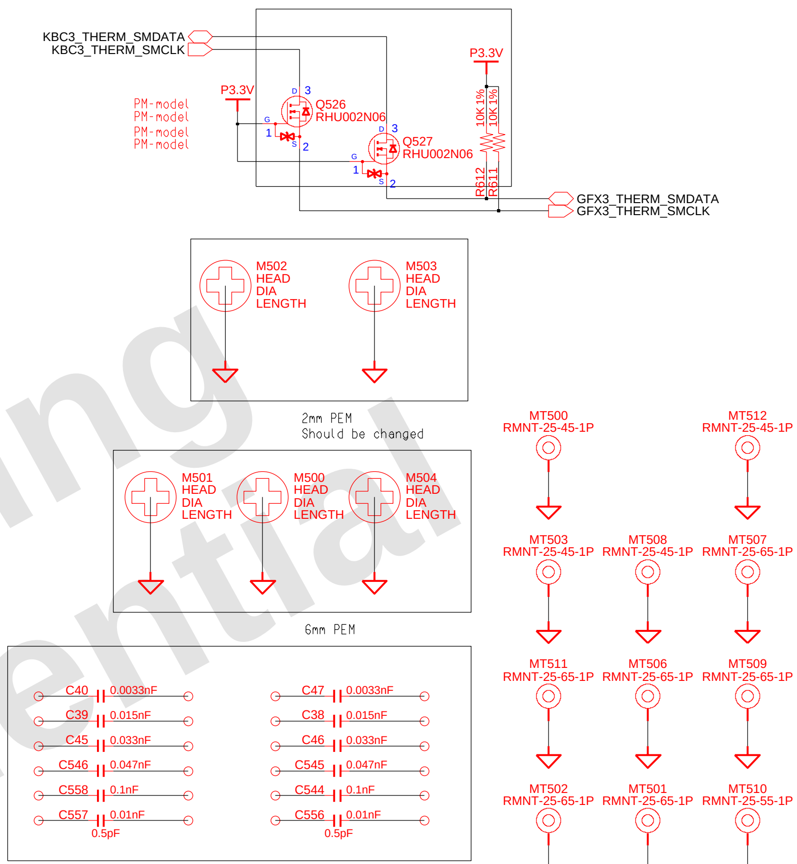
SAMSUNG ELECTRONICS

PART NO. BA41-#####A



DRAW	YOO, BW	DATE	4/8/2006	TITLE	HAINAN C GFX POWER Discharging Logic	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	1.0			PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:20:51 PM			PAGE 46 OF 50





These are for ICT using.

PM-model
PM-model
PM-model
PM-model
PM-model
PM-model
PM-model
PM-model
PM-model
PM-model

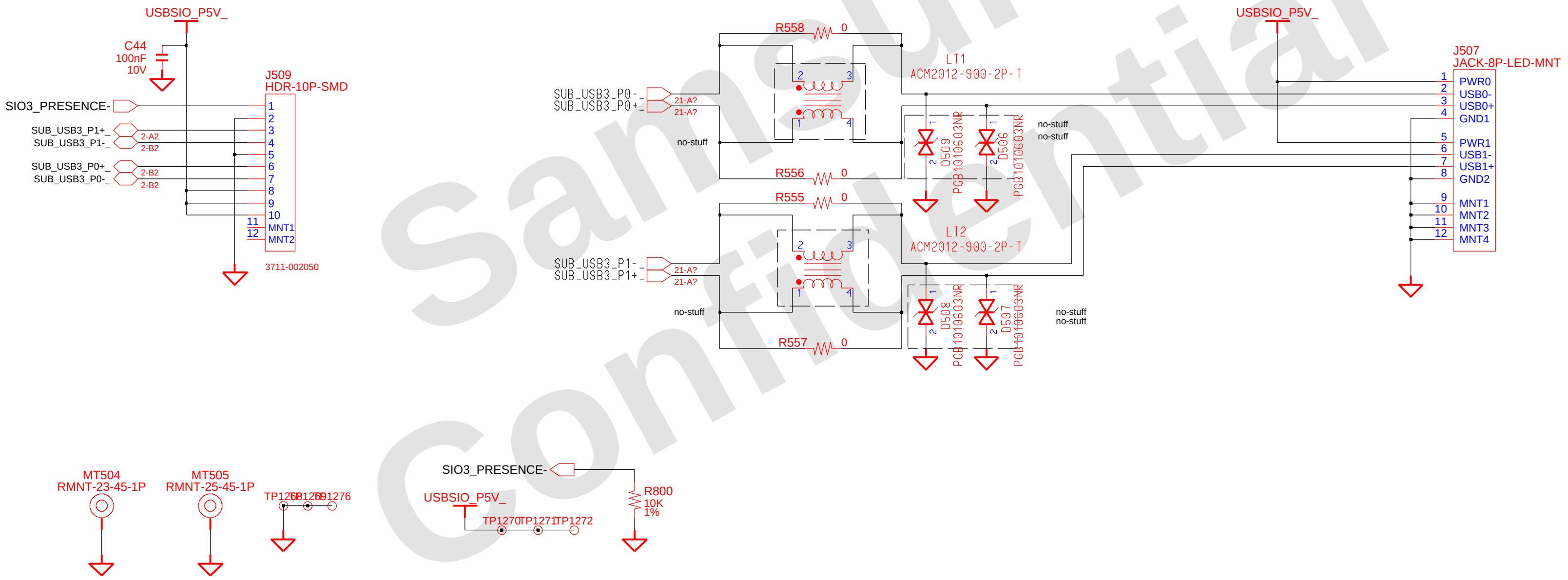
PCB REVISION CONTROL (ICT)

NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW	DATE	TITLE	SAMSUNG ELECTRONICS
YOO, BW	4/8/2006	HAINAN C MAIN	
CHECK BAIK, SS	DEV. STEP DV	Ext GFx connector	PART NO. BA41-#####A
APPROVAL BIN, KK	REV 1.0		
MODULE CODE undefined	LAST EDIT April, 13, 2006 5:21:00 PM		PAGE 47 OF 50

USB & DMB SUBBOARD

USB0, 1 Connector



DRAW	YOO, BW	DATE	4/8/2006	TITLE	HAINAN C POWER USB BOARD	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV			PART NO. BA41-#####A
APPROVAL	BIN, KK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:21:20 PM			PAGE 49 OF 50

TP775 CPU1_VSSSENSE
TP776 CPU2_THERMDA
TP777 CPU2_THERMDC
TP778 CPU3_ALERT*

TP717 HDD3_LED*

TP719 HP_OUT_L
TP720 HP_OUT_R
TP721 IDE5_A0
TP722 IDE5_A1
TP723 IDE5_A2
TP724 IDE5_CS1*
TP725 IDE5_CS3*
TP726 IDE5_D(0)
TP727 IDE5_D(1)
TP728 IDE5_D(10)

TP665 IDE5_D(11)
TP666 IDE5_D(12)
TP667 IDE5_D(13)
TP668 IDE5_D(14)
TP669 IDE5_D(15)
TP670 IDE5_D(2)
TP671 IDE5_D(3)
TP672 IDE5_D(4)
TP673 IDE5_D(5)
TP674 IDE5_D(6)
TP675 IDE5_D(7)
TP676 IDE5_D(8)
TP677 IDE5_D(9)
TP678 IDE5_DACK*
TP679 IDE5_DASP*
TP680 IDE5_DREQ
TP681 IDE5_IDEIRQ
TP682 IDE5_IOR*
TP683 IDE5_IORDY
TP684 IDE5_IOW*
TP685 IDE5_PDIAG*
TP686 ILIM3
TP687 ILIM5

TP690 JCK_SENS_HP
TP691 JCK_SENS_MIC
TP692 KBC3_A20G
TP693 KBC3_BATT_4CELL
TP694 KBC3_BKLTON
TP695 KBC3_BLCKPWRSW*
TP696 KBC3_CAPSLED*
TP634 KBC3_CHGEN
TP635 KBC3_CHKPWRSW*
TP636 KBC3_CPURST*

TP641 KBC3_EXTSMI*
TP642 KBC3_FANCTRL

TP643 KBC3_LANPWRON
TP644 KBC3_LED_ACIN*
TP645 KBC3_LED_CHARGE*
TP646 KBC3_LED_POWER*
TP647 KBC3_NUMLED*

TP649 KBC3_PWRBTN*
TP650 KBC3_PWRGD
TP651 KBC3_PWRON
TP652 KBC3_PWRSW*
TP653 KBC3_RFOFF*
TP654 KBC3_RSMRST*
TP655 KBC3_RST*
TP656 KBC3_RUNSCI*
TP657 KBC3_SCLED*
TP658 KBC3_SMCLK*
TP659 KBC3_SMDATA*
TP660 KBC3_SPKMUTE
TP661 KBC3_SUSPWRON
TP662 KBC3_THERM_SMCLK
TP663 KBC3_THERM_SMDATA
TP664 KBC3_VRON
TP602 KBC3_WAKESCI*

TP606 KBC5_KSI(0)
TP607 KBC5_KSI(1)
TP608 KBC5_KSI(2)
TP609 KBC5_KSI(3)
TP610 KBC5_KSI(4)
TP611 KBC5_KSI(5)
TP612 KBC5_KSI(6)
TP613 KBC5_KSI(7)
TP614 KBC5_KSO(0)
TP615 KBC5_KSO(1)
TP616 KBC5_KSO(10)
TP617 KBC5_KSO(11)
TP618 KBC5_KSO(12)
TP619 KBC5_KSO(13)
TP620 KBC5_KSO(14)
TP621 KBC5_KSO(15)
TP622 KBC5_KSO(2)
TP623 KBC5_KSO(3)
TP624 KBC5_KSO(4)
TP625 KBC5_KSO(5)
TP626 KBC5_KSO(6)
TP627 KBC5_KSO(7)
TP628 KBC5_KSO(8)
TP629 KBC5_KSO(9)
TP630 KBC5_TCLK

TP631 KBC5_TDATA
TP632 LAN3_ACT*

TP597 LAN3_LINK_10*
TP598 LAN3_LINK_100*

TP600 LAN3_WAKE*

TP563 LCD3_BKLTCTRL
TP564 LCD3_BKLTEN
TP565 LCD3_BKLTON
TP566 LCD3_BRIT

TP568 LCD3_EDID_CLK

TP570 LCD3_EDID_DATA
TP571 LCD3_VDDEN
TP572 LID3_SWITCH*
TP573 LPC3_LAD(0)
TP574 LPC3_LAD(1)
TP575 LPC3_LAD(2)
TP576 LPC3_LAD(3)
TP577 LPC3_LFRAME*
TP578 MCH1_HXSWING
TP579 MCH1_HYSWING
TP580 MCH3_BMBUSY*
TP581 MCH3_CFG(10)
TP582 MCH3_CFG(11)
TP583 MCH3_CFG(12)
TP584 MCH3_CFG(13)
TP585 MCH3_CFG(16)
TP586 MCH3_CFG(19)
TP587 MCH3_CFG(20)
TP588 MCH3_CFG(5)
TP589 MCH3_CFG(9)
TP590 MCH3_CLKREQ*
TP591 MCH3_EXTTS0*
TP593 MCH3_ICHSYNC*

TP1156 NUMLED*
TP1157 ODD3_SEL
TP1158 P1.5V_PWRGD
TP1159 PCI3_AD(0)
TP1160 PCI3_AD(1)
TP1161 PCI3_AD(10)
TP1162 PCI3_AD(11)
TP1163 PCI3_AD(12)
TP1164 PCI3_AD(13)
TP1165 PCI3_AD(14)
TP1166 PCI3_AD(15)
TP1167 PCI3_AD(16)
TP1168 PCI3_AD(17)
TP1169 PCI3_AD(18)
TP1170 PCI3_AD(19)
TP1171 PCI3_AD(2)
TP1124 PCI3_AD(20)
TP1125 PCI3_AD(21)
TP1126 PCI3_AD(22)
TP1127 PCI3_AD(23)
TP1128 PCI3_AD(24)
TP1129 PCI3_AD(25)
TP1130 PCI3_AD(26)
TP1131 PCI3_AD(27)
TP1132 PCI3_AD(28)
TP1133 PCI3_AD(29)
TP1134 PCI3_AD(3)
TP1135 PCI3_AD(30)
TP1136 PCI3_AD(31)
TP1137 PCI3_AD(4)
TP1138 PCI3_AD(5)
TP1139 PCI3_AD(6)
TP1140 PCI3_AD(7)
TP1141 PCI3_AD(8)
TP1142 PCI3_AD(9)
TP1143 PCI3_CBE0*
TP1144 PCI3_CBE1*
TP1145 PCI3_CBE2*
TP1146 PCI3_CBE3*
TP1147 PCI3_CLKRUN*
TP1148 PCI3_DEVSEL*
TP1149 PCI3_FRAME*
TP1150 PCI3_GNT0*
TP1151 PCI3_GNT1*
TP1152 PCI3_INTA*
TP1153 PCI3_INTB*
TP1154 PCI3_INTC*
TP1155 PCI3_INTD*
TP1108 PCI3_INTE*
TP1109 PCI3_INTF*
TP1110 PCI3_INTG*
TP1111 PCI3_INTH*
TP1112 PCI3_IRDY*
TP1113 PCI3_PAR
TP1114 PCI3_PERR*
TP1115 PCI3_PLOCK*
TP1116 PCI3_REQ0*
TP1117 PCI3_REQ1*
TP1118 PCI3_REQ2*
TP1119 PCI3_REQ3*
TP1120 PCI3_RST*
TP1121 PCI3_SERR*
TP1122 PCI3_STOP*
TP1123 PCI3_TRDY*

TP947 PEX3_WAKE*
TP948 PLT3_RST*
TP949 PLT3_RSTF*

TP954 PWRON*

TP959 SCLED*

TP972 SMB3_ALERT*
TP973 SMB3_CLK
TP974 SMB3_DATA
TP958 SMB3_LINKALERT*

TP1024 THERM_STP*

TP1032 VCCP3_PWRGD

TP1010 VGA3_BLUE_INT
TP1011 VGA3_DDCCLK
TP1012 VGA3_DDCDATA

TP1015 VGA3_GREEN_INT

TP1017 VGA3_HSYNC
TP1018 VGA3_RED_INT
TP1019 VGA3_VSYNC
TP1020 VRM3_CPU_PWRGD
TP1021 WLON_LED*
TP1022 AD_DC
TP1023 AD_DC
TP1009 AD_DC
TP1008 AD_DC
TP1007 AGND_AUD
TP1006 AGND_AUD
TP1005 AGND_AUD
TP1004 AGND_AUD
TP1003 AGND_P3.3V
TP1002 AGND_P3.3V
TP1001 AGND_P3.3V

TP1090 AGND_P3.3V
TP1091 AMP_VDD

TP1092 AVDD
TP1093 AVDD

TP1094 CB_MD_VCC

TP1095 CB_VCCA

TP1096 CB_VPPA
TP1097 CGND
TP1098 CGND
TP1099 CGND
TP1100 CGND
TP1101 CHG_REF
TP1102 CHG_REF
TP1103 CHG_REF
TP1104 CHG_REF
TP1105 C_AGND
TP1106 C_AGND
TP1107 C_AGND
TP975 C_AGND
TP976 C_GROUND
TP977 C_GROUND
TP978 C_GROUND
TP979 C_GROUND
TP980 GROUND
TP981 GROUND
TP982 GROUND
TP983 GROUND
TP984 INV_VDC
TP985 INV_VDC
TP986 INV_VDC
TP987 INV_VDC
TP988 LCD_VDD3V
TP989 LCD_VDD3V
TP990 LCD_VDD3V
TP991 LCD_VDD3V
TP1179 GROUND
TP1178 GROUND
TP1177 GROUND

TP996 MICOM_P3V
TP997 MICOM_P3V
TP998 P0.9V
TP999 P0.9V
TP1000 P0.9V
TP995 P0.9V

TP1069 P1.5V
TP1070 P1.5V
TP1071 P1.5V
TP1072 P1.5V

TP1074 P1.5V_PCIE
TP1075 P1.5V_PCIE
TP1076 P1.5V_PCIE

TP1077 P1.5V_PCIE
TP1078 P1.8V_AUX
TP1079 P1.8V_AUX
TP1080 P1.8V_AUX
TP1081 P1.8V_AUX
TP1082 P12V_ALWS
TP1083 P12V_ALWS
TP1084 P12V_ALWS
TP1085 P12V_ALWS
TP1086 P2.5V
TP1087 P2.5V
TP1088 P2.5V
TP1089 P2.5V

TP1046 P3.3V_AUX
TP1047 P3.3V_AUX
TP1048 P3.3V_AUX
TP1049 P3.3V_AUX

TP1052 P3.3V_LAN
TP1053 P3.3V_LAN
TP1054 P5V
TP1055 P5V
TP1056 P5V
TP1057 P5V
TP1058 P5V_ALWS
TP1059 P5V_ALWS
TP1060 P5V_ALWS
TP1061 P5V_ALWS
TP1062 P5V_AUX

TP1063 P5V_AUX

TP1064 PRTC_BAT
TP1065 PRTC_BAT

TP1033 VBATT
TP1034 VBATT
TP1035 VBATT
TP1036 VBATT
TP1037 VCCP
TP1038 VCCP
TP1039 VCCP
TP1040 VCCP
TP1041 VCC_CRT
TP1042 VCC_CRT
TP1043 VCC_CRT
TP1044 VCC_CRT

TP1183 GROUND
TP1182 GROUND
TP1181 GROUND
TP1186 GROUND
TP1185 GROUND
TP1184 GROUND
TP1189 GROUND
TP1188 GROUND
TP1187 GROUND

TP912 AUD3_PCBEEP

TP914 AUD5_LINE_OUT_L
TP915 AUD5_LINE_OUT_R

TP918 AUD5_SPK_L+
TP919 AUD5_SPK_L-
TP920 AUD5_SPK_R+
TP921 AUD5_SPK_R-
TP922 BAT3_DETECT*
TP923 BAT3_SMCLK*
TP924 BAT3_SMDATA*
TP925 BAT3_VOLTA
TP926 BLT_DETECT*

TP928 BUF5_PLT_RSTF*
TP929 CAPSLED*
TP930 CBS3_A_A_18
TP931 CBS3_A_A_19
TP932 CBS3_A_D_14
TP933 CBS3_A_D_2
TP934 CBS3_CAD(0)
TP935 CBS3_CAD(1)
TP936 CBS3_CAD(10)
TP937 CBS3_CAD(11)
TP938 CBS3_CAD(12)
TP939 CBS3_CAD(13)
TP940 CBS3_CAD(14)
TP941 CBS3_CAD(15)
TP879 CBS3_CAD(16)
TP880 CBS3_CAD(17)
TP881 CBS3_CAD(18)
TP882 CBS3_CAD(19)
TP883 CBS3_CAD(2)
TP884 CBS3_CAD(20)
TP885 CBS3_CAD(21)
TP886 CBS3_CAD(22)
TP887 CBS3_CAD(23)
TP888 CBS3_CAD(24)
TP889 CBS3_CAD(25)
TP890 CBS3_CAD(26)
TP891 CBS3_CAD(27)
TP892 CBS3_CAD(28)
TP893 CBS3_CAD(29)
TP894 CBS3_CAD(3)
TP895 CBS3_CAD(30)
TP896 CBS3_CAD(31)
TP897 CBS3_CAD(4)
TP898 CBS3_CAD(5)
TP899 CBS3_CAD(6)
TP900 CBS3_CAD(7)
TP901 CBS3_CAD(8)
TP902 CBS3_CAD(9)
TP903 CBS3_CAUDIO
TP904 CBS3_CCBE0*
TP905 CBS3_CCBE1*
TP906 CBS3_CCBE2*
TP907 CBS3_CCBE3*
TP908 CBS3_CCD1*
TP909 CBS3_CCD2*
TP910 CBS3_CCLK
TP847 CBS3_CCLKRUN*
TP848 CBS3_CDEVSEL*
TP849 CBS3_CFRAME*
TP850 CBS3_CGNT*
TP851 CBS3_CINT*
TP852 CBS3_CIRDY*
TP853 CBS3_CPAR
TP854 CBS3_CPERR*
TP855 CBS3_CREQ*
TP856 CBS3_CRST*
TP857 CBS3_CSERR*
TP858 CBS3_CSTOP*
TP859 CBS3_CSTSCHG
TP860 CBS3_CTRDY*
TP861 CBS3_CVS1
TP862 CBS3_CVS2

TP863 CBS3_MD_CLK
TP864 CBS3_MD_DATA0_MS_SDIO
TP865 CBS3_MD_DATA1
TP866 CBS3_MD_DATA2
TP867 CBS3_MD_DATA3
TP868 CBS3_MD_DATA4_XD
TP869 CBS3_MD_DATA5_XD
TP870 CBS3_MD_DATA6_XD
TP871 CBS3_MD_DATA7_XD
TP872 CBS3_MD_VCCEN
TP873 CBS3_MD_XD_ALE
TP874 CBS3_MD_XD_CE*
TP875 CBS3_MD_XD_CLE
TP876 CBS3_MD_XD_WP*
TP877 CBS3_MS_BS_SD_CMD
TP878 CBS3_MS_INS*_XD_CD*
TP819 CBS3_SD_CD_XD_CD*
TP820 CBS3_SD_WP*_XD_R_B*
TP821 CBS3_SPKR
TP822 CBS3_VCC3EN*
TP823 CBS3_VCC5EN*
TP824 CBS3_VPPEN0
TP825 CBS3_VPPEN1

TP826 CHG5_LDO
TP827 CHP3_1394_ROMW*
TP828 CHP3_AZ_AUD_BCLK
TP829 CHP3_AZ_AUD_RST*
TP830 CHP3_AZ_AUD_SDO
TP831 CHP3_AZ_AUD_SYNC
TP832 CHP3_AZ_MDC_BCLK
TP833 CHP3_AZ_MDC_RST*
TP834 CHP3_AZ_MDC_SDO
TP835 CHP3_AZ_MDC_SYNC
TP836 CHP3_AZ_SDI0
TP837 CHP3_AZ_SDI1

TP840 CHP3_CAPSLED*
TP841 CHP3_DPRSLPVR

TP843 CHP3_LDRQ0*
TP844 CHP3_LDRQ1*
TP845 CHP3_NUMLED*
TP846 CHP3_PCISTP*
TP808 CHP3_SATACLKREQ*
TP809 CHP3_SATALED*
TP810 CHP3_SATA_DET*
TP811 CHP3_SCLED*
TP812 CHP3_SERIRQ
TP813 CHP3_SLPS4*
TP814 CHP3_SLPS5*
TP815 CHP3_SMLINK0
TP816 CHP3_SMLINK1
TP817 CHP3_SPKR
TP818 CHP3_WKON_LAN_D

TP942 MIC1
TP943 MIC2
TP944 MINIPCIE3_CLKREQ*
TP945 MIO3_BUTTON*
TP946 MIO_INT_BTN*

TP791 CLK3_DBGLPC
TP792 CLK3_FM48
TP793 CLK3_ICH14
TP794 CLK3_PCLKCB

TP796 CLK3_PCLKICH
TP797 CLK3_PCLKLAN
TP798 CLK3_PCLKMICOM

TP801 CLK3_PWRGD*

TP803 CLK3_SMBCLK
TP804 CLK3_SMBDATA
TP805 CLK3_USB48
TP806 COEX1
TP807 COEX2

DRAW	YOO, BW	DATE	4/8/2006	TITLE HAINAN C POWER TP	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV		
APPROVAL	BIN, KK	REV	1.0		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:21:38 PM		PAGE 50 OF 50

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EXT GFx

CPU :
Chip Set : NVIDIA 7X series
Remarks :

Model Name	: HABANA EXT GFx
PBA Name	:
PCB Code	:
Dev. Step	: MP
Revision	: 1.0
T.R. Date	: 2005.11.14

DRAW	CHECK	APPROVAL
SE LEE	ES CHO	BL LEE

DRAW	DATE	TITLE	SAMSUNG ELECTRONICS
LEE, SE	11/14/2005	HABANA EXT GFX COVER	
CHECK: CHO, ES	DEV. STEP: MP		
APPROVAL: LEE, BL	REV: 1.0		PART NO. BA41-00545A
MODULE CODE	LAST EDIT: November 14, 2005 10:24:53 PM	PAGE 1 OF 12	

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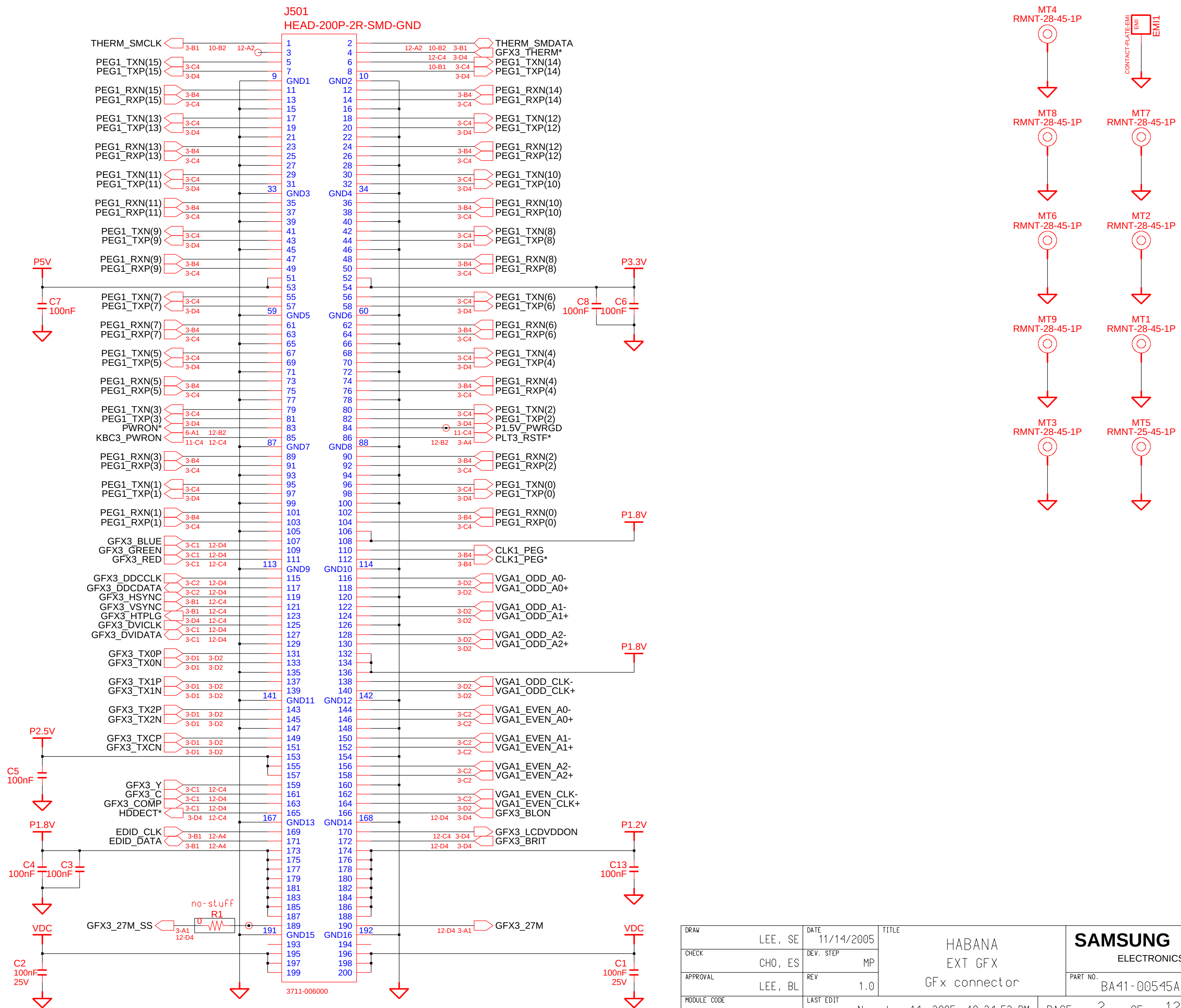

DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA
CHECK	CHO, ES	DEV. STEP	MP		EXT GFX
APPROVAL	LEE, BL	REV	1.0		GFx connector
MODULE CODE		LAST EDIT	November 14, 2005 10:24:53 PM	PAGE 2 OF 12	PART NO. BA41-00545A

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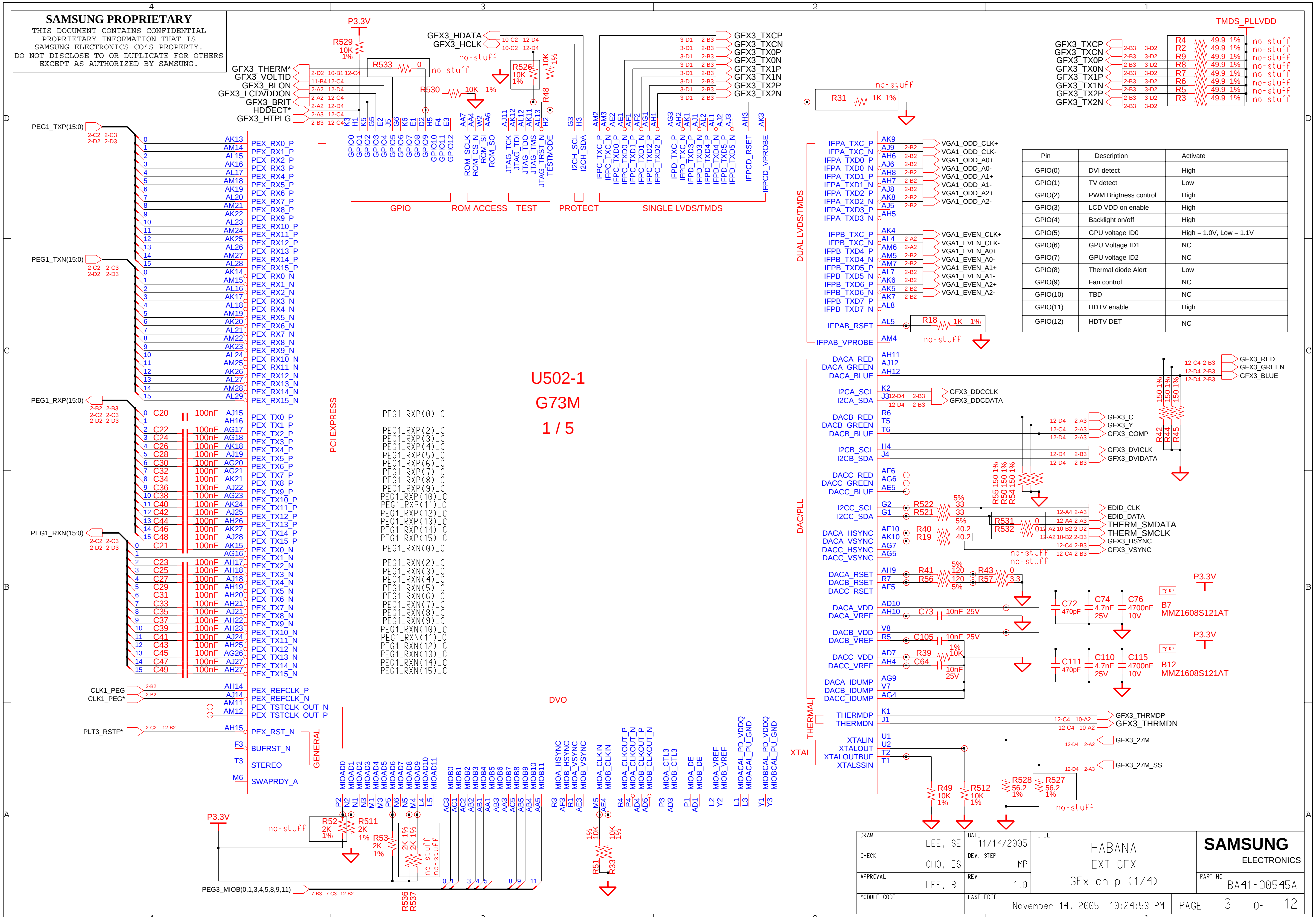

Pin	Description	Activate
GPIO(0)	DVI detect	High
GPIO(1)	TV detect	Low
GPIO(2)	PWM Brigtness control	High
GPIO(3)	LCD VDD on enable	High
GPIO(4)	Backlight on/off	High
GPIO(5)	GPU voltage ID0	High = 1.0V, Low = 1.1V
GPIO(6)	GPU Voltage ID1	NC
GPIO(7)	GPU voltage ID2	NC
GPIO(8)	Thermal diode Alert	Low
GPIO(9)	Fan control	NC
GPIO(10)	TBD	NC
GPIO(11)	HDTV enable	High
GPIO(12)	HDTV DET	NC

DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA
CHECK	CHO, ES	DEV. STEP	MP		EXT GFX
APPROVAL	LEE, BL	REV	1.0		GFx chip (1/4)
MODULE CODE		LAST EDIT	November 14, 2005 10:24:53 PM	PAGE	3 OF 12

SAMSUNG ELECTRONICS
PART NO. BA41-00545A

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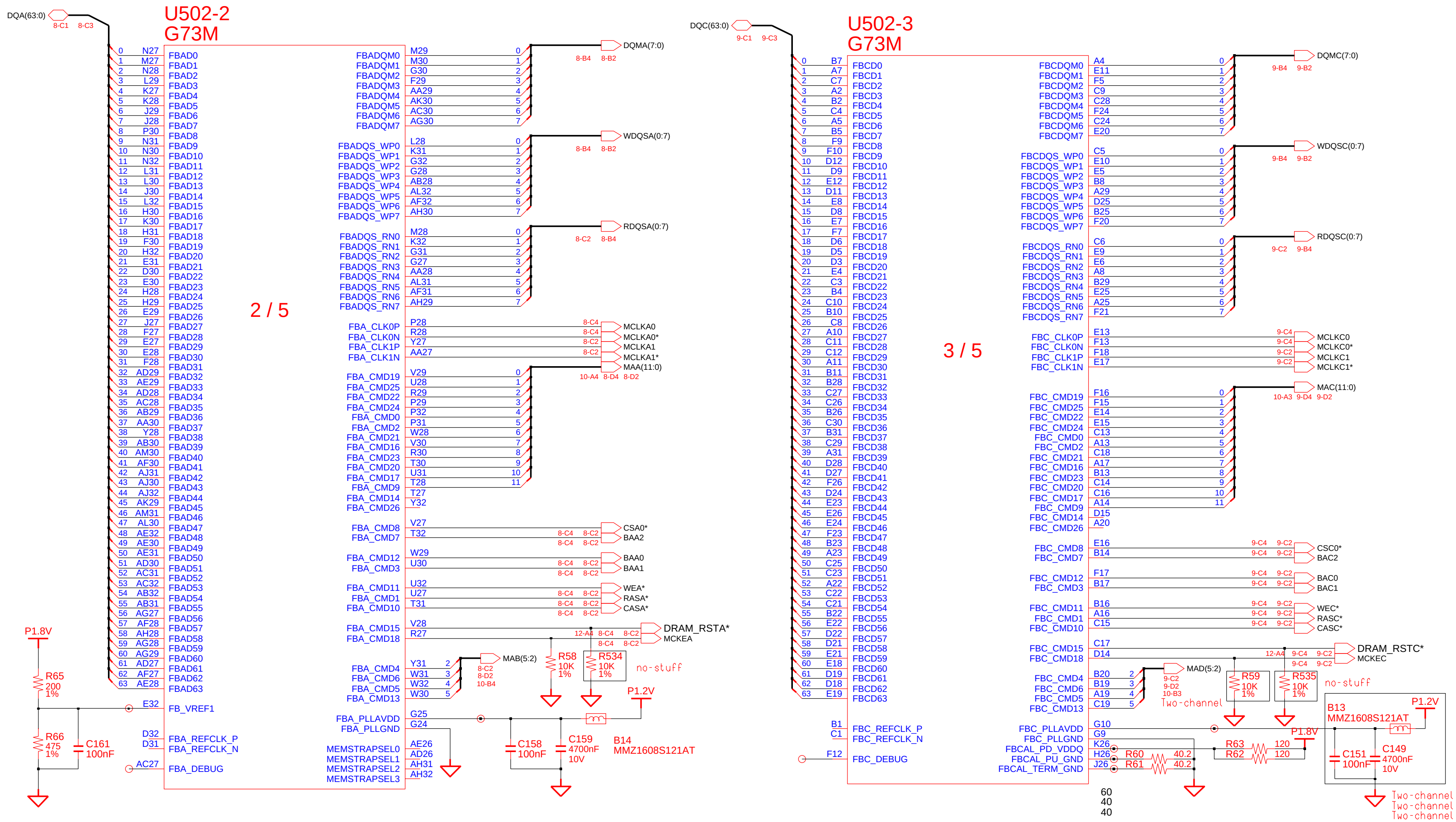
Graphic Memory I/F (Using FBA Channel)

Graphic Memory I/F (Using FBC Channel)



DRAW	LEE, SE	DATE 11/14/2005	TITLE HABANA EXT GFX GFx chip (2/4)	SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP MP		
APPROVAL	LEE, BL	REV 1.0		PART NO. BA41-00545A
MODULE CODE		LAST EDIT November 14, 2005 10:24:53 PM		PAGE 4 OF 12

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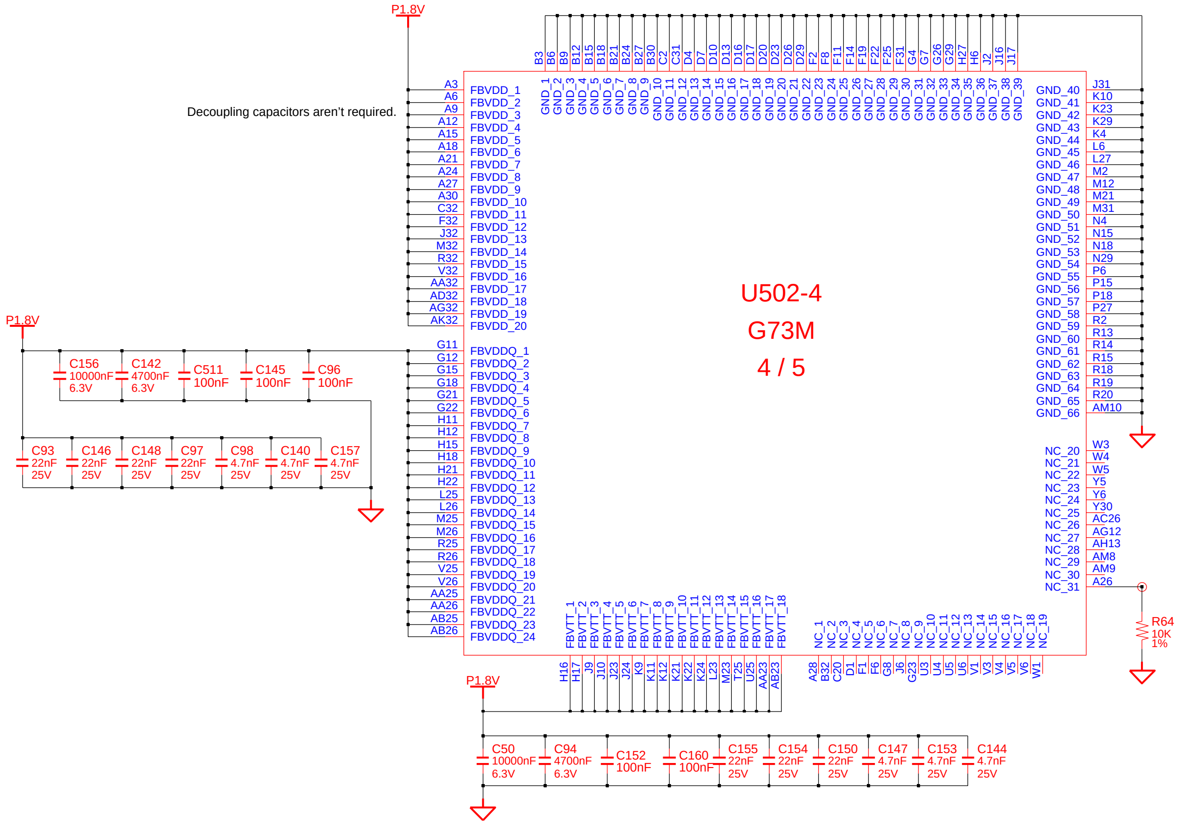

DRAW: LEE, SE	DATE: 11/14/2005	TITLE: HABANA EXT GFX GFx chip (3/4)	SAMSUNG ELECTRONICS
CHECK: CHO, ES	DEV. STEP: MP		
APPROVAL: LEE, BL	REV: 1.0		PART NO. BA41-00545A
MODULE CODE	LAST EDIT: November 14, 2005 10:24:53 PM		PAGE 5 OF 12

COM-22C-015(1996.6.5) REV. 3

d:/users/mobile16/mentor/habana/graphic/gfx_nvidia_mp10

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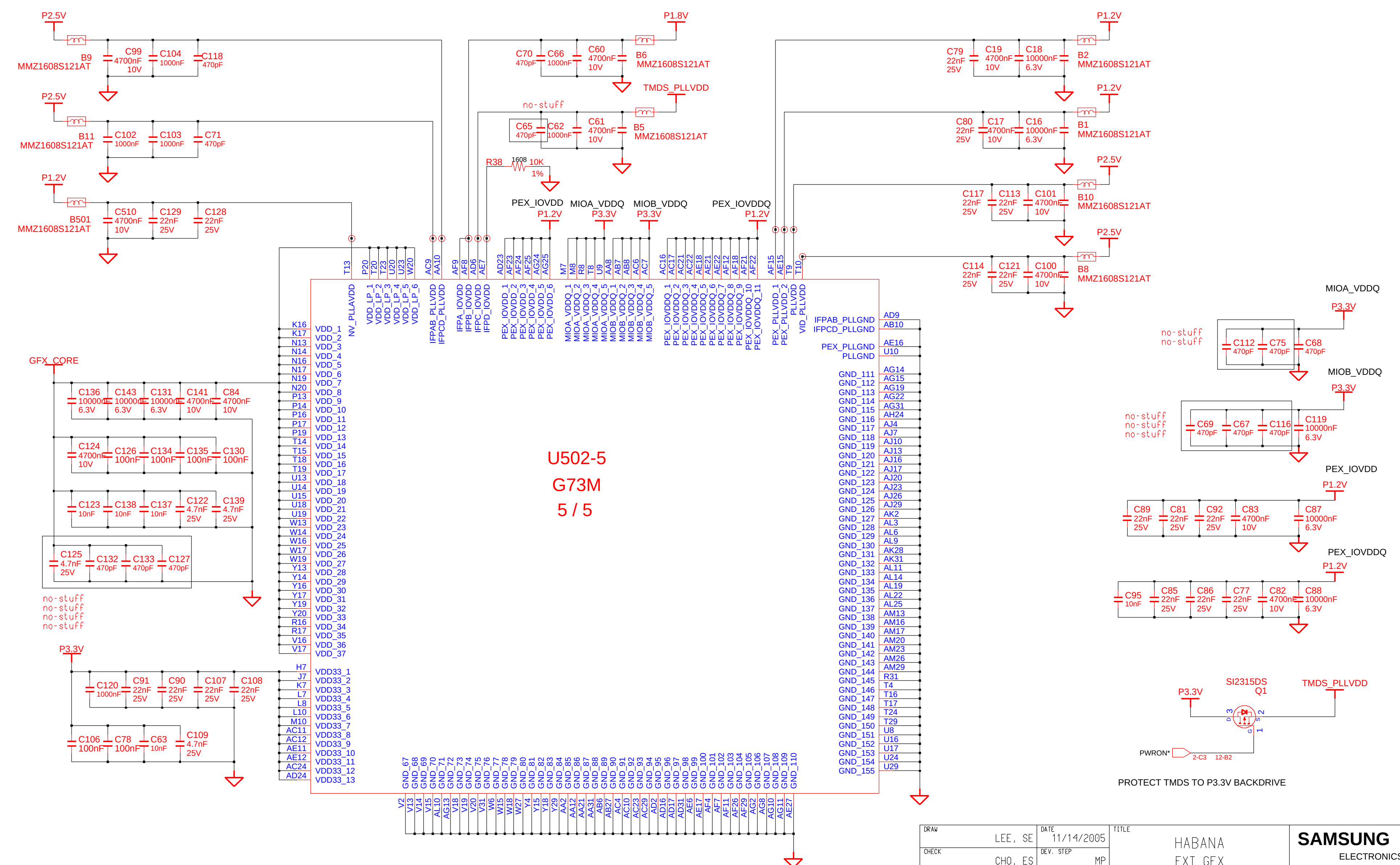
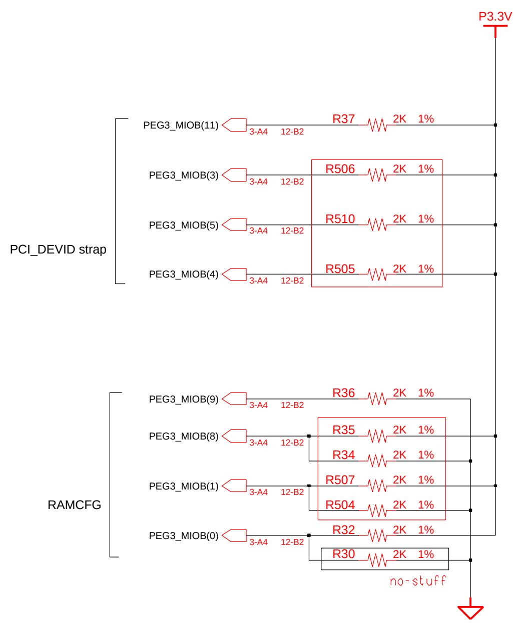


DRAW	DATE	TITLE	
LEE, SE	11/14/2005	HABANA	SAMSUNG ELECTRONICS
CHECK CHO, ES	DEV. STEP MP	EXT GFX	
APPROVAL LEE, BL	REV 1.0	GFx chip (4/4)	PART NO. BA41-00545A
MODULE CODE	LAST EDIT November 14, 2005 10:24:53 PM	PAGE 6 OF 12	

	R37	R506	R510	R505
72M-V	no-stuff	stuff	stuff	stuff
72M	stuff	no-stuff	no-stuff	no-stuff
73M	stuff	no-stuff	no-stuff	no-stuff

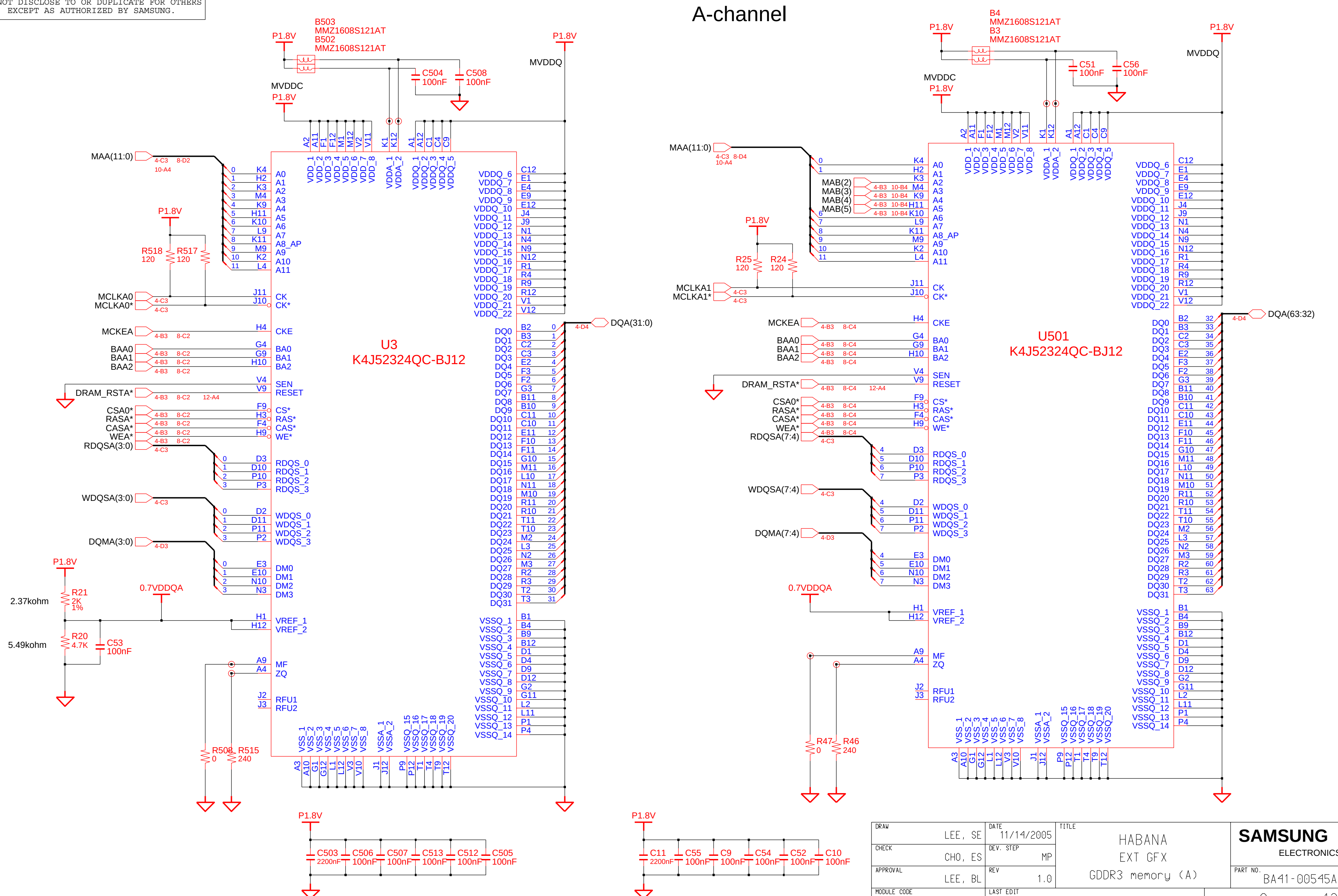
	R35	R34	R507	R504
SS 256Mb	stuff	no-stuff	stuff	no-stuff
INF 256Mb	stuff	no-stuff	no-stuff	stuff
SS 512Mb	no-stuff	stuff	stuff	no-stuff
INF 512Mb	no-stuff	stuff	no-stuff	stuff



Straps	Pin # (Rev.A02)	Descriptions
SUB_VENDOR	MIOAD(1)	0 : No BIOS 1 : Read from BIOS(Default)
RAMCFG(3:0) [9,8,1,0]	MIOB(9) MIOB(8) MIOB(1) MIOB(0)	0111 : samsung GDDR3 256Mbit 0101 : infineon GDDR3 256Mbit 0011 : samsung GDDR3 512Mbit 0001 : infineon GDDR3 512Mbit
CRYSTAL(1:0)	MIOB(2) MIOB(6)	01 : 14.318 MHz 10 : 27 MHz (Default) 11 : Unknown 00 : 13.5 MHz
TV_MODE(1:0)	MIOAD(7) MIOAD(10)	00 : SECAM 01 : NTSC (Default) 10 : PAL 11 : CRT
PCI_DEVID(3:0) [11,3,5,4]	MIOB(11) MIOB(3) MIOB(5) MIOB(4)	72M : 0X01D8 72M-V : 0X01D7 73M : 0X0398
ROM_TYPE(1:0)	MIOB(10) MIOBVSYNC	No ROM (NC)
USER STRAP	MIOAD(2:5)	EDID

DRAW	DATE	TITLE	
LEE, SE	11/14/2005	HABANA	SAMSUNG ELECTRONICS
CHECK: CHO, ES	DEV. STEP: MP	EXT GFX	
APPROVAL: LEE, BL	REV: 1.0	GFx strap option	PART NO. BA41-00545A
MODULE CODE	LAST EDIT: November 14, 2005 10:24:53 PM	PAGE 7 OF 12	

A-channel



DRAW: LEE, SE	DATE: 11/14/2005	TITLE: HABANA EXT GFX GDDR3 memory (A)	SAMSUNG ELECTRONICS
CHECK: CHO, ES	DEV. STEP: MP		
APPROVAL: LEE, BL	REV: 1.0		PART NO. BA41-00545A
MODULE CODE	LAST EDIT: November 14, 2005 10:24:53 PM	PAGE 8 OF 12	

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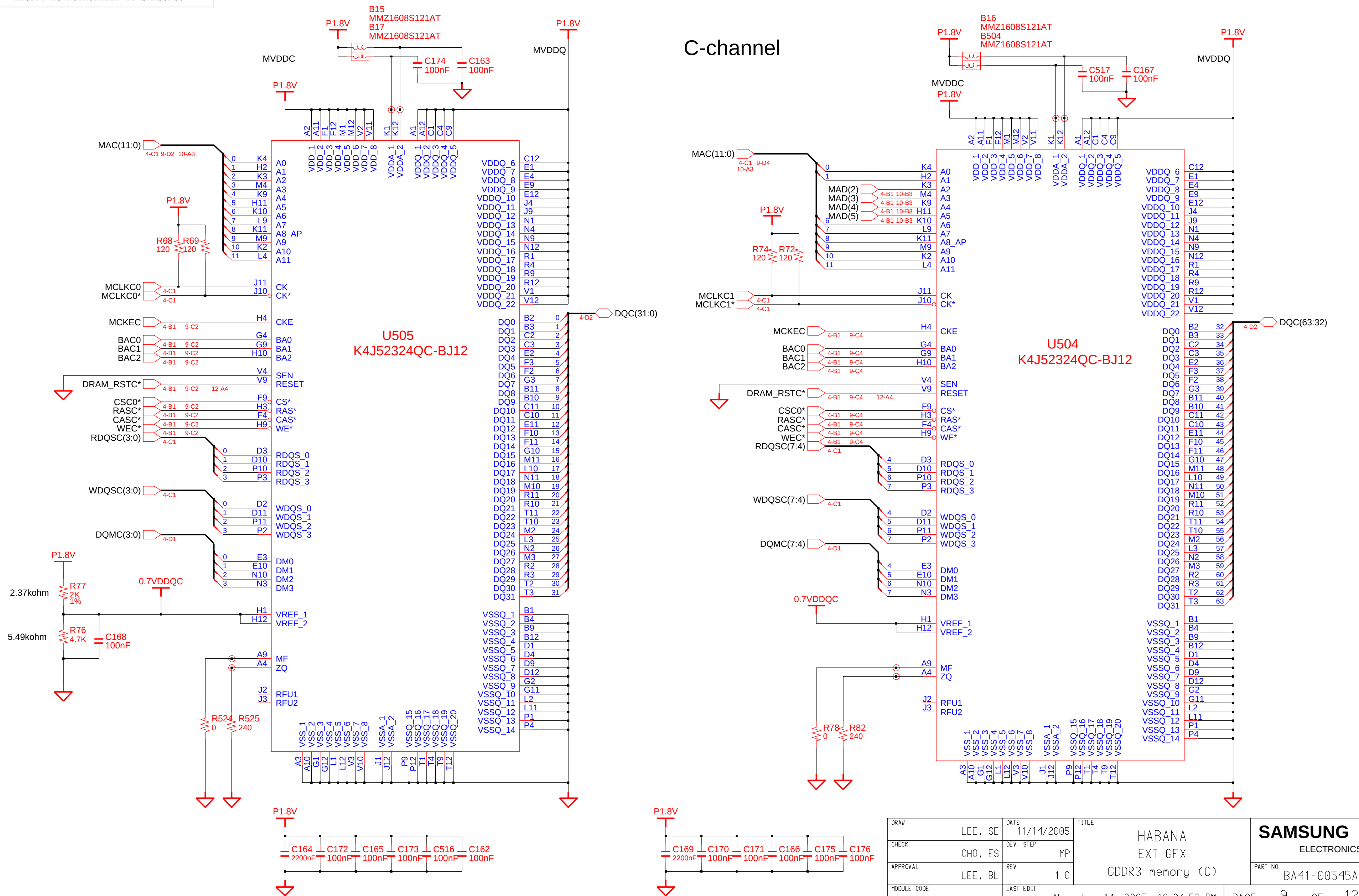
This page is for "2channel-model".

C-channel



DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX GDDR3 memory (C)	SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP			
APPROVAL	LEE, BL	REV	1.0			PART NO. BA41-00545A
MODULE CODE		LAST EDIT	November 14, 2005 10:24:53 PM			PAGE 9 OF 12

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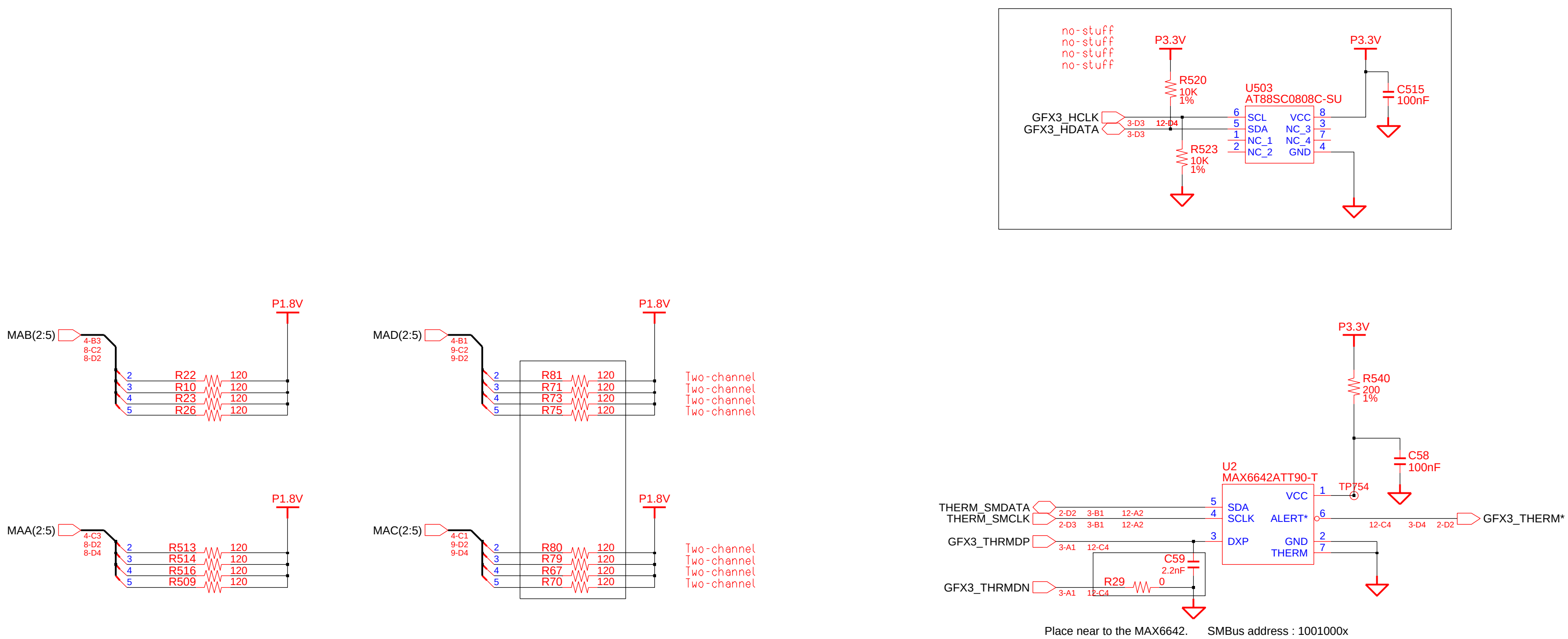
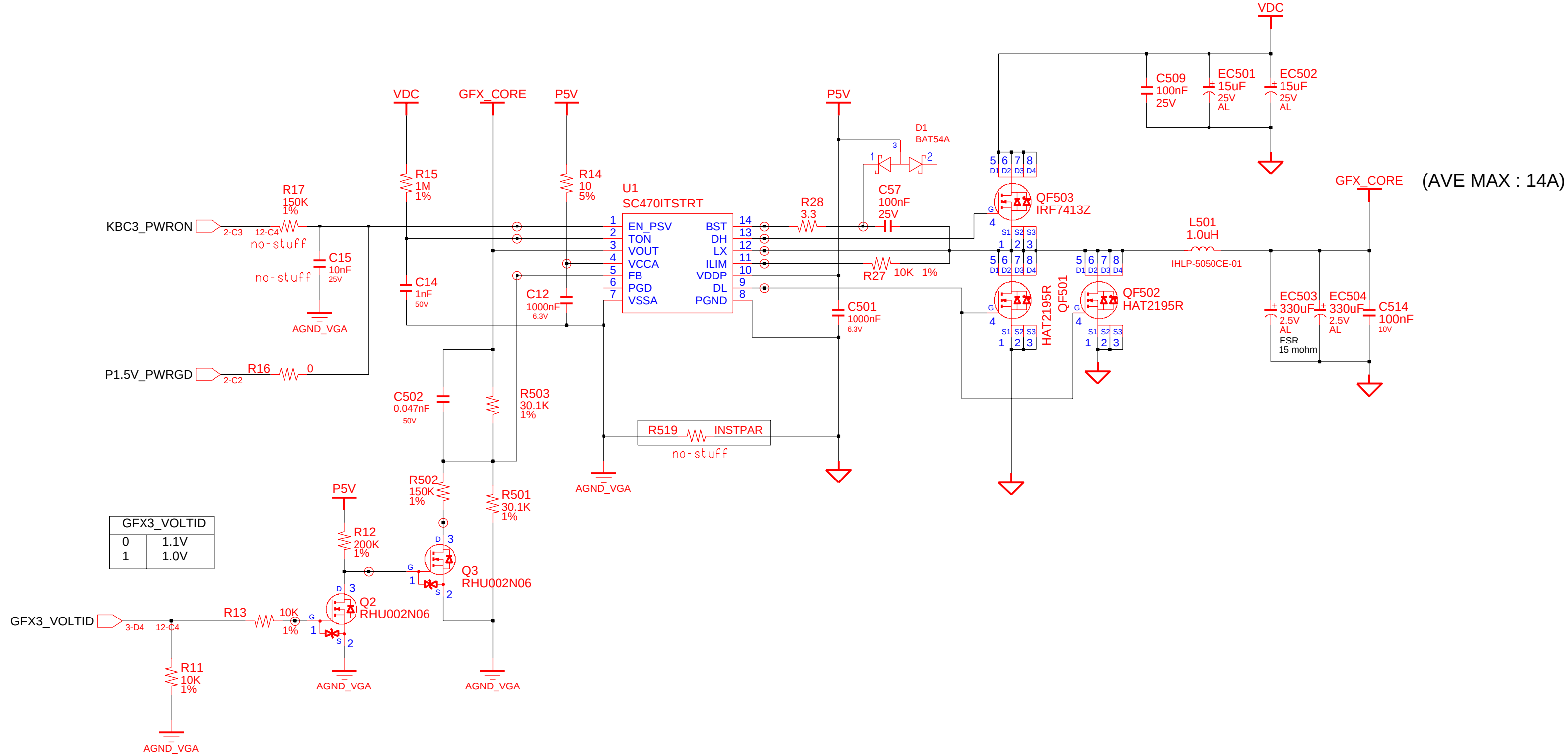


DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX GDDR3 Term. Thermal sensor	SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP			
APPROVAL	LEE, BL	REV	1.0			PART NO. BA41-00545A
MODULE CODE		LAST EDIT	November 14, 2005 10:24:53 PM		PAGE 10 OF 12	

Graphic Core Power



GFX3_VOLTID	
0	1.1V
1	1.0V

DRAW	LEE, SE	DATE	11/14/2005	TITLE
CHECK	CHO, ES	DEV. STEP	MP	HABANA EXT GFX
APPROVAL	LEE, BL	REV	1.0	GFx core Regulator
MODULE CODE		LAST EDIT	November 14, 2005 10:24:53 PM	

SAMSUNG ELECTRONICS
PART NO. BA41-00545A

GFX3_27M
GFX3_27M_SS
GFX3_BLON
GFX3_BLUE
GFX3_BRIT
GFX3_C
GFX3_COMP
GFX3_DDCCLK
GFX3_DDCDATA
GFX3_DVICLK
GFX3_DVIDATA
GFX3_GREEN
GFX3_HCLK
GFX3_HDATA
GFX3_HSYNC
GFX3_HTPLG
GFX3_LCDVDDON
GFX3_RED
GFX3_THERM*
GFX3_THRMDN
GFX3_THRMDP
GFX3_VOLTID
GFX3_VSYNC
GFX3_Y
HDDECT*
KBC3_PWRON

DRAM_RSTA*
DRAM_RSTC*
EDID_CLK
EDID_DATA

PEG3_MIOB(0)
PEG3_MIOB(1)
PEG3_MIOB(11)
PEG3_MIOB(3)
PEG3_MIOB(4)
PEG3_MIOB(5)
PEG3_MIOB(8)
PEG3_MIOB(9)
PLT3_RSTF*
PWRON*

THERM_SMCLK
THERM_SMDATA

P5V
P5V
P5V
P5V
TMDS_PLLVDD
TMDS_PLLVDD

VDC
VDC
VDC
VDC
VDC

0.7VDDQA
0.7VDDQA

0.7VDDQC
0.7VDDQC

AGND_VGA
AGND_VGA

GFX_CORE
GFX_CORE
GFX_CORE
GFX_CORE
GFX_CORE
GROUND
GROUND
GROUND
GROUND
GROUND
P1.2V
P1.2V
P1.2V
P1.2V
P1.2V
P1.8V
P1.8V
P1.8V
P1.8V
P1.8V
P2.5V
P2.5V
P2.5V
P2.5V
P2.5V
P3.3V
P3.3V
P3.3V
P3.3V
P3.3V
P5V

DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA	SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP		EXT GFX	
APPROVAL	LEE, BL	REV	1.0		GDDR3 Term. Thermal sensor	PART NO. BA41-00545A
MODULE CODE		LAST EDIT	November 14, 2005 10:24:53 PM			PAGE 12 OF 12