

SAMOA(DDR3)

CPU : PENRYN SFF
Chip Set : CANTIGA GS & ICH9M SFF
Remarks : INTEL MONTEVINA SFF

Model Name : SAMOA
PCB Part No : BA41-00905A(Nanya)
BA41-00906A(GCE)
Dev. Step : PR/MP
Revision : 1.1
T.R. Date :

DRAW	CHECK	APPROVAL
Jun PARK	HJ KIM	JS EUH

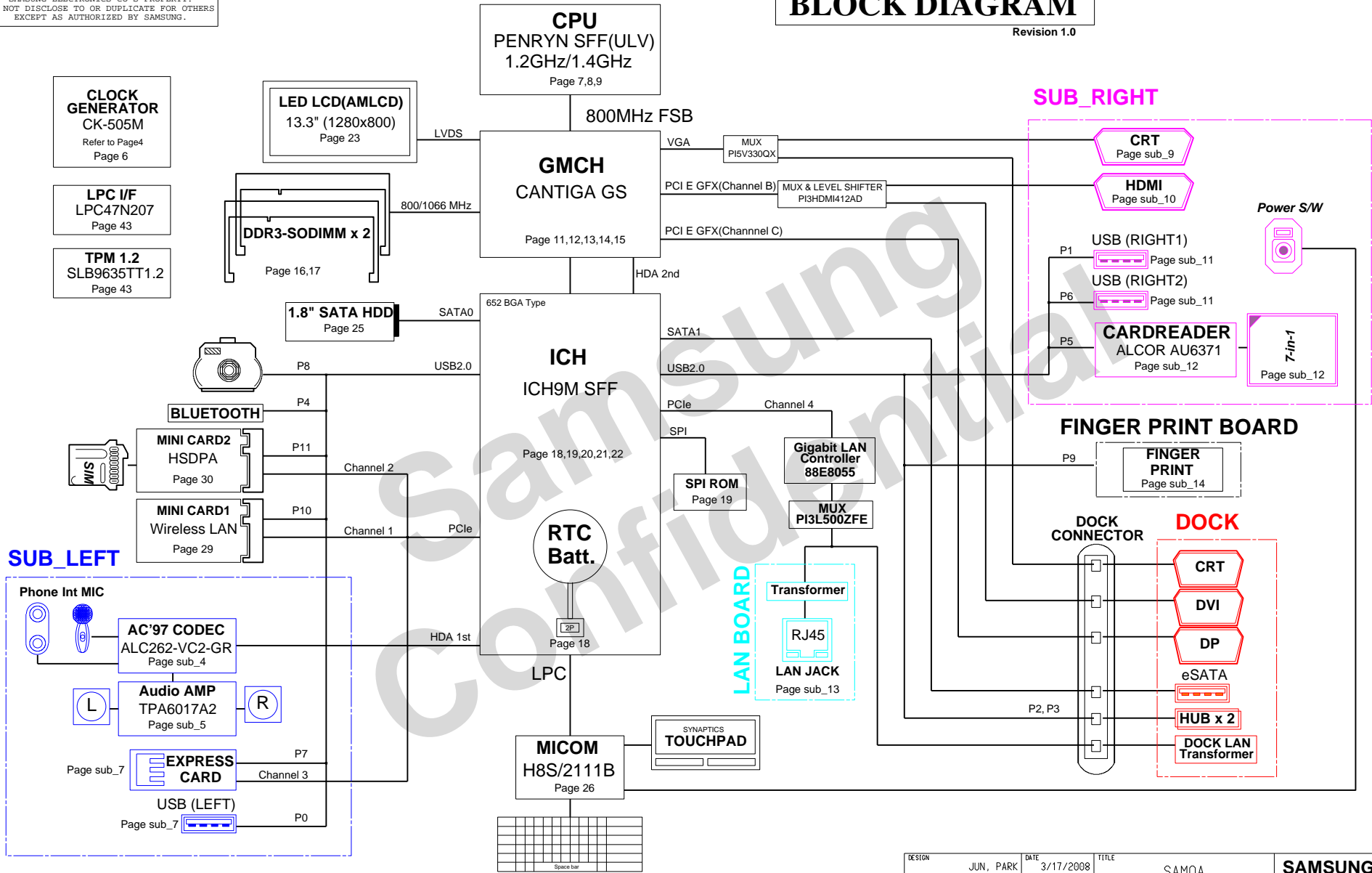
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DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN COVER	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1			PART NO: BA41-0XXXXA
MODULE CODE		LAST EDIT	August 22, 2008 10:40:53 AM	PAGE	1	OF 44

BLOCK DIAGRAM

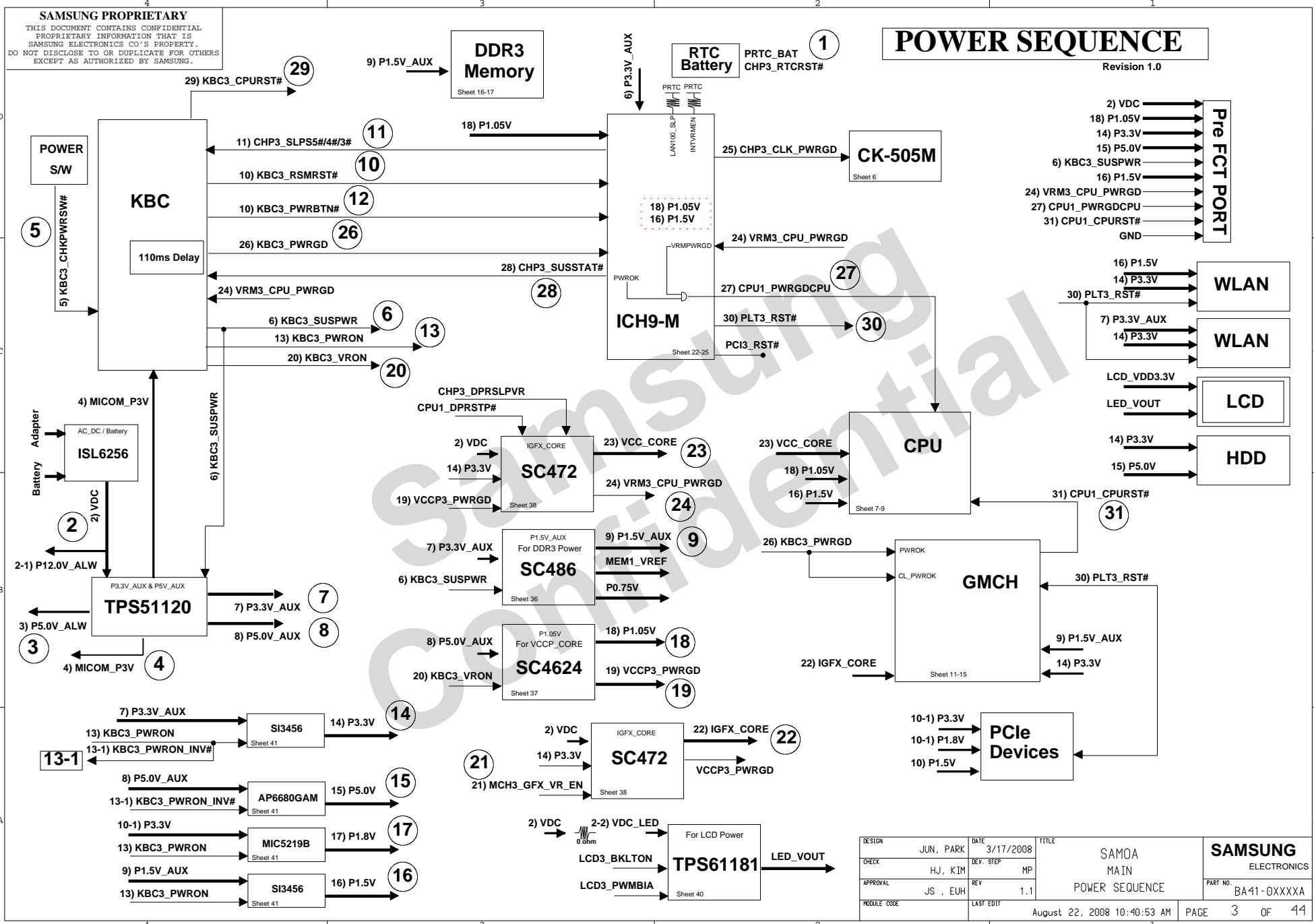
Revision 1.0



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS PART NO: BA41-0XXXXA
CHECK	HJ, KIM	DEV. STEP	MP	BLOCK DIAGRAM		
APPROVAL	JS, EUH	REV	1.1			
MODULE CODE		LAST EDIT	August 22, 2008 10:40:53 AM	PAGE	2 OF 44	

POWER SEQUENCE

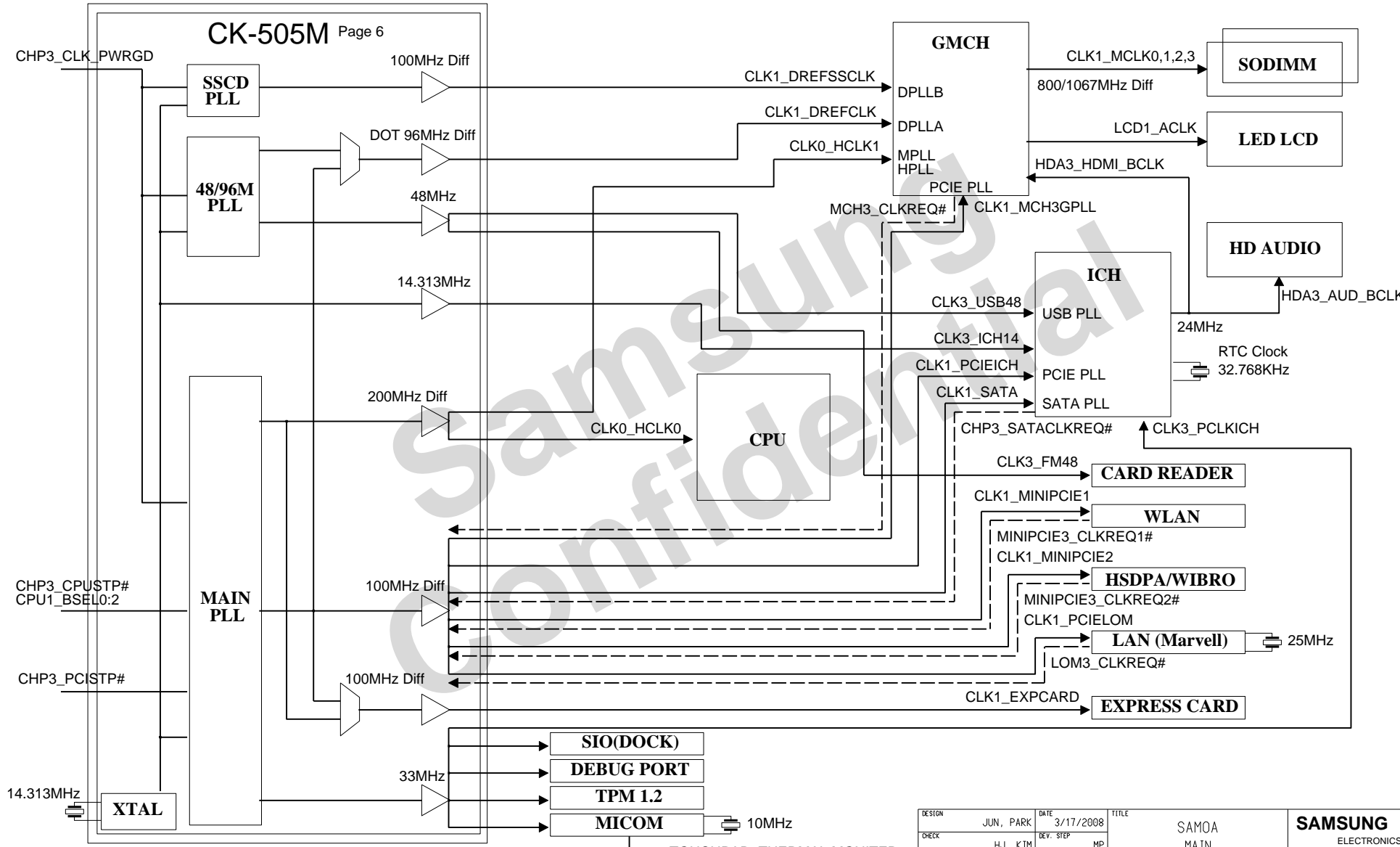
Revision 1.0



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN POWER SEQUENCE	SAMSUNG ELECTRONICS PART NO: BA41-0XXXXA
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1			
MODULE CODE		LAST EDIT	August 22, 2008 10:40:53 AM	PAGE	3 OF 44	

CLOCK DISTRIBUTION

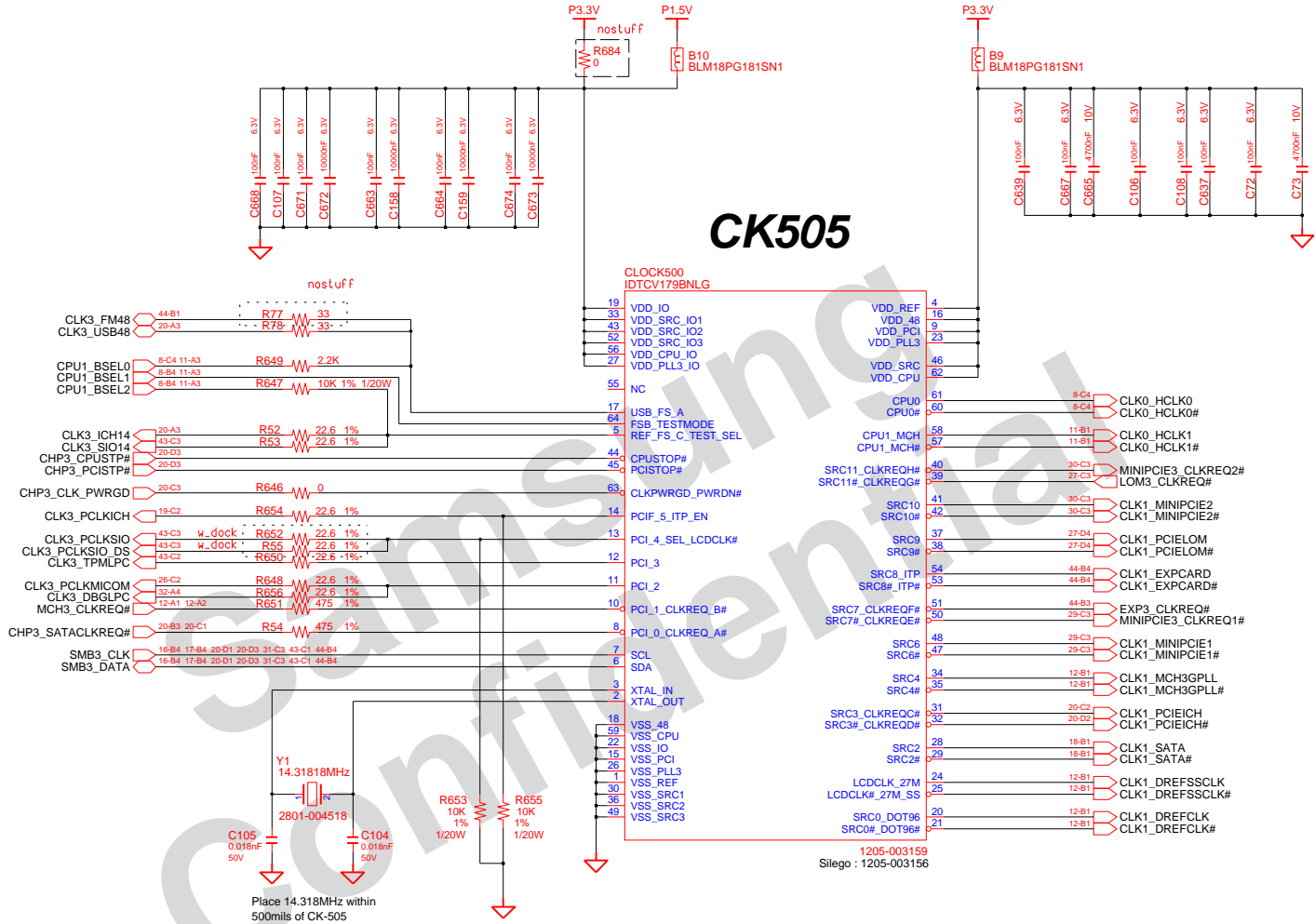
Revision 1.0



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	CLOCK DISTRIBUTION		
APPROVAL	JS, EUH	REV	1.1	August 22, 2008 10:40:53 AM		PART NO. BA41-0XXXXA
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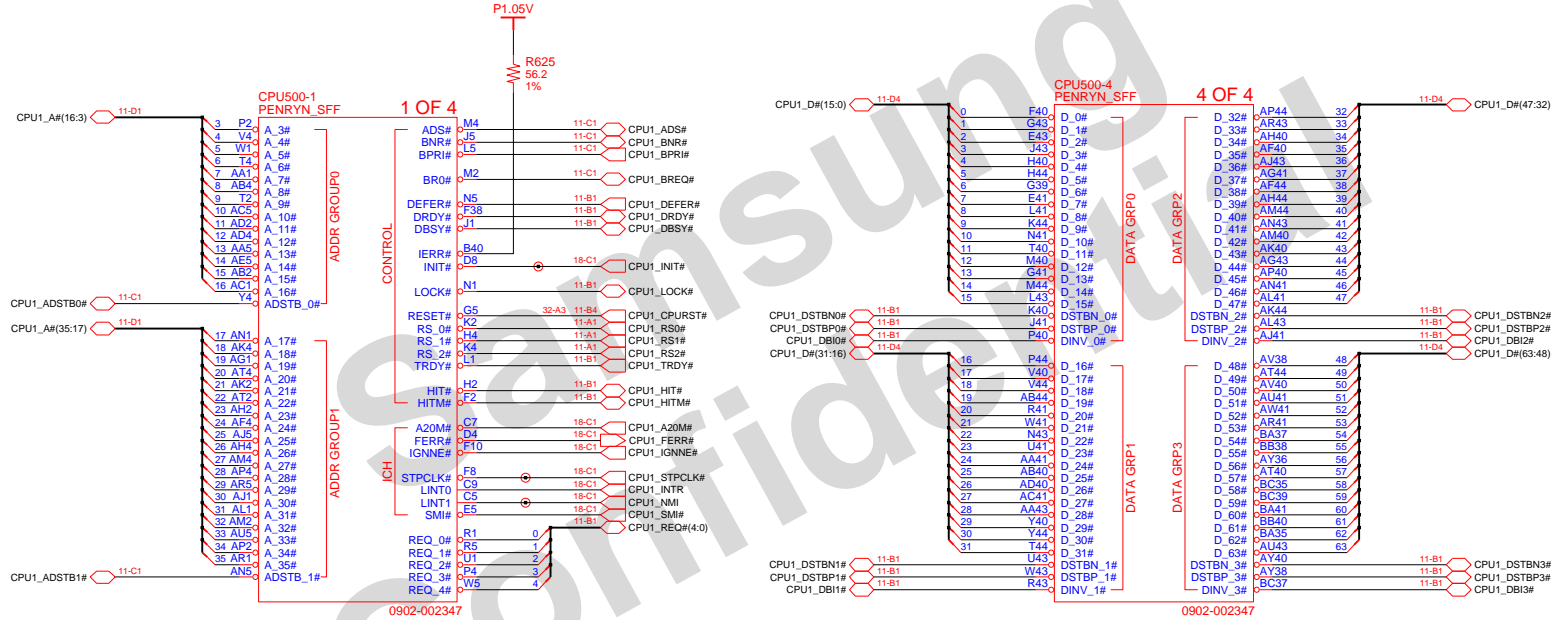
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FSC BSEL2	FSB BSEL1	FSA BSEL0	HOST CLK
0	0	0	266 MHz
0	0	1	RSVD
0	1	0	200 MHz
0	1	1	166 MHz
1	0	0	RSVD
1	0	1	RSVD
1	1	0	RSVD
1	1	1	RSVD



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN CLOCK GENERATOR	SAMSUNG	ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			PART NO.	BA41-0XXXXA
APPROVAL	JS, EUH	REV	1.1				
MODULE CODE		LAST EDIT		August 22, 2008 10:40:53 AM	PAGE	6	OF 44

ULV CPU(Penryn SFF)



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	PENRYN ULV CPU(1/3)		
APPROVAL	JS, EUH	REV	1.1			PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT		August 22, 2008 10:40:53 AM		PAGE	7 OF 44

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ULV CPU(Penryn SFF)

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

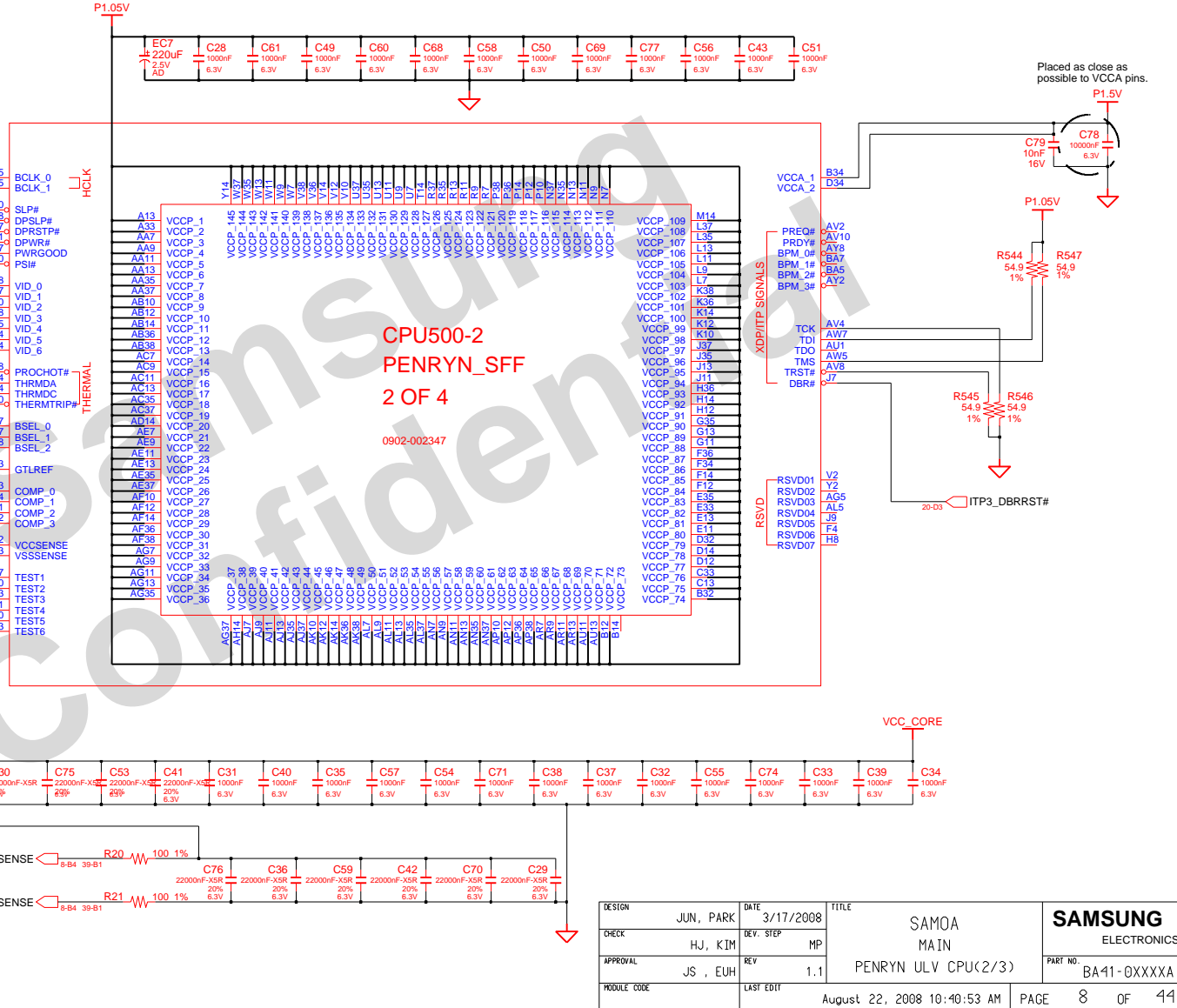
USE PROCHOT*
 56ohm -> 68ohm

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

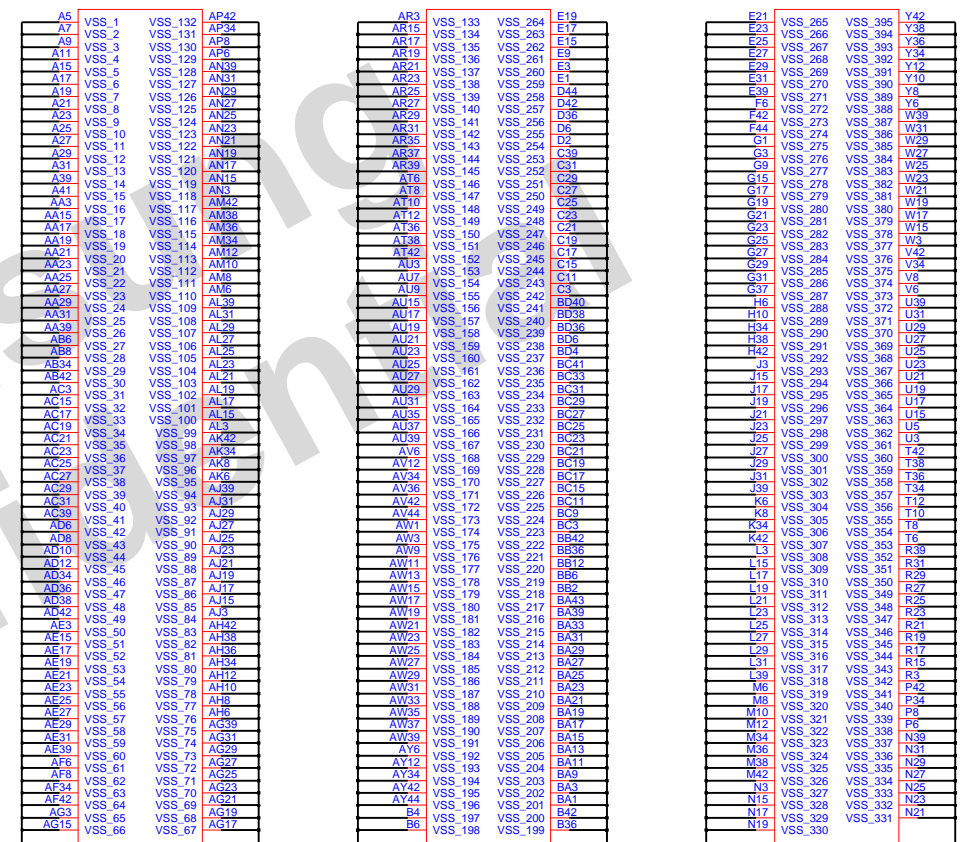
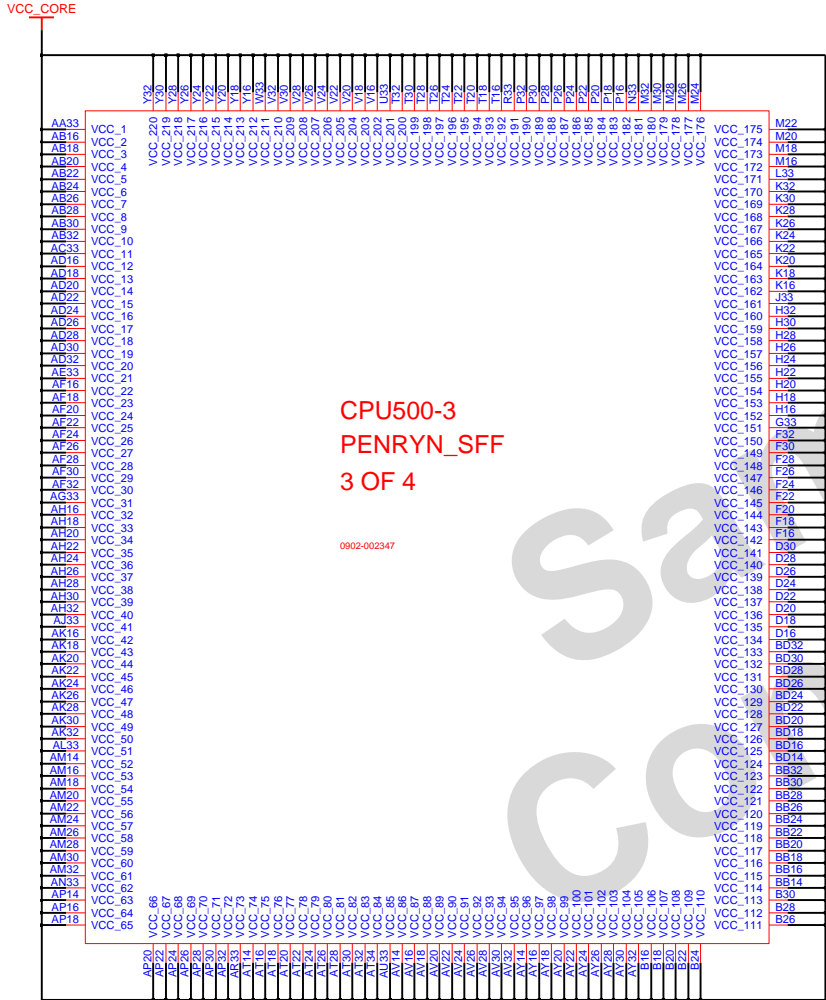
VCC/VSSsense lines between the Penryn CPU and the VR should have a trace width of 18mil on 7mil spacing with trace impedance of Zo=27.4ohm. Place PU and PD within 1 inch of CPU



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	REV	1.1	
APPROVAL	JS, EUH	REV	1.1	PENRYN ULV CPU(2/3)		PART NO. BA11-0XXXXA
MODULE CODE		LAST EDIT	August 22, 2008 10:40:53 AM	PAGE	8	OF 44

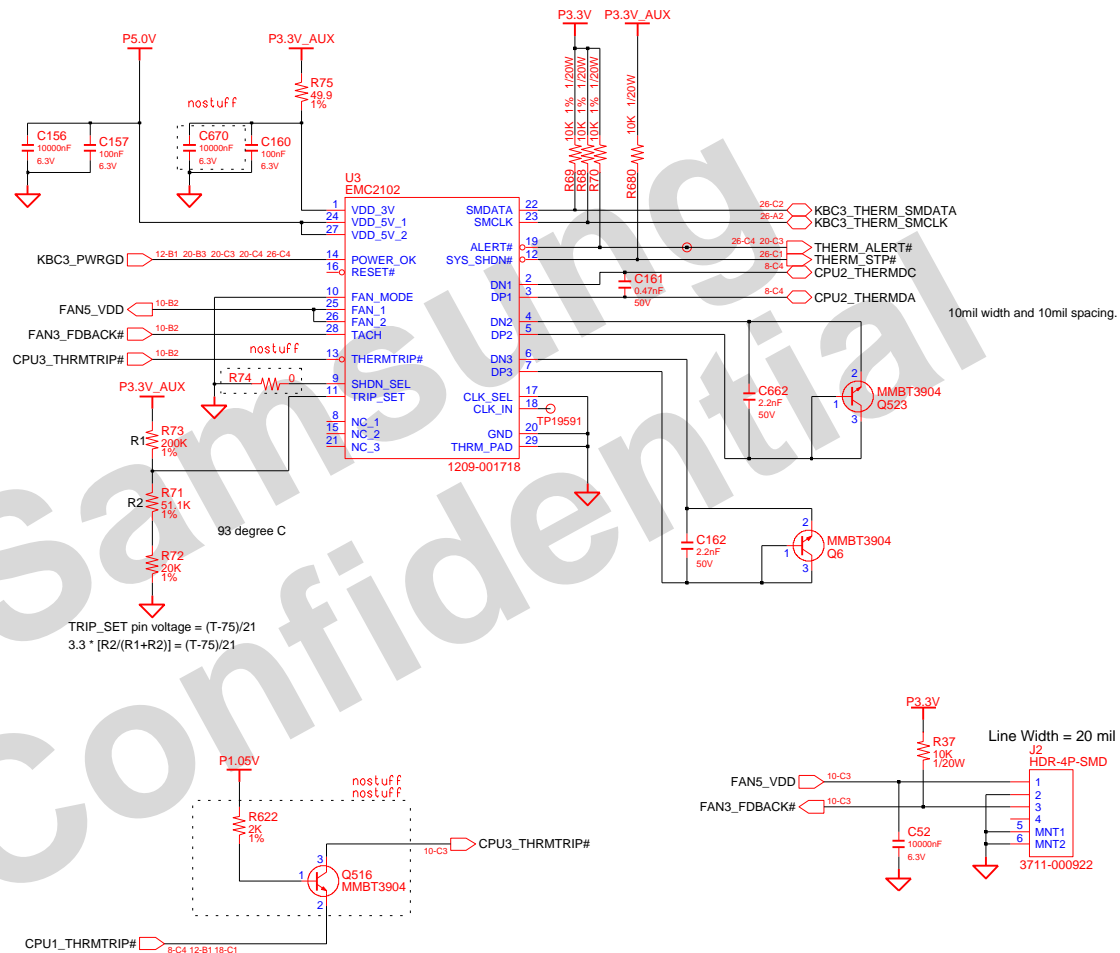
ULV CPU(Penryn SFF)

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DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN		SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	PENRYN ULV CPU(3/3)			
APPROVAL	JS, EUH	REV	1.1	August 22, 2008 10:40:53 AM			PART NO.
MODULE CODE							BA-41-0XXXXA
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THERMAL MONITOR



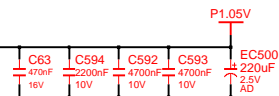
FAN MODE	
0	0% Drive
Open	60% drive after spin up routine
1	75% drive after spin up routine

SHDN_SEL	
0	Intel Mode
High-Z	Diode Mode
1	Disabled

$$\text{TRIP_SET pin voltage} = (T-75)/21$$

$$3.3 * [R2/(R1+R2)] = (T-75)/21$$

DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	THERMAL MONITOR		
APPROVAL	JS, EUH	REV	1.1			PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT		August 22, 2008 10:40:53 AM		PAGE	10 OF 44



CPU1_D#(63:0) 7-B1 7-B2 7-C1 7-C2

CPU1_A#(35:3) 7-C4

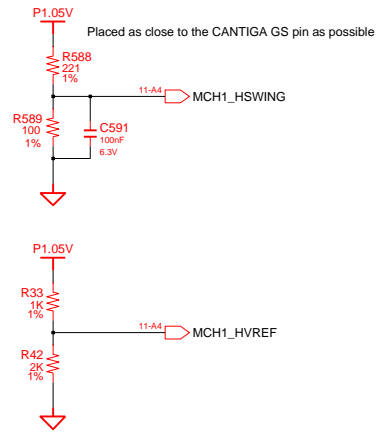
GMCH(CANTIGA GS)

GMCH500-1
CANTIGA-GS
1 OF 5
0904-002394

HOST DATA BUS

HOST ADDRESS BUS

HOST CONTROL



CPU1_CPURST# 7-C3 CPU1_SL# 8-C4 32-A3

MCH1_HSWING 11-C4

MCH1_HVREF 11-C4

CPU1_BSEL0 8-B3 8-C4 CPU1_BSEL1 8-B3 8-B4 CPU1_BSEL2 8-C3 8-B4

MCH3_CFG16 15-C1 MCH3_CFG7 15-C1 MCH3_CFG6 15-C1

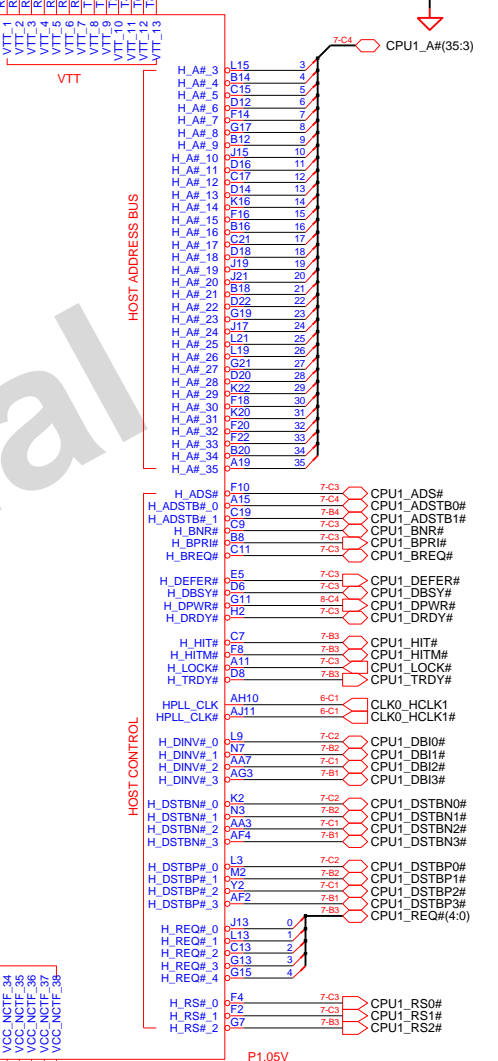
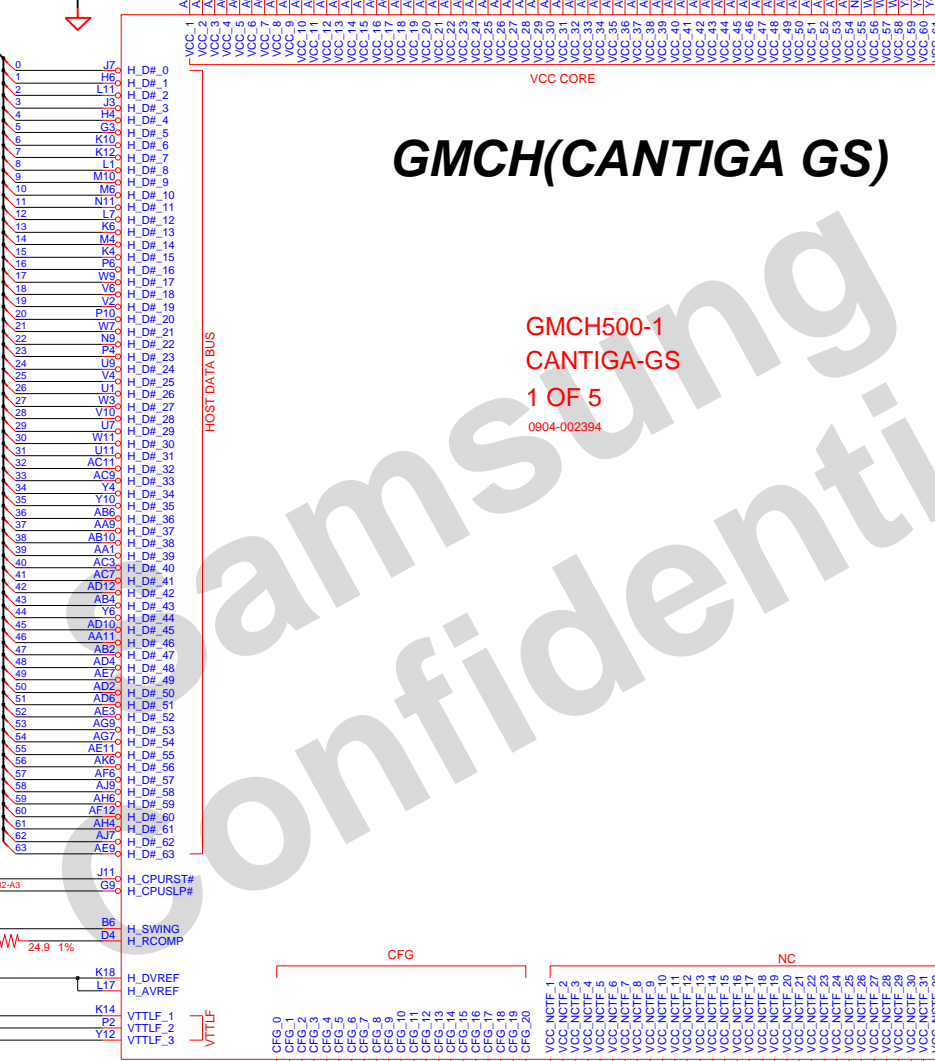
VTTFL_1 VTTFL_2 VTTFL_3

CAPACITORS: C80, C62, C84

RESISTORS: R592

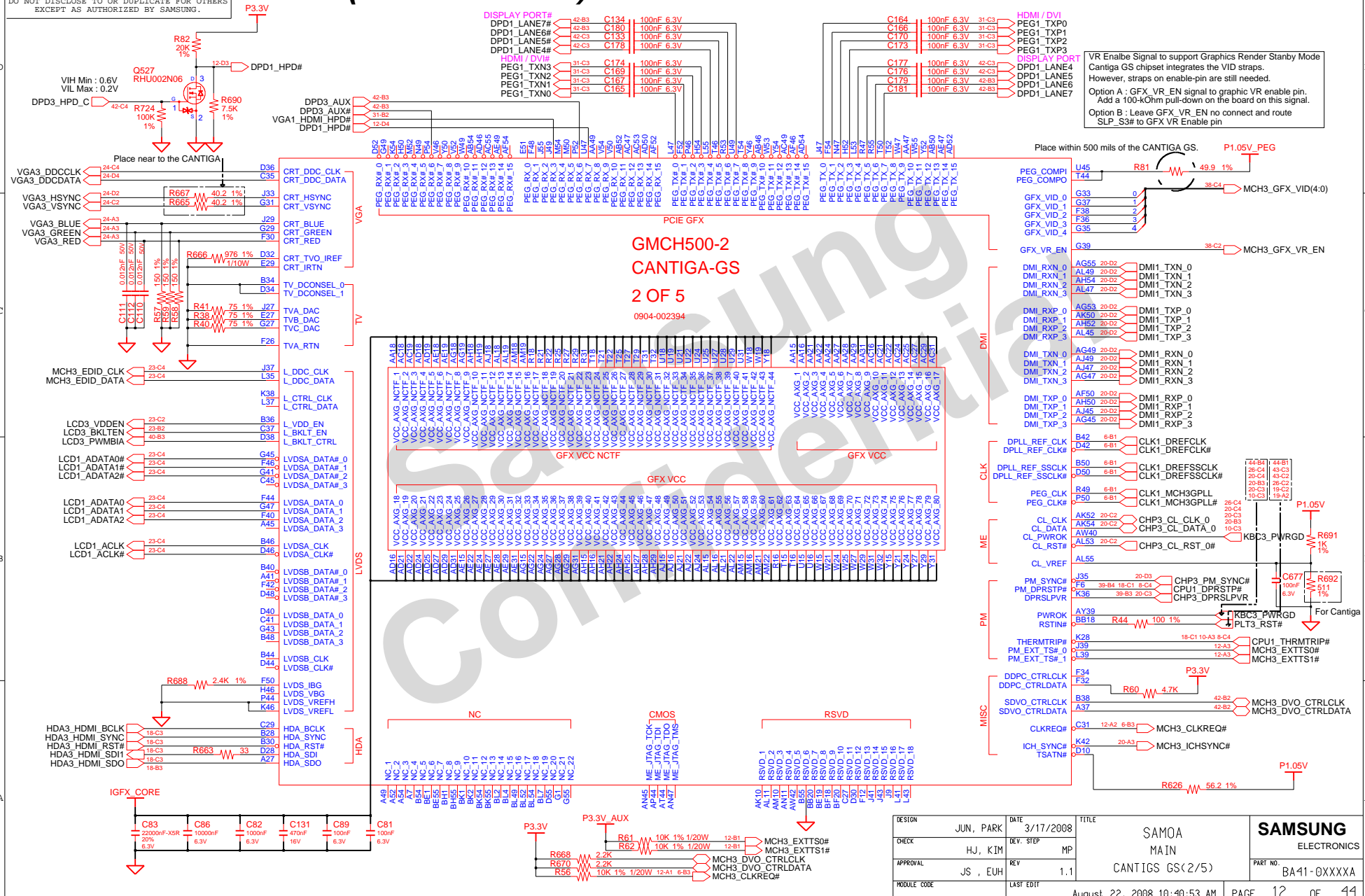
RESISTORS: R592

RESISTORS: R592



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	APPROVAL	REV	
APPROVAL	JS, EUH	REV	1.1	CANTIGA GS(1/5)		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT		August 22, 2008 10:40:53 AM		PAGE	11 OF 44

GMCH(CANTIGA GS)



VR Enable Signal to support Graphics Render Standby Mode
Cantiga GS chipset integrates the VID straps.
However, straps on enable-pin are still needed.
Option A : GFX_VR_EN signal to graphic VR enable pin.
Add a 100-kOhm pull-down on the board on this signal.
Option B : Leave GFX_VR_EN no connect and route
SLP_S3# to GFX_VR Enable pin

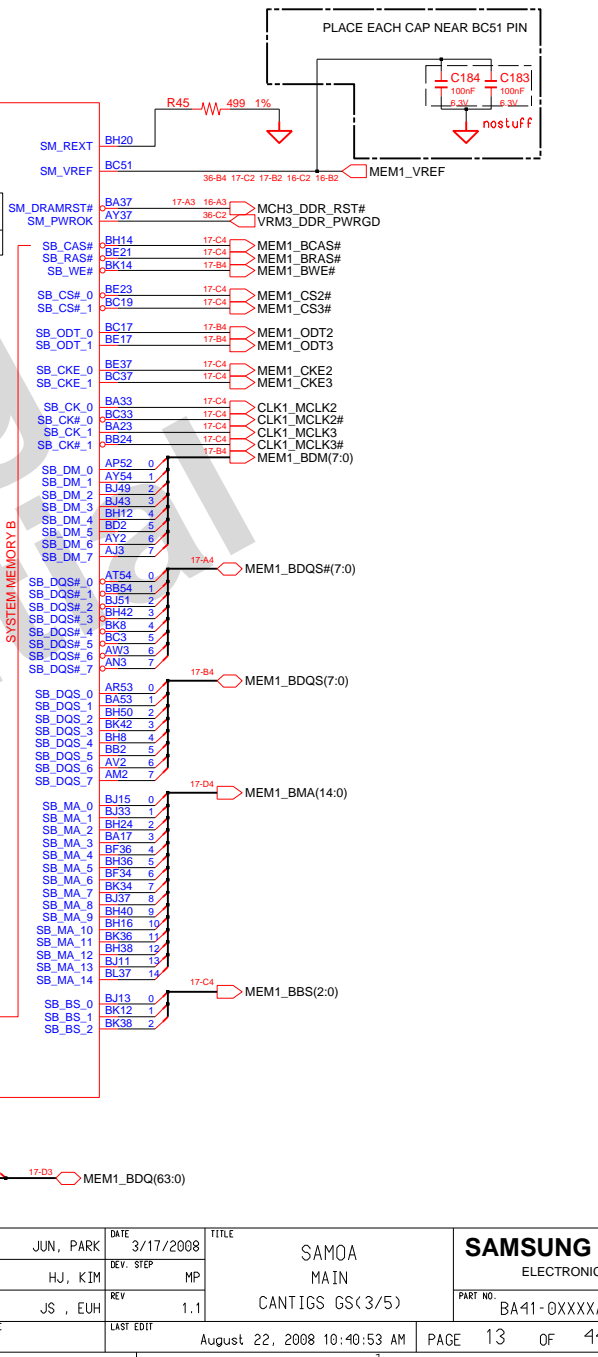
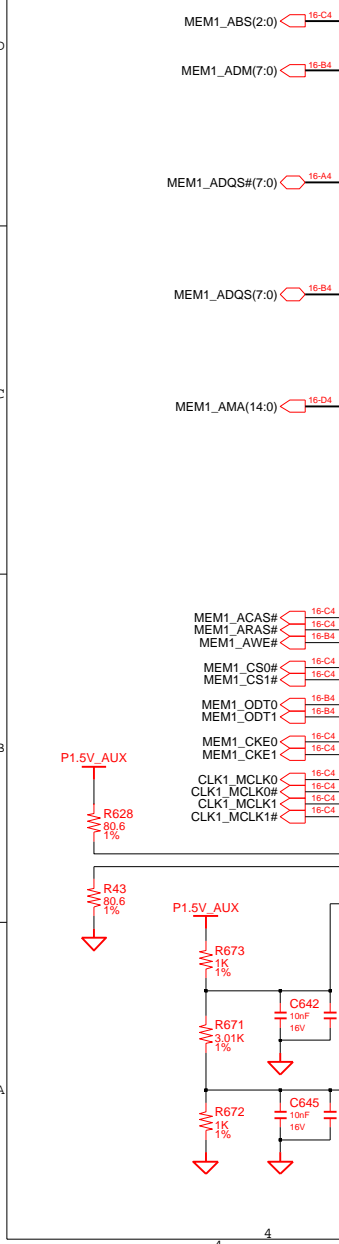
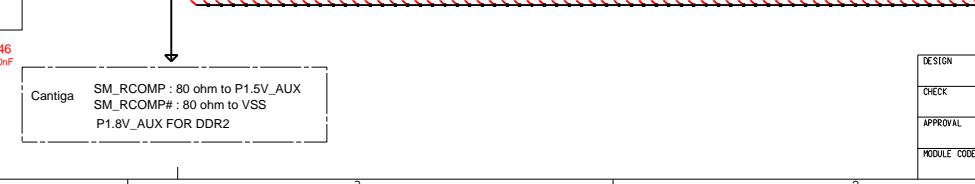
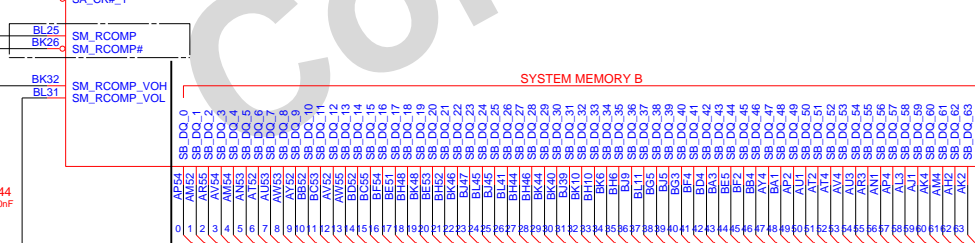
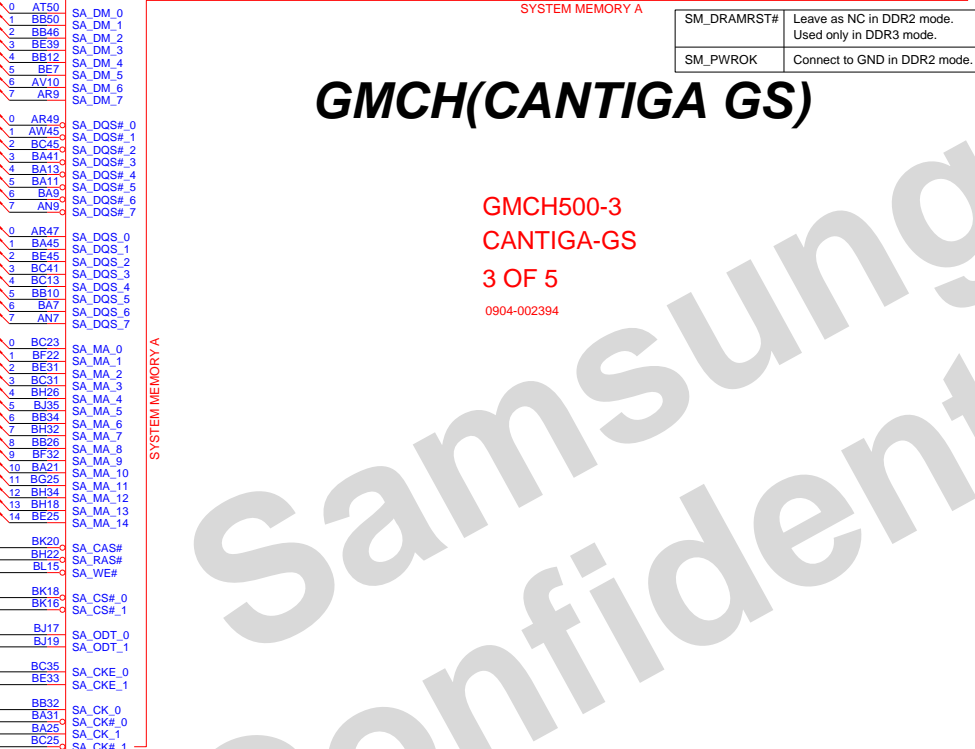
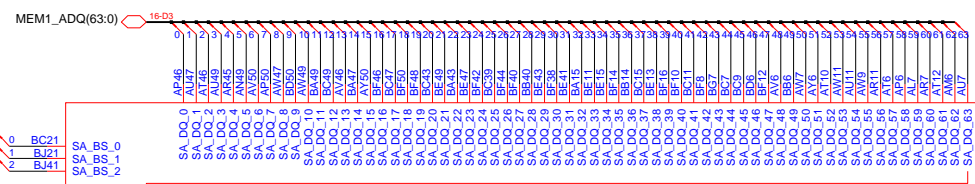
GMCH500-2
CANTIGA-GS
2 OF 5
0904-002394

DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA	SAMSUNG
CHECK	HJ, KIM	DEV. STEP	MP		MAIN	ELECTRONICS
APPROVAL	JS, EUH	REV	1.1		CANTIGS GS(2/5)	PART NO. BA1-0XXXXA
MODULE CODE		LAST EDIT			August 22, 2008 10:40:53 AM	PAGE 12 OF 44

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GMCH(CANTIGA GS)

**GMCH500-3
CANTIGA-GS
3 OF 5
0904-002394**

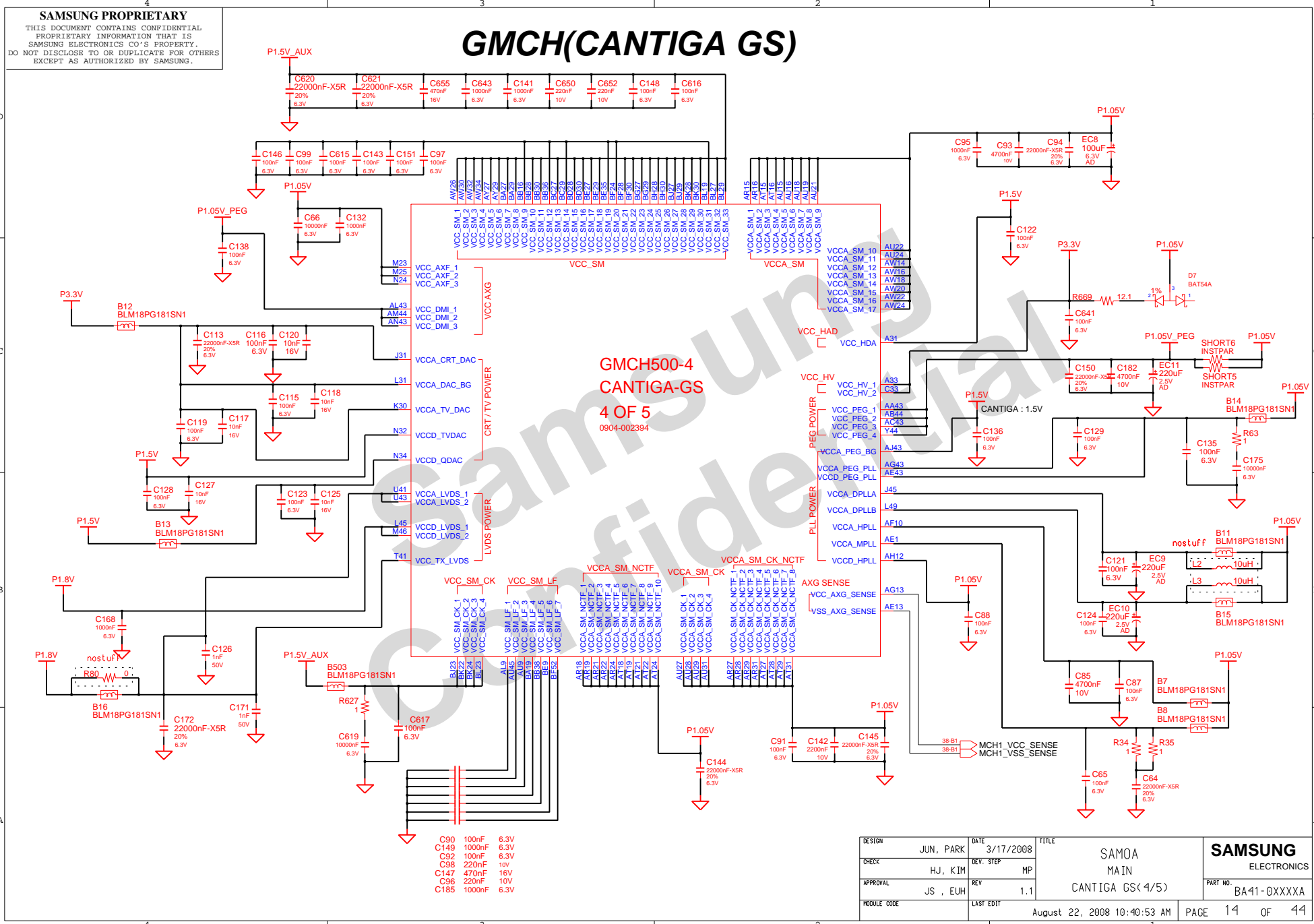


Cantiga SM_RCOMP : 80 ohm to P1.5V_AUX
 SM_RCOMP# : 80 ohm to VSS
 P1.8V_AUX FOR DDR2

DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	CANTIGS GS(3/5)		
APPROVAL	JS, EUH	REV	1.1	August 22, 2008 10:40:53 AM		PART NO. BA41-0XXXXX
MODULE CODE		LAST EDIT		PAGE	13	OF 44

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GMCH(CANTIGA GS)



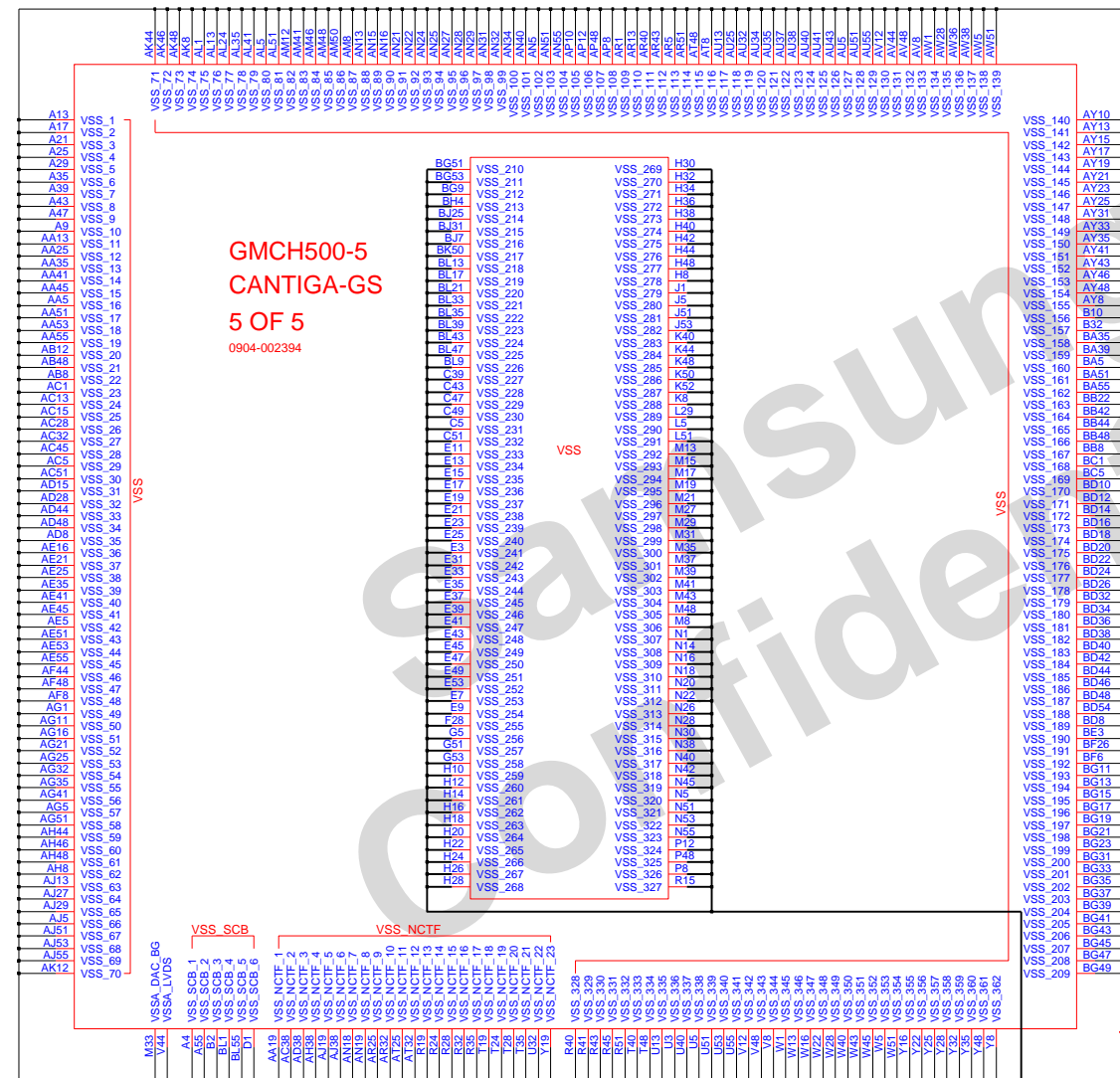
GMCH500-4
CANTIGA-GS
4 OF 5
0904-002394

C90	100nF	6.3V
C149	1000nF	6.3V
C92	100nF	6.3V
C88	220nF	10V
C147	470nF	16V
C96	220nF	10V
C185	1000nF	6.3V

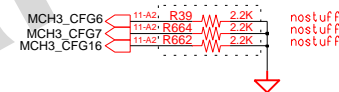
DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	CANTIGA GS(4/5)		
APPROVAL	JS, EUH	REV	1.1	PART NO. BA41-0XXXXA		PAGE 14 OF 44
MODULE CODE		LAST EDIT		August 22, 2008 10:40:53 AM		

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GMCH(CANTIGA GS)



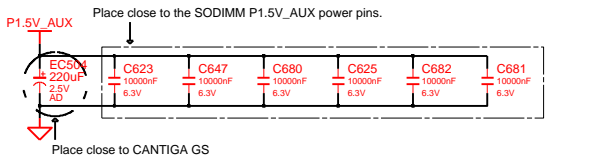
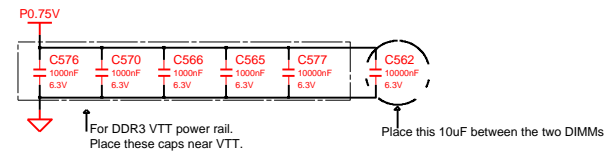
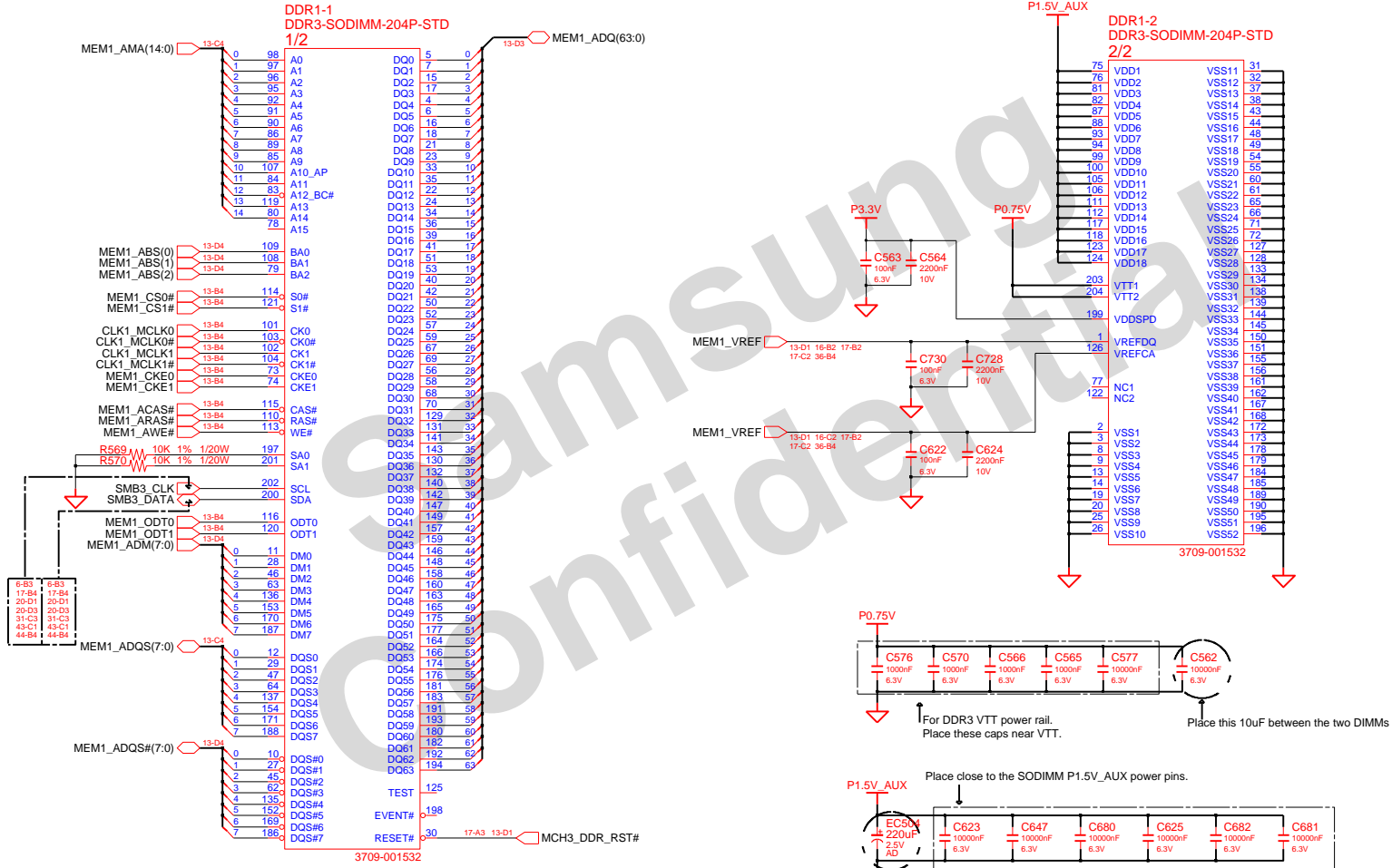
CFG#	Current Setting (def.: default Option)	
	Low	High
CFG(6)	ITPM Host Interface Enable	ITPM Host Interface Disable (def.)



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	CANTIGS GS(5/5)		
APPROVAL	JS, EUH	REV	1.1			PART NO. BA11-0XXXXA
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DDR3 SO-DIMM #0

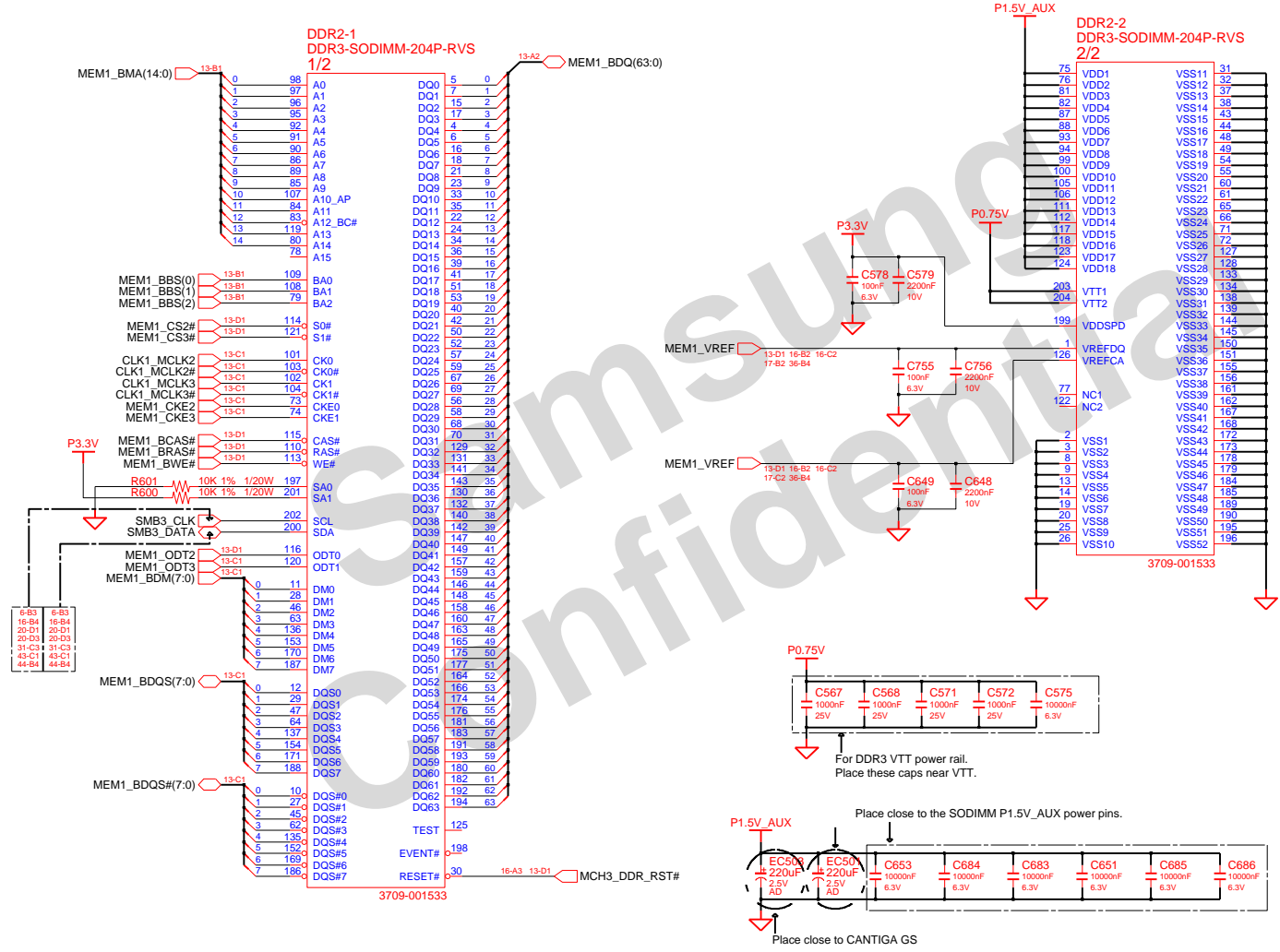
Height : 4.0mm (Standard)



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	PART NO. BA41-0XXXXA		
APPROVAL	JS, EUH	REV	1.1	DDR3 SODIMM CH.0		August 22, 2008 10:40:53 AM
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DDR3 SO-DIMM #1

Height : 4.0mm (Reverse)

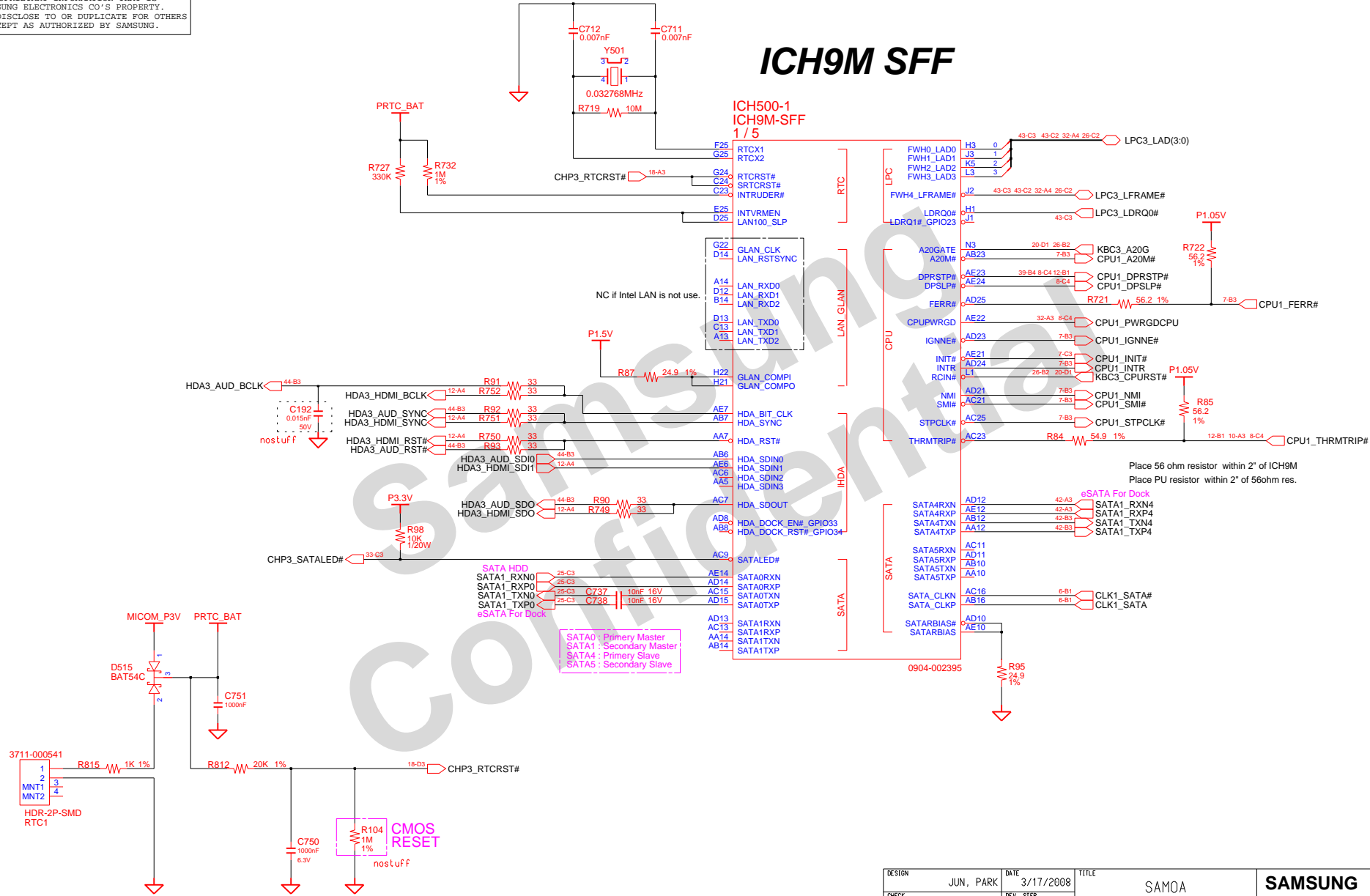


DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1		DDR3 SODIMM CH.1	PART NO. BA11-0XXXXA
MODULE CODE		LAST EDIT		August 22, 2008 10:40:53 AM	PAGE	17 OF 44

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ICH9M SFF

ICH500-1
 ICH9M-SFF
 1 / 5

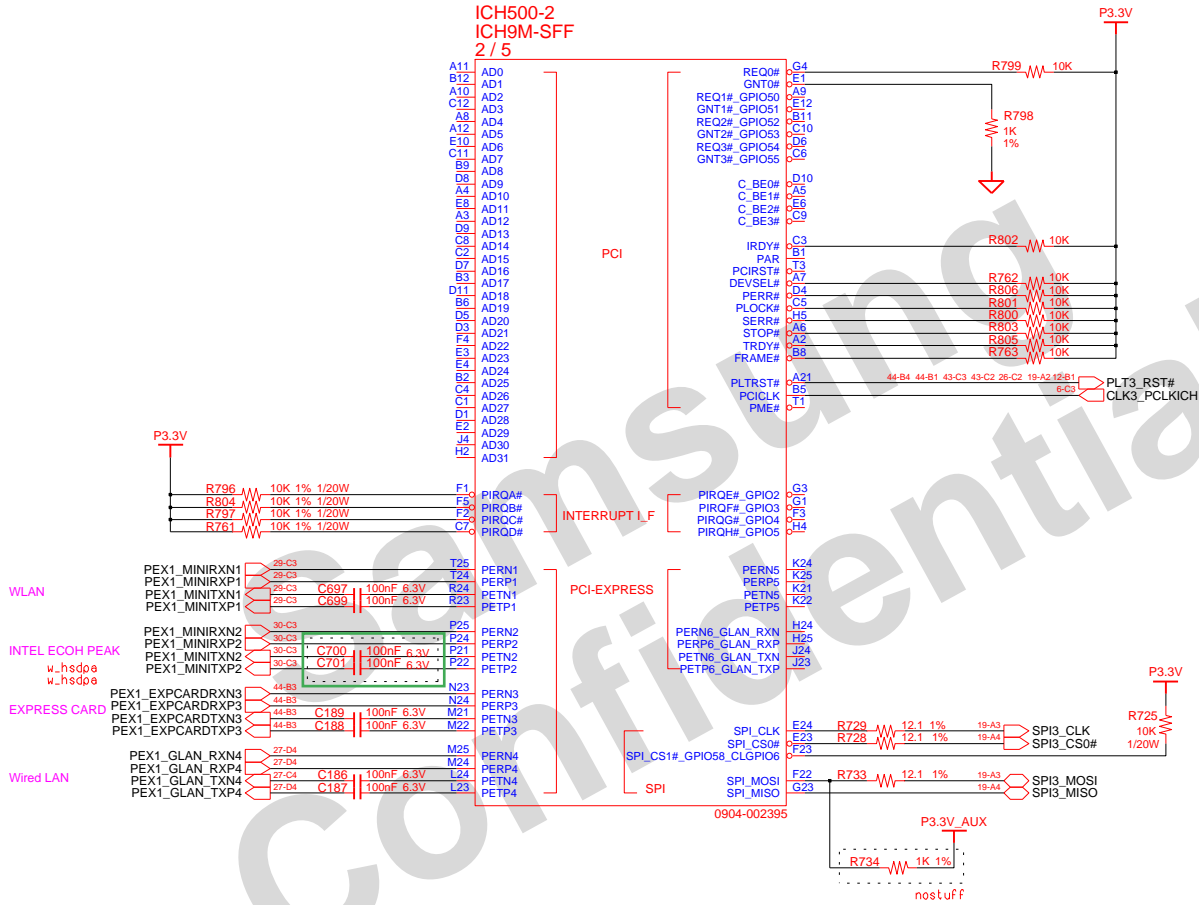


Place 56 ohm resistor within 2" of ICH9M
 Place PU resistor within 2" of 56ohm res.

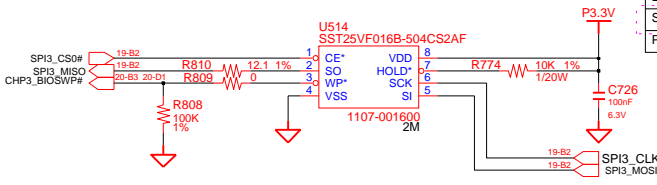
DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	ICH9M SFF(1/5)		
APPROVAL	JS, EUH	REV	1.1			PART NO. BA41-0XXXXA
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ICH9M SFF

ICH500-2
 ICH9M-SFF
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SPI ROM



Boot BIOS Select

BIOS	PCI3_GNT0#	SPI3_CS1#
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW

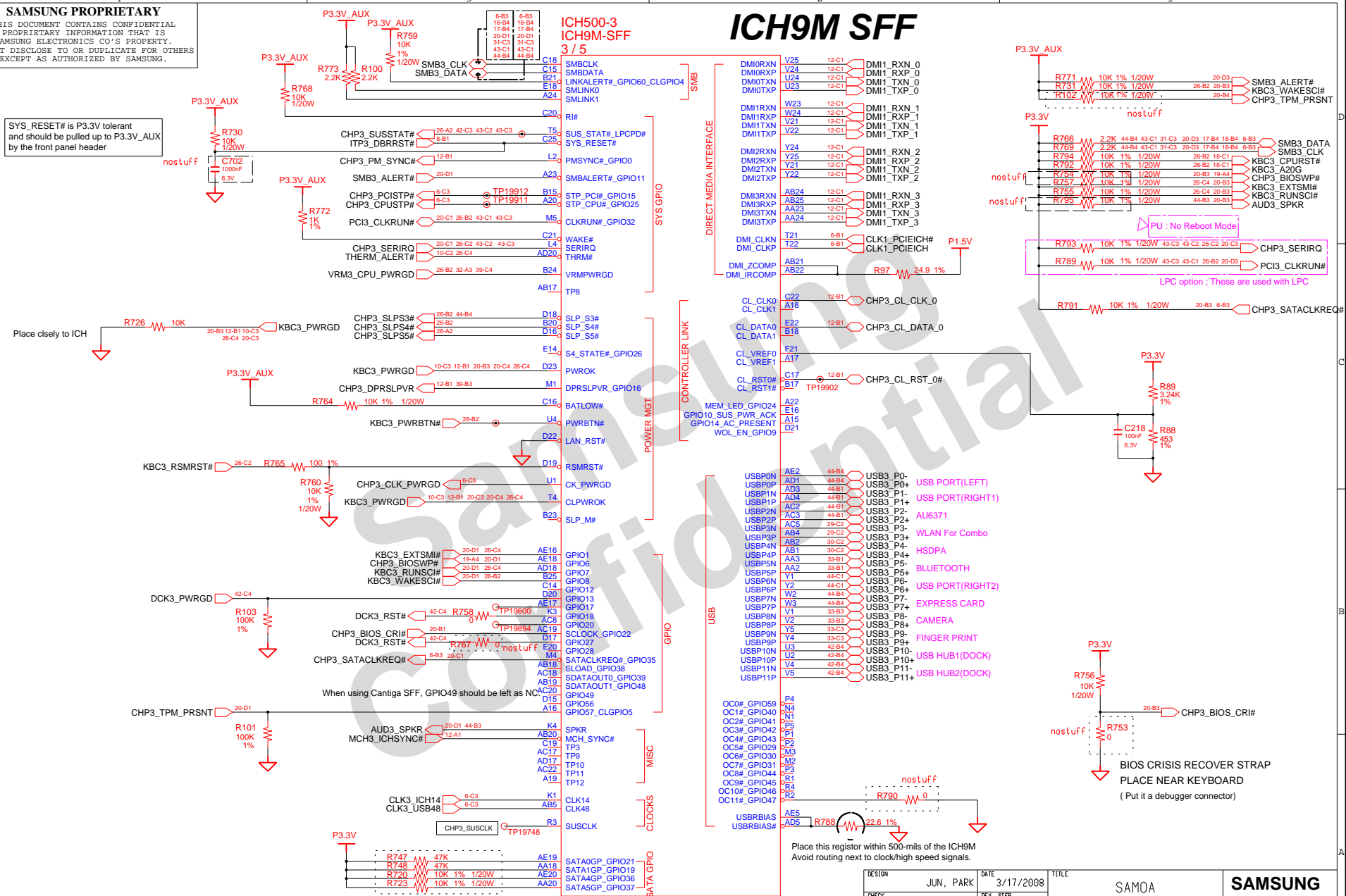
DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	ICH9M SFF (2/5)		
APPROVAL	JS, EUH	REV	1.1	PART NO. BA41-0XXXXA		
MODULE CODE	LAST EDIT		August 22, 2008 10:40:53 AM		PAGE 19 OF 44	

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ICH9M SFF

ICH500-3 ICH9M-SFF 3/5

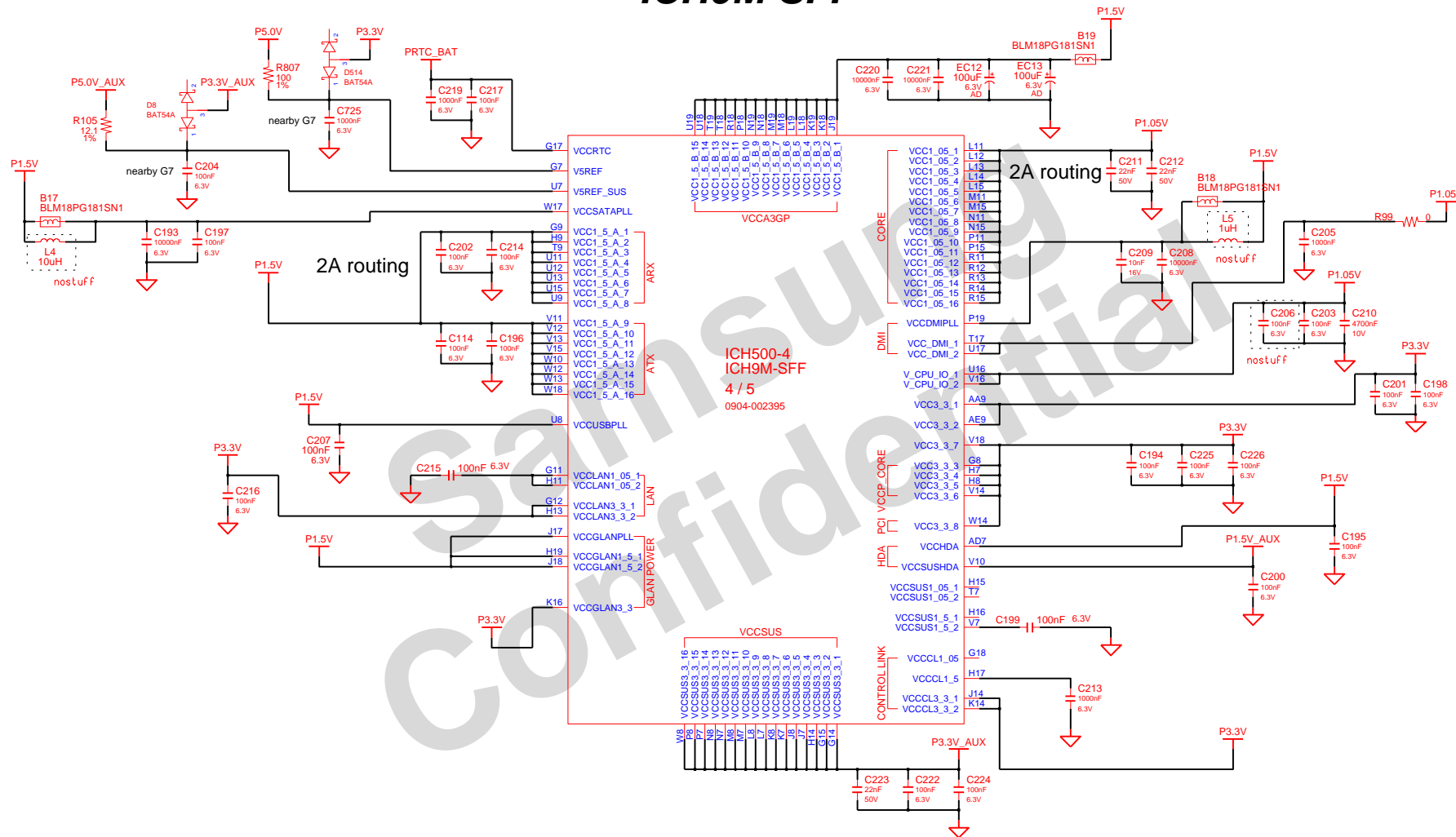
SYS_RESET# is P3.3V tolerant
 and should be pulled up to P3.3V_AUX
 by the front panel header



Place this register within 500-mils of the ICH9M
 Avoid routing next to clock/high speed signals.

DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	ICH9M SFF (3/5)		
APPROVAL	JS, EUH	REV	1.1			PART NO. BA11-0XXXXA
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ICH9M SFF



ICH500-4
ICH9M-SFF
4 / 5
0904-002395

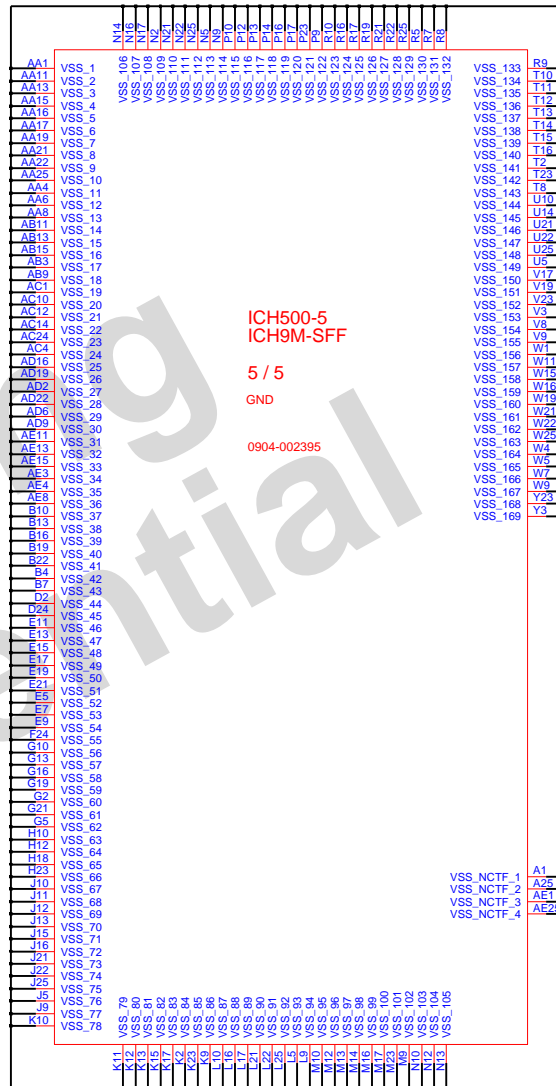
DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	ICH9M SFF (4/5)		
APPROVAL	JS, EUH	REV	1.1			PART NO. BA41-0XXXXA
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BIOS CODE

ICH9M SFF

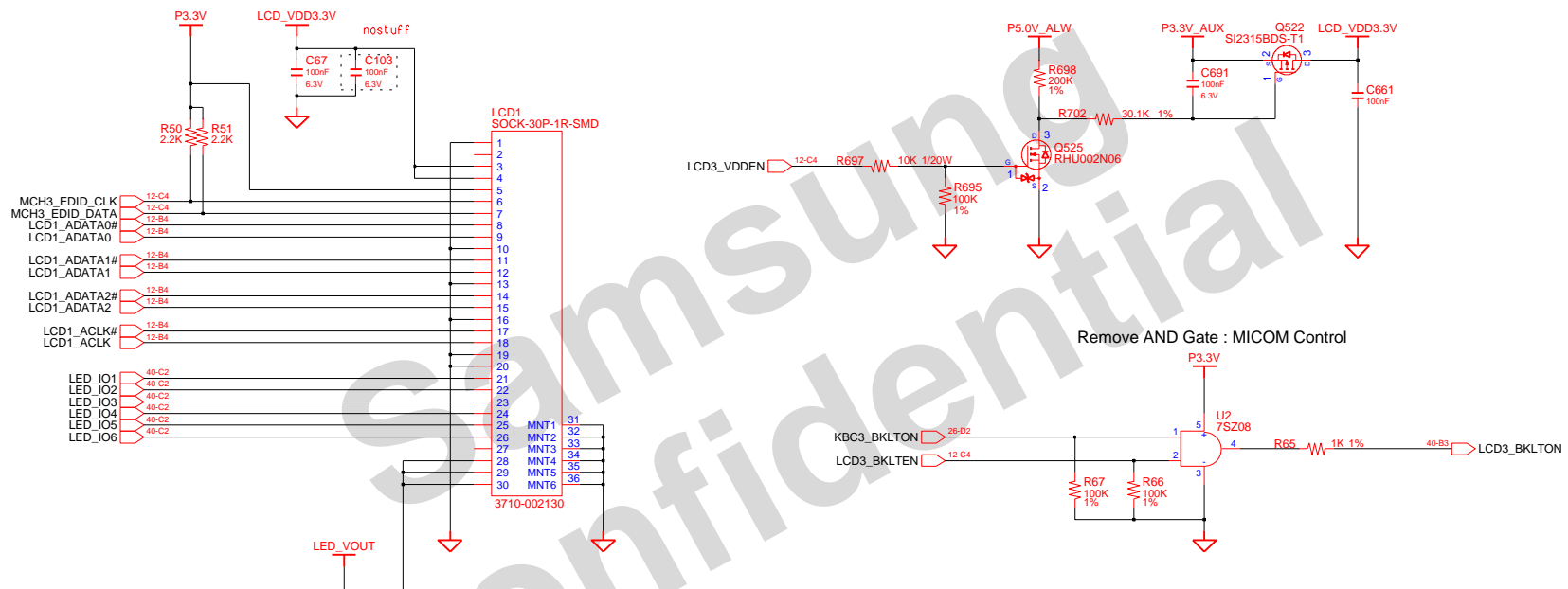
- 02 VERIFY REAL MODE
- 03 DISABLE NMI
- 04 GET CPU TYPE
- 06 INIT. SYSTEM H/W
- 08 INIT. CHIPSET REG.
- 09 SET IN POST FLAG
- 0A INIT CPU.REG
- 0B CPU CACHE ON
- 0C INIT.CACHE TO POST
- 0E INIT. I/O VALUE
- 0F ENABLE THE L-BUS IDE
- 10 INIT. POWER MANAGER
- 11 LOAD ALTERNATE REG.
- 13 PCI BUS MASTER RESET WITH INITIAL POST VALUE
- 14 INIT. KEYBOARD CONTROLLER
- 16 CHECK CHECKSUM
- 18 8254 TIMER INIT.
- 1A 8237 DMA CONTROLLER INIT.
- 1C RESET INTERRUPT CONTROLLER
- 20 TEST DRAM REFRESH
- 22 TEST 8742 KEYBOARD CONTROLLER
- 24 SET ES SEGMENT REG. TO 4GB
- 26 ENABLE A20
- 28 AUTO SIZING DRAM
- 32 COMPUTE THE CPU SPEED
- 34 TESET CMOS RAM
- 38 SHADOW SYSTEM BIOS ROM
- 3A AUTO SIZING CACHE
- 3C CONFIGURE ADVANCED CHIPSET REG.
- 3D LOAD ALTER REG. WITH CMOS VALUE
- 42 INIT. INTERRUPT VECTOR
- 44 INIT. BIOS INTERRUPT
- 46 CHECK ROM COPYRIGHT NOTICE
- 47 INIT. I20 SUPPORT IF INSTALLED
- 48 CHECK VIDEO CONFIGURE AGAINST CMOS
- 49 INIT. PCI BUS AND DEVICE
- 4A INIT. ALL VIDEO BIOS ROM
- 4C SHADOW VIDEO BIOS ROM
- 50 DISPLAY CPU TYPE AND SPEED
- 52 TEST KEYBOARD
- 54 SET KEYCLICK IF ENABLED
- 56 ENABLE KEYBOARD
- 58 TEST FOR UNEXPECTED INTERRUPTS
- 5A DISPLAY " PRESS SETUP"
- 5C TEST RAM BETWEEN 512K AND 640K
- 60 TEST EXTENDED MEMORY
- 62 TEST EXTENDED MEMORY ADDRESS LINE
- 64 JUMP TO USER PATCH 1

- 66 CONFIGURE ADVANCE CACHE REG.
- 6A DISPLAY EXTERNAL CACHE SIZE
- 6C DISPLAY SHADOW MESSAGE
- 6E DISPLAY NON-DISPOSABLE SEGMENT
- 70 DISPLAY ERROR MESSAGE
- 72 CHECK FOR CONFIGURATION ERROR
- 74 TEST REAL-TIME CLOCK
- 76 CHECK FOR KEYBOARD ERROR
- 7C SETUP HARDWARE INTERRUPT VECTOR
- 7E TEST COPROCESSER IF PRESENT
- 80 DISABLE ON-BOARD I/O PORT
- 82 DETECT AND INSTALL EXT.RS232C
- 84 DETECT AND INSTALL EXT.PARALLEL
- 86 RE-INIT. ON-BOARD I/O PORT
- 88 INIT. BIOS DATA ROM
- 8A INIT.EXTENDED BIOS DATA AREA
- 8C INIT. FDD CONTROLLER
- 9A SHADOW OPTION ROMS
- 9C SETUP POWER MANAGEMENT
- 9E ENABLE H/W INTERRUPT
- A0 SET TIME OF DAY
- A4 INIT. TYPOMATIC RATE
- A8 ERASE F2 PROMPT
- AA SCAN FOR F2 KEY STROKE
- AC ENTER SETUP
- AE CLEAR IN POST FLAG
- B0 CHECK FOR ERRORS
- B2 POST DONE-PREPARE TO BOOT O/S
- B4 ONE BEEP
- B6 CHECK PASSWORD (OPTION)
- B7 ACPI INIT
- BA DMI INIT
- BE CLEAR SCREEN
- C0 TRY BOOT WITH INT19
- D0 INTERRUPT HANDLER ERROR
- D2 UNKNOWN INTERRUPT ERROR
- D4 PENDING INTERRUPT ERROR
- D6 SHUTDOWN 5
- DA SHUTDOWN ERROR
- DA EXTENDED BLOCK MOVE
- DC SHUTDOWN 10
- 89 ENABLE NMI
- 90 INIT. HDD CONTROLLER
- 91 INIT. LOCAL BUS HDD CONTROLLER
- 92 JUMP TO USER PATCH 2
- 94 DISABLE A20 ADDRESS LINE
- 96 CLEAR HUGE ES SEGMENT REG.
- 98 SEARCH FOR OPTION ROMS



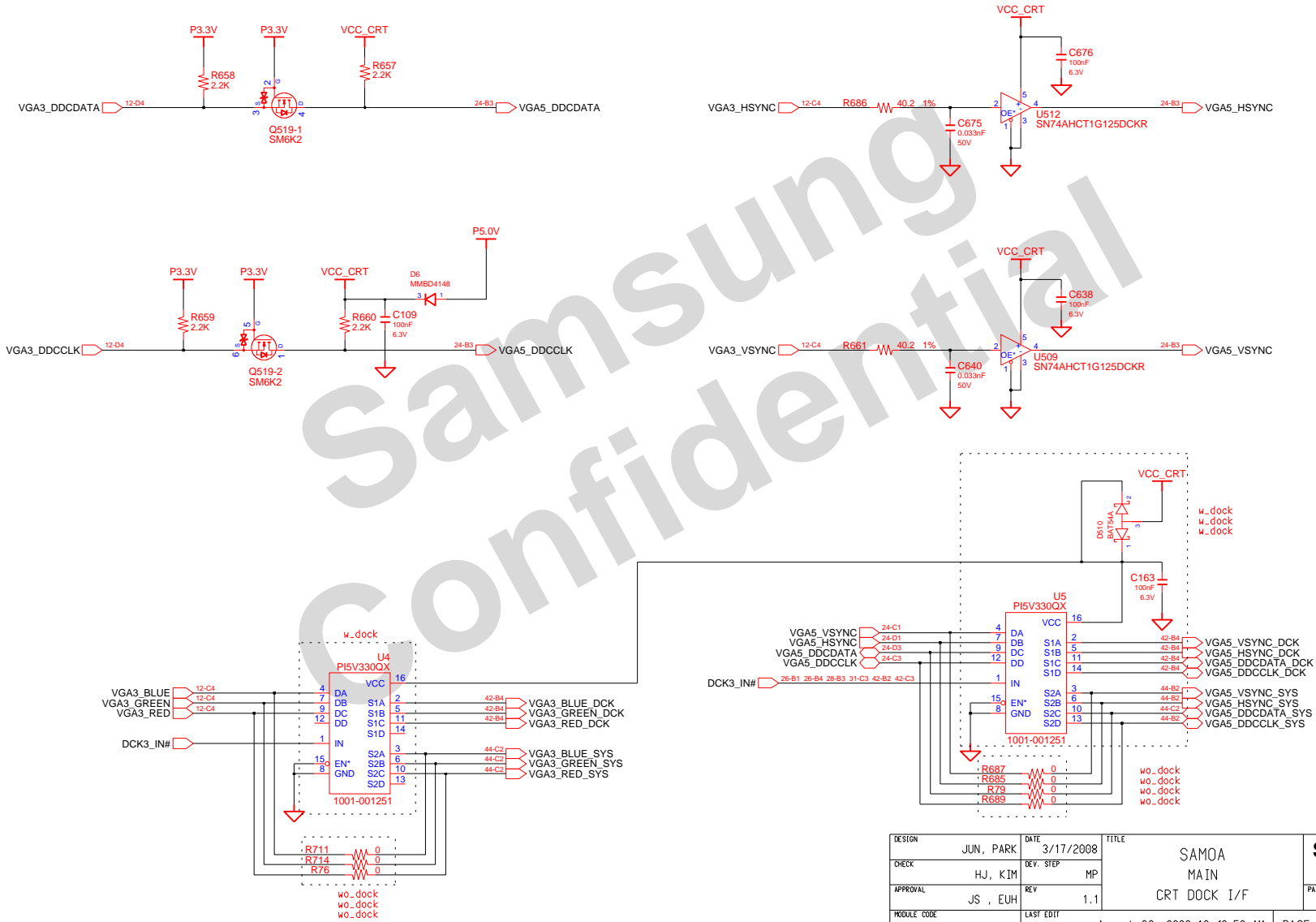
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CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1		ICH9M SFF(5/5)	PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT		August 22, 2008 10:40:53 AM	PAGE 22 OF 44	

LED LCD CONNECTOR



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN LED LCD I/F	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1			
MODULE CODE		LAST EDIT	August 22, 2008 10:40:53 AM	PAGE 23 OF 44		

CRT DOCK I/F



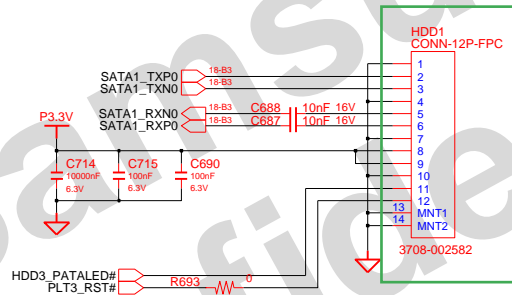
DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN		SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	CRT DOCK I/F		PART NO.	
APPROVAL	JS, EUH	REV	1.1			BA41-0XXXXA	
MODULE CODE	LAST EDIT		August 22, 2008 10:40:53 AM		PAGE	24	OF 44

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1.8" SATA HDD I/F

Samsung Confidential

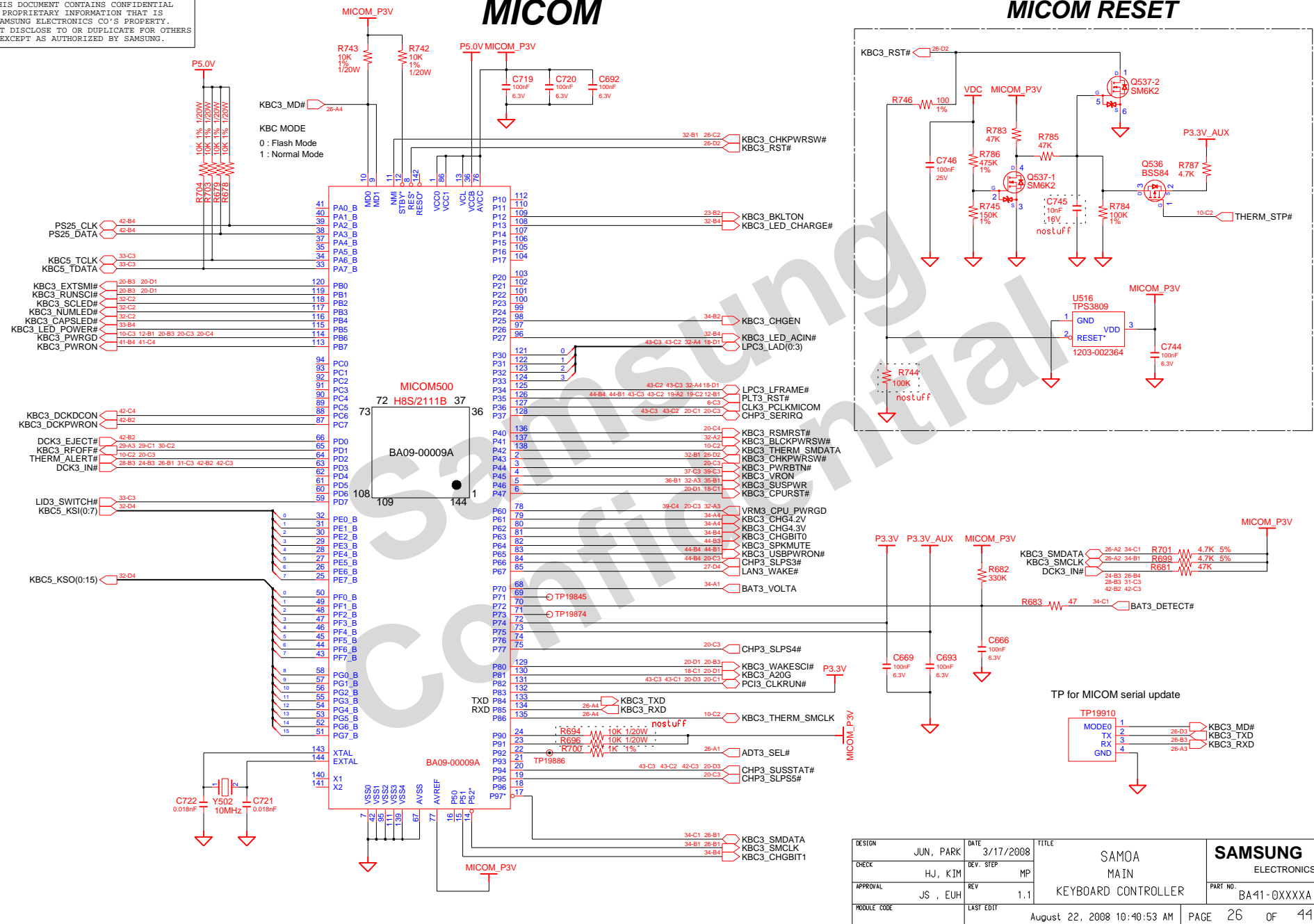


DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	1.8inch SATA HDD I/F		
APPROVAL	JS, EUH	REV	1.1	PART NO. BA41-0XXXXA		PAGE 25 OF 44
MODULE CODE	LAST EDIT		August 22, 2008 10:40:53 AM			

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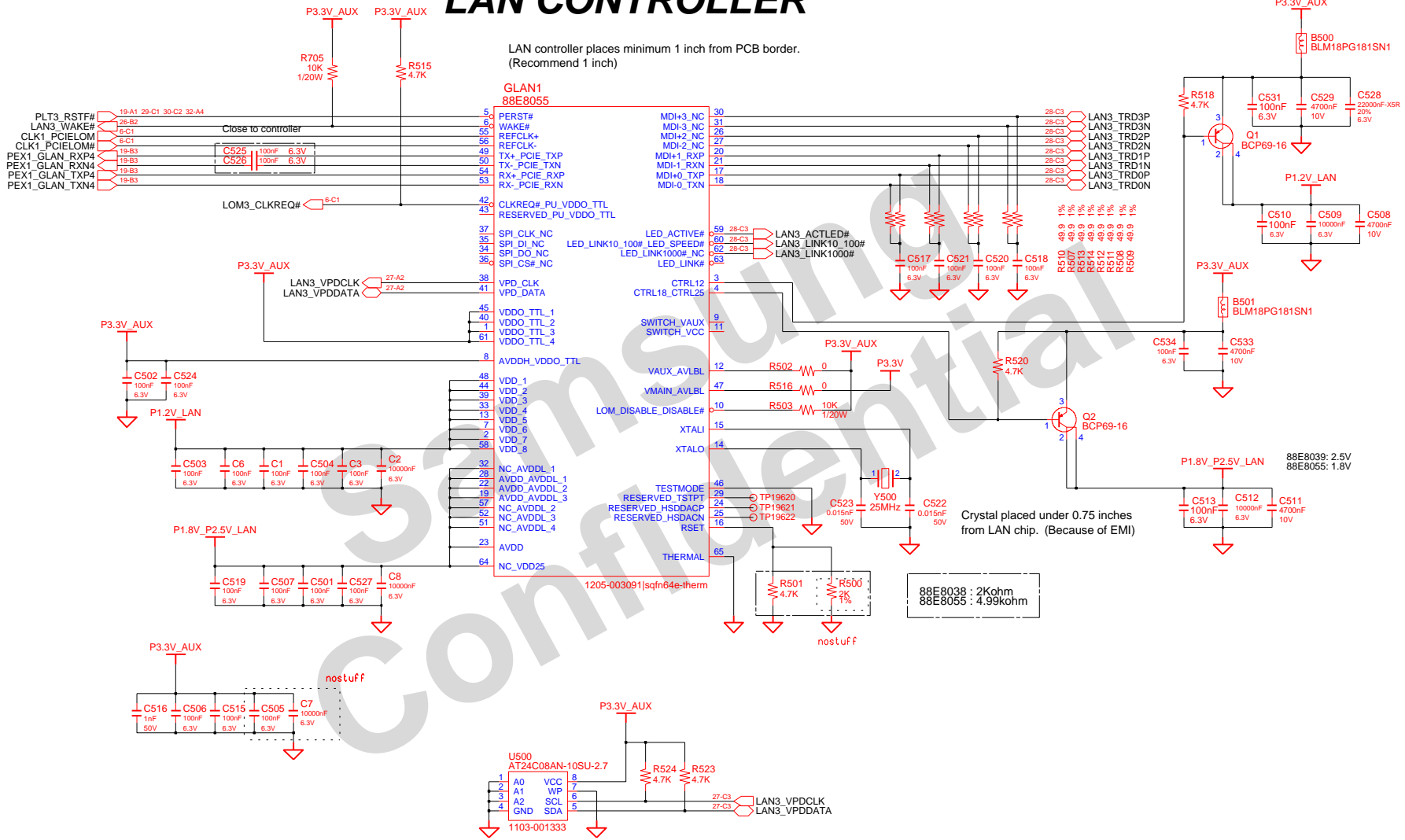
MICOM

MICOM RESET



LAN CONTROLLER

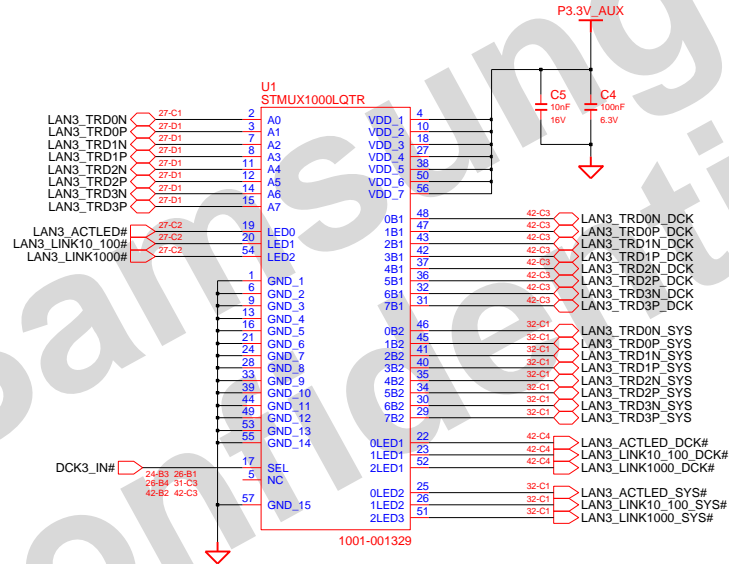
LAN controller places minimum 1 inch from PCB border.
(Recommend 1 inch)



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN LAN CONTROLLER	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1		PART NO.	BA41-0XXXXA
MODULE CODE		LAST EDIT		August 22, 2008 10:40:53 AM	PAGE	27 OF 44

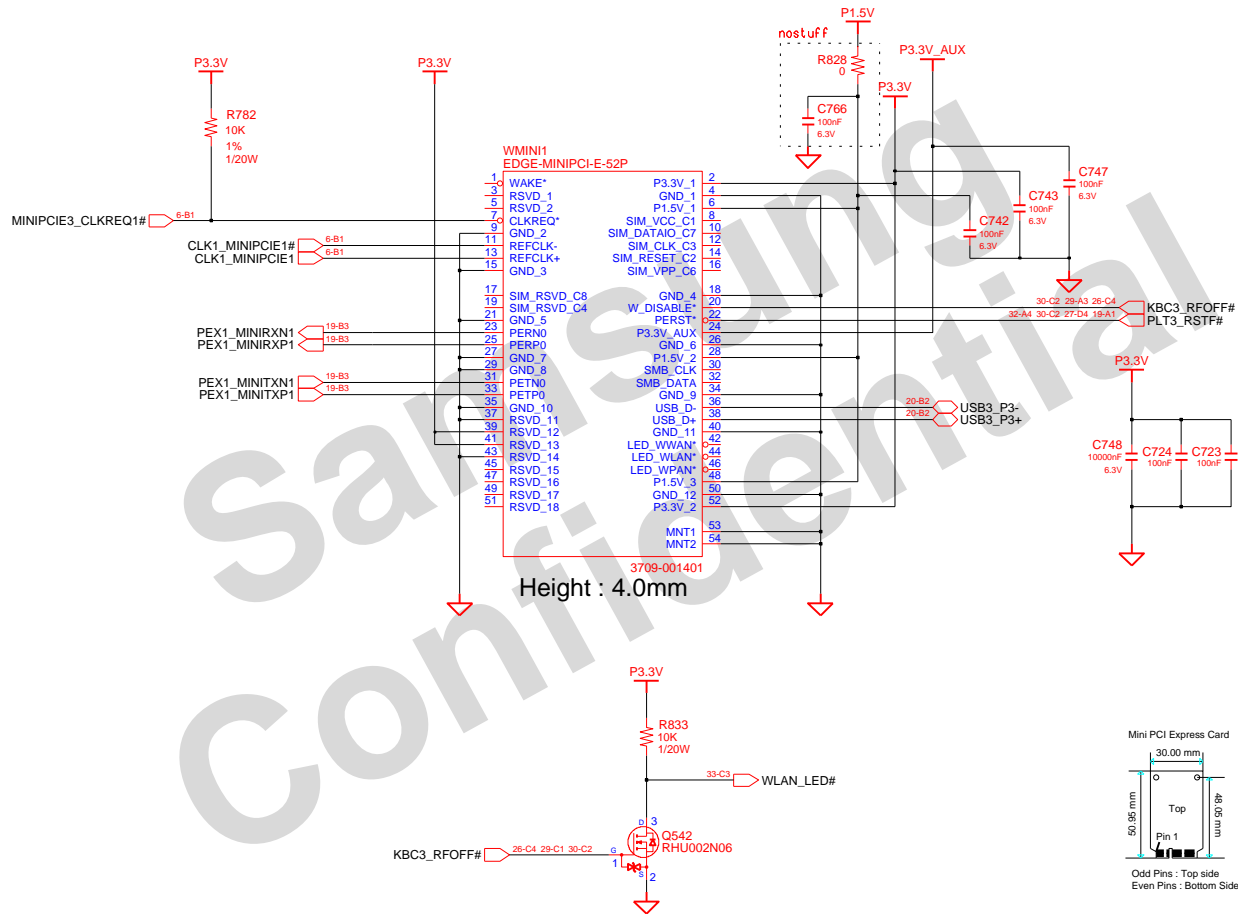
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LAN PASSTHRU BRIDGE CHIP



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN LAN DOCK I/F	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1			PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT	August 22, 2008 10:40:53 AM	PAGE	28	OF 44

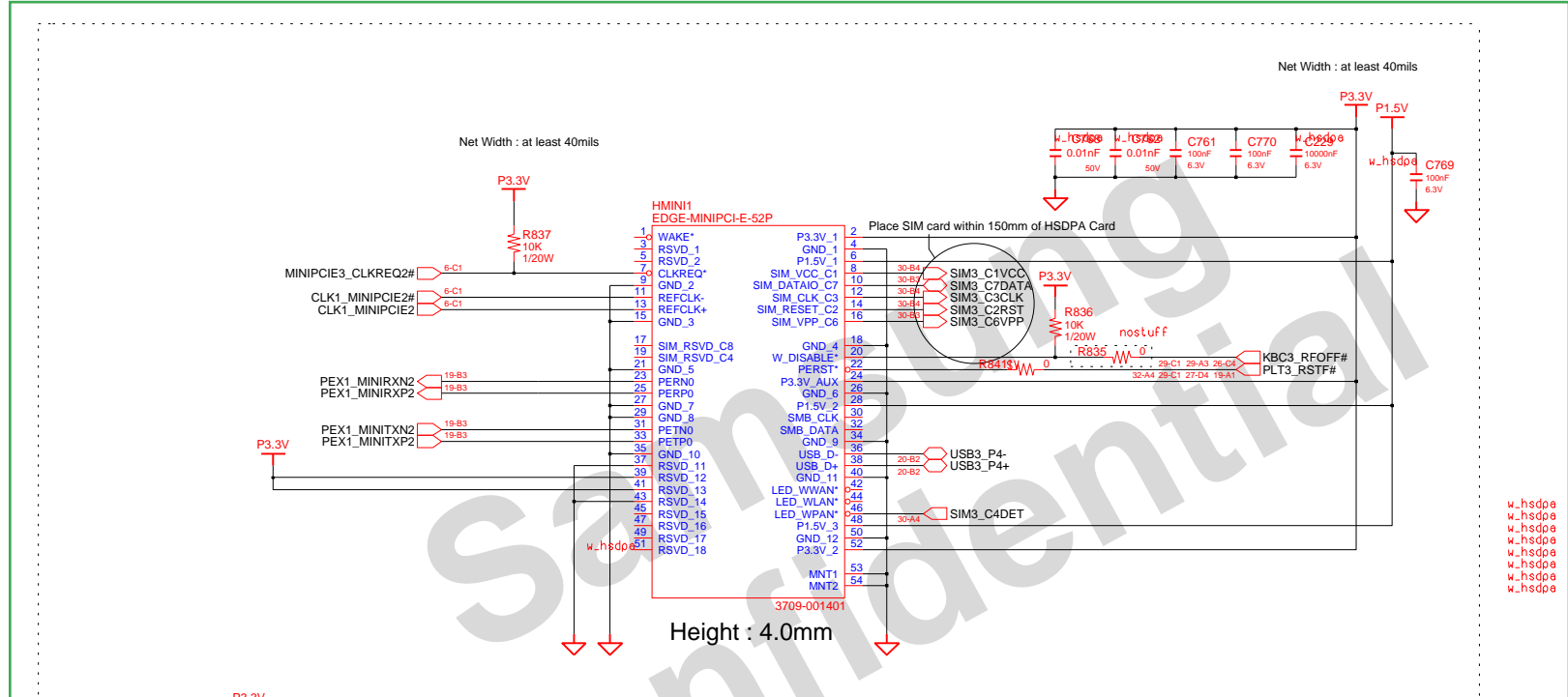
MINICARD(WLAN)



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN WIRELESS LAN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1		PART NO.	BA41-0XXXXA
MODULE CODE		LAST EDIT		August 22, 2008 10:40:53 AM	PAGE	29 OF 44

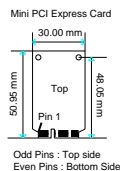
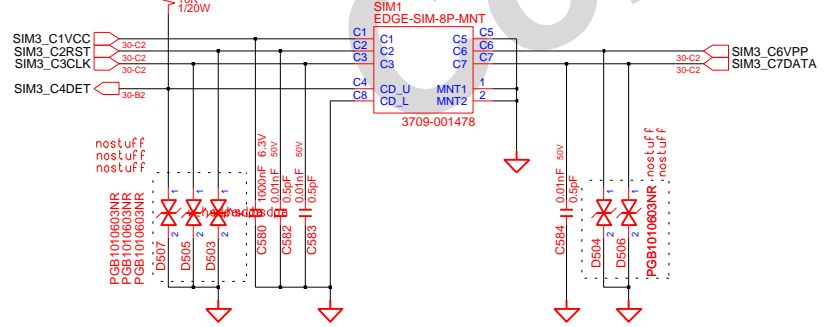
MINICARD(HSDPA)

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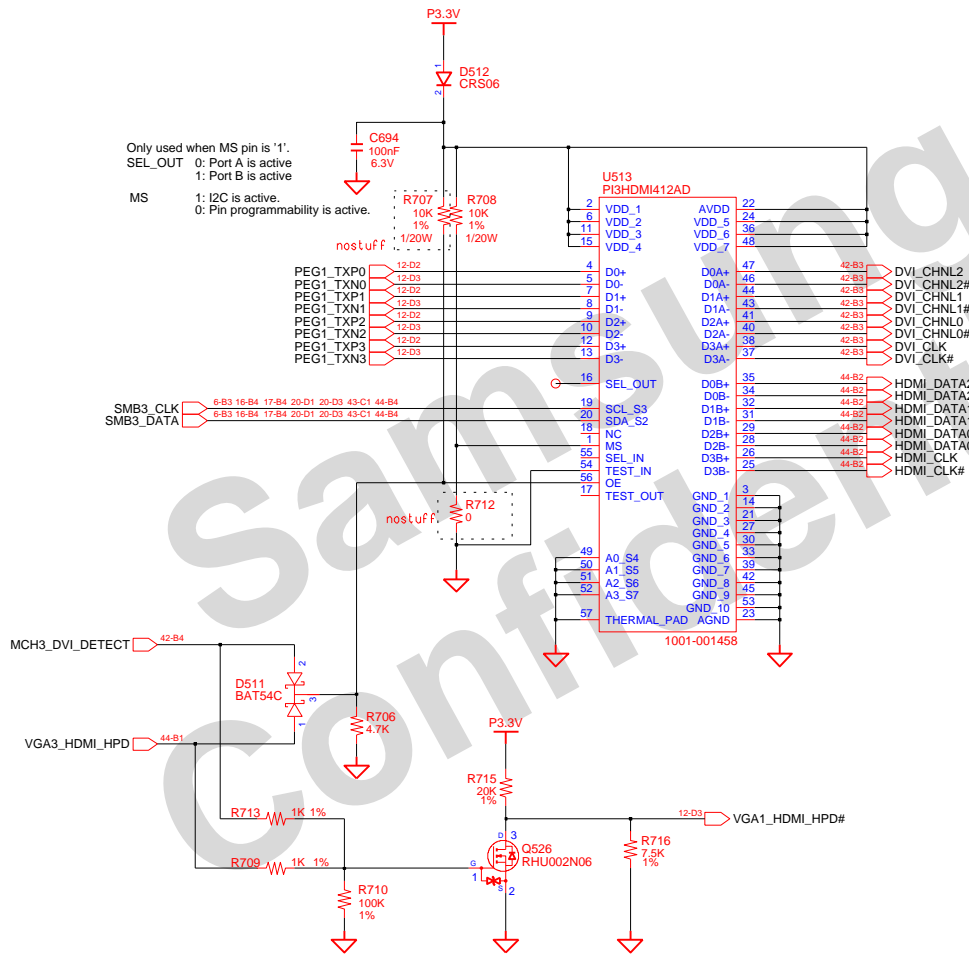
Height : 4.0mm

SIM CONNECTOR



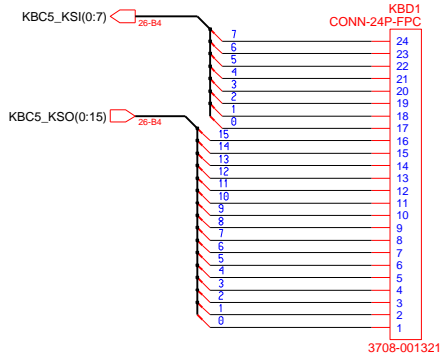
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CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1			PART NO. BA11-0XXXXA
MODULE CODE		LAST EDIT		August 22, 2008 10:40:53 AM	PAGE	30 OF 44

HDMI & DVI I/F

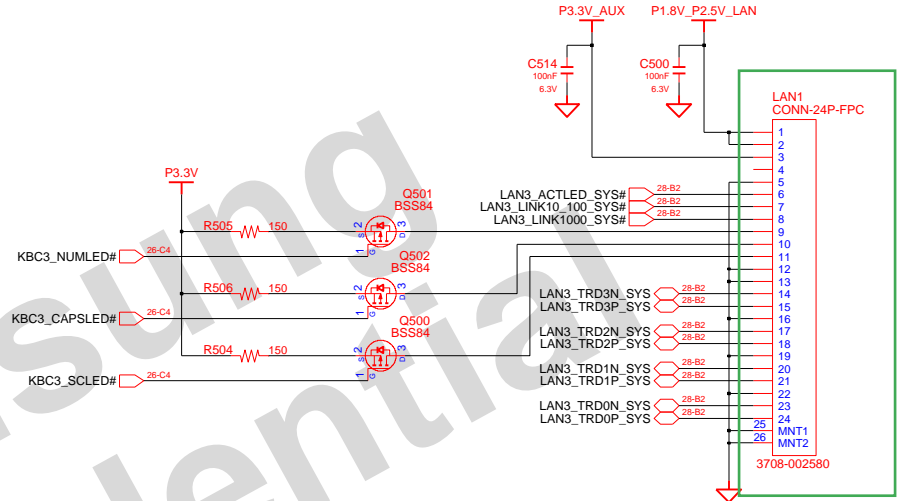


DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	HDMI & DVI I/F		
APPROVAL	JS, EUH	REV	1.1			PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT			August 22, 2008 10:40:53 AM	PAGE	31 OF 44

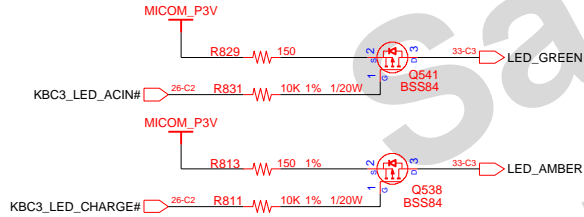
KEYBOARD CONNECTOR



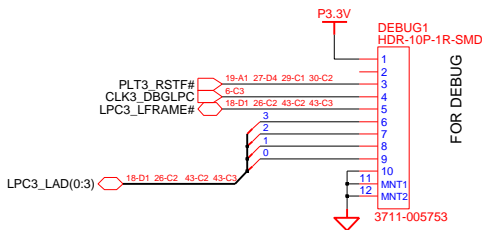
LAN BOARD CONNECTOR



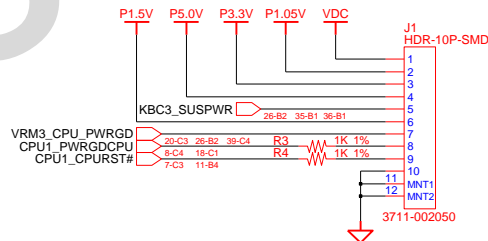
ADAPTERIN / CHARGING LED



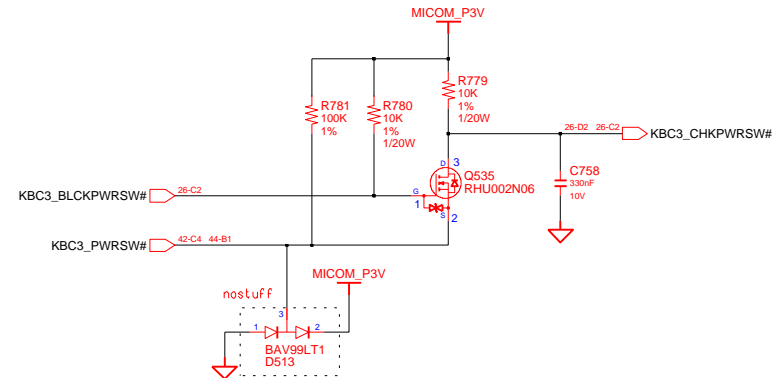
DEBUG PORT



Pre FCT PORT

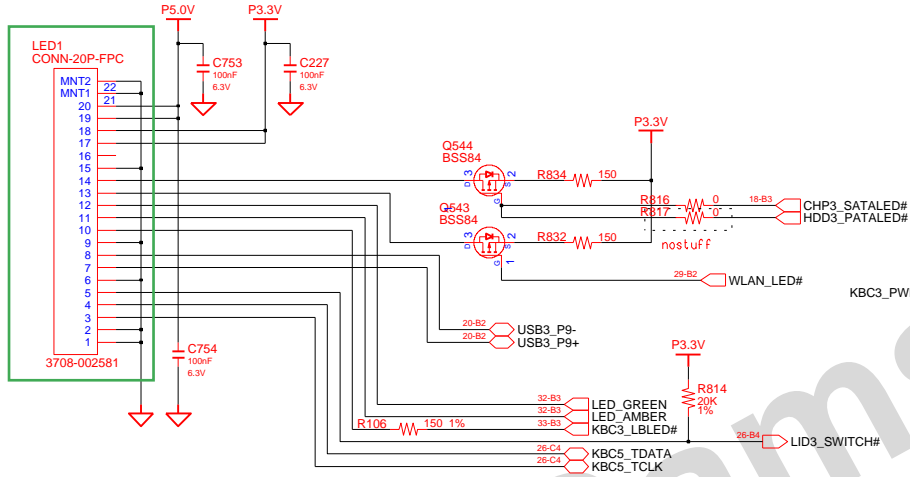


POWER S/W

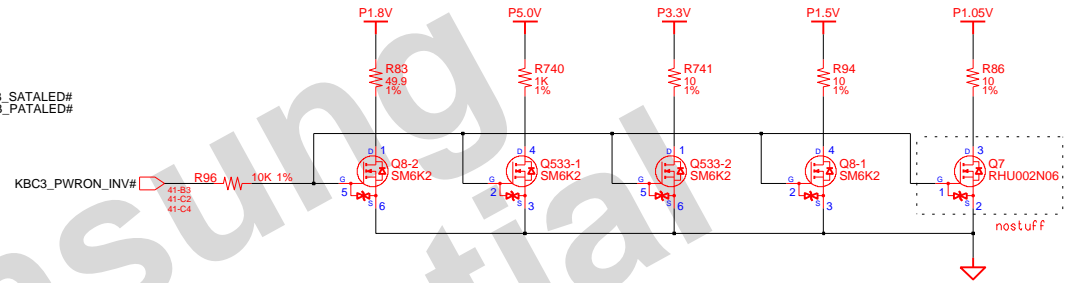


DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	PART NO. BA11-0XXXXA
CHECK	HJ, KIM	DEV. STEP	MP	KBD/LED/DEBUG/SUB CONN.		
APPROVAL	JS, EUH	REV	1.1	August 22, 2008 10:40:53 AM		PAGE 32 OF 44
MODULE CODE	LAST EDIT					

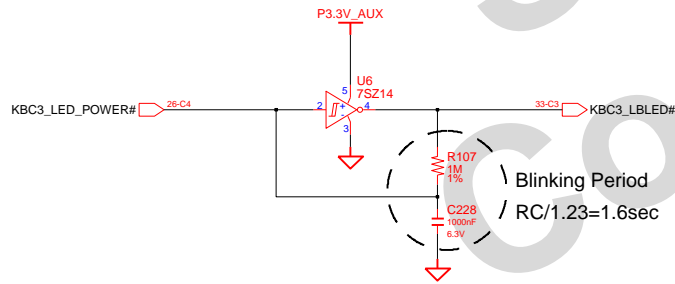
LED & T/P FPC CONNECTOR



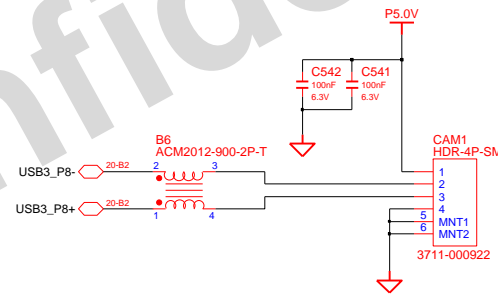
DISCHARGE



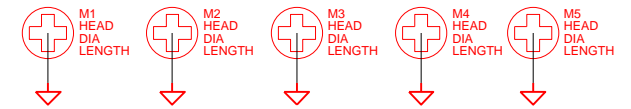
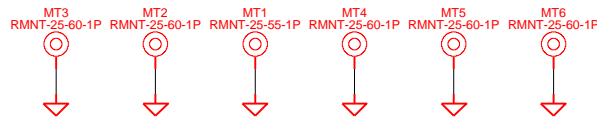
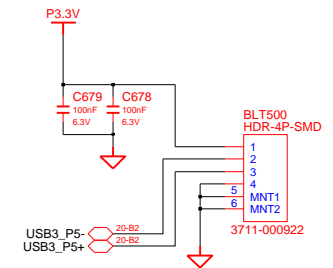
POWR ON / LB LED



CAMERA



BLUETOOTH



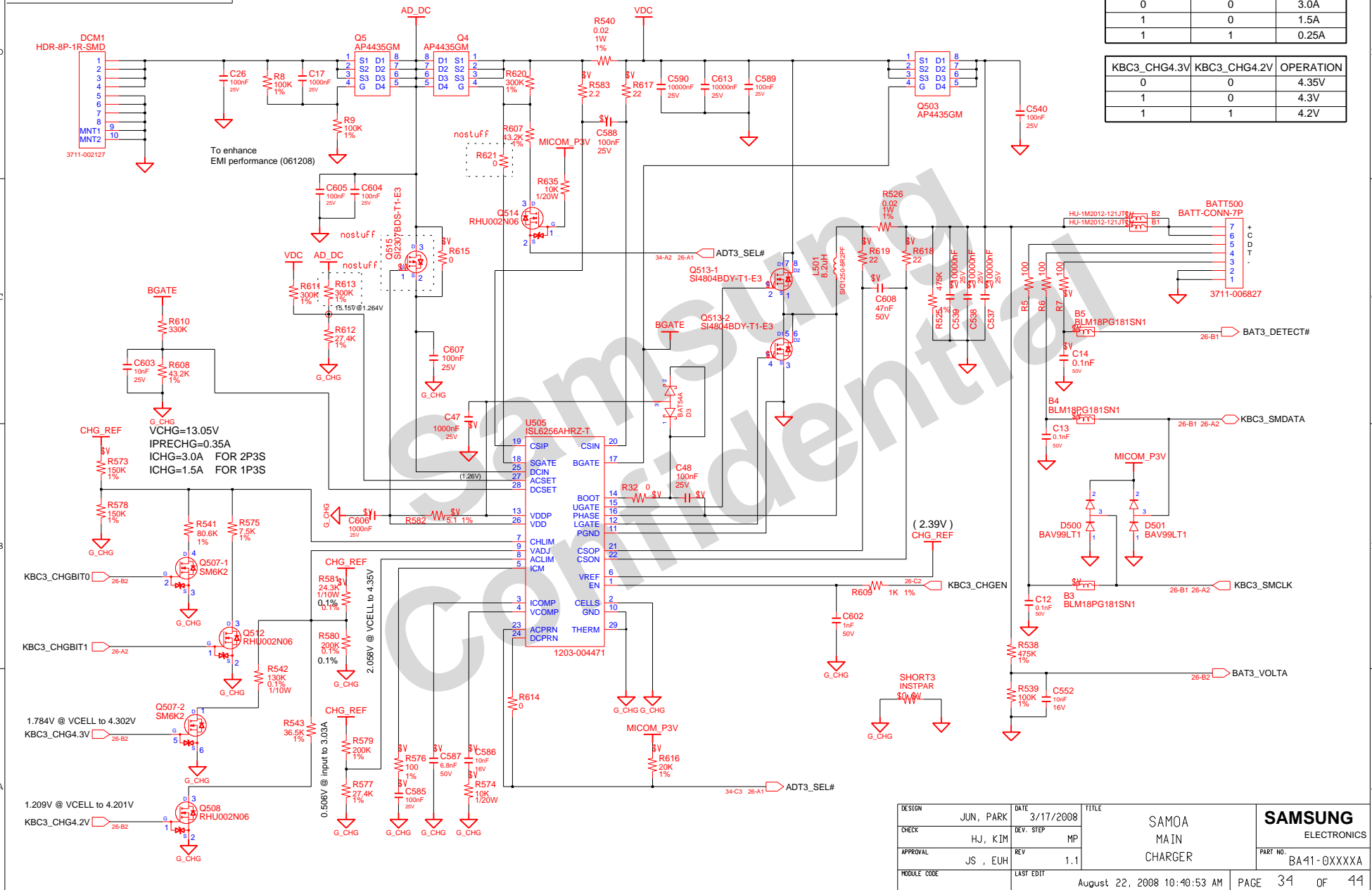
DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN		SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	CAMERA, BLUETOOTH & LED		PART NO.	
APPROVAL	JS, EUH	REV	1.1	August 22, 2008 10:40:53 AM		BA41-0XXXXA	PAGE 33 OF 44
MODULE CODE	LAST EDIT						

CHARGER & POWER MANAGEMENT

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KBC3_CHGBIT0	KBC3_CHGBIT1	OPERATION
0	0	3.0A
1	0	1.5A
1	1	0.25A

KBC3_CHG4.3V	KBC3_CHG4.2V	OPERATION
0	0	4.35V
1	0	4.3V
1	1	4.2V

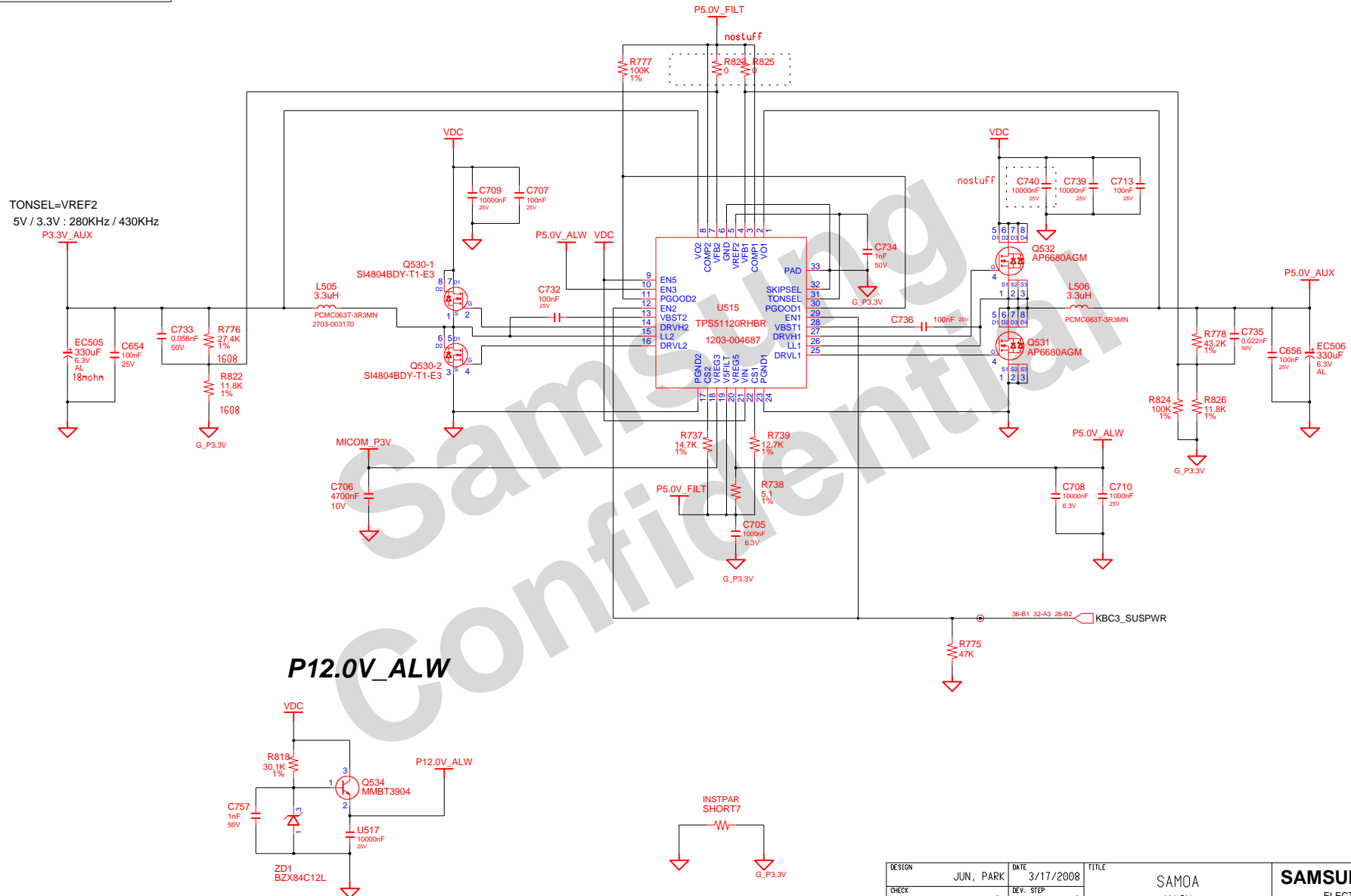


DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN CHARGER
CHECK	HJ, KIM	DEV. STEP	MP		
APPROVAL	JS, EUH	REV	1.1		
MODULE CODE	LAST EDIT			PART NO. BA11-0XXXXA	
August 22, 2008 10:40:53 AM				PAGE	34 OF 44

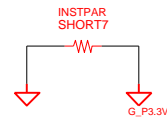
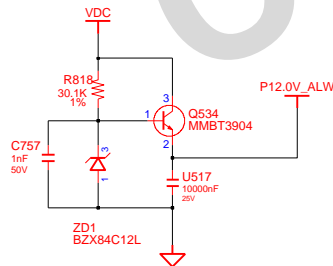
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P5.0V_AUX & P3.3V_AUX

TONSEL=VREF2
 5V / 3.3V : 280KHz / 430KHz
 P3.3V_AUX

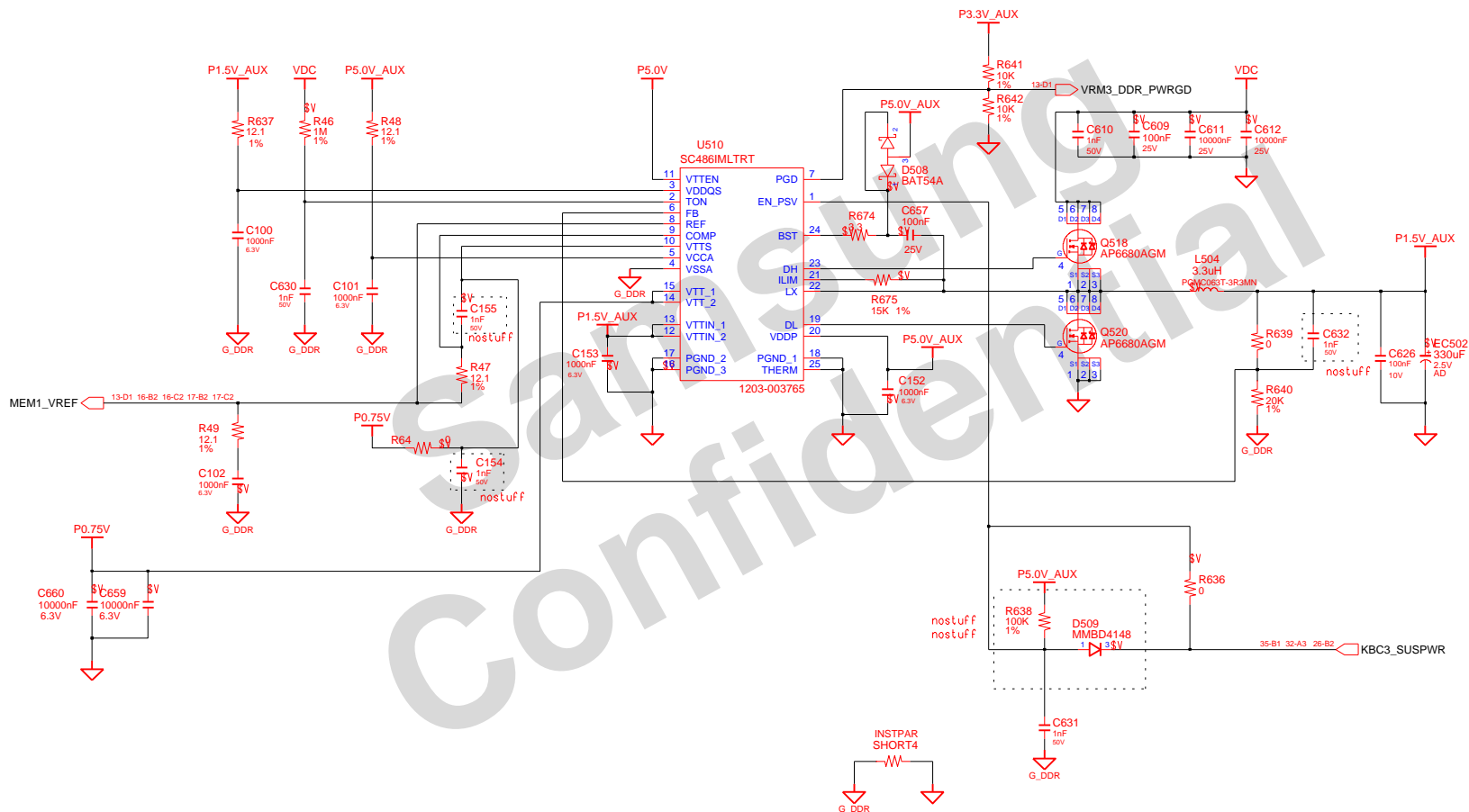


P12.0V_ALW



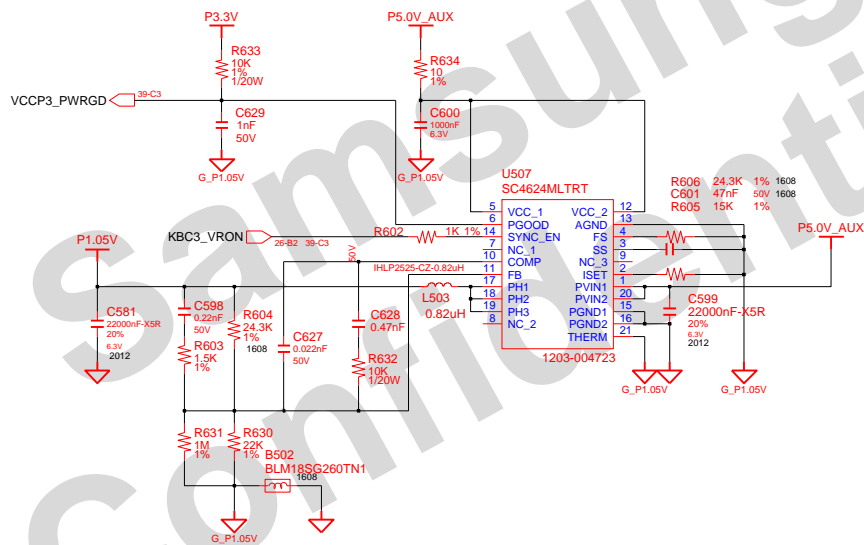
DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	P5.0V & P3.3V		
APPROVAL	JS, EUH	REV	1.1	PART NO. BA41-0XXXXA		PAGE 35 OF 44
MODULE CODE	LAST EDIT		August 22, 2008 10:40:53 AM			

DDR3 Power



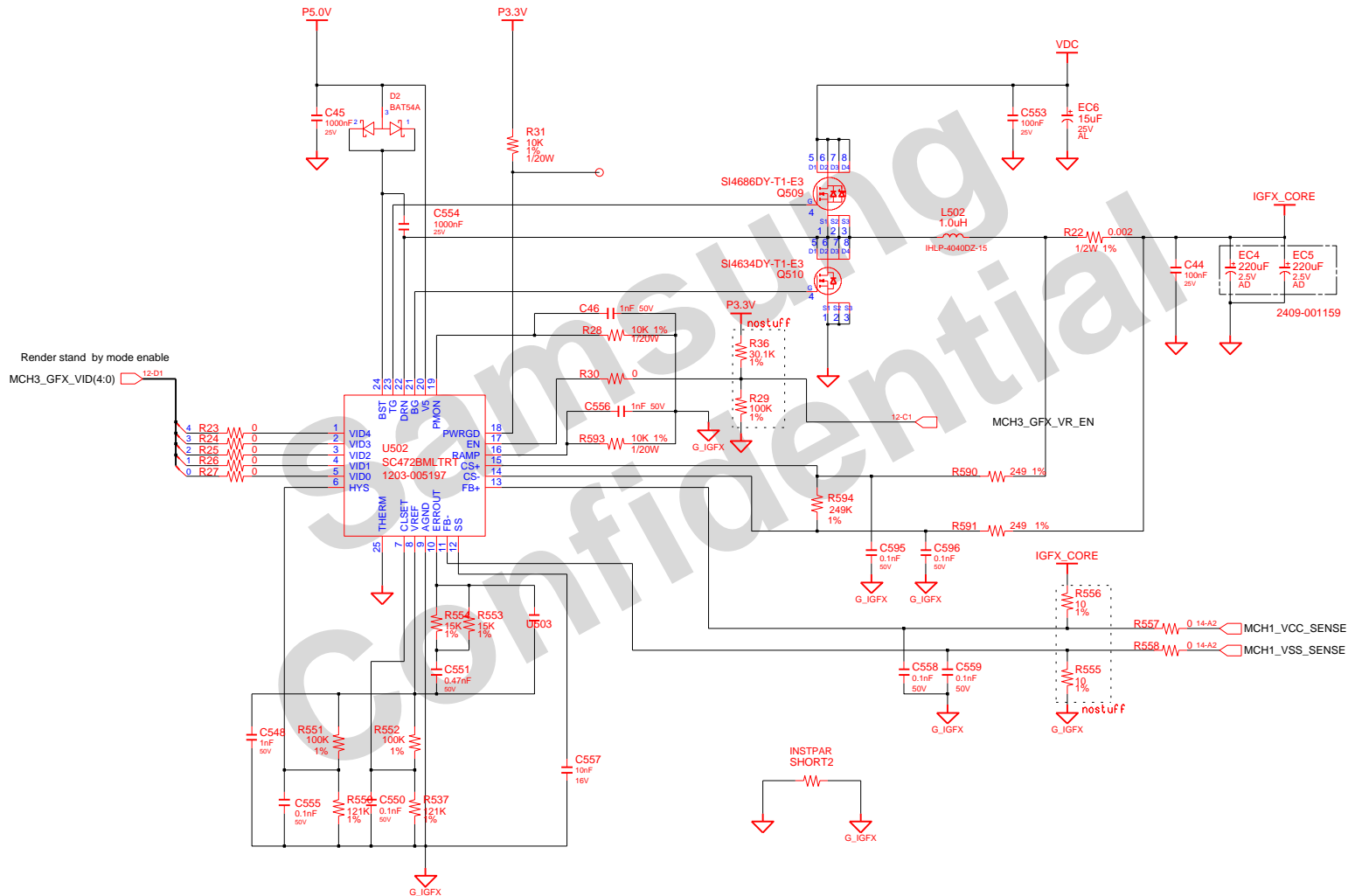
DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	DDR3 POWER		
APPROVAL	JS, EUH	REV	1.1			PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT			August 22, 2008 10:40:53 AM	PAGE	36 OF 44

VCCP_CORE



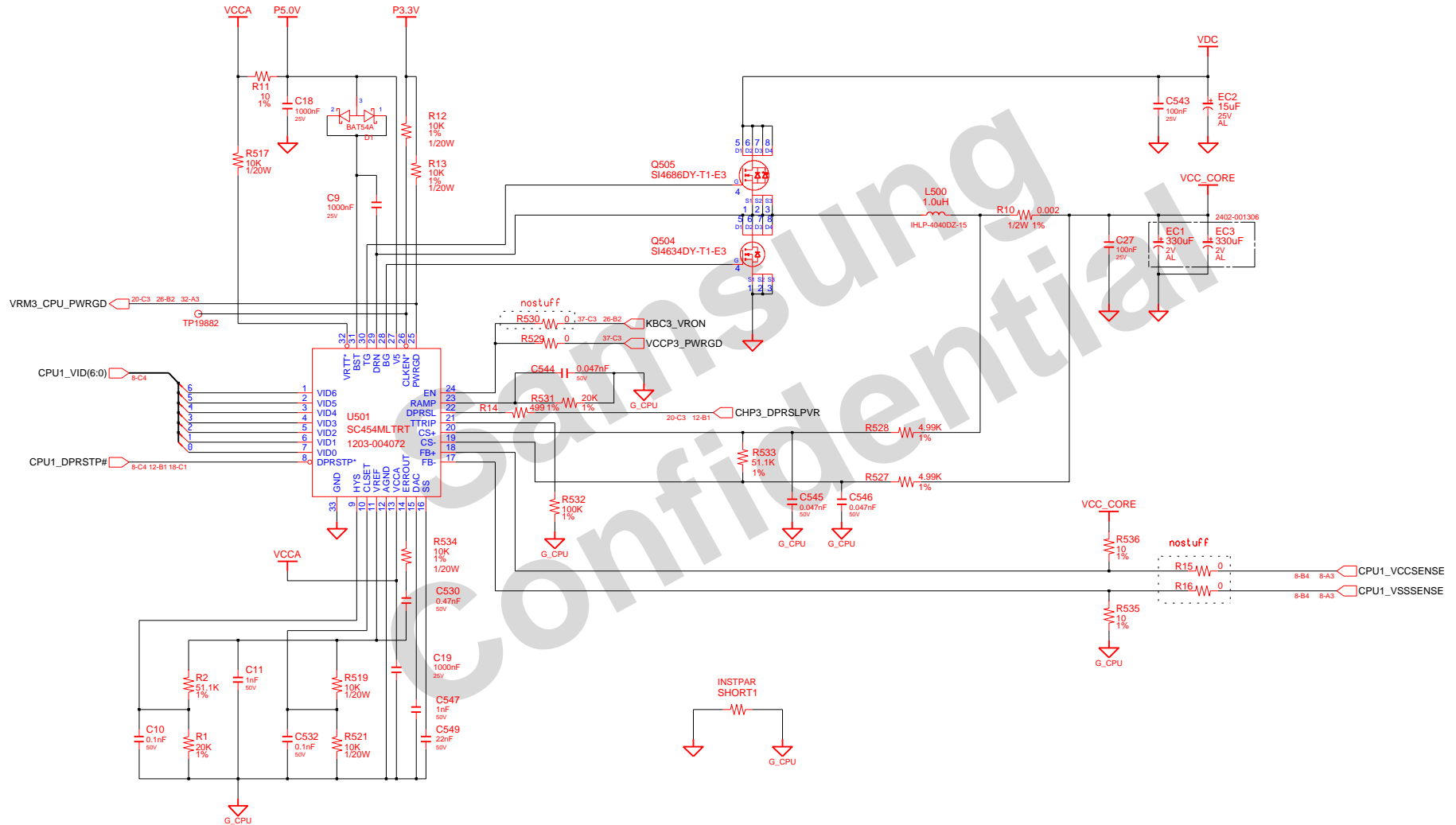
DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN DDR2 POWER	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1		PART NO.	BA41-0XXXXA
MODULE CODE		LAST EDIT	August 22, 2008 10:40:53 AM		PAGE	37 OF 44

INTERNAL GFX CORE



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	INTERNAL GFX CORE		
APPROVAL	JS, EUH	REV	1.1	INTERNAL GFX CORE		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT			August 22, 2008 10:40:53 AM	PAGE	38 OF 44

CPU VRM POWER

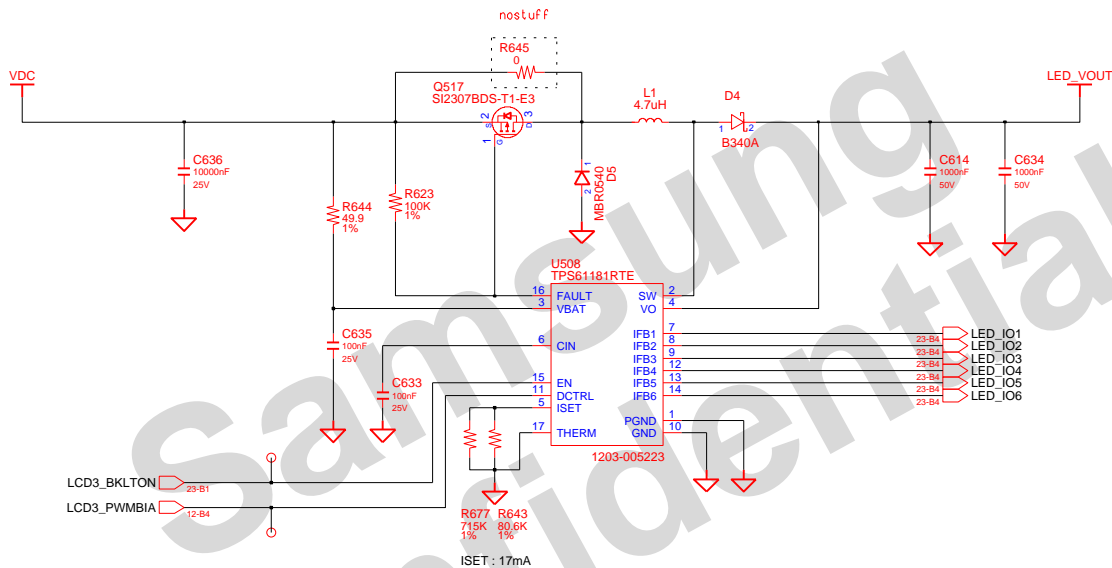


DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN CPU VRM POWER	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1		PART NO.	BA41-0XXXXA
MODULE CODE		LAST EDIT	August 22, 2008 10:40:53 AM	PAGE	39	OF 44

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LED DRIVER



LCD3_BKLTON 23-B1

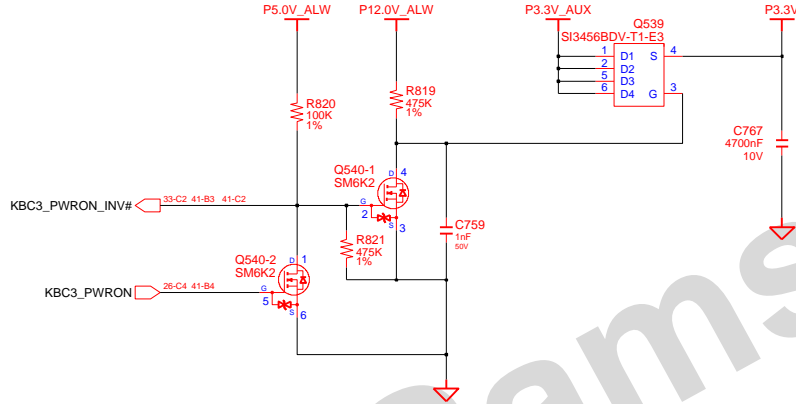
LCD3_PWMBIA 12-B4

ISET : 17mA

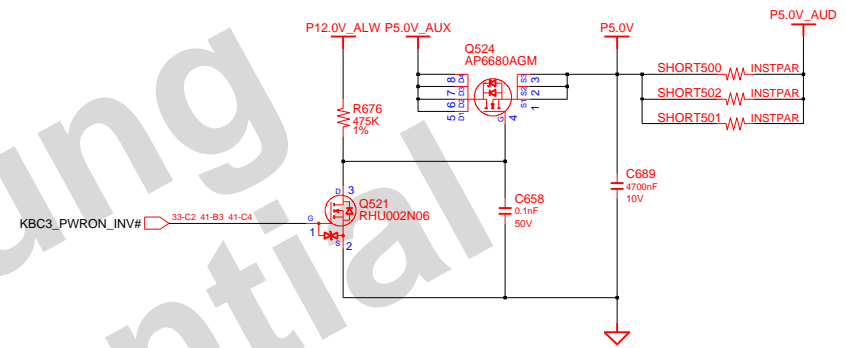
DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN LED DRIVER	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1	PART NO.	BA41-0XXXXA	
MODULE CODE		LAST EDIT	August 22, 2008 10:40:53 AM	PAGE	40	OF 44

SWITCHED POWER

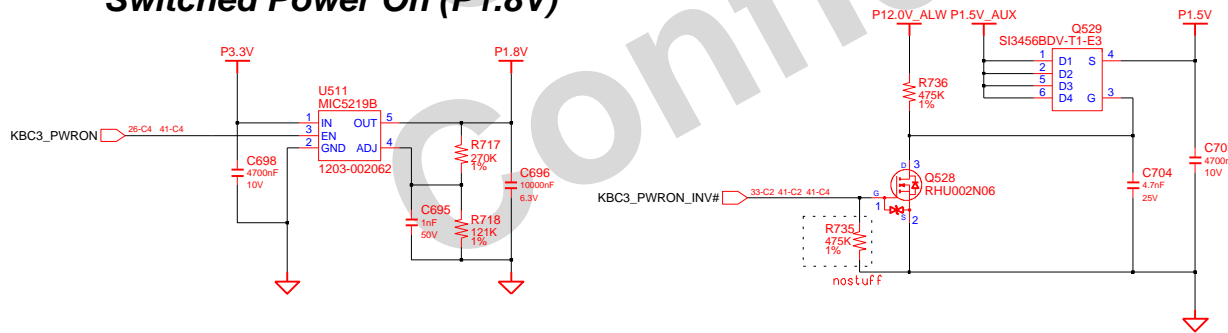
Switched Power On (P3.3V)



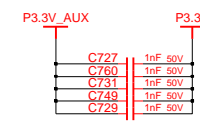
Switched Power On (P5V)



Switched Power On (P1.5V)

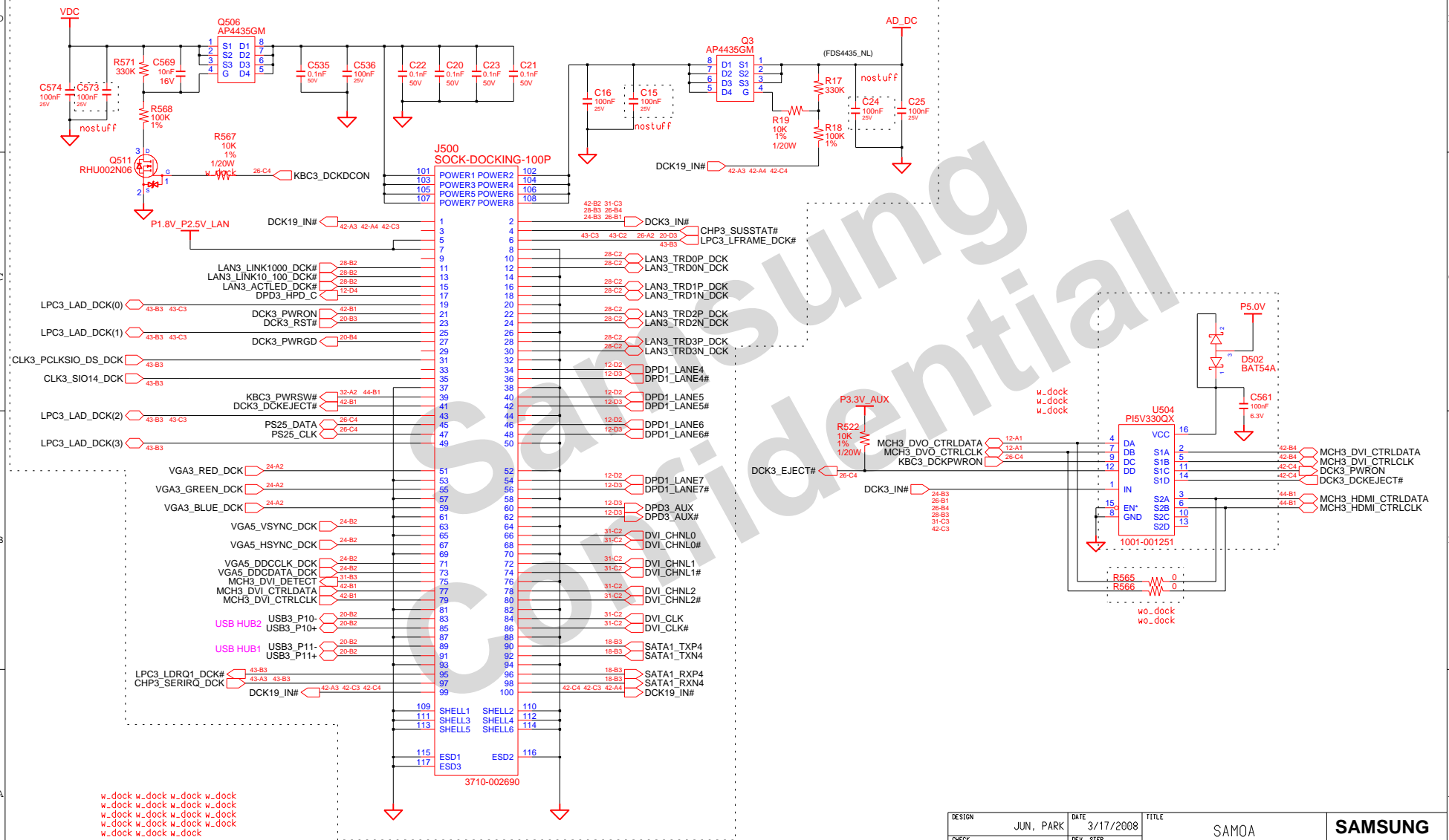


Stiching caps(For EMC)



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	SWITCHED POWER		
APPROVAL	JS, EUH	REV	1.1	August 22, 2008 10:40:53 AM		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT			PAGE	41	OF 44

DOCKING CONNECTOR

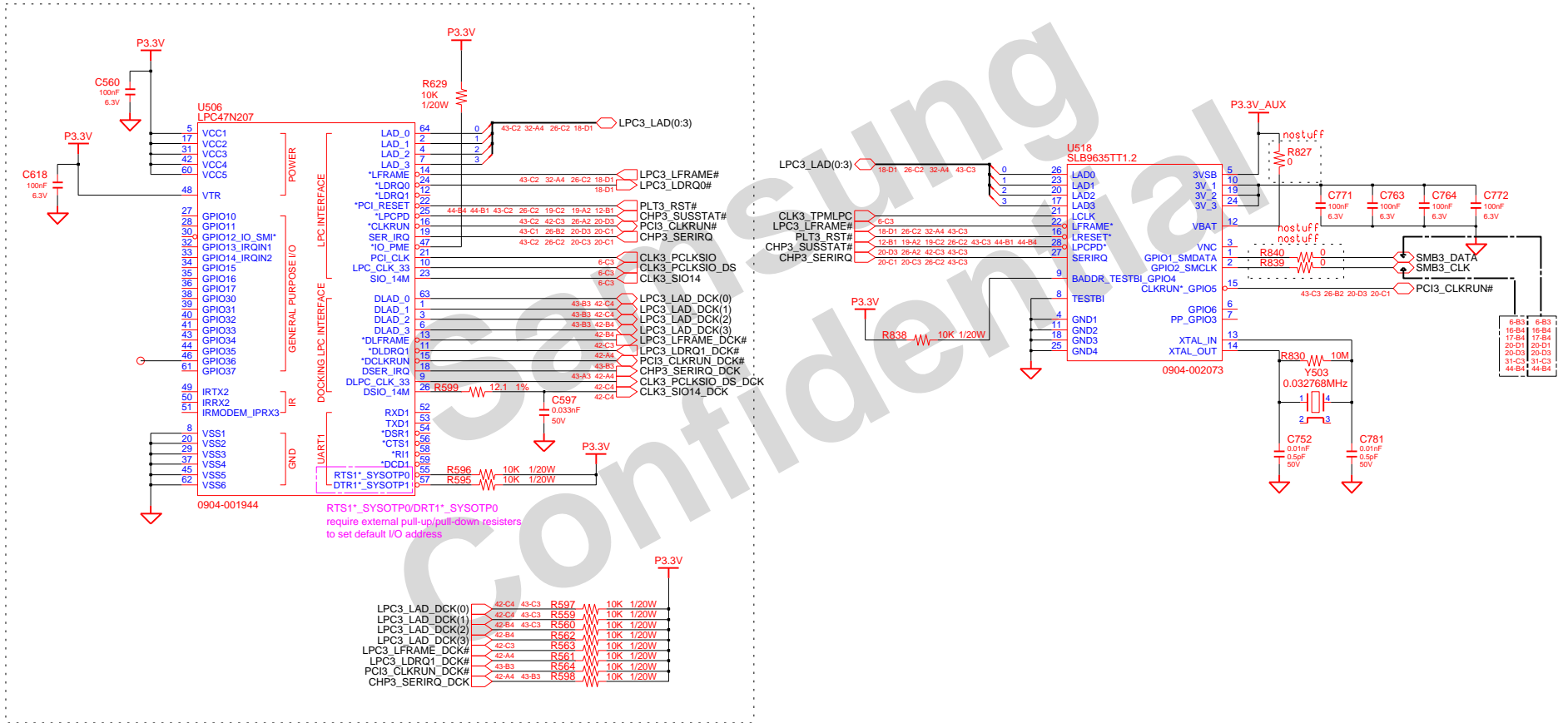


DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN DOCKING I/F	SAMSUNG ELECTRONICS PART NO. BA41-0XXXXA
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1			
MODULE CODE		LAST EDIT				

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LPC I/F

TPM 1.2



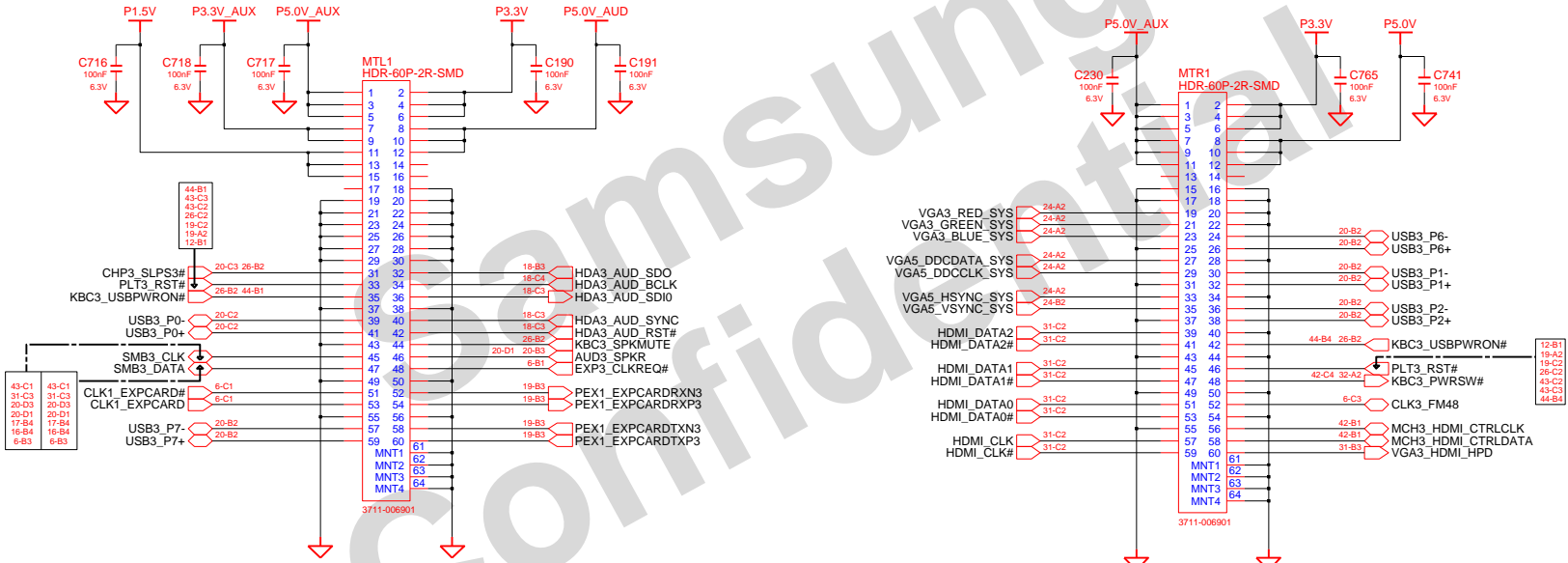
w_dock w_dock
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 w_dock w_dock
 w_dock w_dock
 w_dock w_dock
 w_dock w_dock
 w_dock w_dock

DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN LPC I/F	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1			
MODULE CODE		LAST EDIT				
				August 22, 2008 10:40:53 AM	PAGE	43 OF 44

MAIN to SUB CONNECTOR

FOR SUB_LEFT BOARD

FOR SUB_RIGHT BOARD



DESIGN	JUN, PARK	DATE	1/4/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	LEFT SUB CONNECTOR		
APPROVAL	JS, EUH	REV	1.1			PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT			August 22, 2008 10:40:53 AM	PAGE 44	OF 44

SAMOA SUB

CPU : PENRYN SFF
 Chip Set : CANTIGA GS & ICH9M SFF
 Remarks : INTEL MONTEVINA SFF

Model Name : SAMOA SUB BOARD
 PCB Code : BA41-00903A(Nanya_CHN)
 BA41-00904A(GCE_CHN)
 Dev. Step : PR/MP
 Revision : 1.1
 T.R. Date :

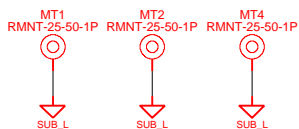
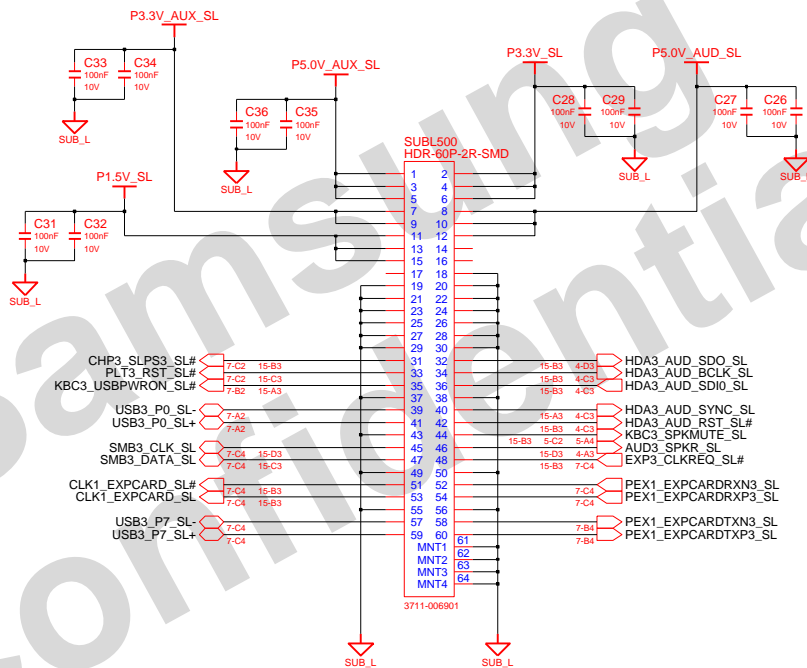
DESIGN	CHECK	APPROVAL
Jun PARK	HJ KIM	JS EUH

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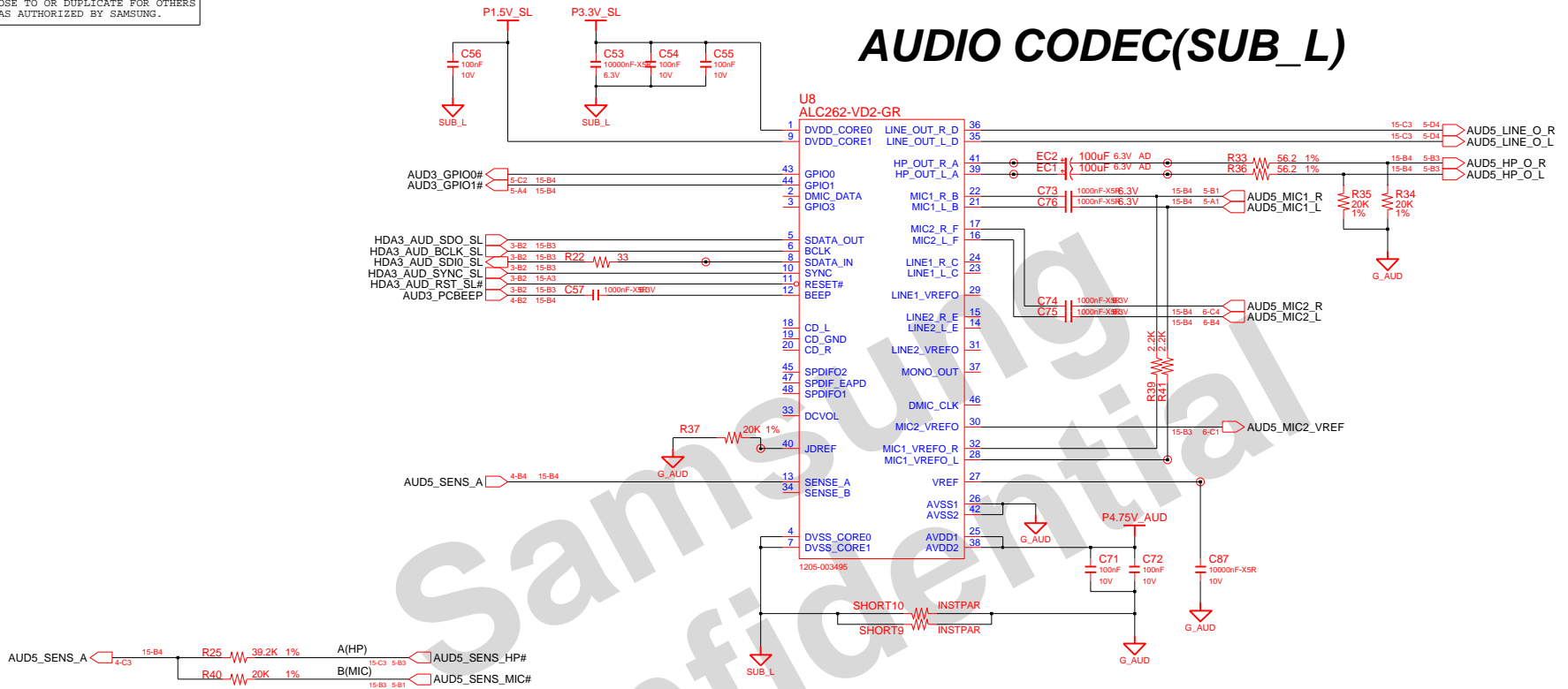
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CHECK	HJ, KIM	DEV. STEP	MP	PART NO.			BA41-#####A
APPROVAL	JS, EUH	REV	1.1				
MODULE CODE		LAST EDIT	August 22, 2008 10:42:11 AM		PAGE	1 OF 15	

MAIN to SUB CONNECTOR(SUB_L)

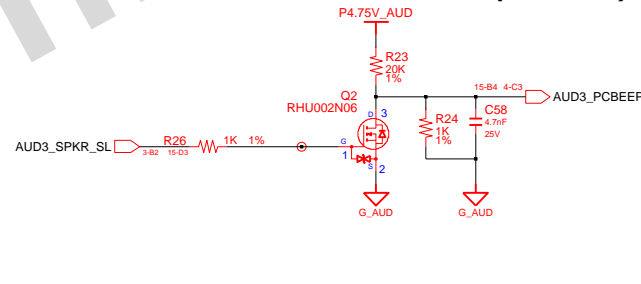
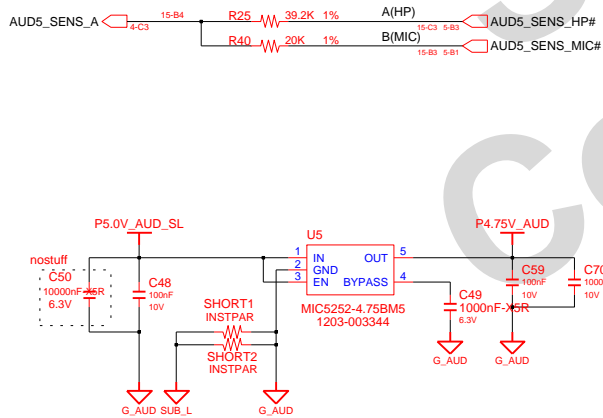


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APPROVAL	JS, EUH	REV	1.1	PART NO. BA41-####A		
MODULE CODE	LAST EDIT			August 22, 2008 10:42:11 AM	PAGE	3 OF 15

AUDIO CODEC(SUB_L)

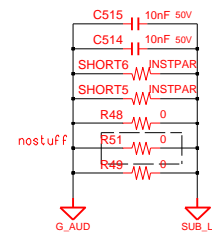


PC BEEP SOUND(SUB_L)



1.AGND_AUD	Audio Ground
2.GND	Digital Ground

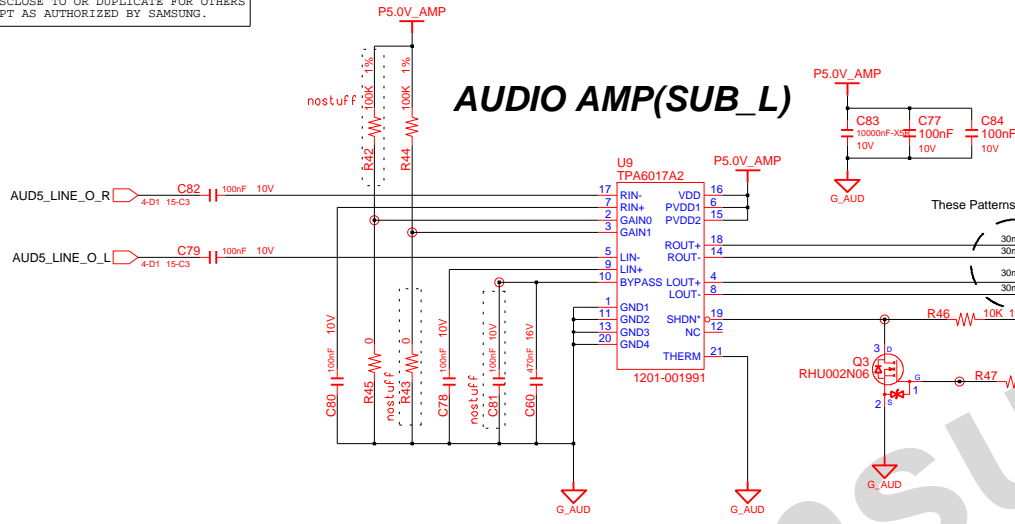
ALL 1608 SIZE



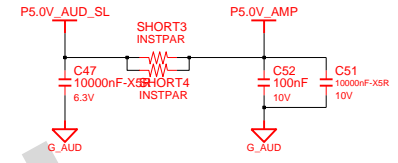
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CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1			PART NO. BA41-#####A
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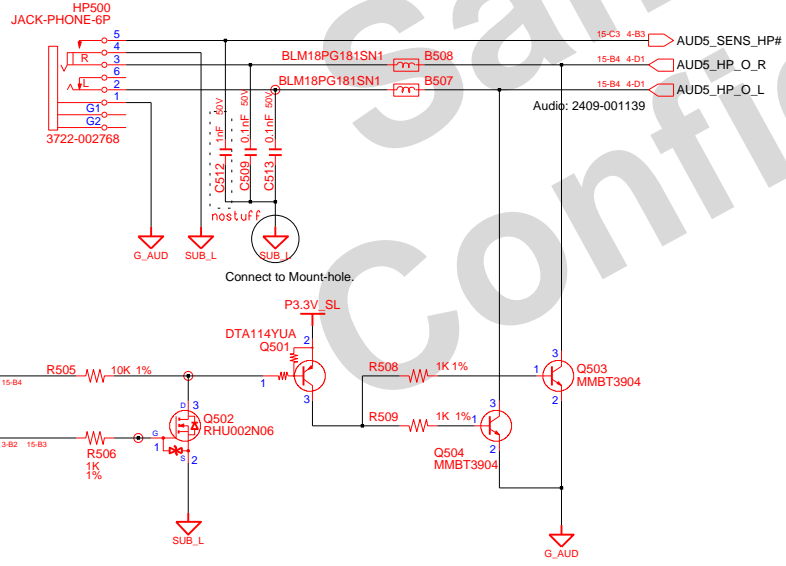
AUDIO AMP(SUB_L)



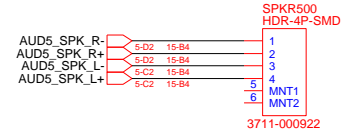
AMP_VDD(SUB_L)



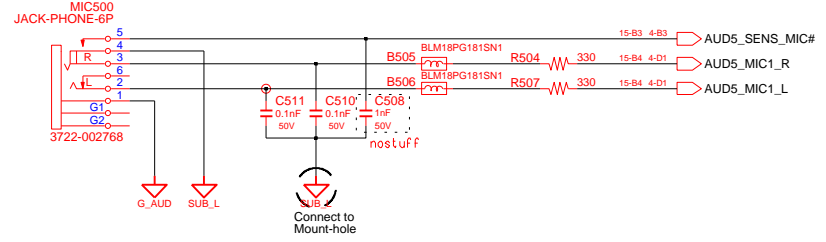
HEADPHONE(SUB_L)



INTERNAL STEREO SPEAKERS(SUB_L)

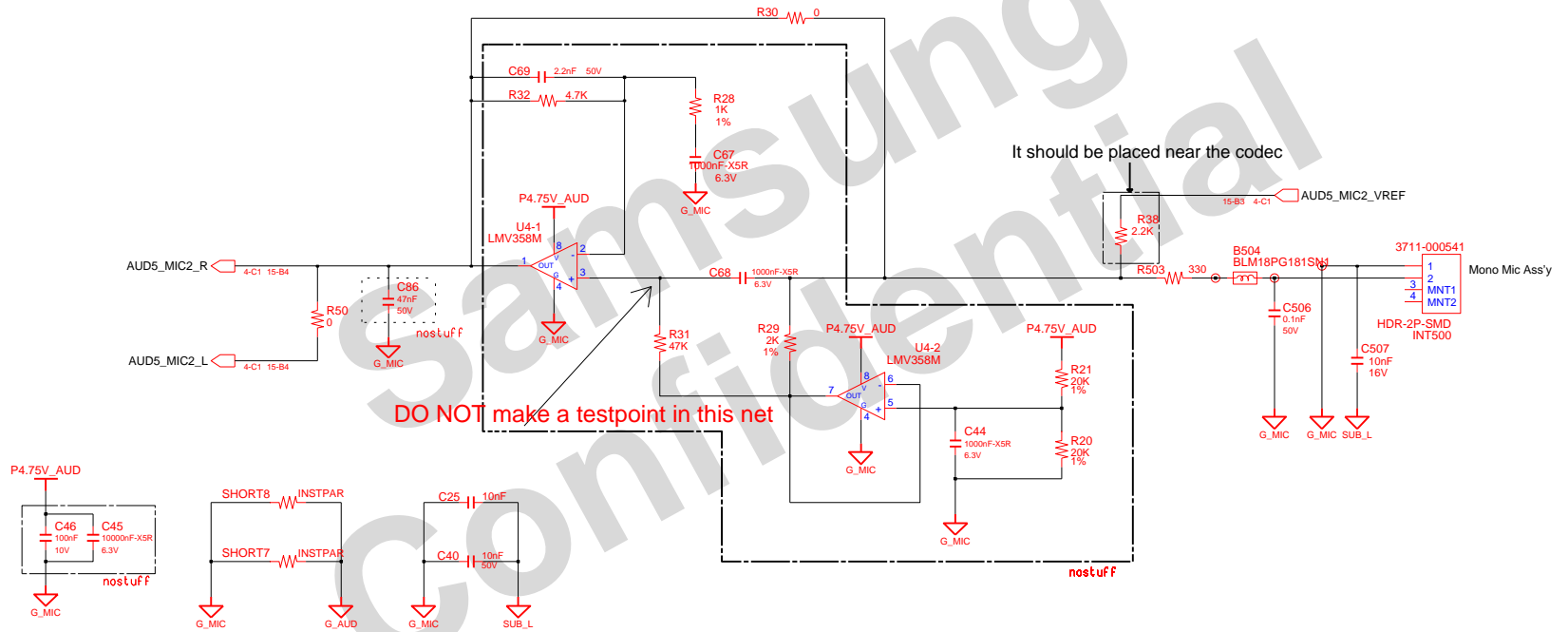


MIC JACK(SUB_L)



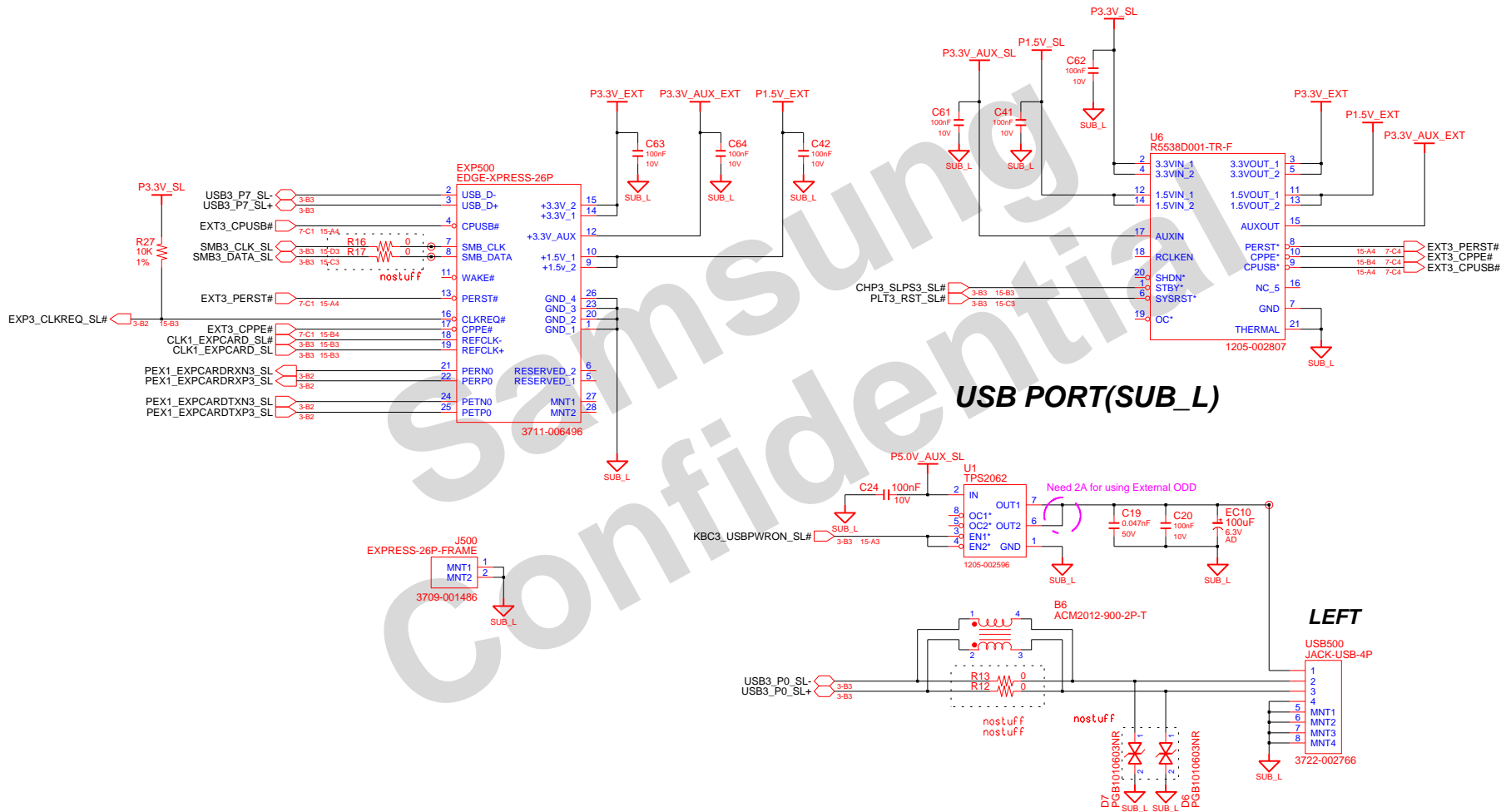
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CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1		PART NO.	BA41-####A
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INTERNAL MIC(SUB_L)



DESIGN	JUN, PARK	DATE	1/17/2008	TITLE	SAMOA SUB LEFT INTERNAL MIC	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1			
MODULE CODE		LAST EDIT	August 22, 2008 10:42:11 AM	PAGE 6 OF 15		

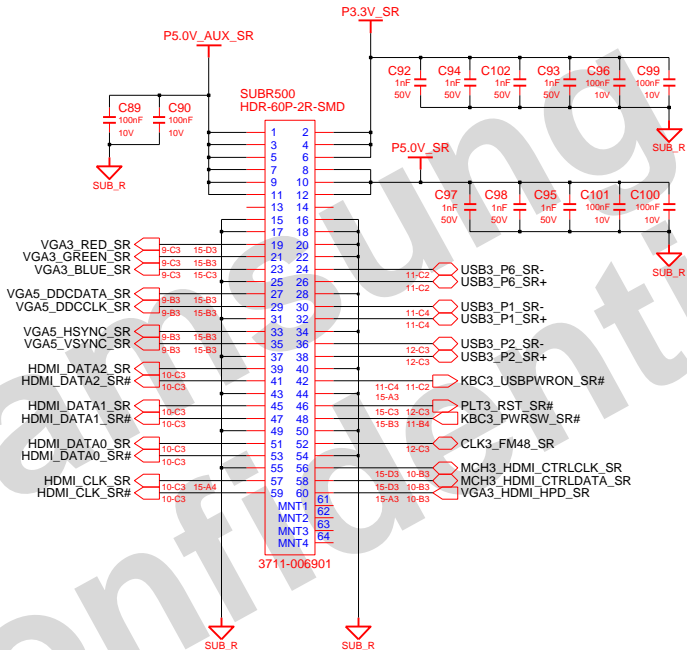
EXPRESS CARD(SUB_L)



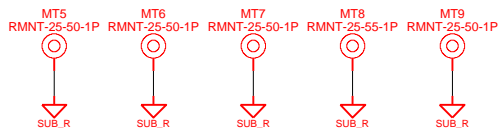
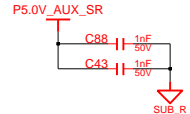
USB PORT(SUB_L)

DESIGN	JUN, PARK	DATE	1/17/2008	TITLE	SAMOA SUB LEFT	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	EXPRESS CARD & USB PORT		
APPROVAL	JS, EUH	REV	1.1	PART NO. BA41-#####A		
MODULE CODE		LAST EDIT	August 22, 2008 10:42:11 AM	PAGE	7	OF 15

MAIN to SUB CONNECTOR(SUB_R)

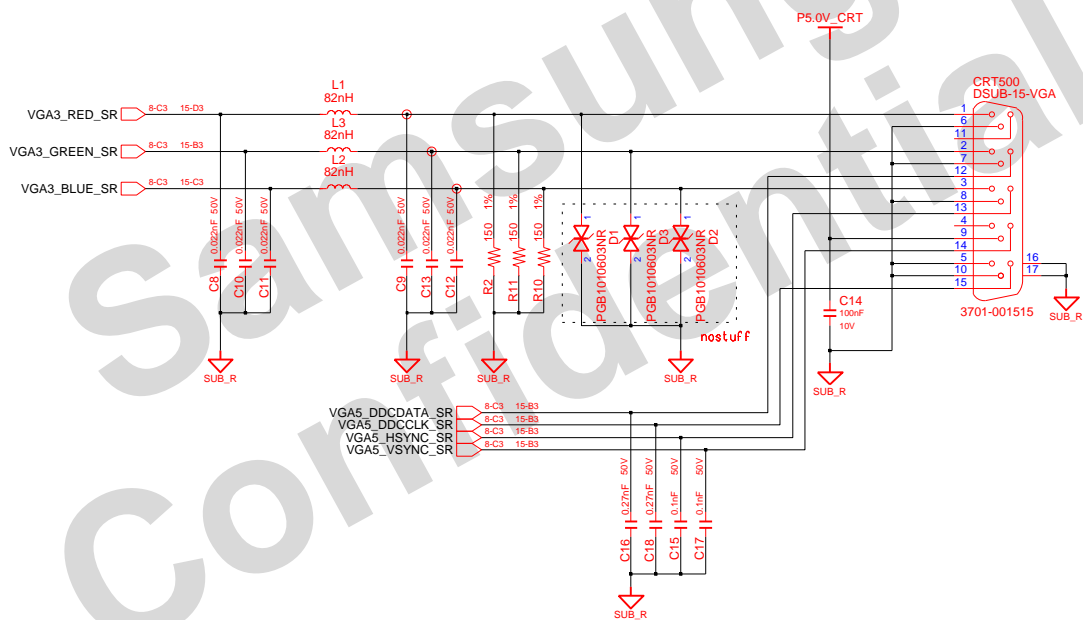


Stiching caps(For EMC)



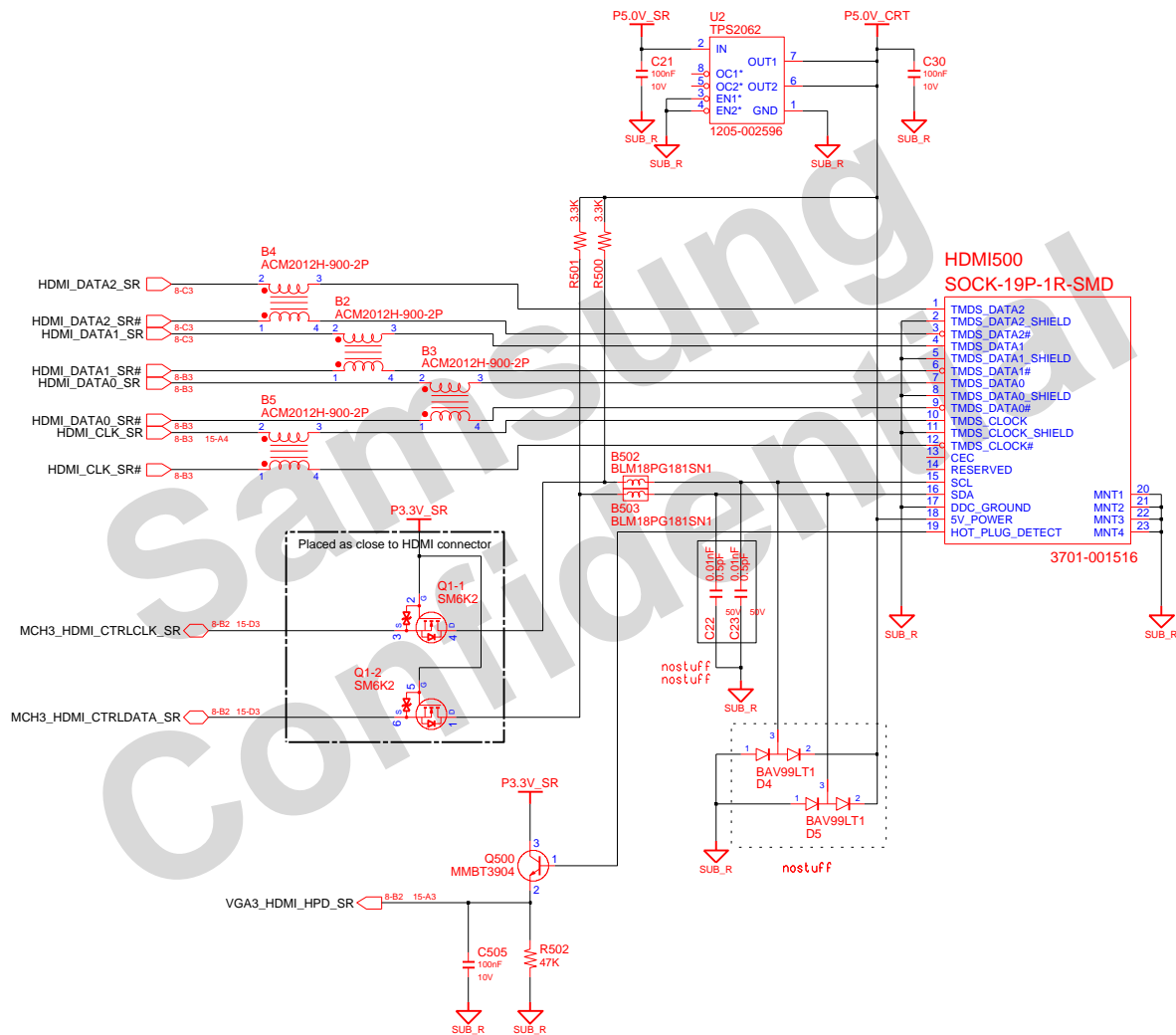
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APPROVAL	JS, EUH	REV	1.1	PART NO.	BA41-#####A	
MODULE CODE	LAST EDIT			August 22, 2008 10:42:11 AM	PAGE 8 OF 15	

CRT CONNECTOR(SUB_R)



DESIGN	JUN, PARK	DATE	1/17/2008	TITLE	SAMOA SUB RIGHT CRT CONNECTOR	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1		PART NO.	BA41-####A
MODULE CODE		LAST EDIT	August 22, 2008 10:42:11 AM	PAGE	9	OF 15

HDMI CONNECTOR(SUB_R)

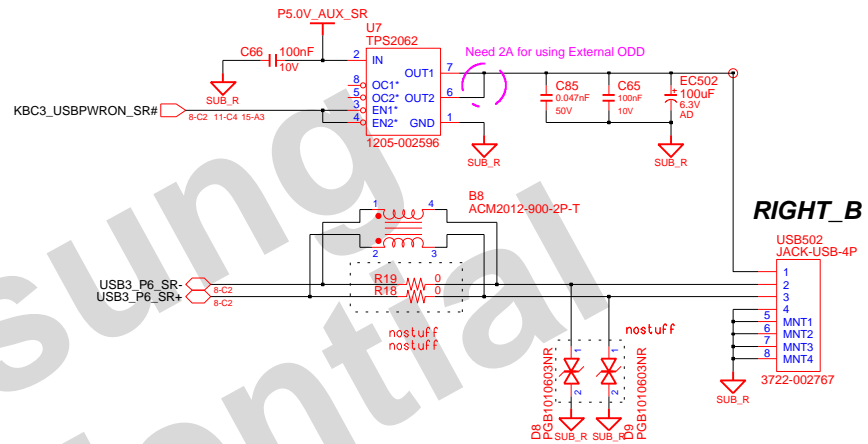
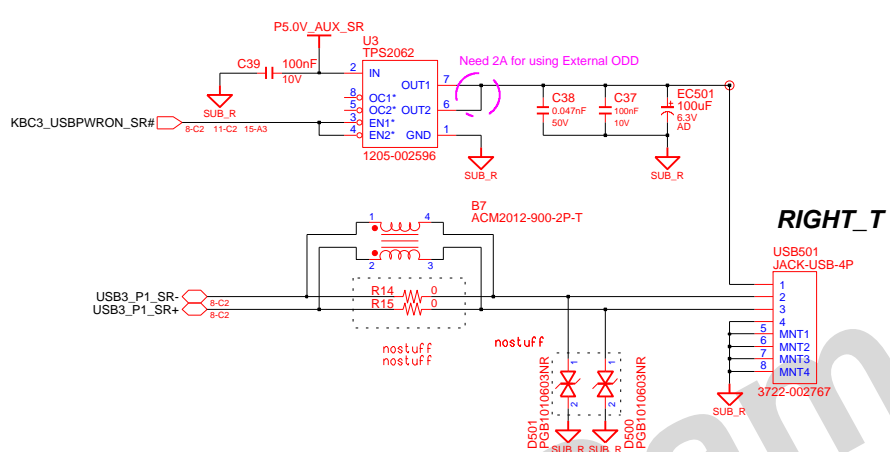


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CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1		PART NO.	BA41-#####A
MODULE CODE		LAST EDIT	August 22, 2008 10:42:11 AM	PAGE	10	OF 15

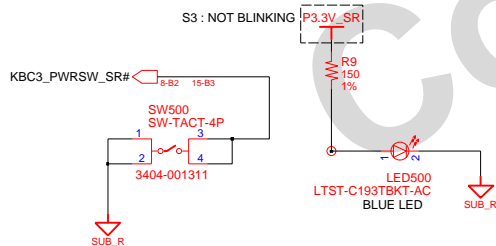
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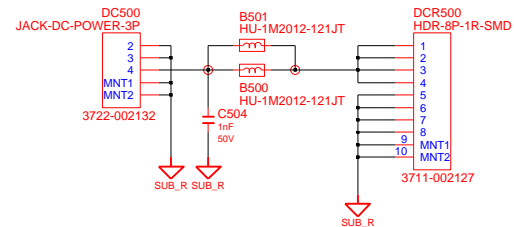
USB PORT(SUB_R)



POWER S/W(SUB_R)



DC JACK(SUB_R)

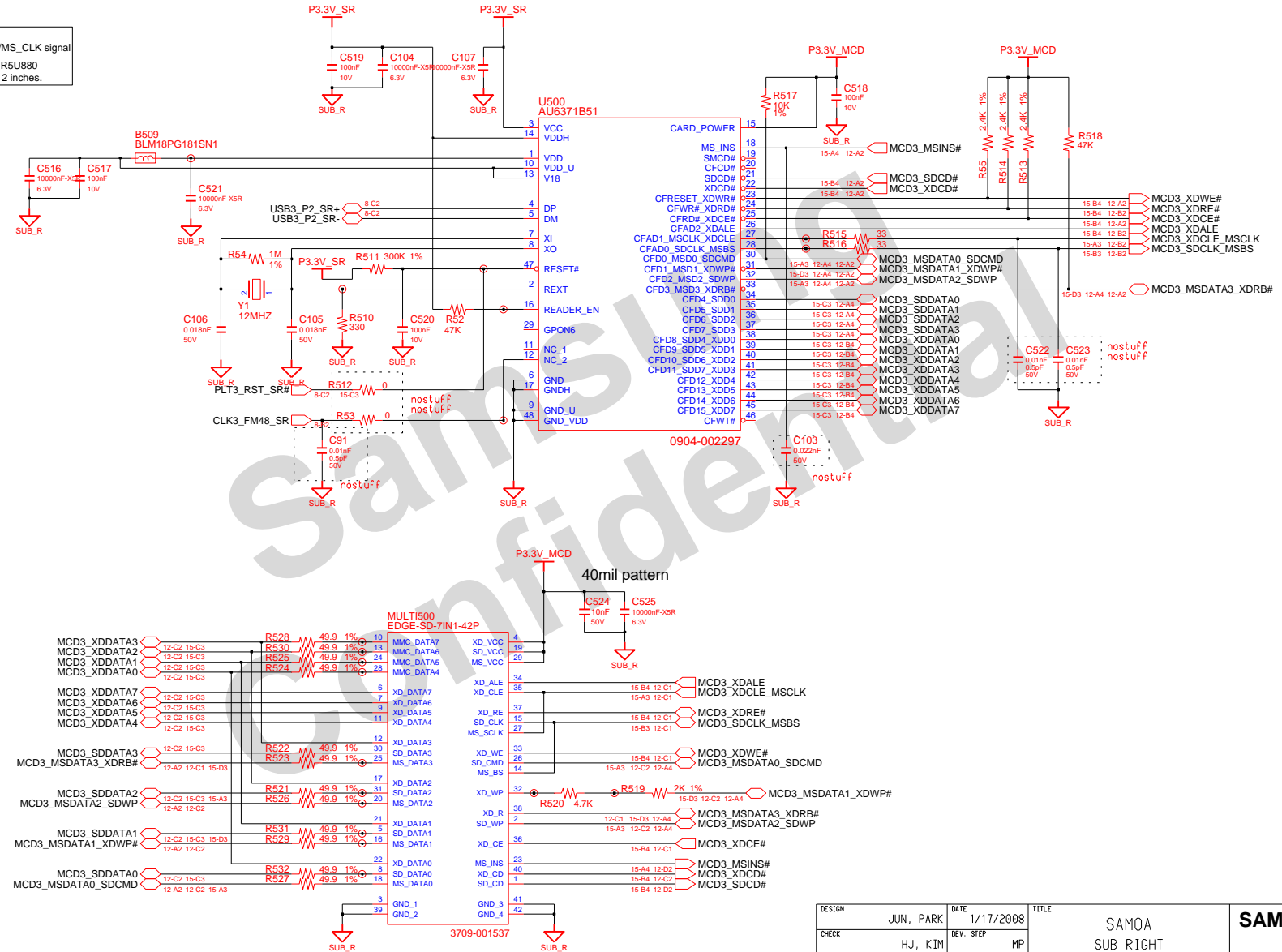


DESIGN	JUN, PARK	DATE	1/17/2008	TITLE	SAMOA SUB RIGHT	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	USB,POWER S/W&DC JACK		
APPROVAL	JS, EUH	REV	1.1		PART NO.	BA41-####A
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CARD READER(AU6371, SUB_R)

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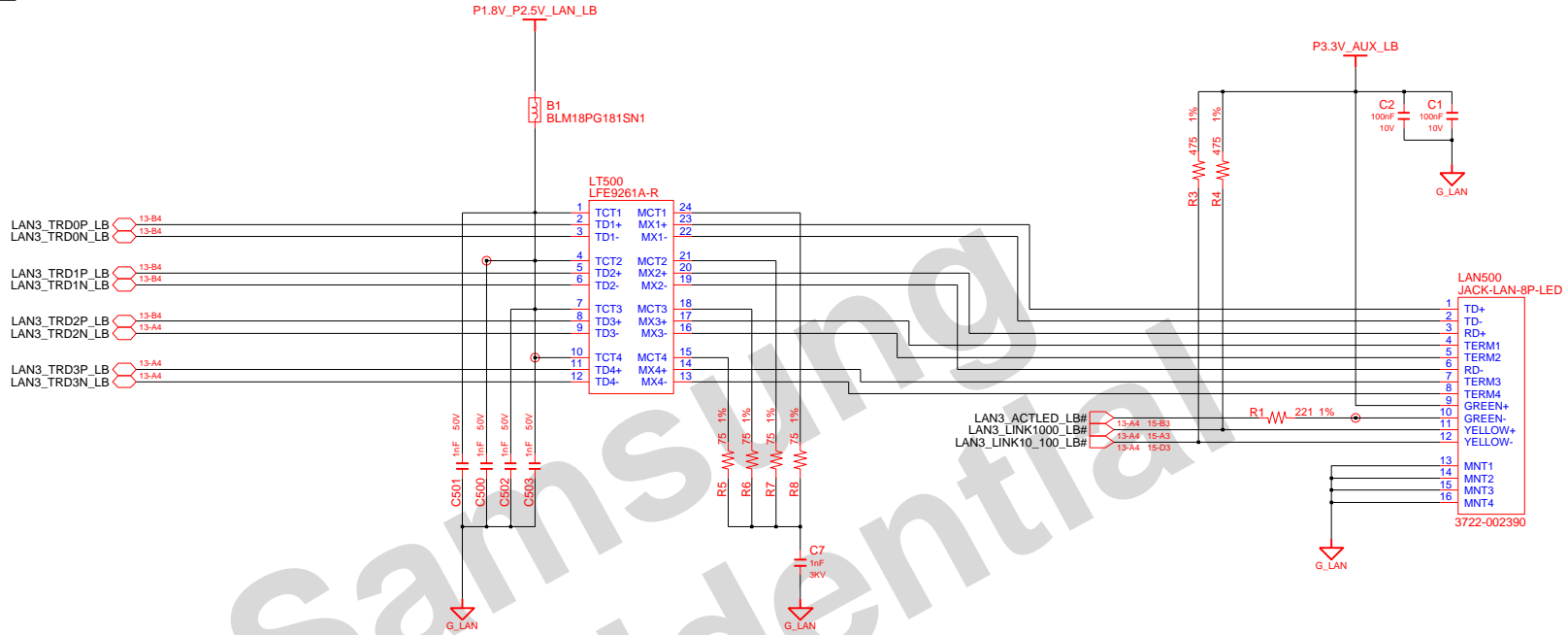
40mil pattern
 Apply shield GND for SD/MMC/MS_CLK signal
 P3.3V_MCD distance between R5U880
 and socket should be less than 2 inches.



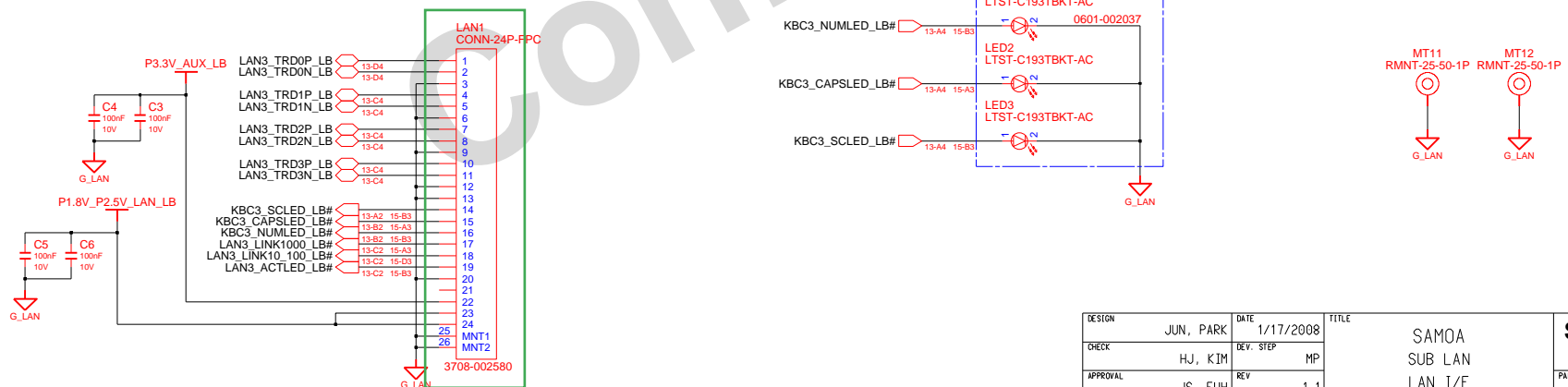
40 mil trace for medica card socket ground

DESIGN	JUN, PARK	DATE	1/17/2008	TITLE	SAMOA SUB RIGHT	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	CARD READER & 7-IN-1		
APPROVAL	JS, EUH	REV	1.1	PART NO. BA41-#####		PAGE 12 OF 15
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LAN JACK BOARD

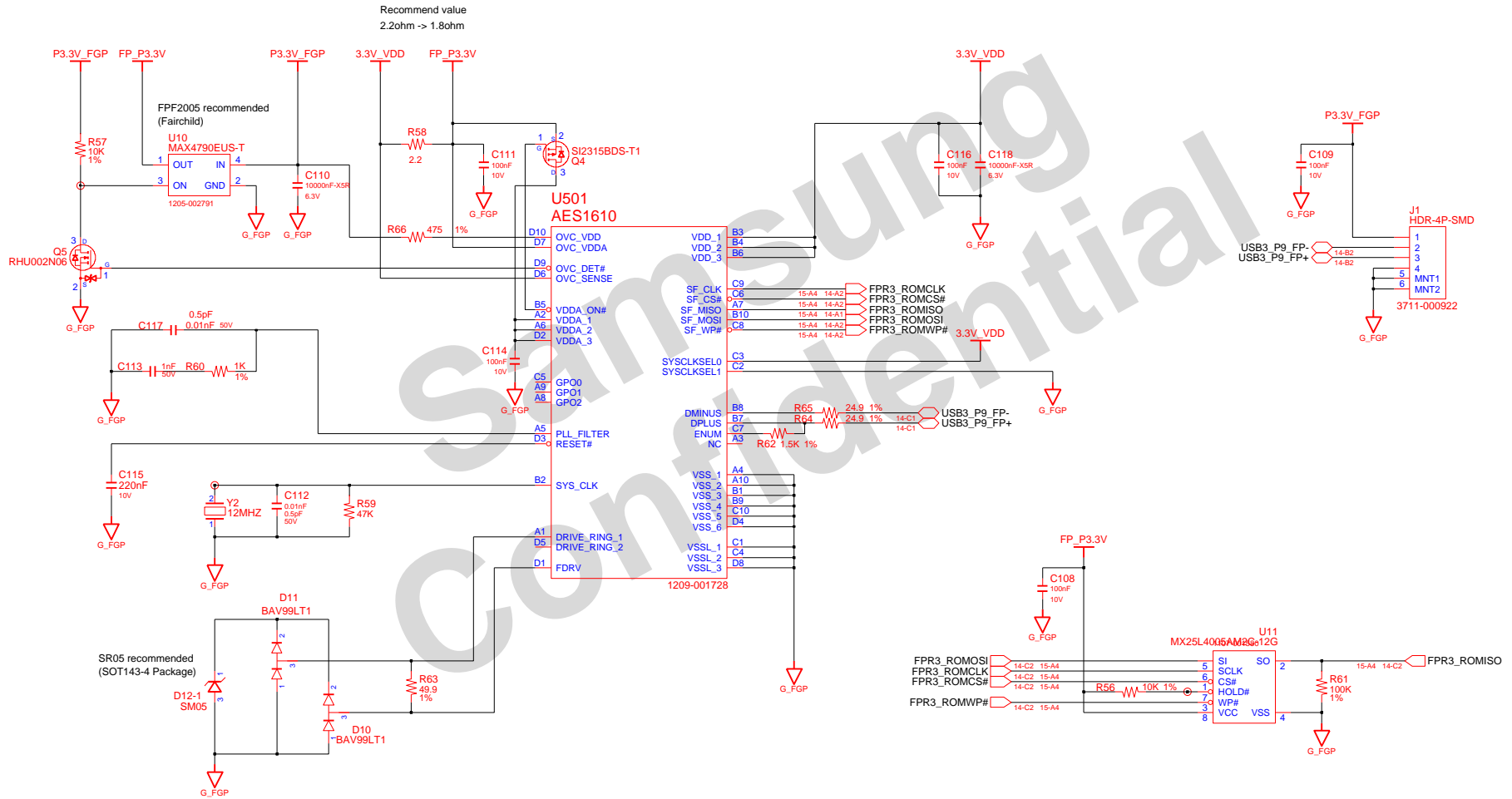


LAN SUB BOARD CONNECTOR



DESIGN	JUN, PARK	DATE	1/17/2008	TITLE	SAM0A SUB LAN LAN I/F	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1			PART NO. BA41-#####A
MODULE CODE		LAST EDIT		August 22, 2008 10:42:11 AM	PAGE	13 OF 15

FINGER PRINT BOARD



DESIGN	JUN, PARK	DATE	1/17/2008	TITLE	SAM0A SUB FINGER PRINT FINGER PRINT I/F	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.1			PART NO. BA41-#####A
MODULE CODE		LAST EDIT		August 22, 2008 10:42:11 AM	PAGE 14 OF 15	