7. 회로도

1) System

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts	
Cardbus	AD25	0	A,B,C	
LAN	AD21	2	G	
MiniPCI SLOT1	AD23	1	E, F	
MiniPCI SLOT2	AD22	3	D, G	<-- PLYMOUTH
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C USB2.0 #3 : ???	
Hub to PCI	AD30(internal)	-	-	
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B	
Internal MAC	AD24(internal)	-	E	
AC Link	-	-	B	

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V	Northwood-B
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V	(Interposer B'd)
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V	
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1	1.148 V	
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V	
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V	
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V	
0	0	0	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V	
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V	
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V	
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V	
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V	
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V	
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V	
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V	
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V	
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V	
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V	
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V	
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V	
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V	
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V	
Highest Freq. 0	1	0	1	1	0	1.356 V	1	1	0	1	1	0	0.844 V	Lowest Freq.
0	1	0	1	1	1	1.340 V	1	1	0	1	1	1	0.828 V	
0	1	1	0	0	0	1.324 V	1	1	1	0	0	0	0.812 V	
0	1	1	0	0	1	1.308 V	1	1	1	0	0	1	0.796 V	
0	1	1	0	1	0	1.292 V	1	1	1	0	1	0	0.780 V	
0	1	1	0	1	1	1.276 V	1	1	1	0	1	1	0.764 V	
0	1	1	1	0	0	1.260 V	1	1	1	1	0	0	0.748 V	Deeper Sleep
0	1	1	1	0	1	1.244 V	1	1	1	1	0	1	0.732 V	
0	1	1	1	1	0	1.228 V	1	1	1	1	1	0	0.716 V	
0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V	

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308~1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P3.3V_DTV	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)

I2C / SMB Address

Devices	Address	Hex	Bus
ICH6	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1,2	SYSTEM PORT B
3	AUDIO B'D
4	BLUETOOTH
5	PORT REPLICATOR

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.

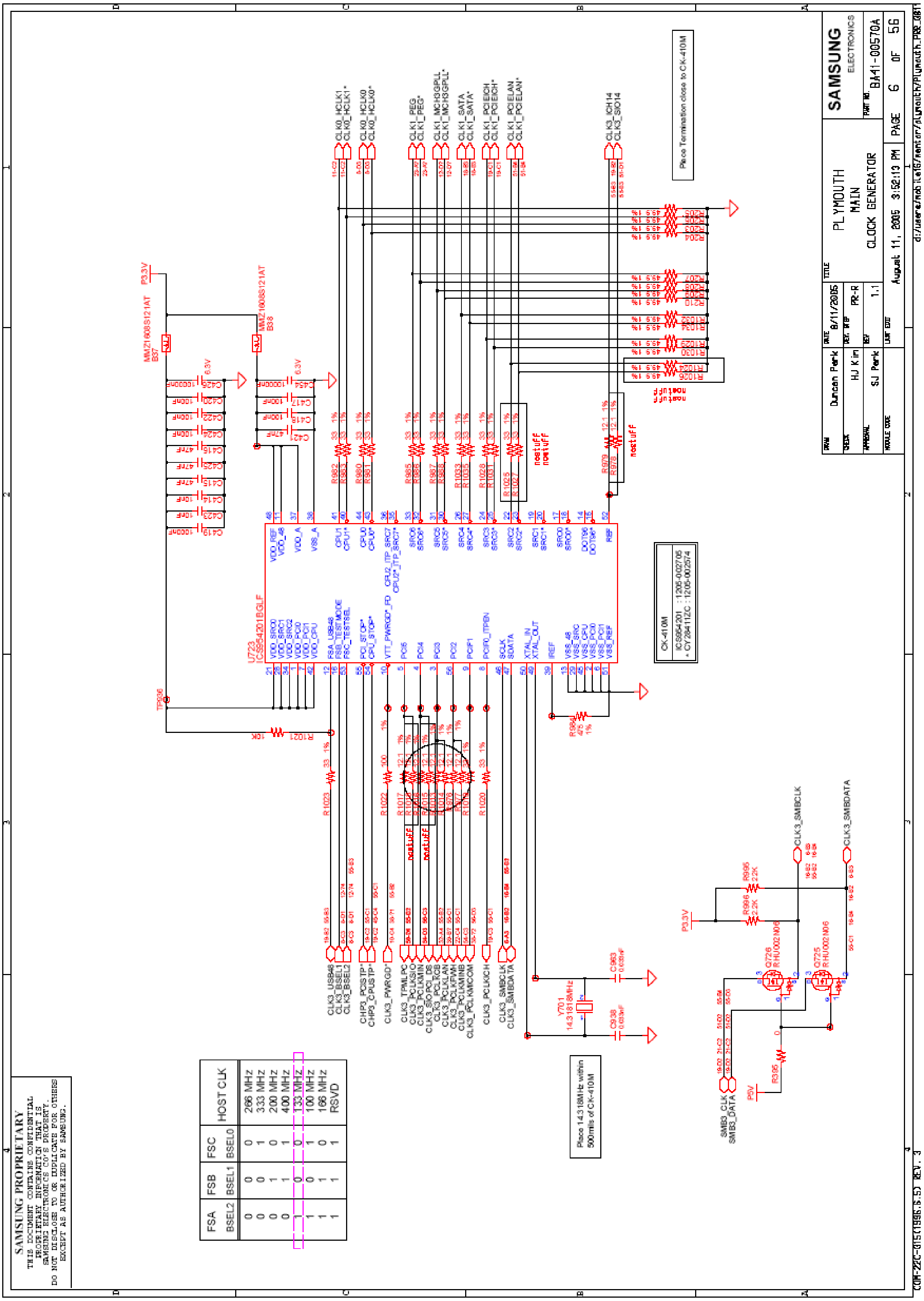
CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

REVISION HISTORY

See rev notes in the changes file for more information.

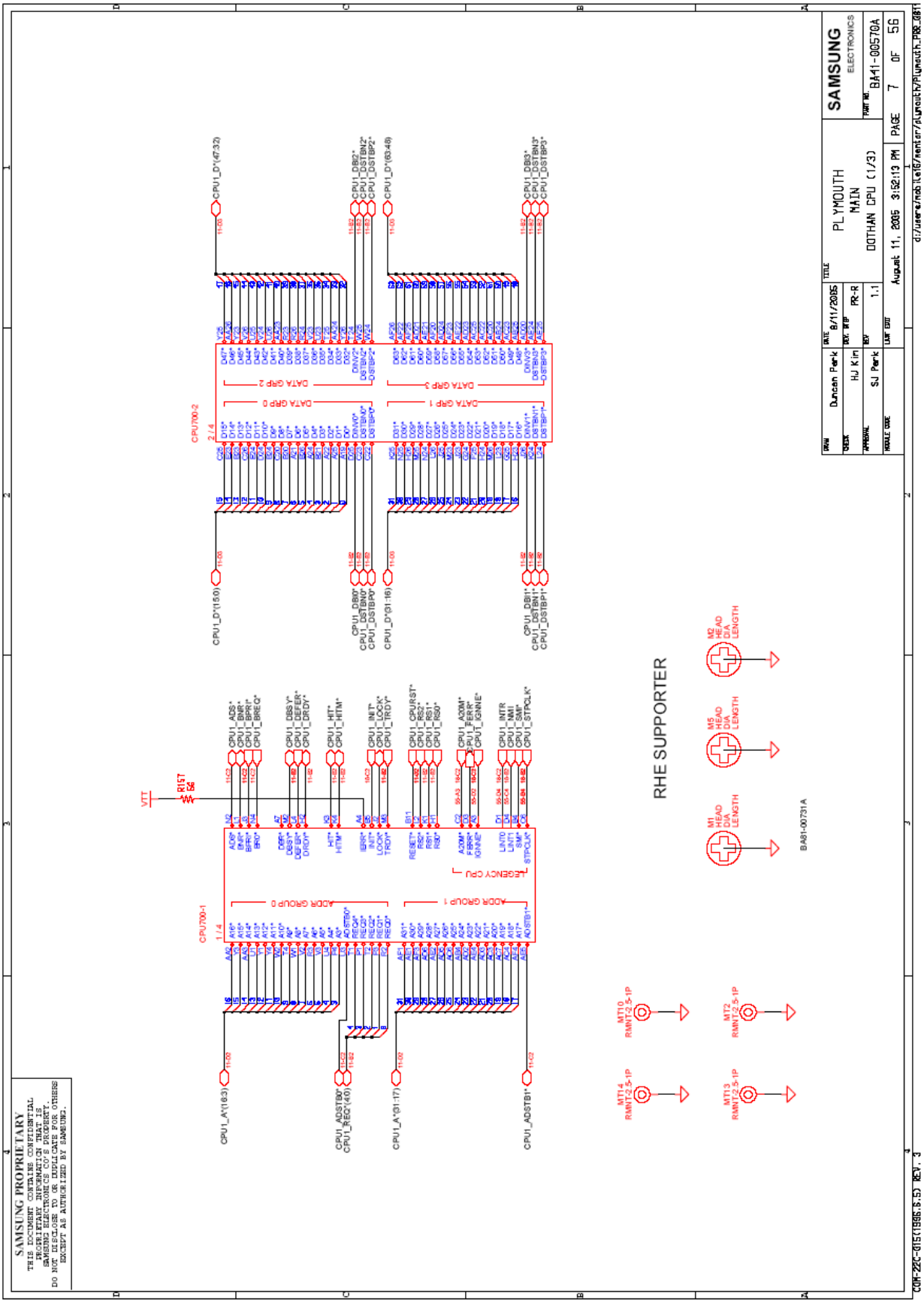
DRAW: Duncan Park	DATE: 8/11/2005	TITLE: PLYMOUTH MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS
CHECK: HJ Kim	DEV. DEP: PR-R		
APPROVAL: SJ Park	REV: 1.1		PART NO.: BA41-00570A
MODULE CODE:	LAST EDIT: August 11, 2005 3:52:13 PM	PAGE 5 OF 56	

7. 회로도

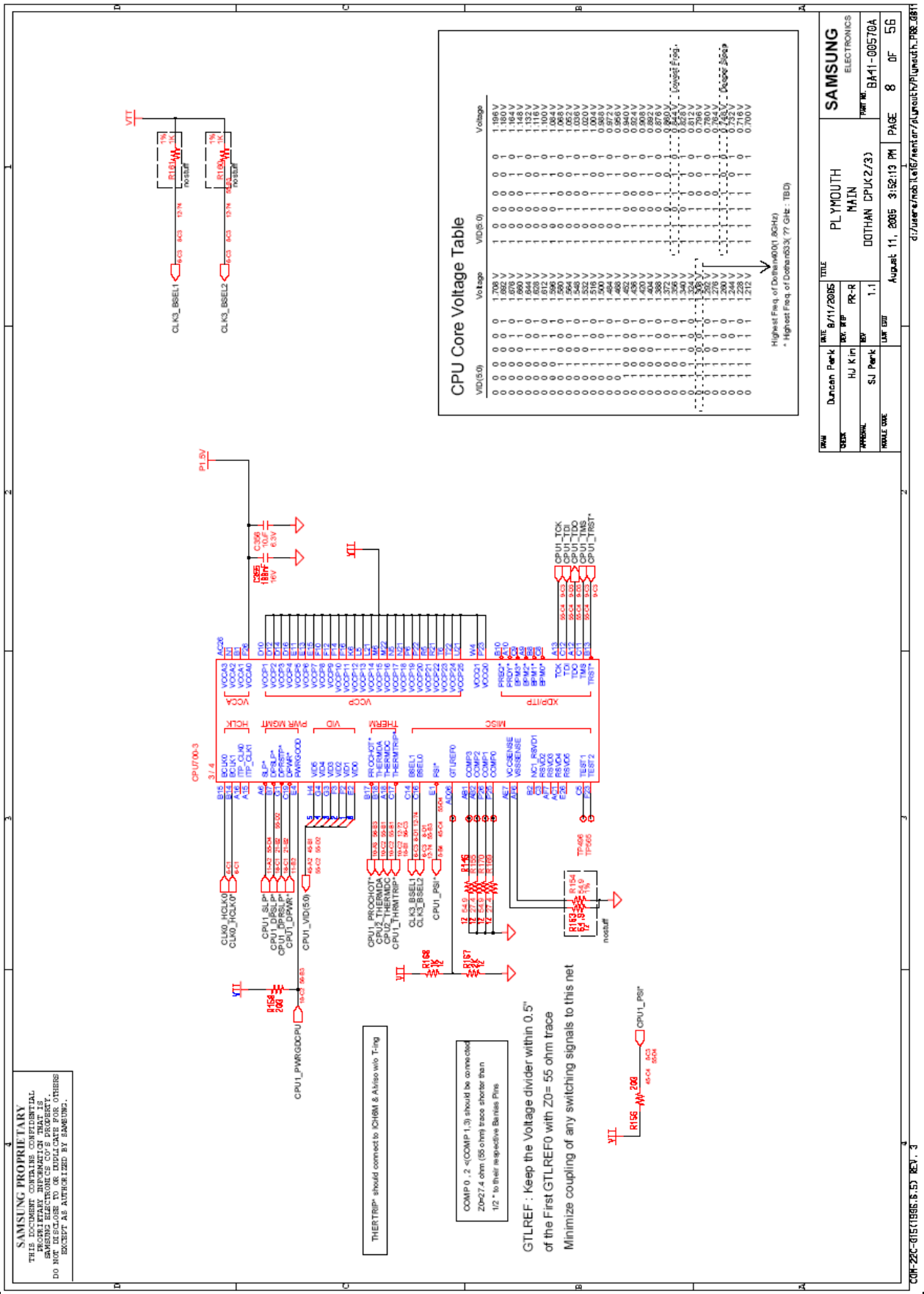


SAMSUNG PROPRIETARY
SAMSUNG ELECTRONICS
PLYMOUTH MAIN
CLOCK GENERATOR
BA41-00570A
PAGE 6 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
PR-R
1.1
U723
ICS954201BGLF
CK-410M
Place Termination close to CK-410M
Place 14.318MHz within 500mils of CK-410M
Y701
14.31818MHz
FSA
FSB
FSC
BSEL2
BSEL1
BSEL0
HOST CLK
266 MHz
333 MHz
200 MHz
400 MHz
133 MHz
100 MHz
166 MHz
RSVD

7. 회로도


SAMSUNG PROPRIETARY
SAMSUNG ELECTRONICS
PLYMOUTH
MAIN
DOTHAN CPU (1/3)
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 7 OF 56
RHE SUPPORTER
BA91-00731A

7. 회로도


CPU Core Voltage Table
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
DOTHAN CPUK2/33
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 8 OF 56
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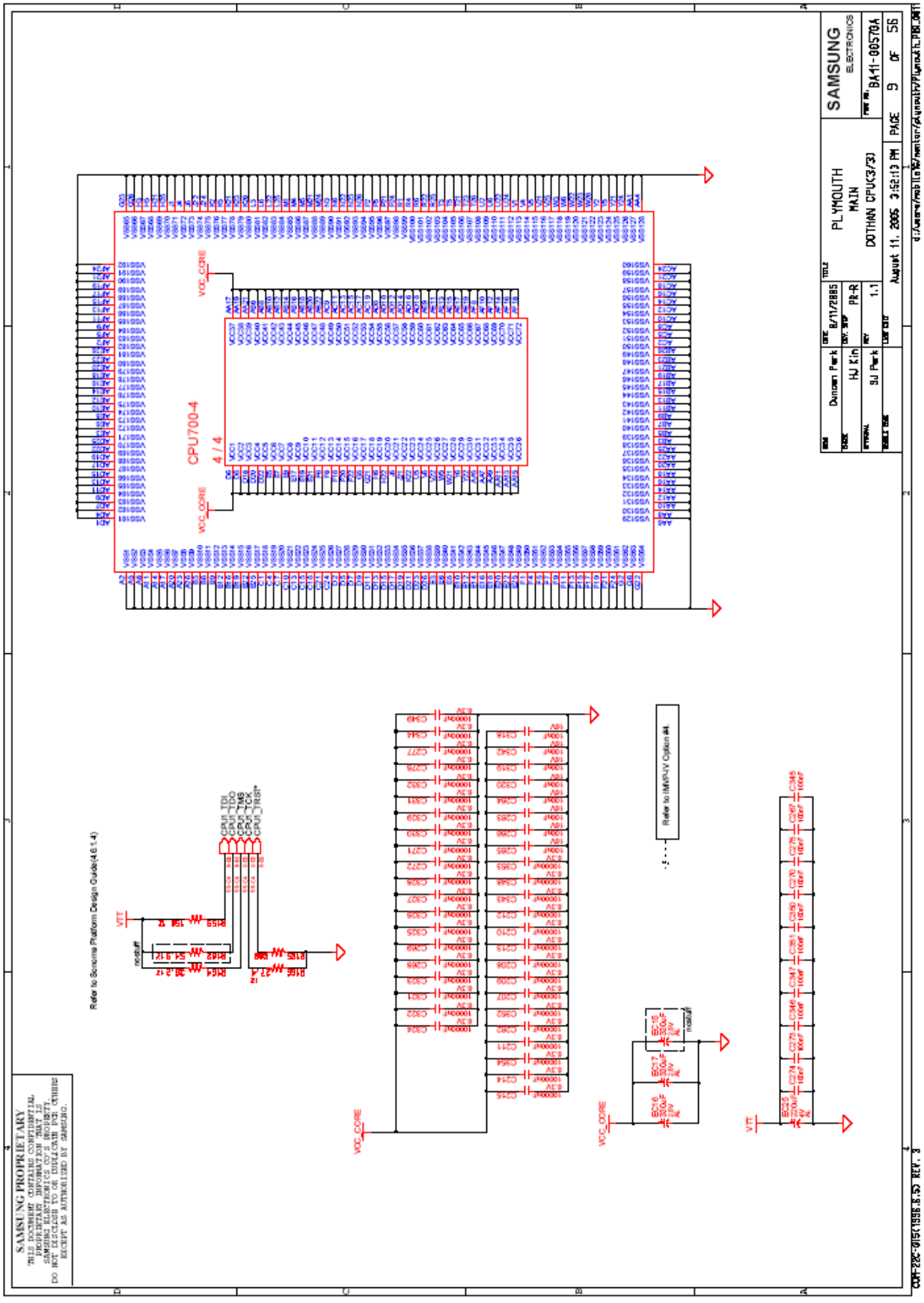
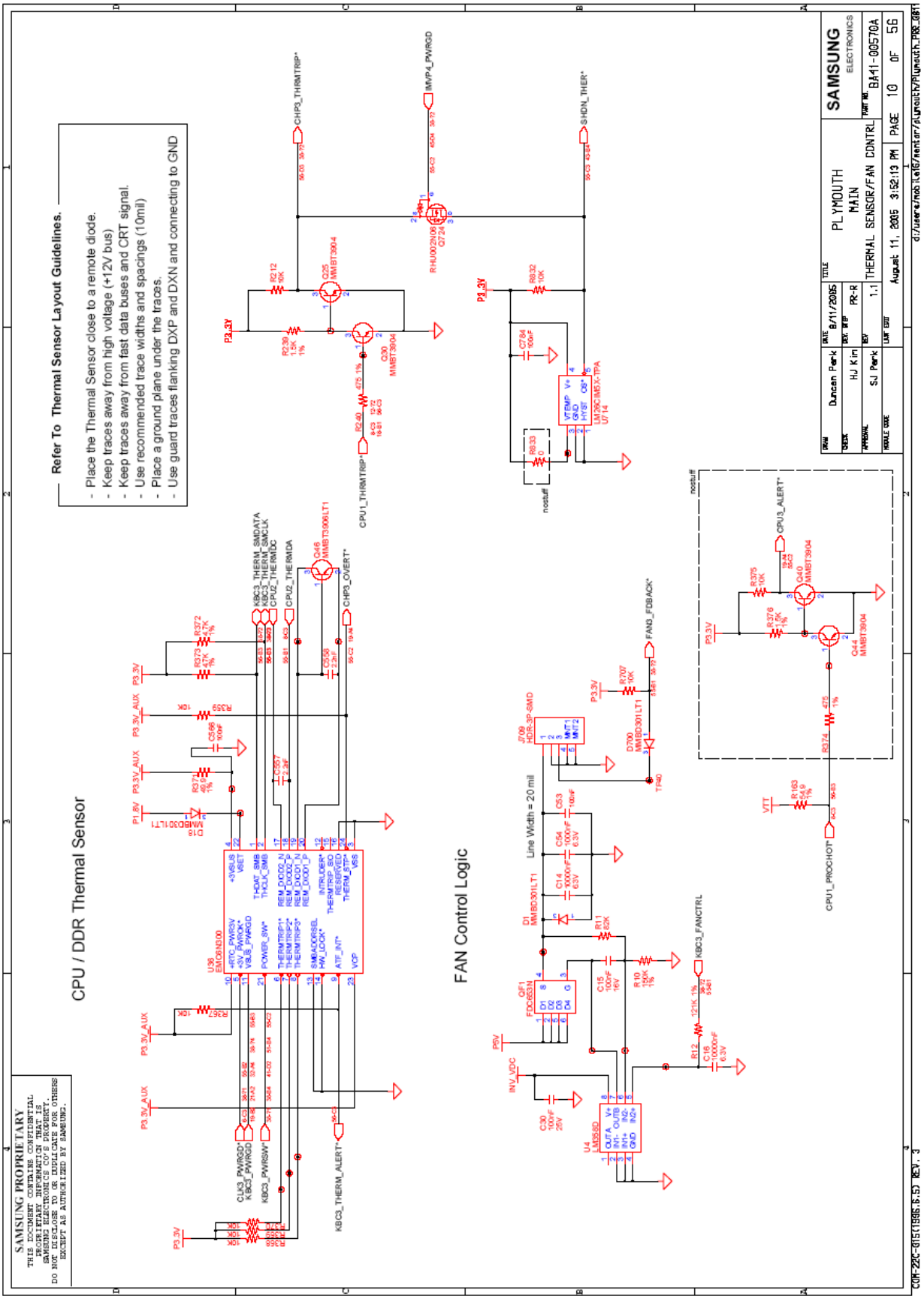
THIS DOCUMENT CONTAINS CONFIDENTIAL PROPRIETARY INFORMATION THAT IS SAMSUNG ELECTRONICS CO'S PROPERTY. DO NOT DISCLOSE TO OR DUPLICATE FOR OTHERS EXCEPT AS AUTHORIZED BY SAMSUNG.
THERTRIP* should connect to ICH6M & Alviso w/o T-ing
COMP0,2 <(COMP1,3) should be connected ZO=27.4 ohm (55 ohm) trace shorter than 1/2 " to their respective Banias Pins
GTLREF : Keep the Voltage divider within 0.5" of the First GTLREF0 with ZO= 55 ohm trace
Minimize coupling of any switching signals to this net

7. 회로도


CPU700-4
4 / 4
VCC_CORE
PLYMOUTH
MAIN
DOTHAN CPUC3/3J
SAMSUNG
ELECTRONICS
Duncan Park
HJ Kim
SJ Park
August 11, 2005
SAMSUNG PROPRIETARY
Refer to Sonoma Platform Design Guide(4.6.1-4)
Refer to IMVP-IV Option #1
CPU_TDI
CPU_TDO
CPU_TMS
CPU_TCK
CPU_TRST*
VTT

7. 회로도


CPU / DDR Thermal Sensor
FAN Control Logic
Refer To Thermal Sensor Layout Guidelines.
- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND
SAMSUNG PROPRIETARY
SAMSUNG
PLYMOUTH
MAIN
THERMAL SENSOR/FAN CONTRL
BA41-00570A
PAGE 10 OF 56
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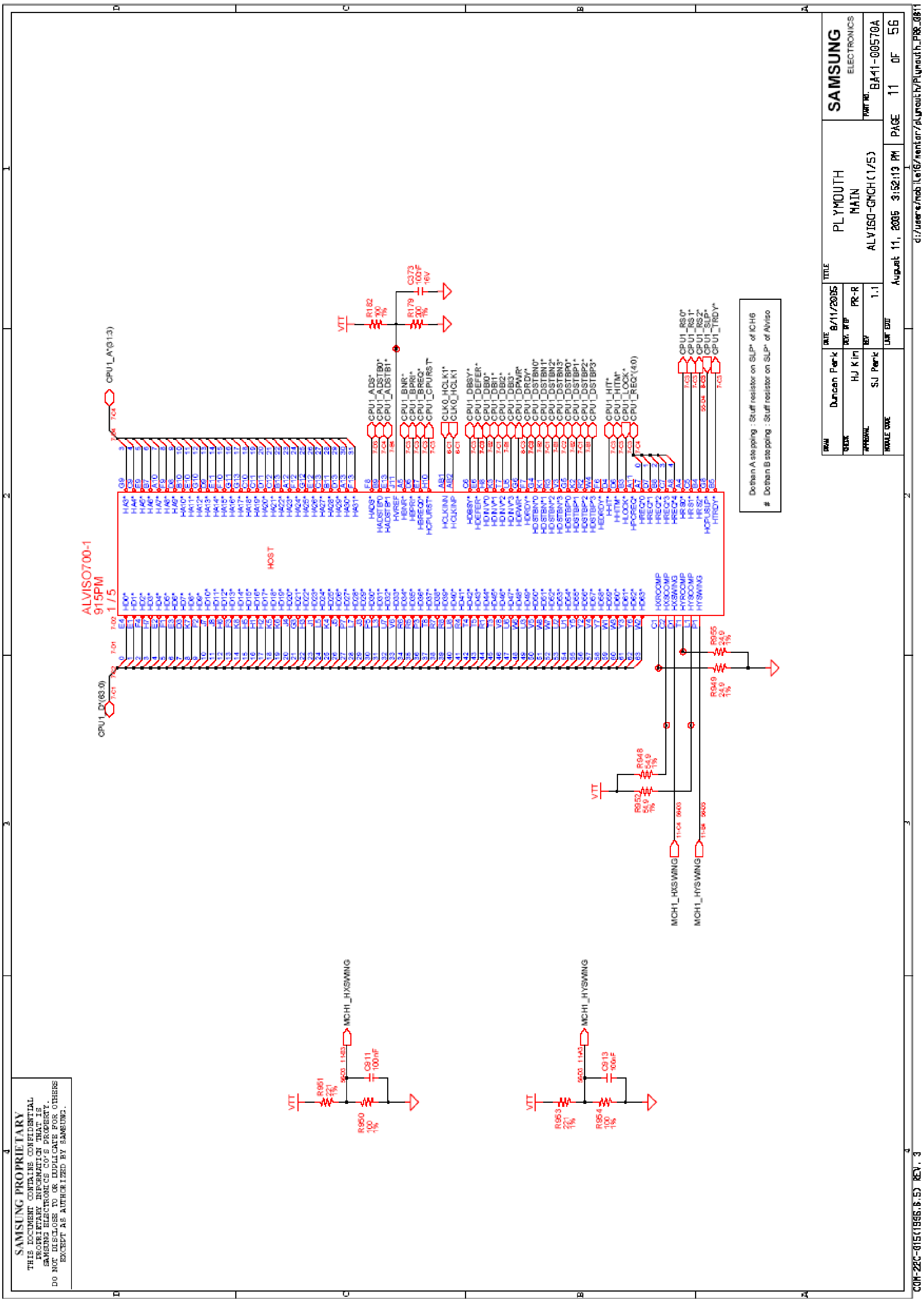
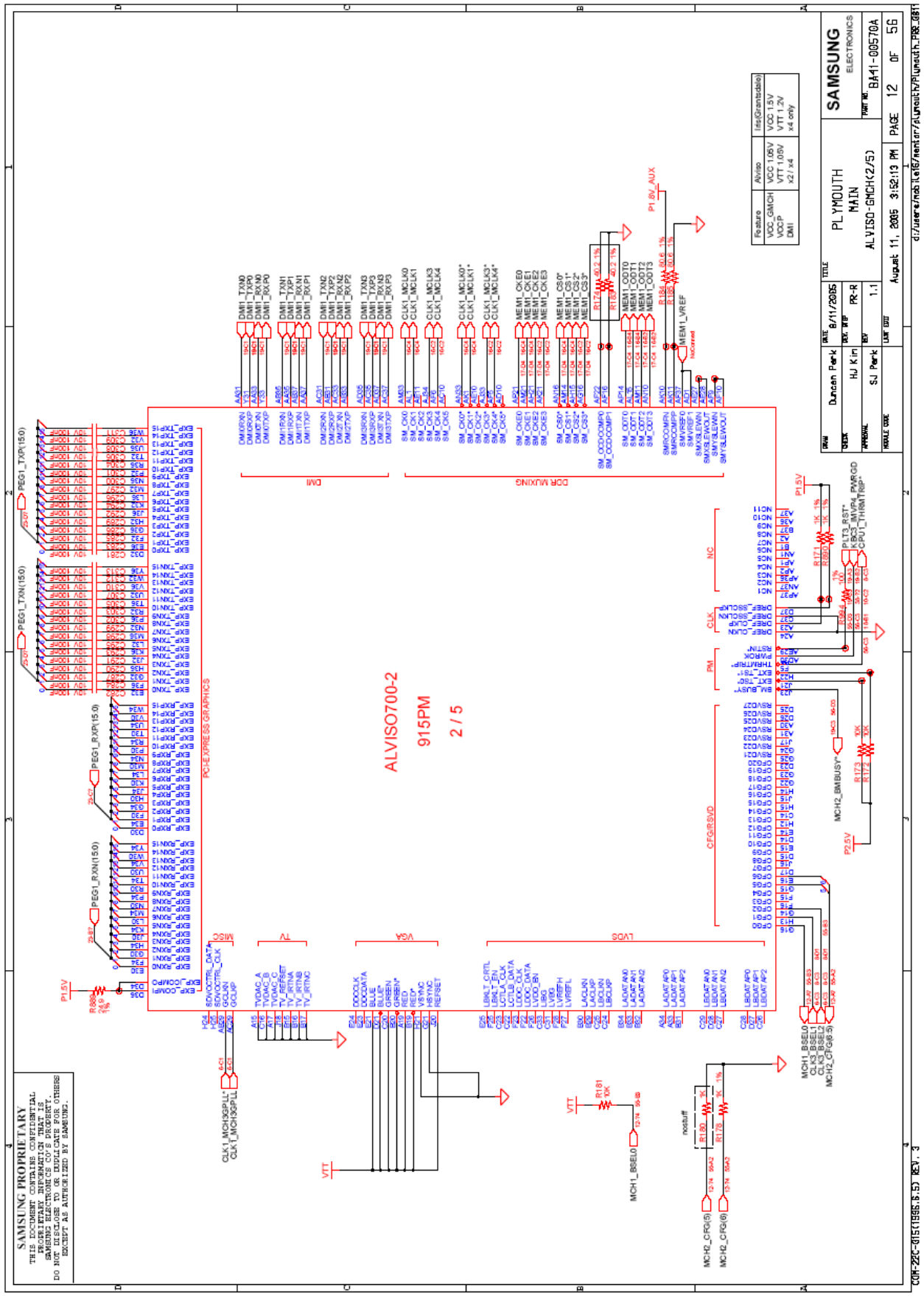
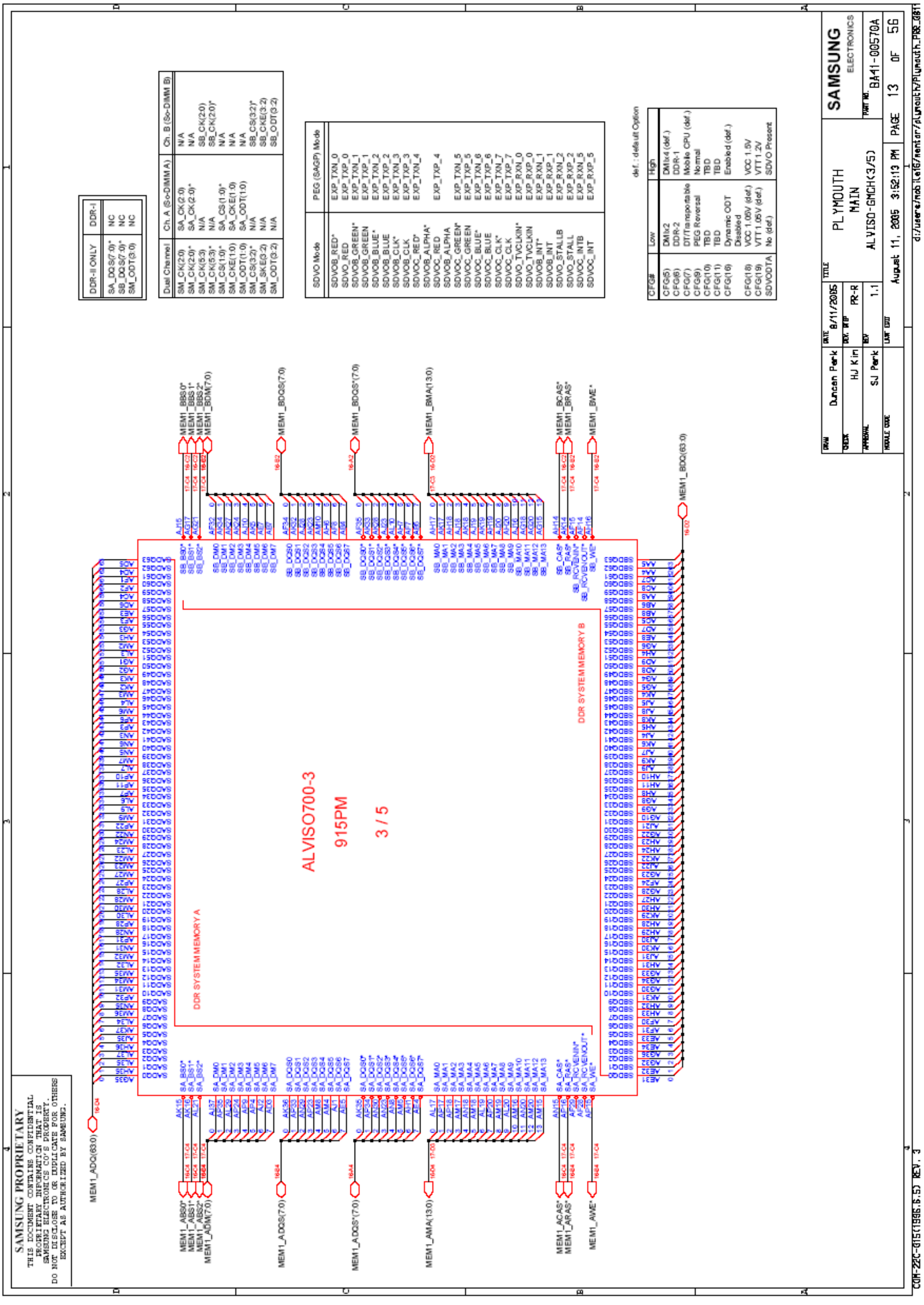
7. 회로도


SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
ALVISO-GMCH(1/5)
BA41-00570A
ALVISO700-1
915PM
1 / 5
HOST
SAMSUNG PROPRIETARY

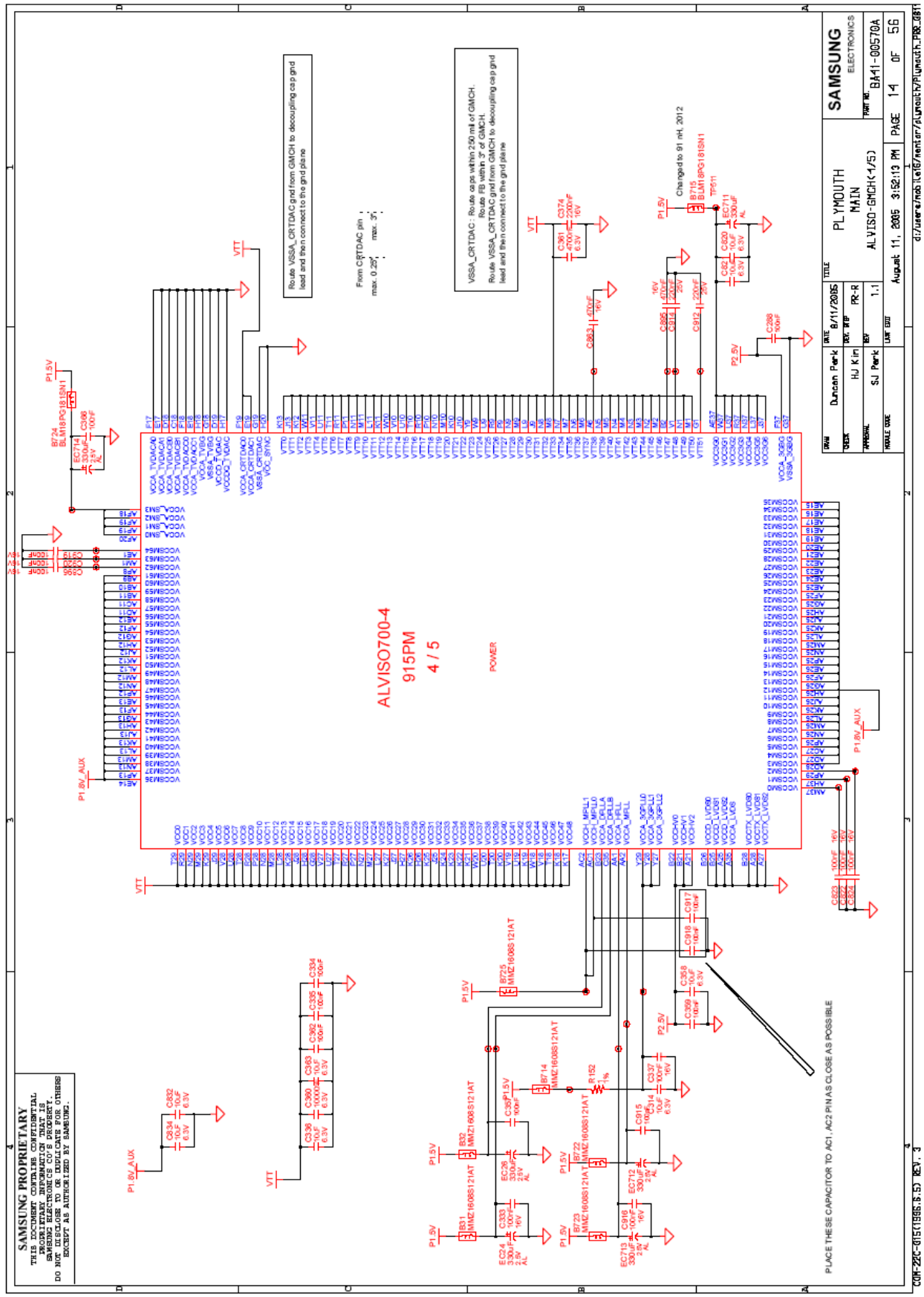
7. 회로도


ALVISO700-2
915PM
2 / 5
SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
ALVISO-GMCH(2/5)
BA41-00570A
PAGE 12 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
PR-R
1.1
PCI-EXPRESS GRAPHICS
DDR MUXING
DMI
LVDS
VGA
TV
MISC
NC
CLK
PM
CFG/RSVD

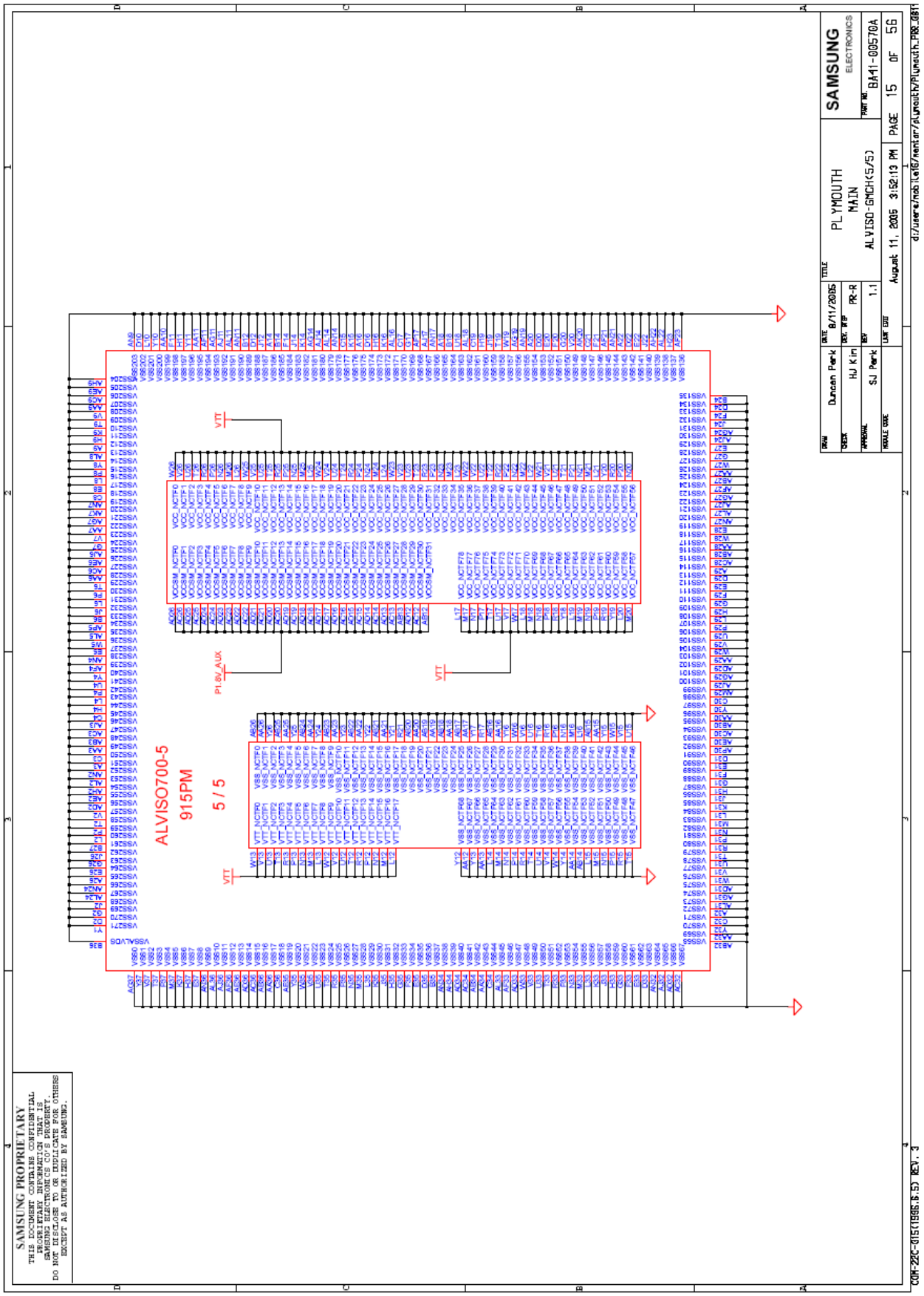
7. 회로도



7. 회로도


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
ALVISO-GMCH(4/5)
BA41-00570A
PAGE 14 OF 56
August 11, 2005 3:52:13 PM
ALVISO700-4
915PM
4 / 5
POWER
PLACE THESE CAPACITOR TO AC1 ,AC2 PIN AS CLOSE AS POSSIBLE

7. 회로도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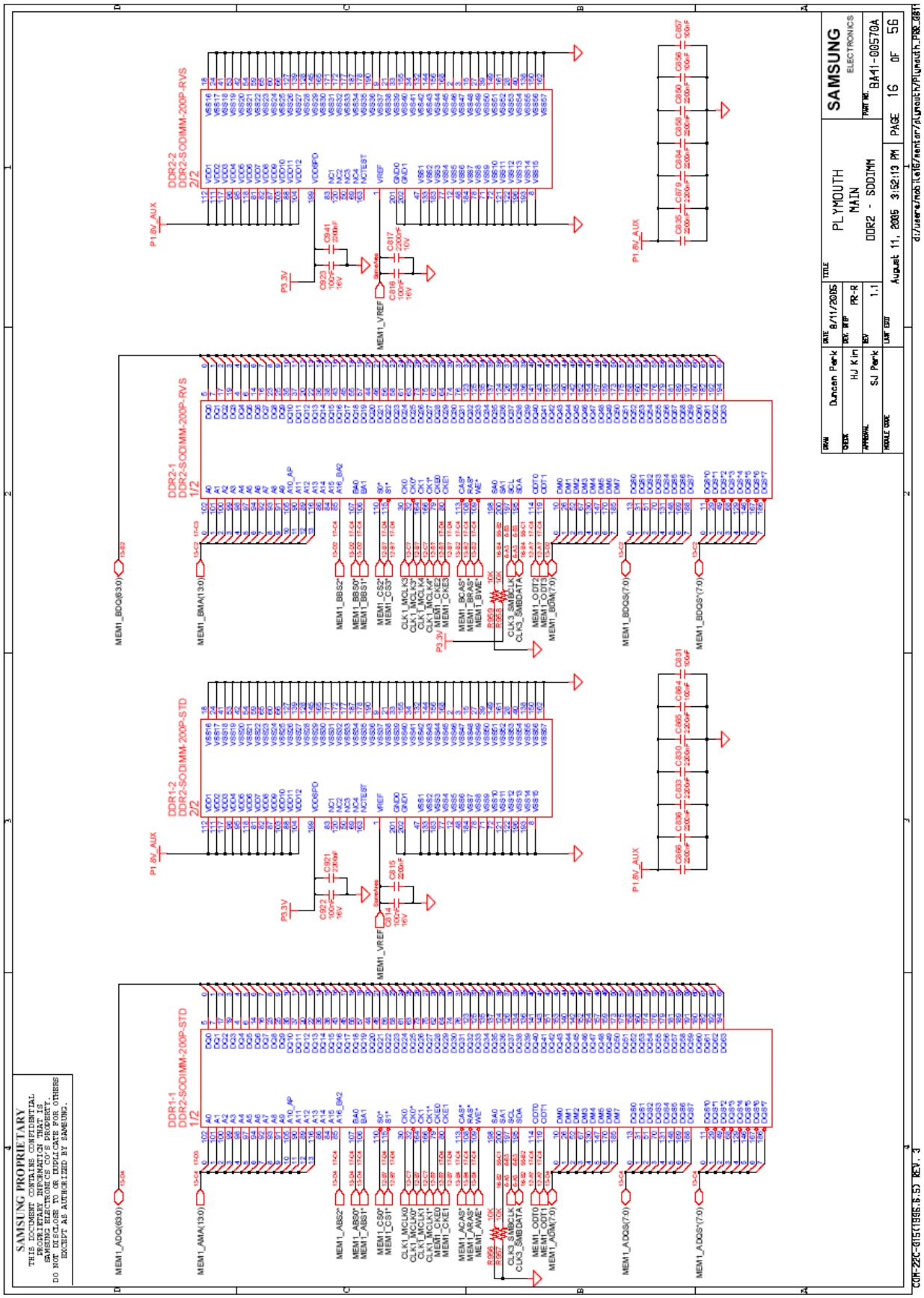
ALVISO700-5
915PM
5 / 5
VTT
P1.8V_AUX
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
ALVISO-GMCH(5/5)
BA41-00570A
PAGE 15 OF 56
Duncan Park
HJ Kim
SJ Park
8/11/2005
PR-R
1.1
August 11, 2005 3:52:13 PM
d:/users/mobile6/rentar/plymouth/Plymouth.PRJ

7. 회로도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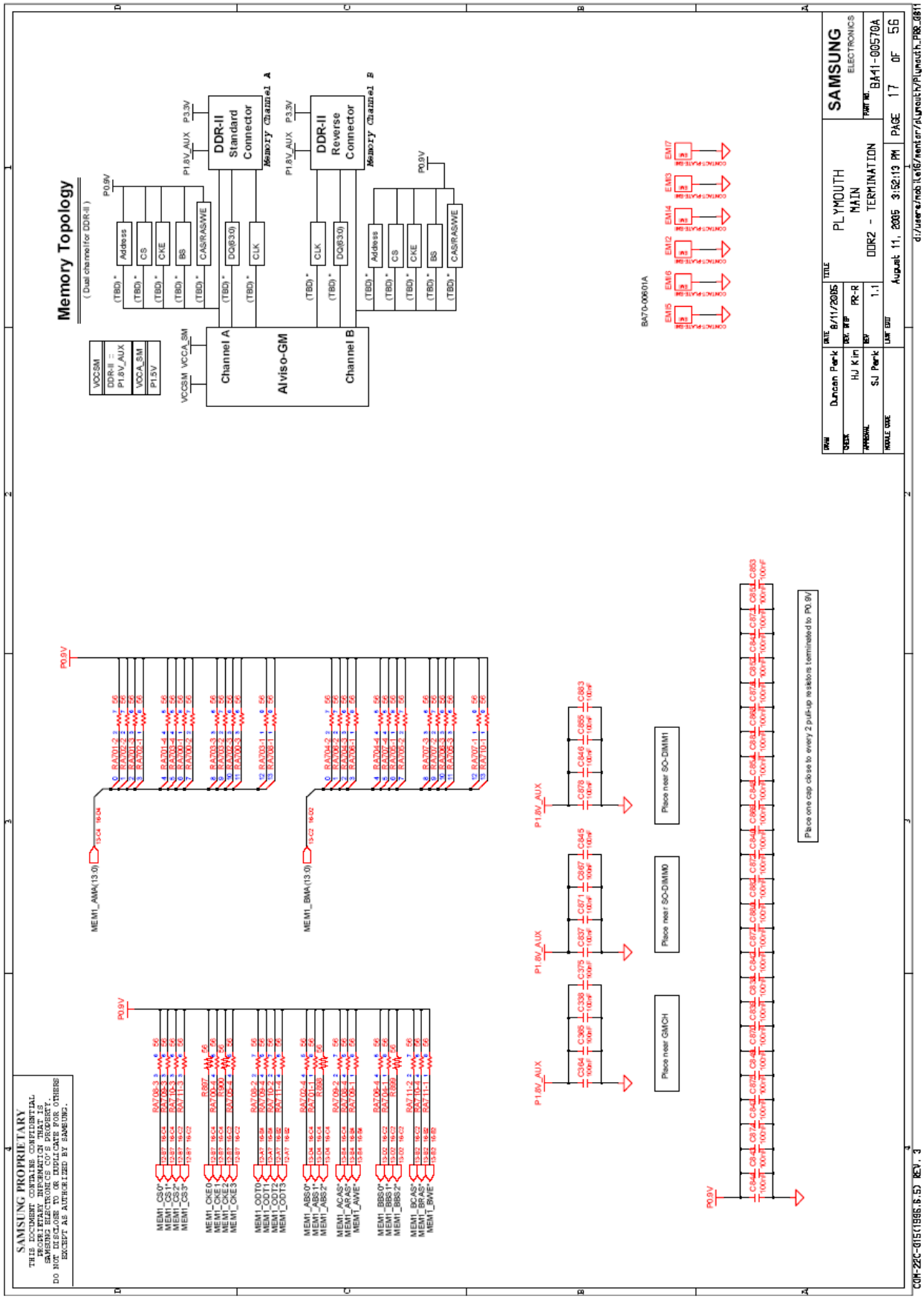
SAMSUNG ELECTRONICS
PLYMOUTH
MAIN
DDR2 - SODIMM
PART NO. BA41-00570A
PAGE 16 OF 56
August 11, 2005 3:52:13 PM
d:/users/mobile6/sentar7/plymouth/Plymouth.PRJ.dft
DRAWN Duncan Park
DESIGN HJ Kim
APPROVAL SJ Park
DATE 8/11/2005
REV 1.1
DDR1:1 DDR2-SODIMM-200P-STD 1/2
DDR1:2 DDR2-SODIMM-200P-STD 2/2
DDR2:1 DDR2-SODIMM-200P-RVS 1/2
DDR2:2 DDR2-SODIMM-200P-RVS 2/2
MEM1_ADQ(63:0)
MEM1_BDQ(63:0)
MEM1_AMA(13:0)
MEM1_BMA(13:0)
MEM1_ADQS(7:0)
MEM1_BDQS(7:0)
P1.8V_AUX
P3.3V
MEM1_VREF

7. 회로도


Memory Topology
(Dual channel for DDR-II)
Alviso-GM
Channel A
Channel B
DDR-II Standard Connector
DDR-II Reverse Connector
Memory Channel A
Memory Channel B
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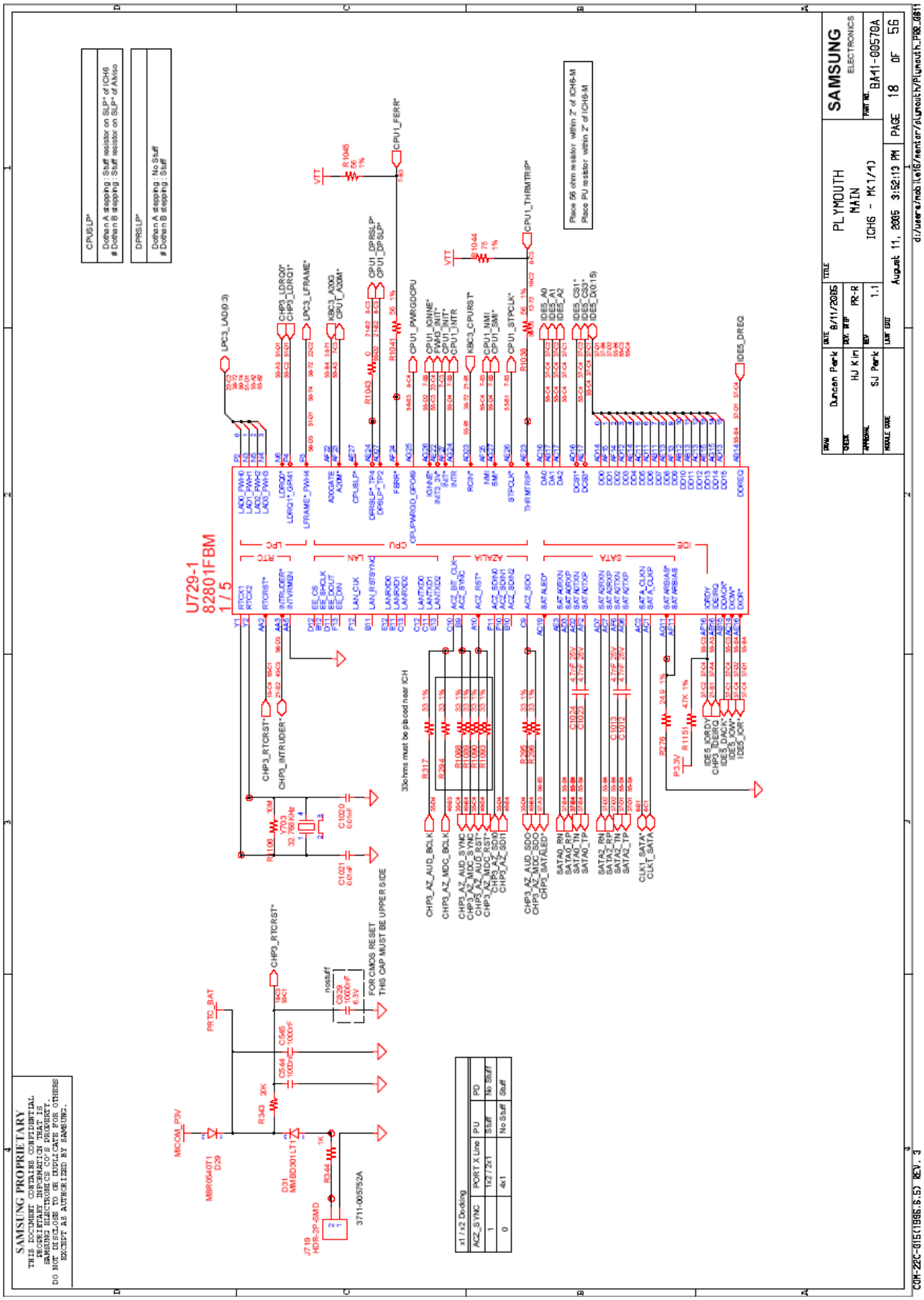
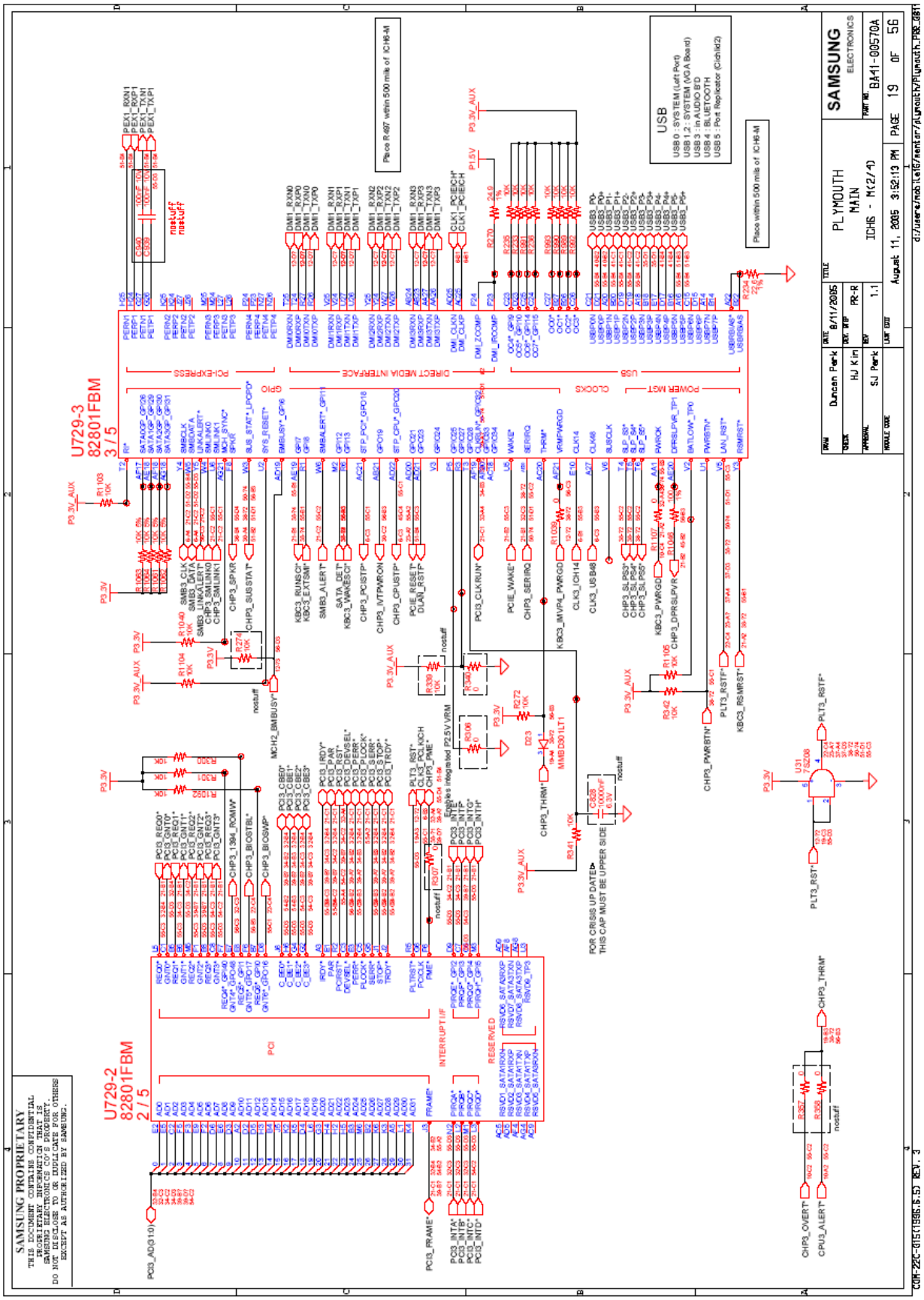
PLYMOUTH
MAIN
DDR2 - TERMINATION
BA41-00570A
PAGE 17 OF 56
August 11, 2005 3:52:13 PM
Duncan Park 8/11/2005
HJ Kim PR-R
SJ Park 1.1
Place near GMCH
Place near SO-DIMM0
Place near SO-DIMM1
Place one cap close to every 2 pull-up resistors terminated to P0.9V

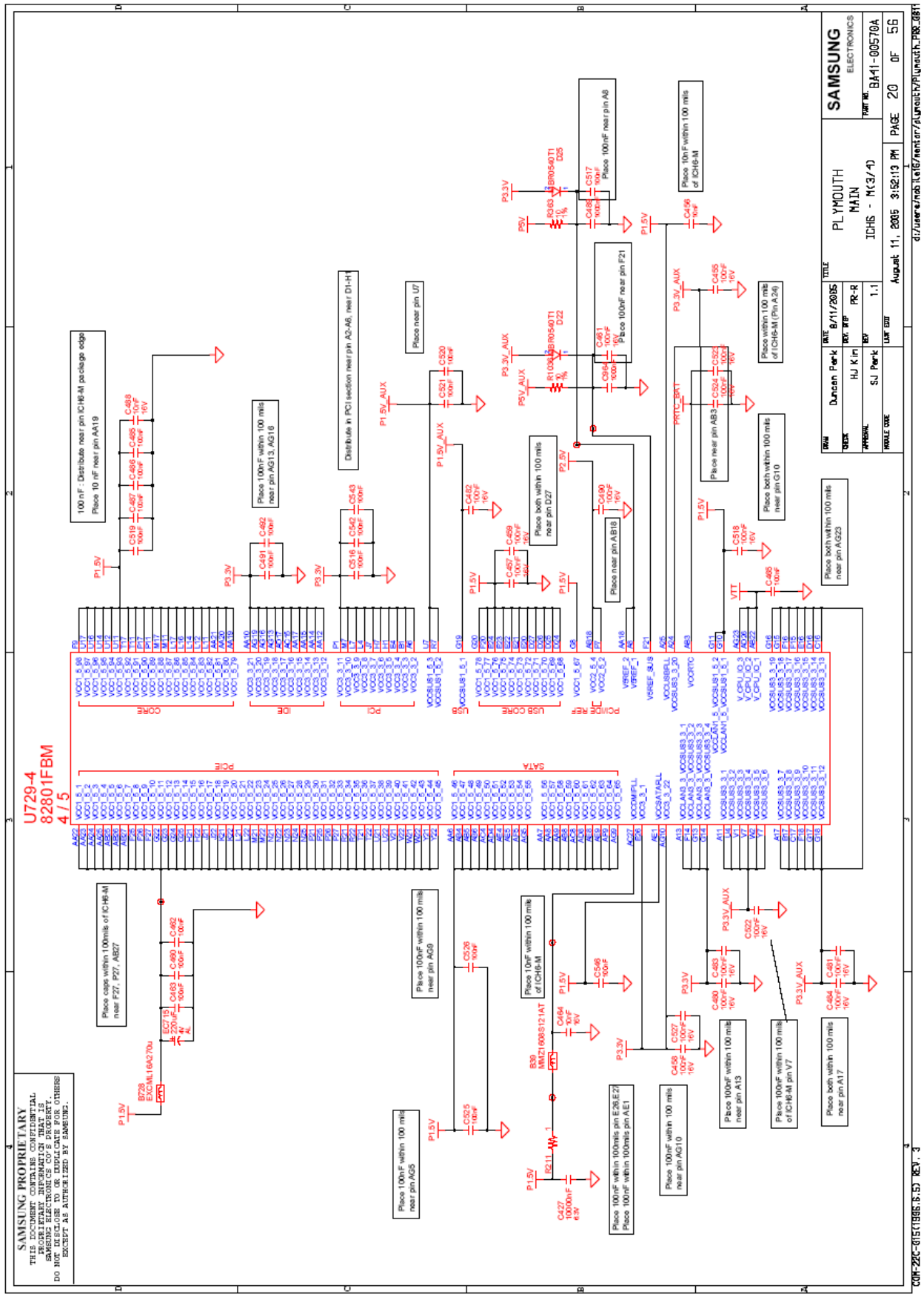
7. 회로도



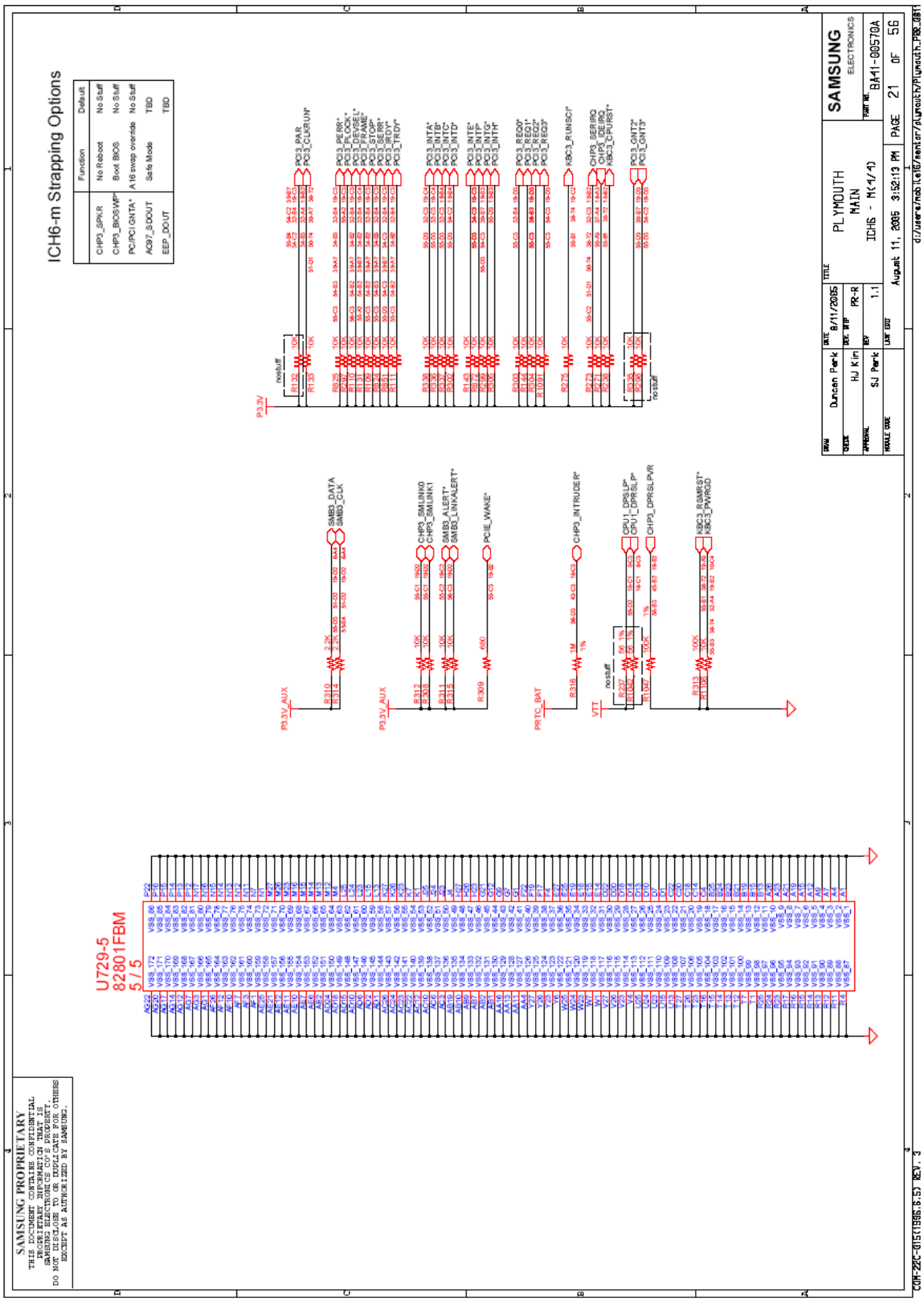
7. 회로도



7. 회로도



7. 회로도


ICH6-m Strapping Options
SAMSUNG PROPRIETARY
SAMSUNG
PLYMOUTH
MAIN
ICH6 - M(1/4)
BA41-00570A
August 11, 2005 3:52:13 PM
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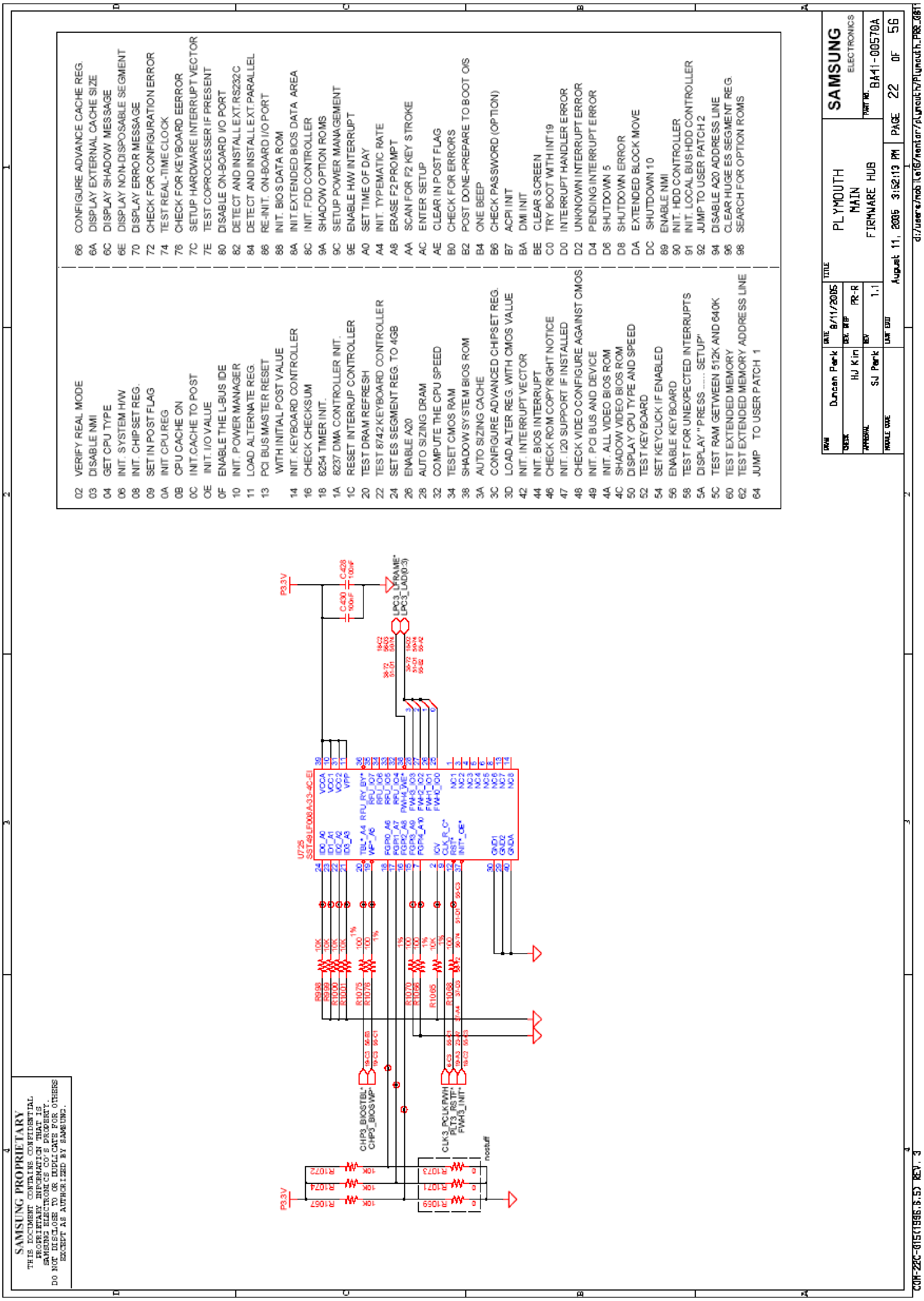
U729-5
82801FBM
5/5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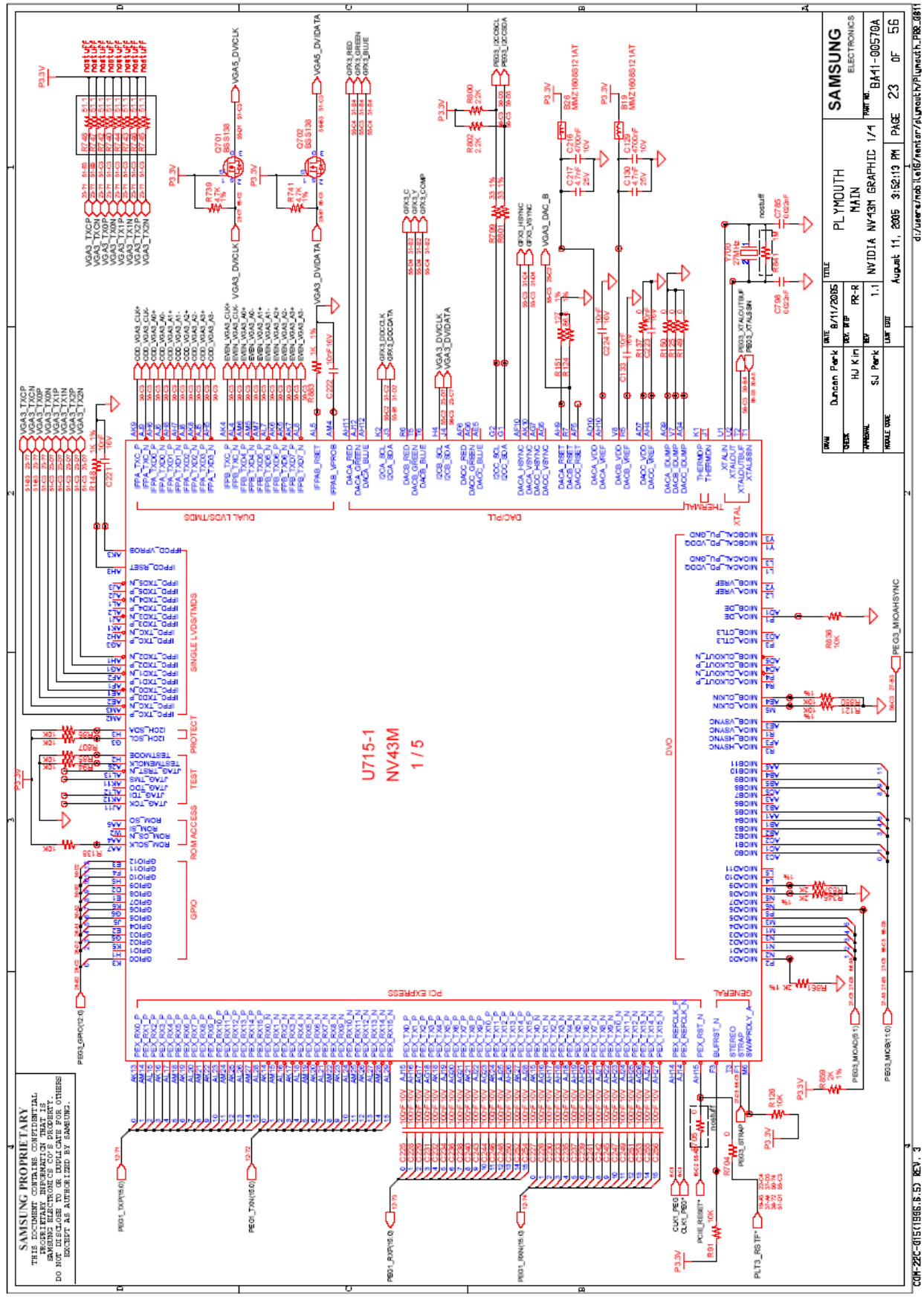
U725
SST49LF008A-33-4C-EI
P3.3V
C430 100nF
C428 100nF
LPC3_LFRAME*
LPC3_LAD(0:3)
CHP3_BIOSTBL*
CHP3_BIOSWP*
CLK3_PCLKFWH
PLT3_RSTF*
FWH3_INIT*
nostuff
02 VERIFY REAL MODE
03 DISABLE NMI
04 GET CPU TYPE
06 INIT. SYSTEM H/W
08 INIT. CHIPSET REG.
09 SET IN POST FLAG
0A INIT CPU REG
0B CPU CACHE ON
0C INIT.CACHE TO POST
0E INIT. I/O VALUE
0F ENABLE THE L-BUS IDE
10 INIT. POWER MANAGER
11 LOAD ALTERNATE REG.
13 PCI BUS MASTER RESET WITH INITIAL POST VALUE
14 INIT. KEYBOARD CONTROLLER
16 CHECK CHECKSUM
18 8254 TIMER INIT.
1A 8237 DMA CONTROLLER INIT.
1C RESET INTERRUP CONTROLLER
20 TEST DRAM REFRESH
22 TEST 8742 KEYBOARD CONTROLLER
24 SET ES SEGMENT REG. TO 4GB
26 ENABLE A20
28 AUTO SIZING DRAM
32 COMPUTE THE CPU SPEED
34 TESET CMOS RAM
38 SHADOW SYSTEM BIOS ROM
3A AUTO SIZING CACHE
3C CONFIGURE ADVANCED CHIPSET REG.
3D LOAD ALTER REG. WITH CMOS VALUE
42 INIT. INTERRUPT VECTOR
44 INIT. BIOS INTERRUPT
46 CHECK ROM COPYRIGHT NOTICE
47 INIT. I20 SUPPORT IF INSTALLED
48 CHECK VIDEO CONFIGURE AGAINST CMOS
49 INIT. PCI BUS AND DEVICE
4A INIT. ALL VIDEO BIOS ROM
4C SHADOW VIDEO BIOS ROM
50 DISPLAY CPU TYPE AND SPEED
52 TEST KEYBOARD
54 SET KEYCLICK IF ENABLED
56 ENABLE KEYBOARD
58 TEST FOR UNEXPECTED INTERRUPTS
5A DISPLAY "PRESS ...... SETUP"
5C TEST RAM GETWEEN 512K AND 640K
60 TEST EXTENDED MEMORY
62 TEST EXTENDED MEMORY ADDRESS LINE
64 JUMP TO USER PATCH 1
66 CONFIGURE ADVANCE CACHE REG.
6A DISPLAY EXTERNAL CACHE SIZE
6C DISPLAY SHADOW MESSAGE
6E DISPLAY NON-DISPOSABLE SEGMENT
70 DISPLAY ERROR MESSAGE
72 CHECK FOR CONFIGURATION ERROR
74 TEST REAL-TIME CLOCK
76 CHECK FOR KEYBOARD EERROR
7C SETUP HARDWARE INTERRUPT VECTOR
7E TEST COPROCESSER IF PRESENT
80 DISABLE ON-BOARD I/O PORT
82 DETECT AND INSTALL EXT.RS232C
84 DETECT AND INSTALL EXT.PARALLEL
86 RE-INIT. ON-BOARD I/O PORT
88 INIT. BIOS DATA ROM
8A INIT.EXTENDED BIOS DATA AREA
8C INIT. FDD CONTROLLER
9A SHADOW OPTION ROMS
9C SETUP POWER MANAGEMENT
9E ENABLE H/W INTERRUPT
A0 SET TIME OF DAY
A4 INIT. TYPEMATIC RATE
A8 ERASE F2 PROMPT
AA SCAN FOR F2 KEY STROKE
AC ENTER SETUP
AE CLEAR IN POST FLAG
B0 CHECK FOR ERRORS
B2 POST DONE-PREPARE TO BOOT O/S
B4 ONE BEEP
B6 CHECK PASSWORD (OPTION)
B7 ACPI INIT
BA DMI INIT
BE CLEAR SCREEN
C0 TRY BOOT WITH INT19
D0 INTERRUPT HANDLER ERROR
D2 UNKNOWN INTERRUPT ERROR
D4 PENDING INTERRUPT ERROR
D6 SHUTDOWN 5
D8 SHUTDOWN ERROR
DA EXTENDED BLOCK MOVE
DC SHUTDOWN 10
89 ENABLE NMI
90 INIT. HDD CONTROLLER
91 INIT. LOCAL BUS HDD CONTROLLER
92 JUMP TO USER PATCH 2
94 DISABLE A20 ADDRESS LINE
96 CLEAR HUGE ES SEGMENT REG.
98 SEARCH FOR OPTION ROMS
DRAW Duncan Park
CHECK HJ Kim
APPROVAL SJ Park
DATE 8/11/2005
DEV. STEP PR-R
REV 1.1
TITLE PLYMOUTH MAIN FIRMWARE HUB
SAMSUNG ELECTRONICS
PART NO. BA41-00570A
August 11, 2005 3:52:13 PM PAGE 22 OF 56
COM-22C-015(1996.6.5) REV. 3

7. 회로도


SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
NVIDIA NV43M GRAPHIC 1/4
BA41-00570A
PAGE 23 OF 56
August 11, 2005 3:52:13 PM
U715-1
NV43M
1 / 5
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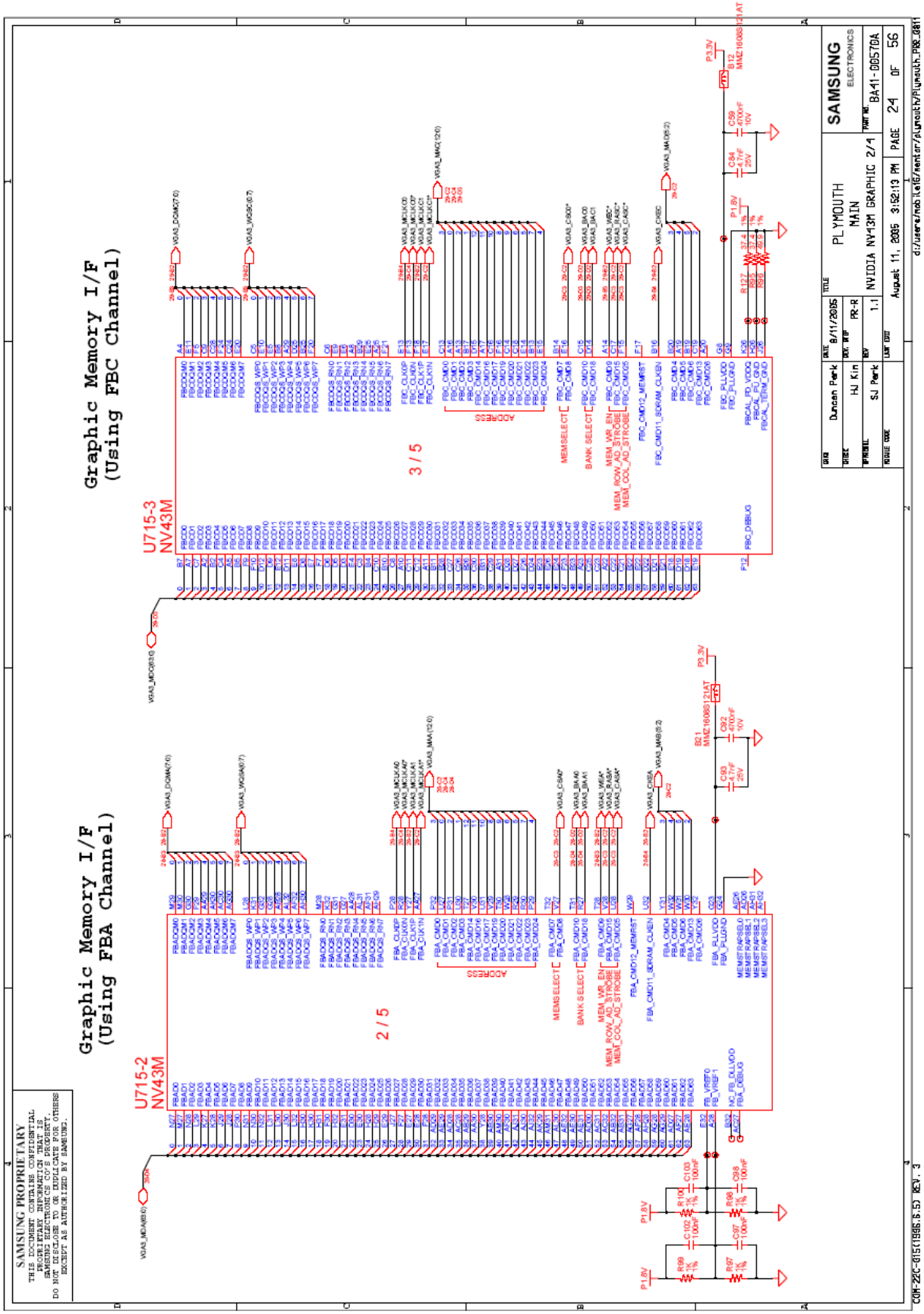
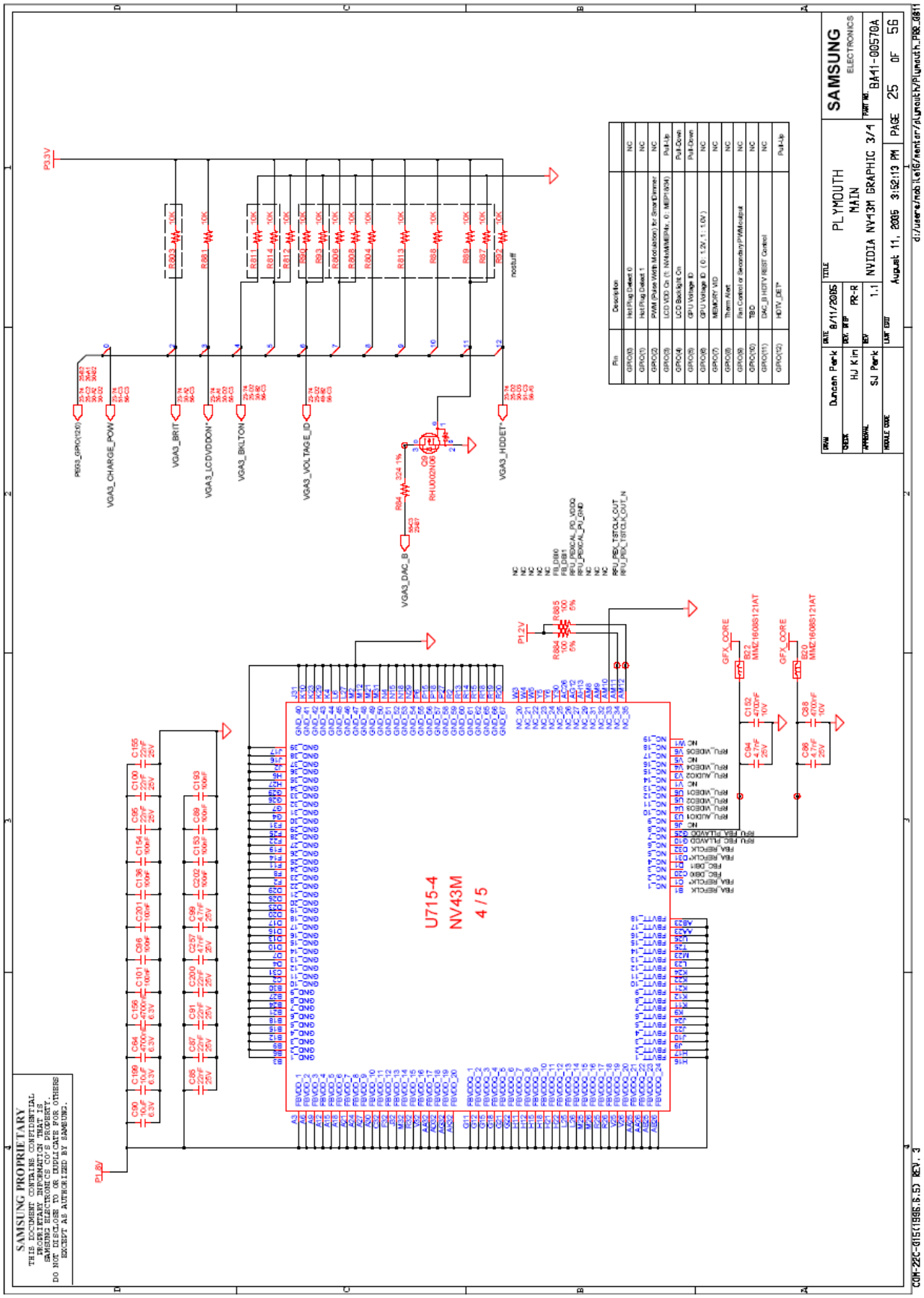
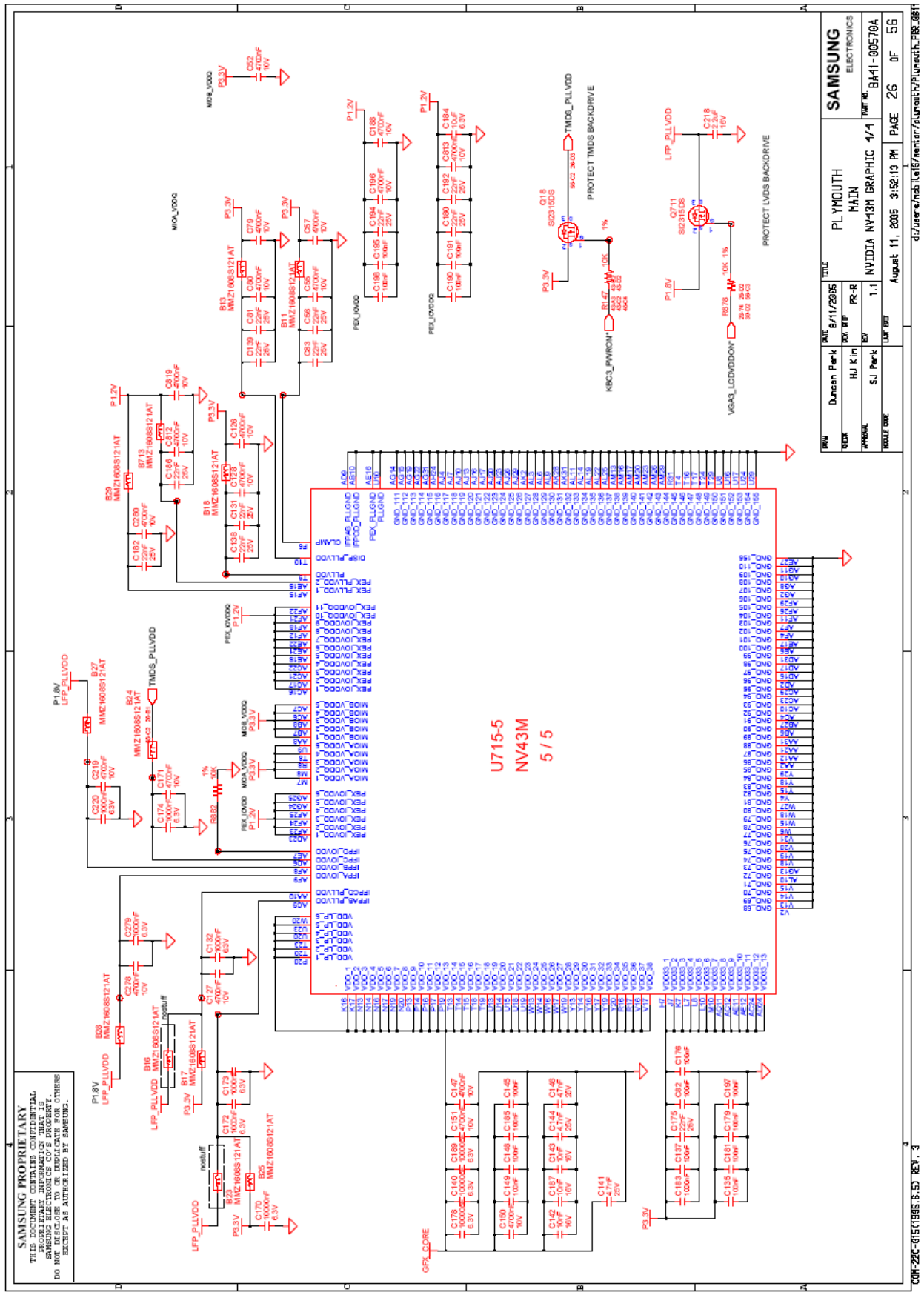
7. 회로도


Graphic Memory I/F
(Using FBA Channel)
U715-2
NV43M
2 / 5
Graphic Memory I/F
(Using FBC Channel)
U715-3
NV43M
3 / 5
SAMSUNG PROPRIETARY
SAMSUNG
PLYMOUTH
MAIN
NVIDIA NV43M GRAPHIC 2/4
BA41-00570A
Duncan Park
HJ Kim
SJ Park
8/11/2005
August 11, 2005 3:52:13 PM
PAGE 24 OF 56

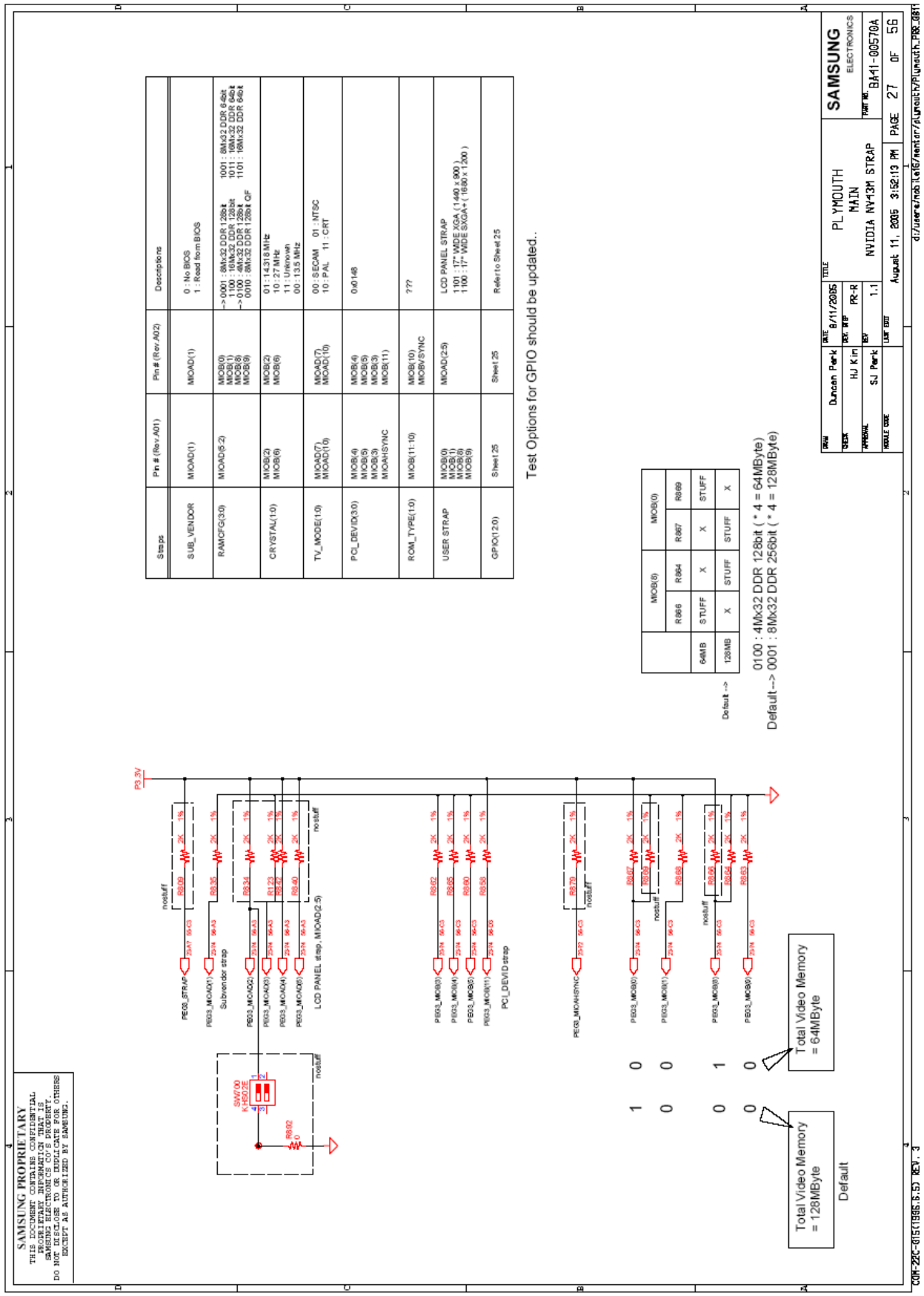
7. 회로도


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
NVIDIA NV43M GRAPHIC 3/4
BA41-00570A
U715-4
NV43M
4 / 5

7. 회로도


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
NVIDIA NV43M GRAPHIC 4/4
BA41-00570A
PAGE 26 OF 56
August 11, 2005 3:52:13 PM
U715-5
NV43M
5 / 5
PROTECT TMDS BACKDRIVE
PROTECT LVDS BACKDRIVE

7. 회로도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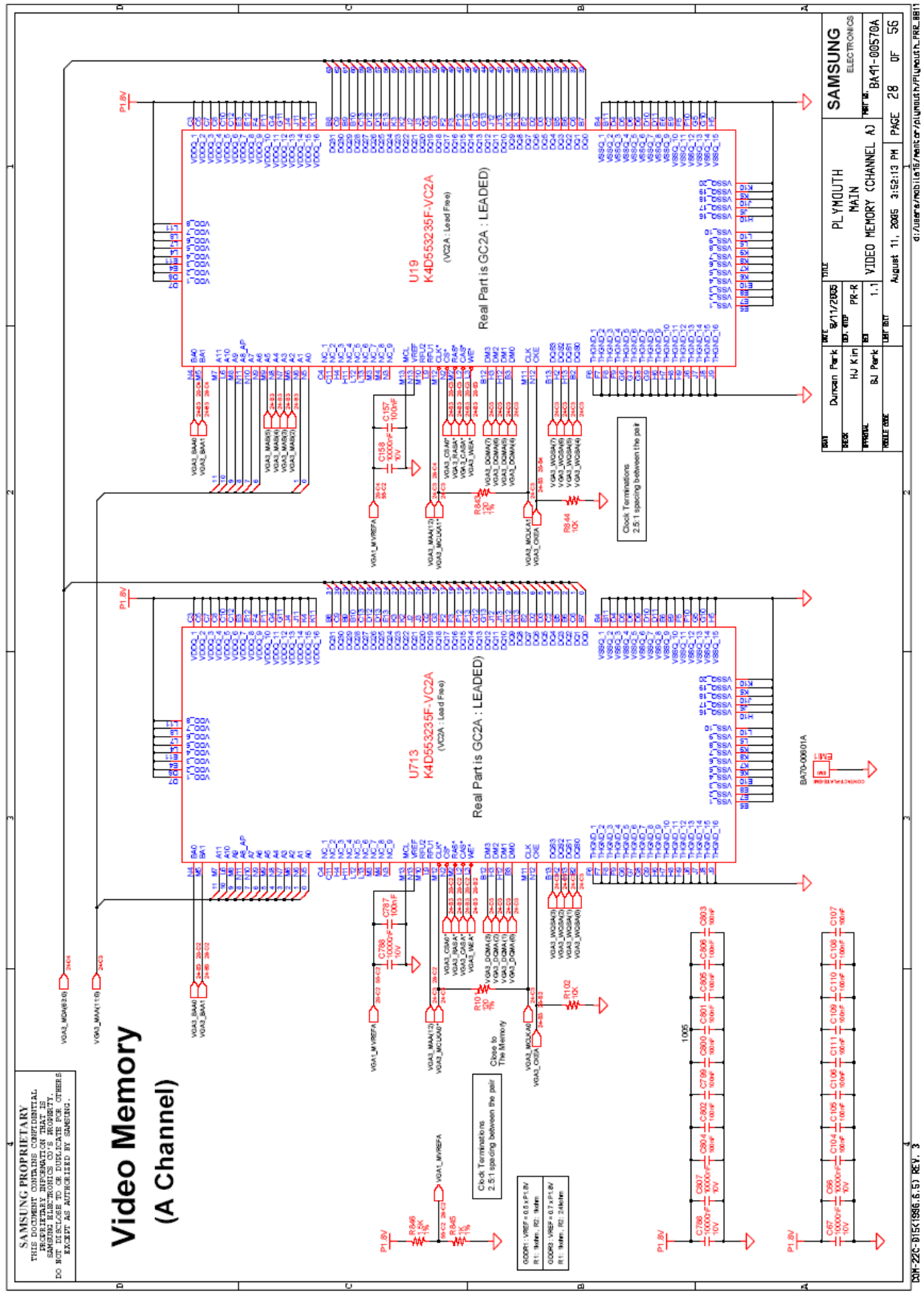
Steps
Pin # (Rev.A01)
Pin # (Rev.A02)
Descriptions
SUB_VENDOR
MIOAD(1)
MIOAD(1)
0 : No BIOS
1 : Read from BIOS
RAMCFG(3:0)
MIOAD(5:2)
MIOB(0)
MIOB(1)
MIOB(8)
MIOB(9)
0001 : 8Mx32 DDR 128bit
1100 : 16Mx32 DDR 128bit
0100 : 4Mx32 DDR 128bit
0010 : 8Mx32 DDR 128bit QF
1001 : 8Mx32 DDR 64bit
1011 : 16Mx32 DDR 64bit
1101 : 16Mx32 DDR 64bit
CRYSTAL(1:0)
MIOB(2)
MIOB(6)
MIOB(2)
MIOB(6)
01 : 14.318 MHz
10 : 27 MHz
11 : Unknown
00 : 13.5 MHz
TV_MODE(1:0)
MIOAD(7)
MIOAD(10)
MIOAD(7)
MIOAD(10)
00 : SECAM 01 : NTSC
10 : PAL 11 : CRT
PCI_DEVID(3:0)
MIOB(4)
MIOB(5)
MIOB(3)
MIOAHSYNC
MIOB(4)
MIOB(5)
MIOB(3)
MIOB(11)
0x0148
ROM_TYPE(1:0)
MIOB(11:10)
MIOB(10)
MIOBV/SYNC
???
USER STRAP
MIOB(0)
MIOB(1)
MIOB(8)
MIOB(9)
MIOAD(2:5)
LCD PANEL STRAP
101 : 17" WIDE XGA (1440 x 900)
1100 : 17" WIDE SXGA+ (1680 x 1200)
GPIO(12:0)
Sheet 25
Sheet 25
Refer to Sheet 25
Test Options for GPIO should be updated..
MIOB(8)
MIOB(0)
R666
R664
R667
R669
64MB
STUFF
X
X
STUFF
128MB
X
STUFF
STUFF
X
Default -->
0100 : 4Mx32 DDR 128bit (* 4 = 64MByte)
Default--> 0001 : 8Mx32 DDR 256bit (* 4 = 128MByte)
P3.3V
PEG_STRAP
PEG3_MIOAD(1)
Subvendor strap
PEG3_MIOAD(2)
PEG3_MIOAD(3)
PEG3_MIOAD(4)
PEG3_MIOAD(5)
LCD PANEL strap, MIOAD(2:5)
PEG3_MIOB(3)
PEG3_MIOB(4)
PEG3_MIOB(5)
PEG3_MIOB(11)
PCI_DEVID strap
PEG3_MIOAHSYNC
PEG3_MIOB(0)
PEG3_MIOB(1)
PEG3_MIOB(8)
PEG3_MIOB(9)
SW700
K H502E
R892
0
nostuff
1 0
0 0
0 1
0 0
Total Video Memory
= 64MByte
Total Video Memory
= 128MByte
Default
DRW
Duncan Park
8/11/2005
CHECK
HJ Kim
APPROVAL
SJ Park
MODULE CODE
TITLE
PLYMOUTH
MAIN
NVIDIA NV43M STRAP
PART NO.
BA41-00570A
LAST EDIT
August 11, 2005 3:52:13 PM
PAGE 27 OF 56
SAMSUNG
ELECTRONICS
COM-22C-015(1986.6.5) REV. 3
d:/users/mobile6/mentor/plymouth/Plymouth_PRR.ddb

7. 회로도


Video Memory
(A Channel)
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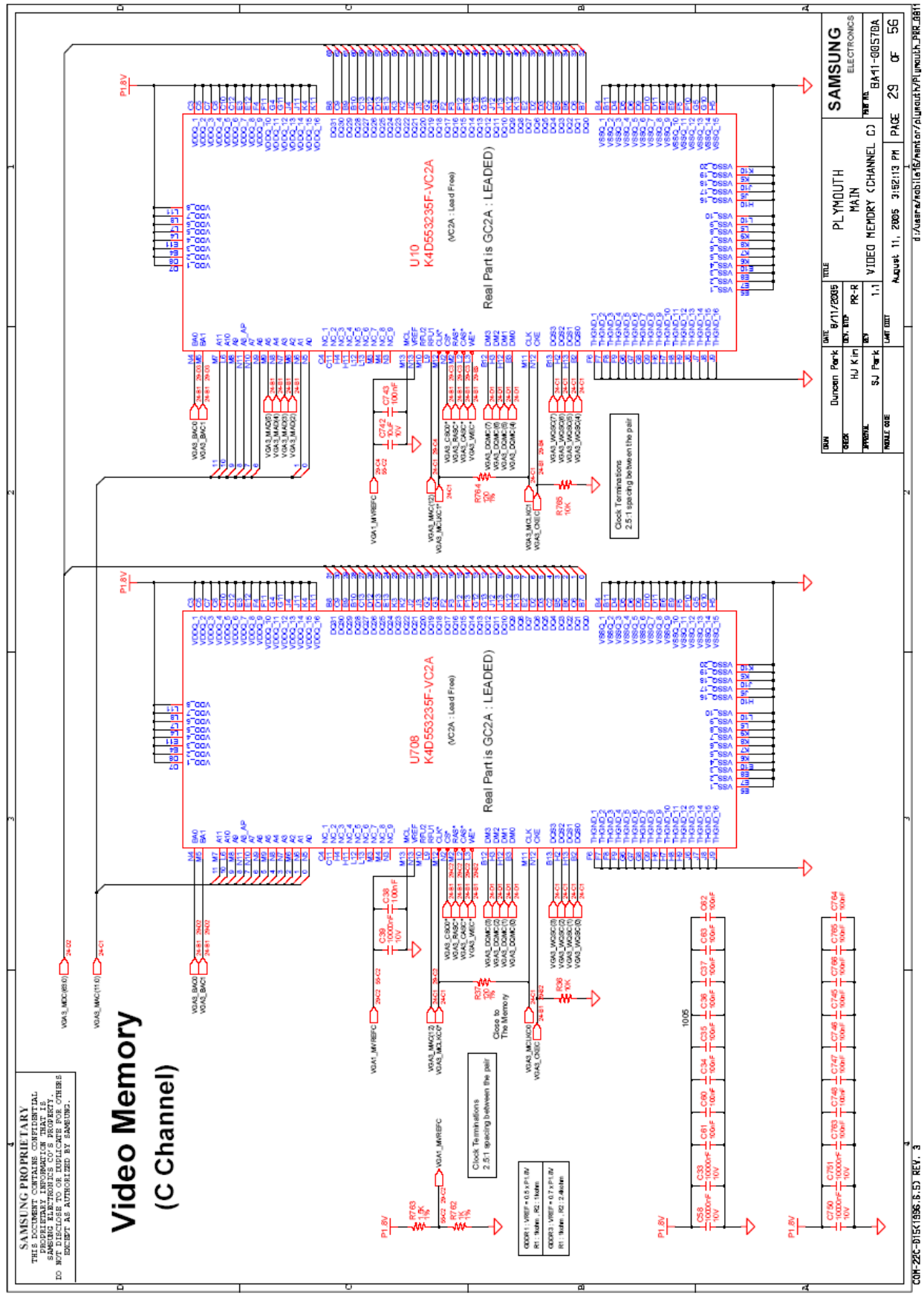
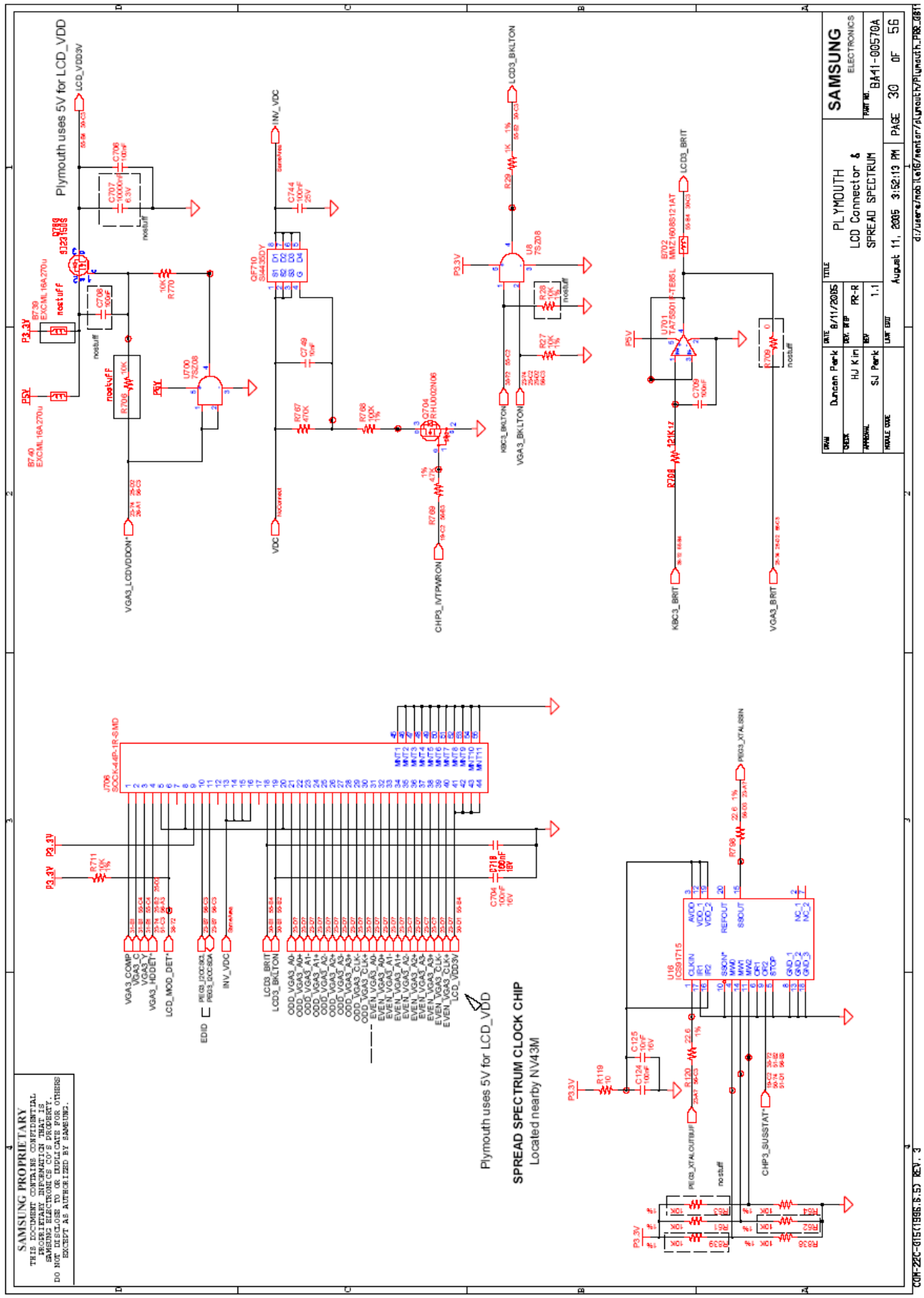
U19
K4D553235F-VC2A
(VC2A : Lead Free)
Real Part is GC2A : LEADED)
U713
K4D553235F-VC2A
(VC2A : Lead Free)
Real Part is GC2A : LEADED)
Clock Terminations
2.5:1 spacing between the pair
Close to
The Memory
P1.8V
PLYMOUTH
MAIN
VIDEO MEMORY (CHANNEL A)
SAMSUNG
ELECTRONICS
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 28 OF 56

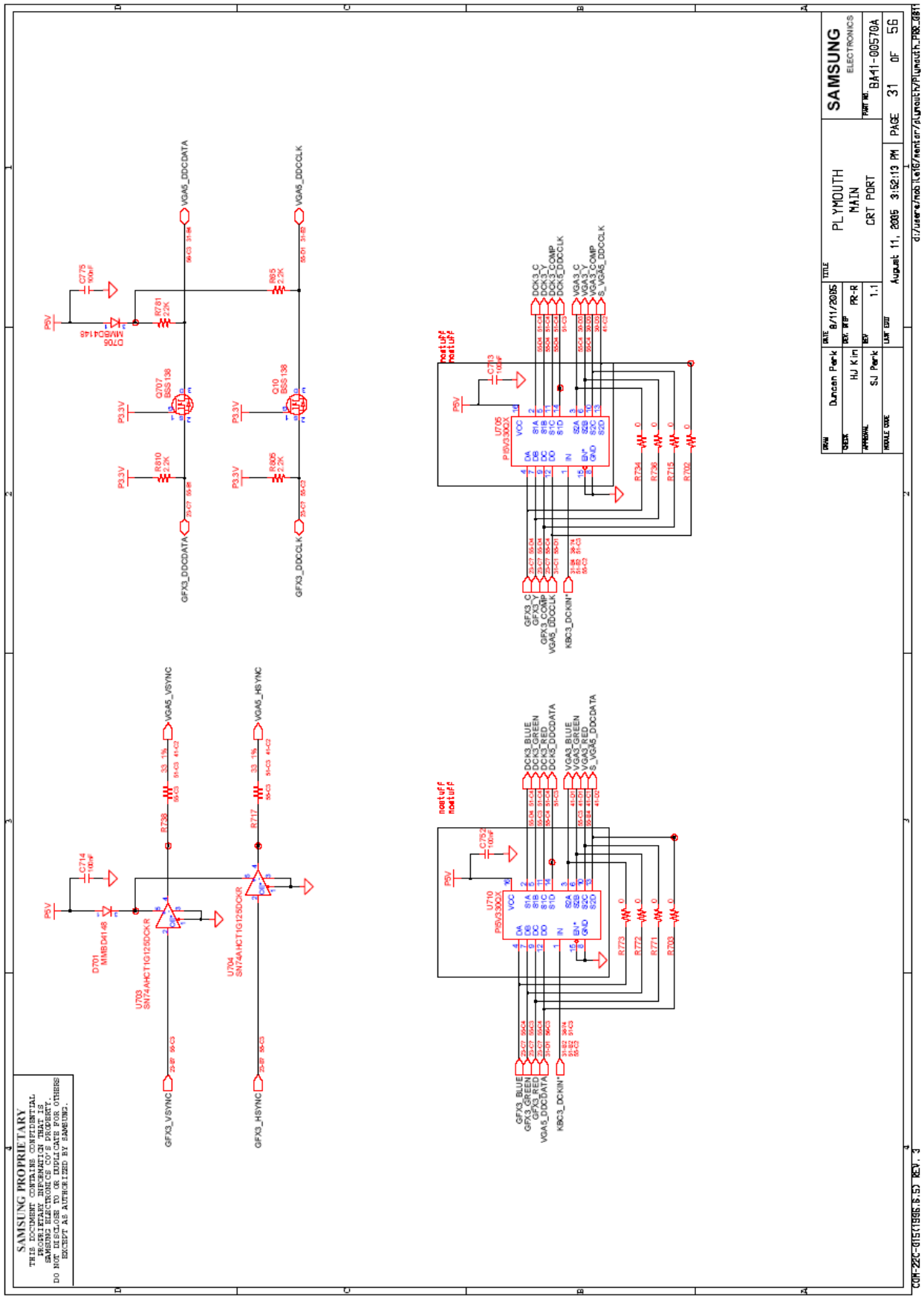
7. 회로도


Video Memory
(C Channel)
U10
K4D553235F-VC2A
(VC2A : Lead Free)
Real Part is GC2A : LEADED
U708
K4D553235F-VC2A
(VC2A : Lead Free)
Real Part is GC2A : LEADED
Clock Terminations
2.5:1 spacing between the pair
Close to
The Memory
SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
VIDEO MEMORY (CHANNEL C)
BA41-00857DA
PAGE 29 OF 56
August 11, 2005 3:52:13 PM

7. 회로도


Plymouth uses 5V for LCD_VDD
SPREAD SPECTRUM CLOCK CHIP
Located nearby NV43M
SAMSUNG PROPRIETARY
SAMSUNG
PLYMOUTH
LCD Connector &
SPREAD SPECTRUM
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 30 OF 56

7. 회로도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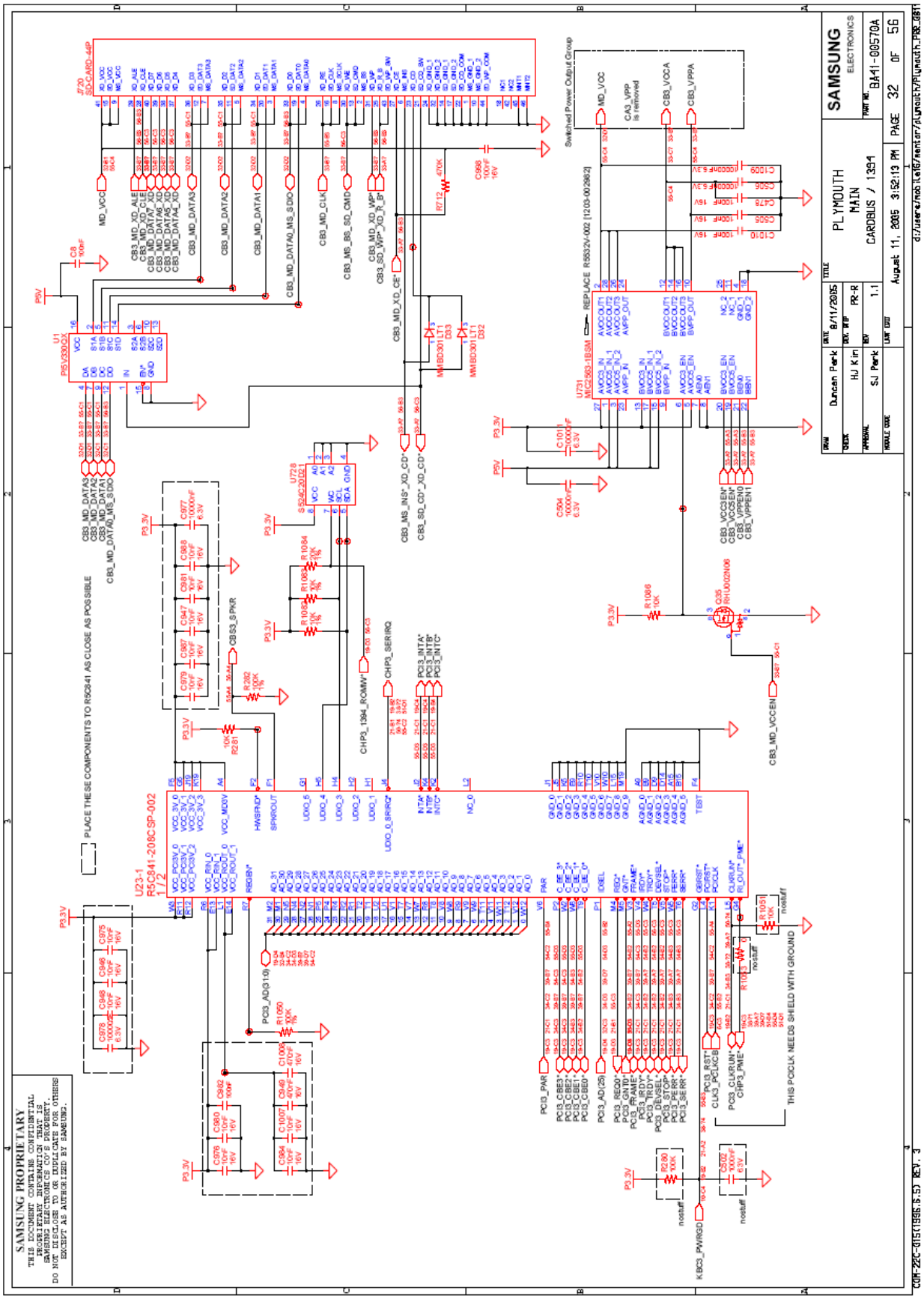
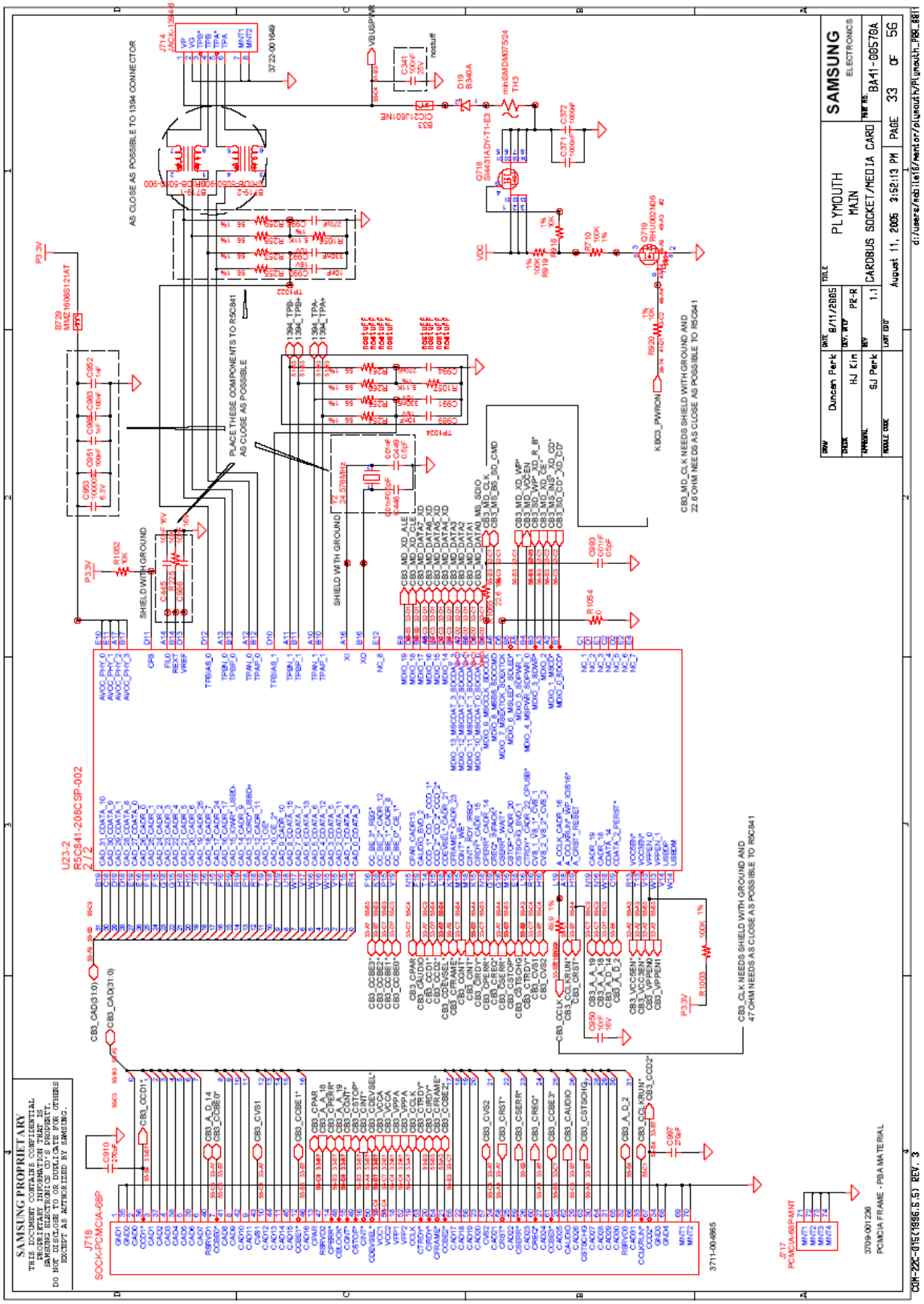
PLYMOUTH
MAIN
CRT PORT
SAMSUNG ELECTRONICS
BA41-00570A
PAGE 31 OF 56
August 11, 2005 3:52:13 PM
d:/users/mobile16/mentor/plymouth/PLymouth_PRR_0811
COM-22C-015(1996.6.5) REV.3

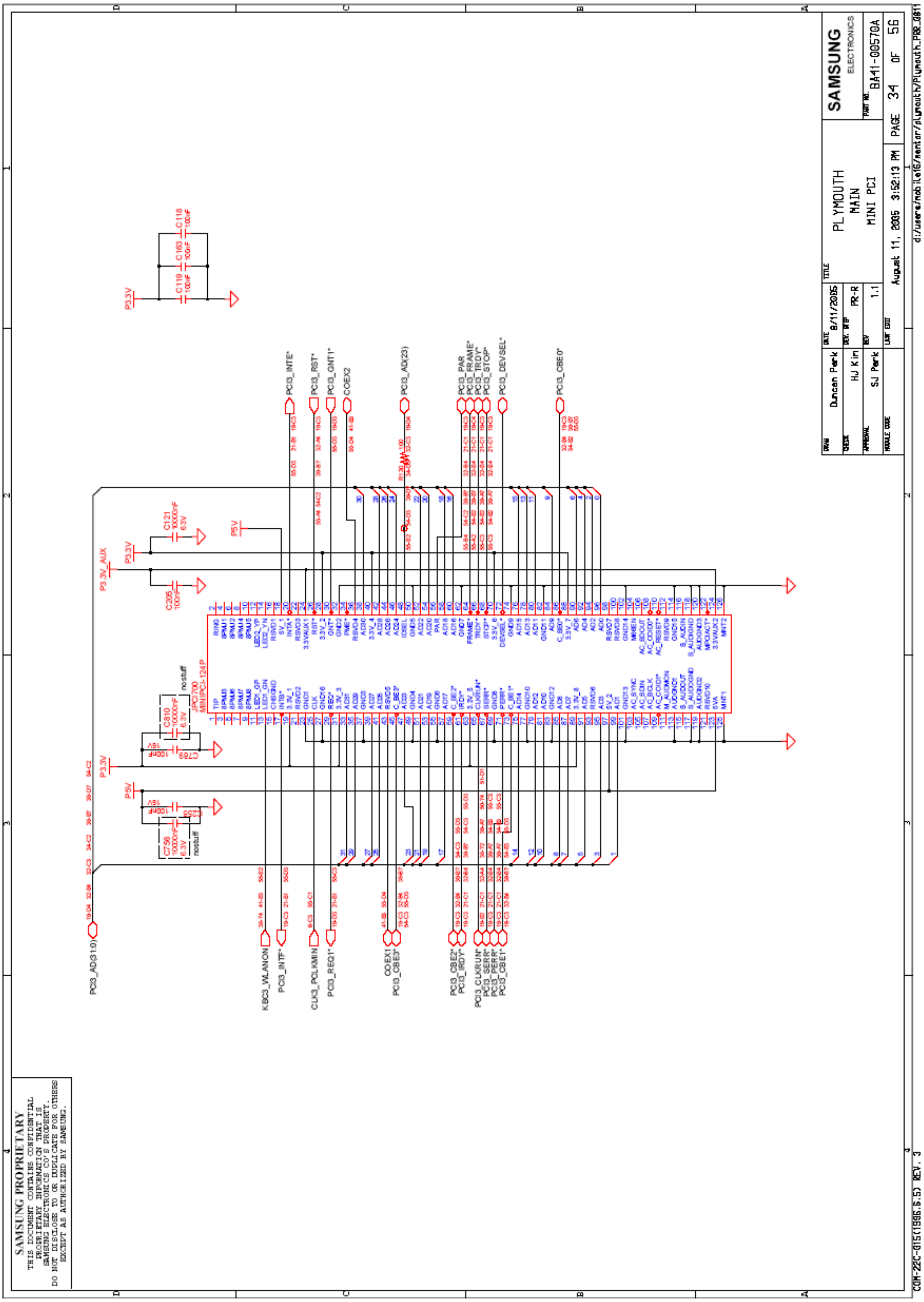
7. 회로도



7. 회로도



7. 회로도


SAMSUNG ELECTRONICS
PLYMOUTH
MAIN
MINI PCI
BA41-00570A
PAGE 34 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
PR-R
1.1
SAMSUNG PROPRIETARY
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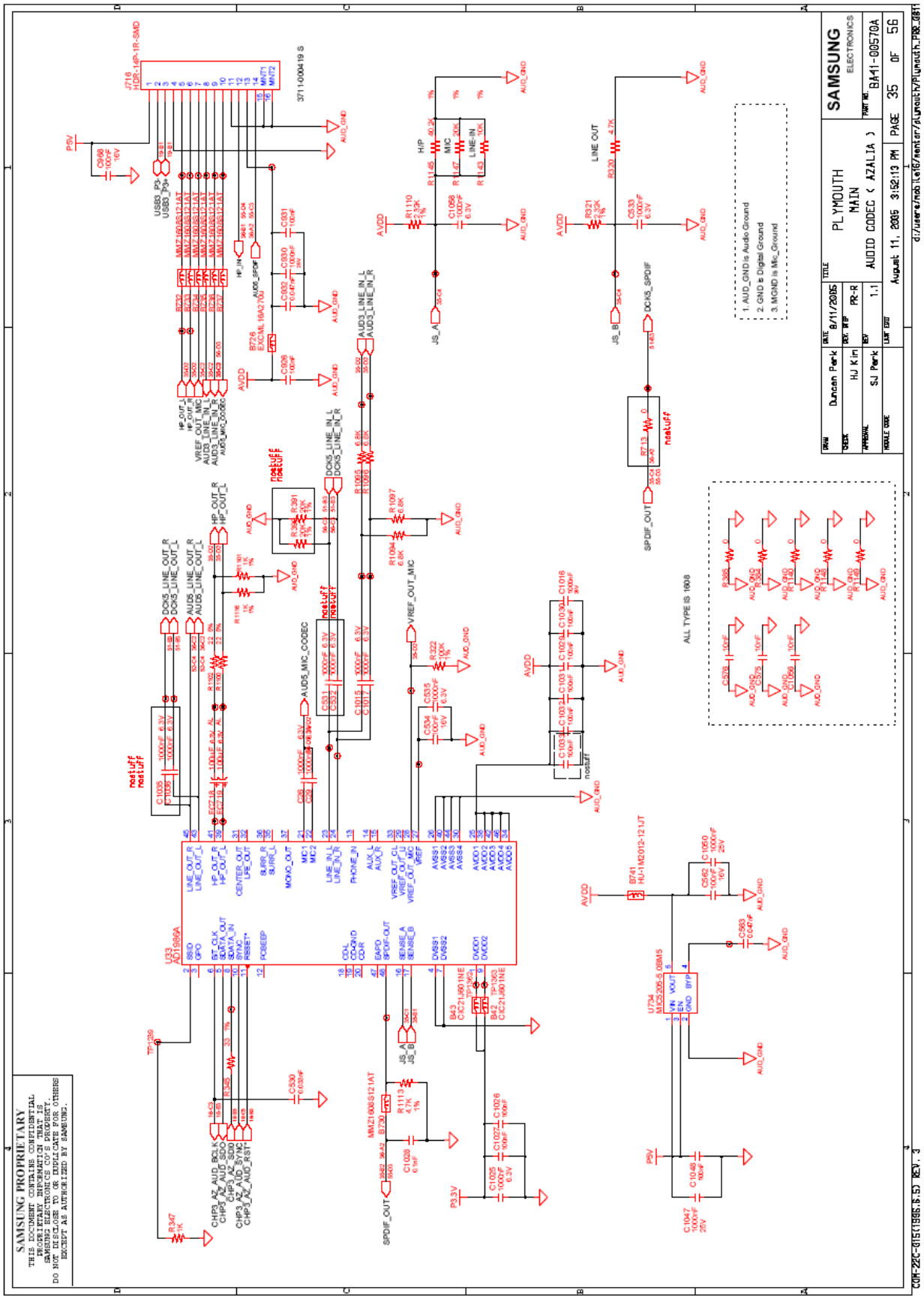
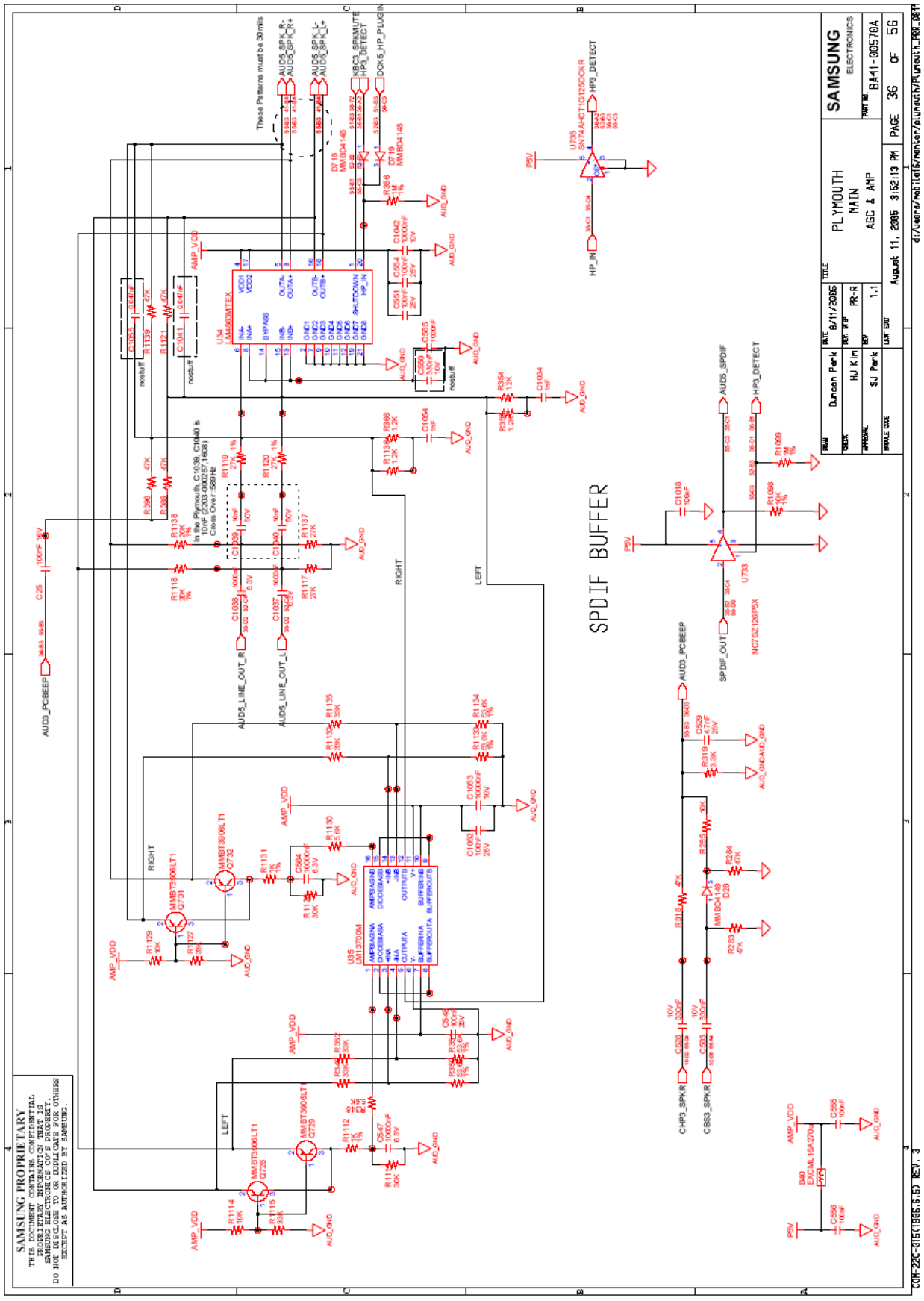
JMPCI700
MINIPCI-124P
COM-22C-015(1996.6.5) REV. 3

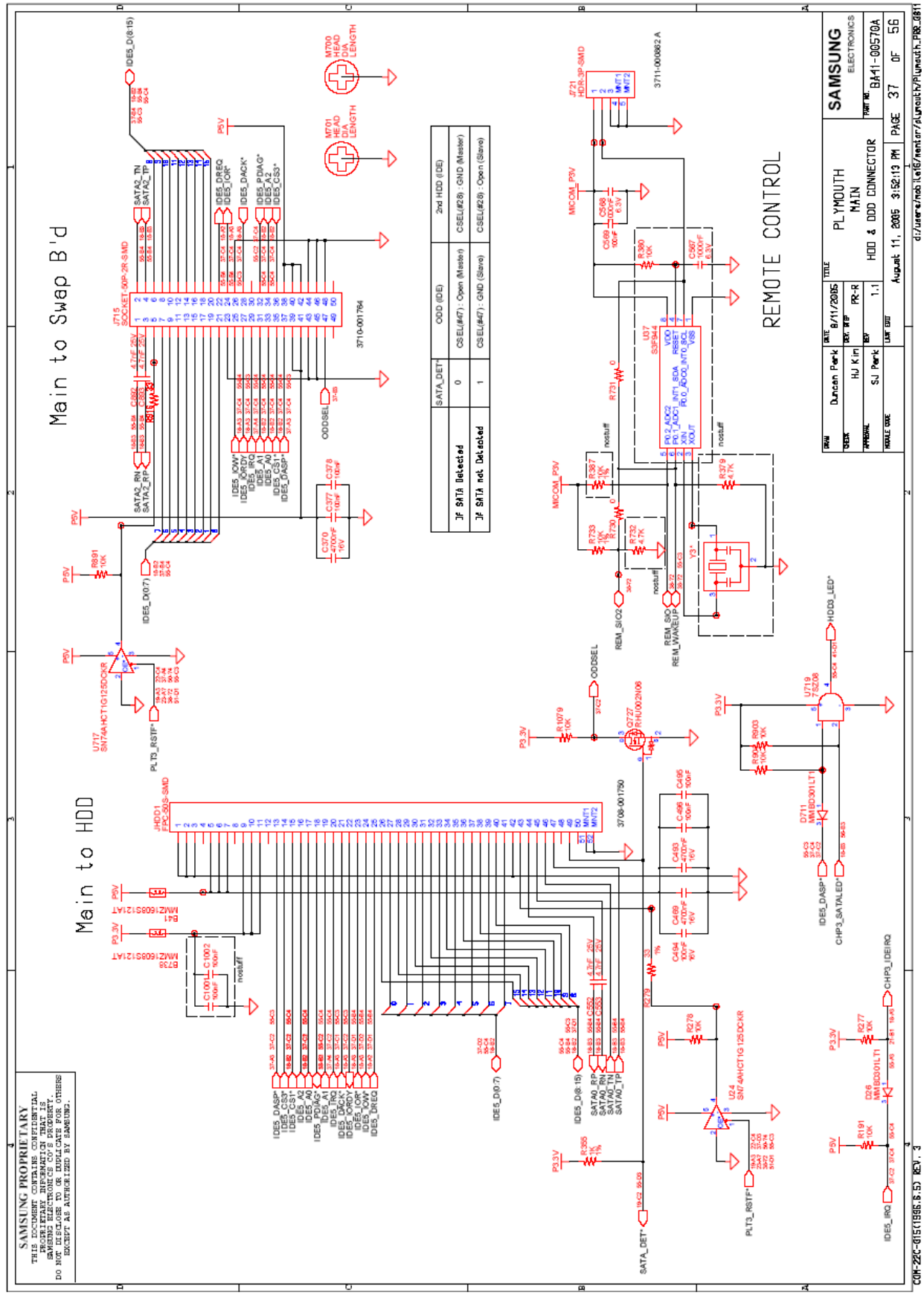
7. 회로도


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
AUDIO CODEC (AZALIA)
BA41-00570A
PAGE 35 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
1. AUD_GND is Audio Ground
2. GND is Digital Ground
3. MGND is Mic_Ground
ALL TYPE IS 1608

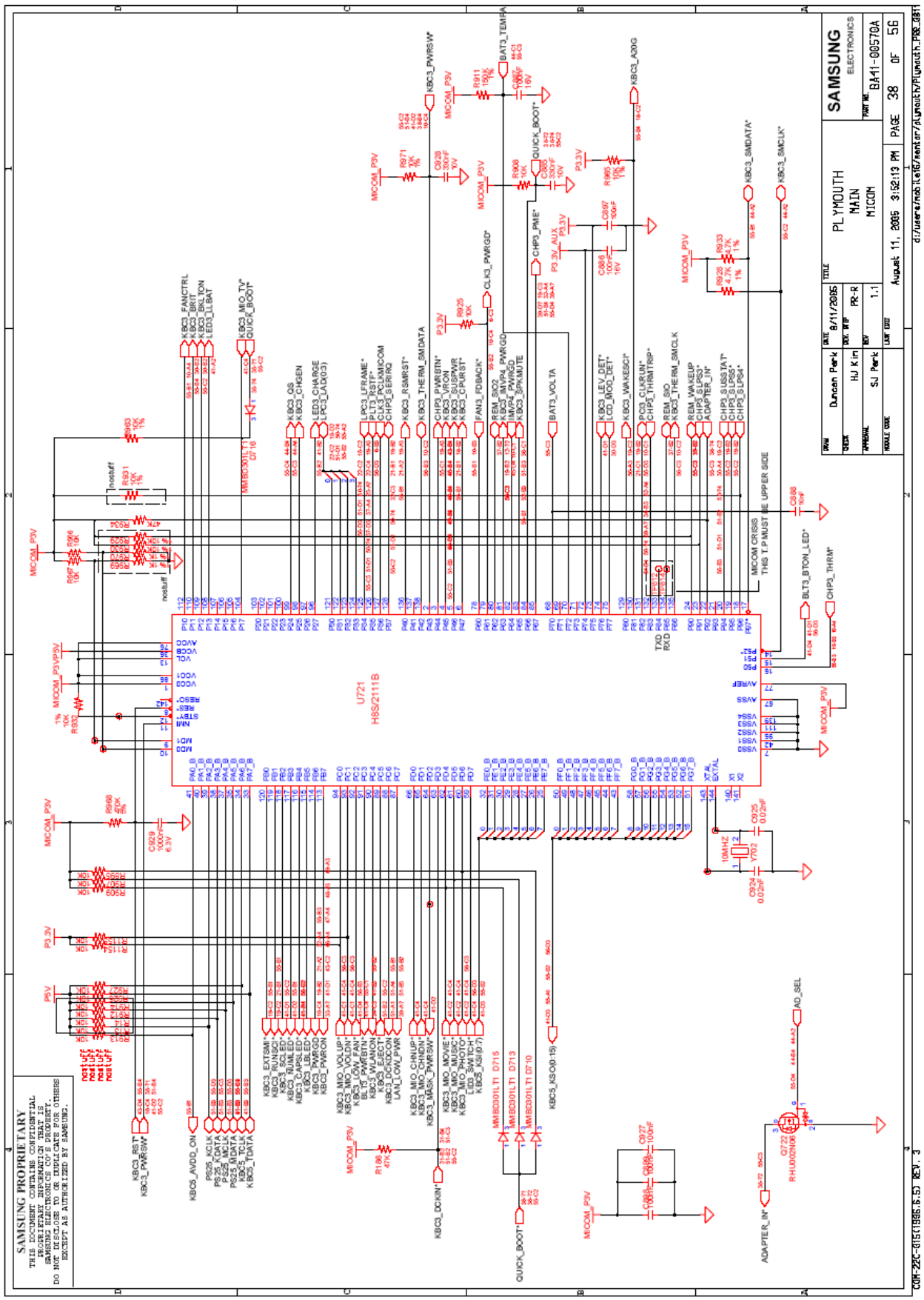
7. 회로도


SPDIF BUFFER
SAMSUNG PROPRIETARY
SAMSUNG
PLYMOUTH
MAIN
AGC & AMP
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 36 OF 56

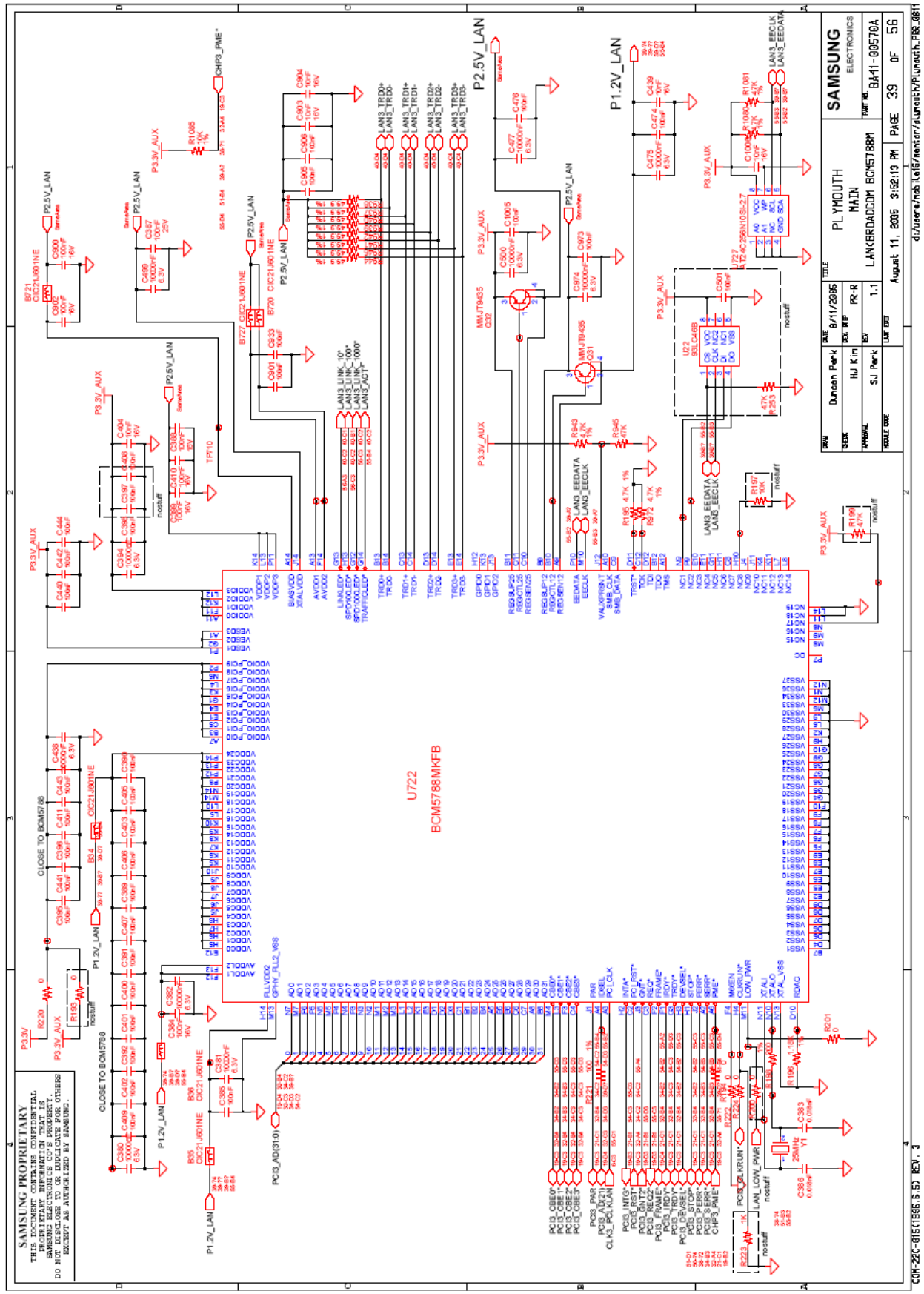
7. 회로도


Main to Swap B'd
Main to HDD
REMOTE CONTROL
SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
HDD & ODD CONNECTOR
BA41-00570A
PAGE 37 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
FR-R
1.1
SATA_DET*
JF SATA Detected
JF SATA not Detected
ODD (IDE)
2nd HDD (IDE)
CSEL(#47) : Open (Master)
CSEL(#47) : GND (Slave)
CSEL(#28) : GND (Master)
CSEL(#28) : Open (Slave)

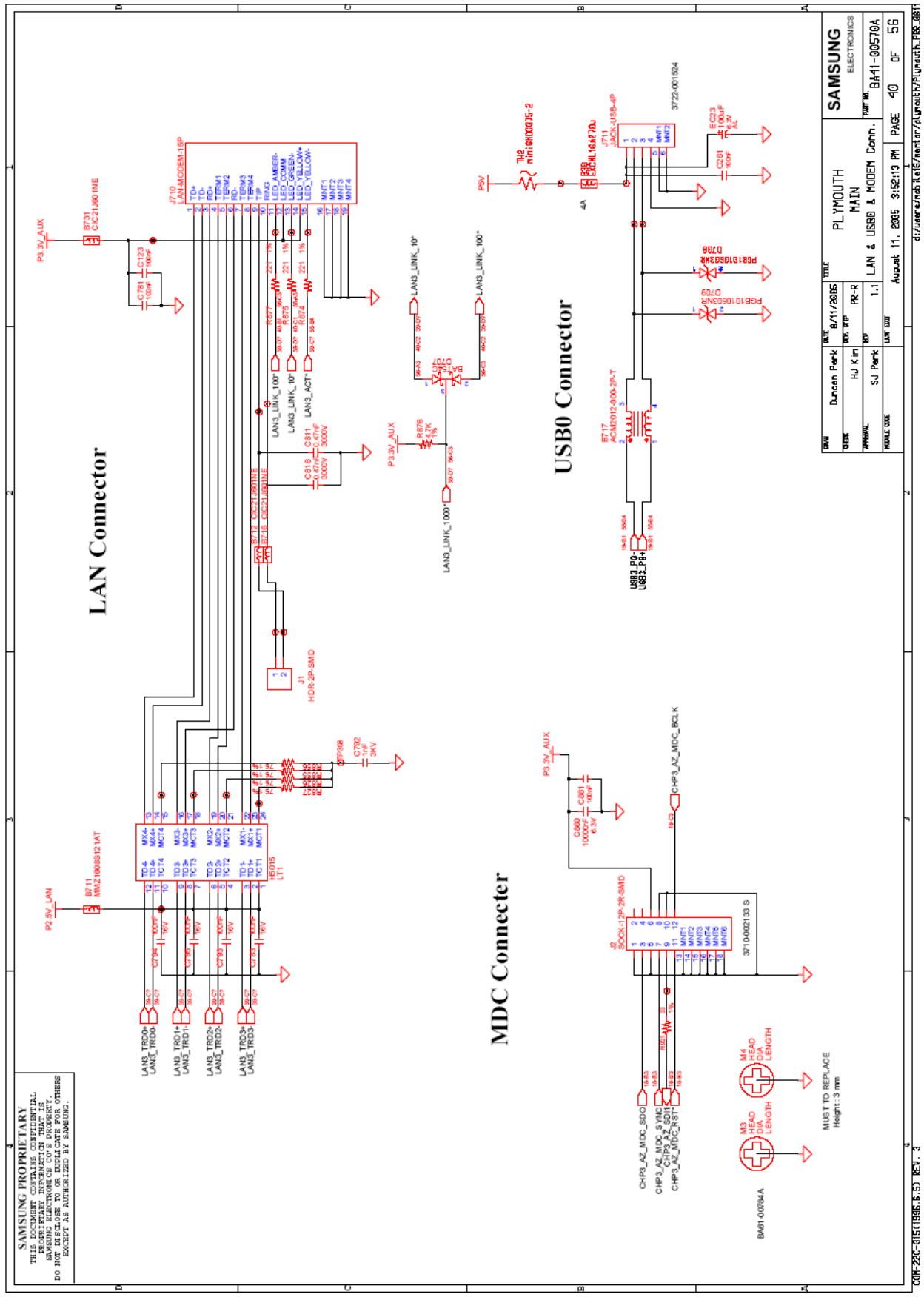
7. 회로도


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
MICOM
BA41-00570A
PAGE 38 OF 56
August 11, 2005 3:52:13 PM
U721
H8S/2111B

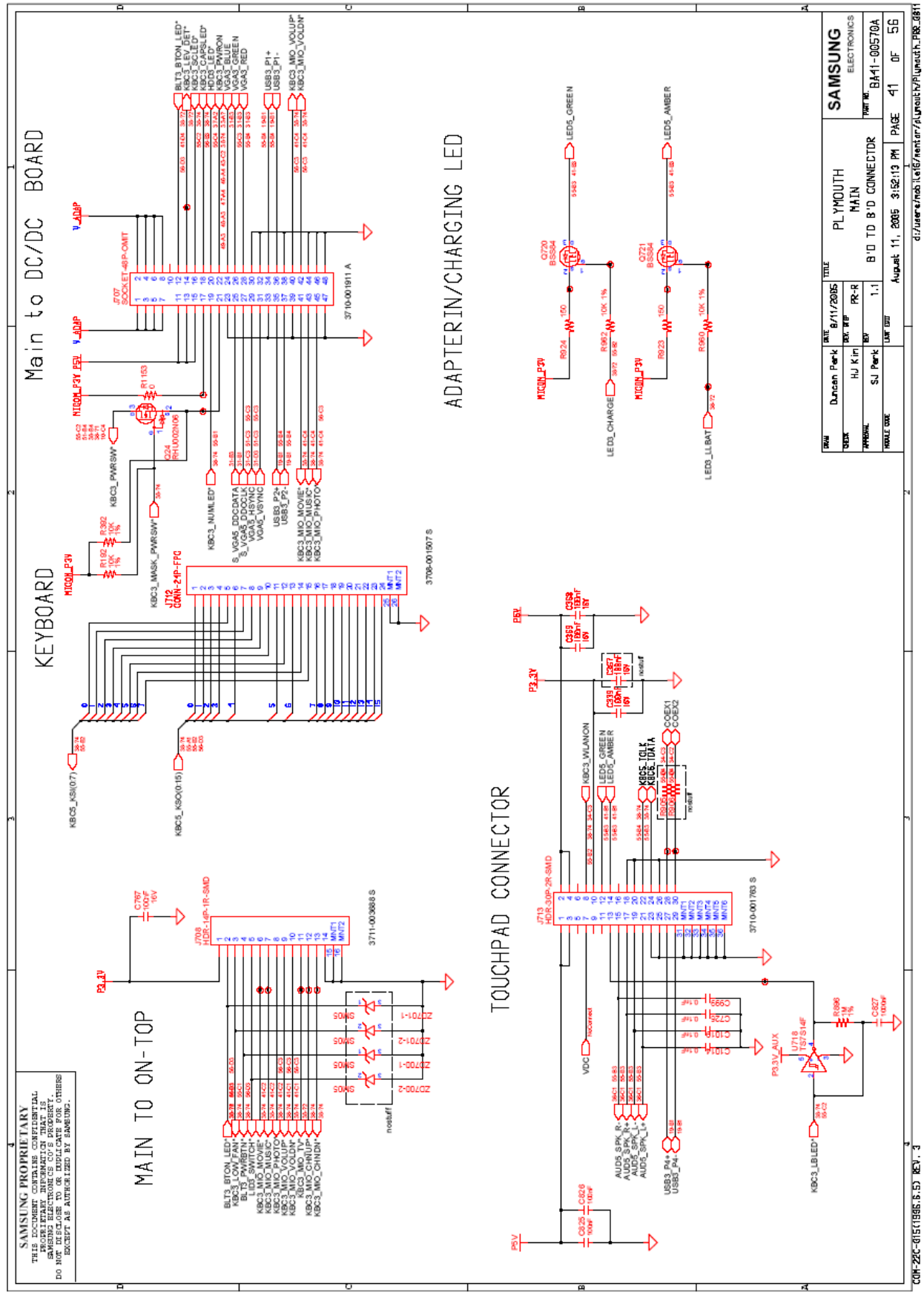
7. 회로도


SAMSUNG PROPRIETARY
SAMSUNG ELECTRONICS
SAMSUNG
PLYMOUTH
MAIN
LAN(BROADCOM BCM5788M
BA41-00570A
August 11, 2005 3:52:13 PM
U722
BCM5788MKFB
P2.5V_LAN
P1.2V_LAN
P3.3V_AUX
CLOSE TO BCM5788

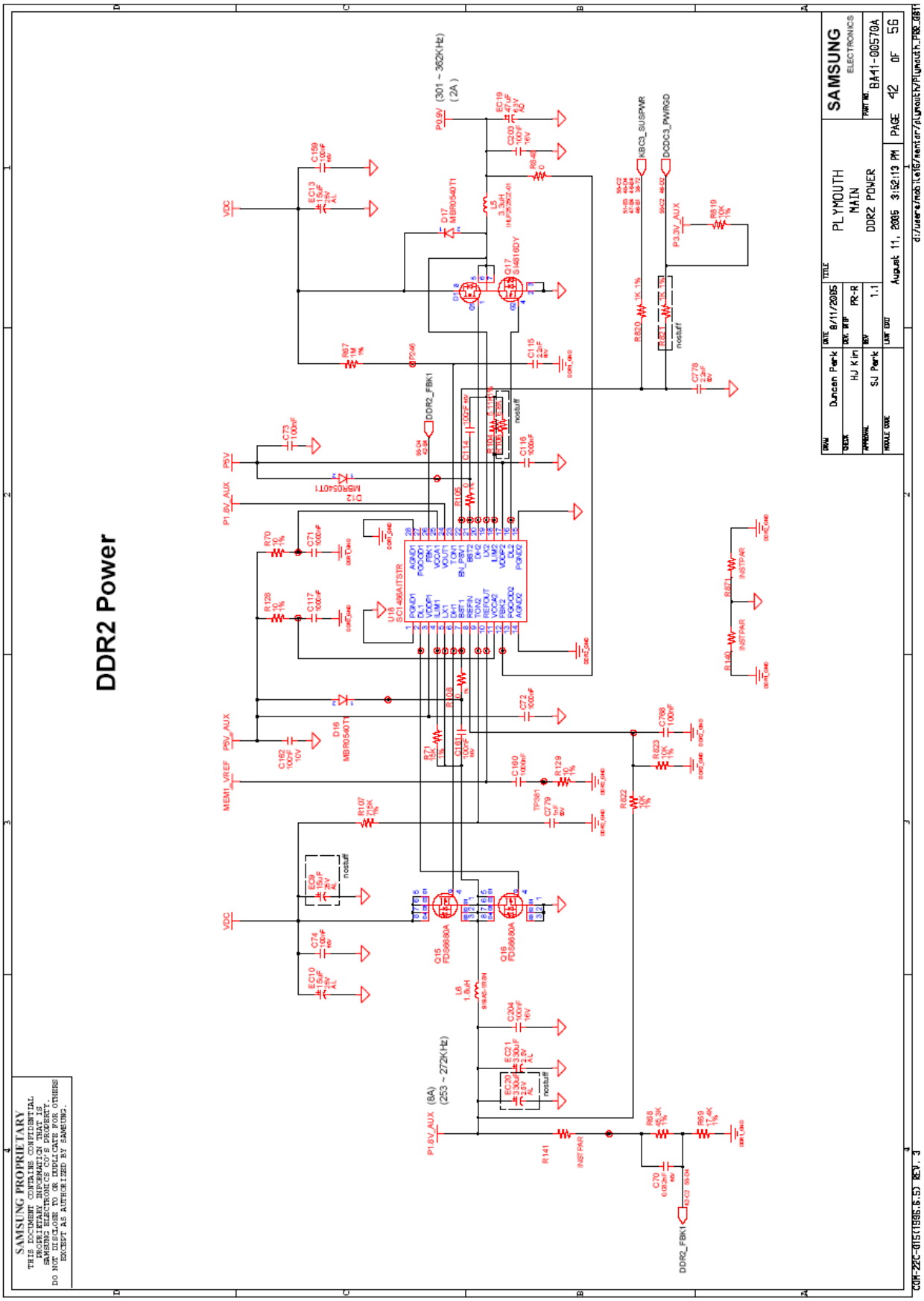
7. 회로도


LAN Connector
USB0 Connector
MDC Connecter
SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
LAN & USB0 & MODEM Conn.
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 40 OF 56

7. 회로도


Main to DC/DC BOARD
KEYBOARD
MAIN TO ON-TOP
ADAPTERIN/CHARGING LED
TOUCHPAD CONNECTOR
SAMSUNG PROPRIETARY
PLYMOUTH
MAIN
B'D TO B'D CONNECTOR
SAMSUNG ELECTRONICS
BA41-00570A

7. 회로도


DDR2 Power
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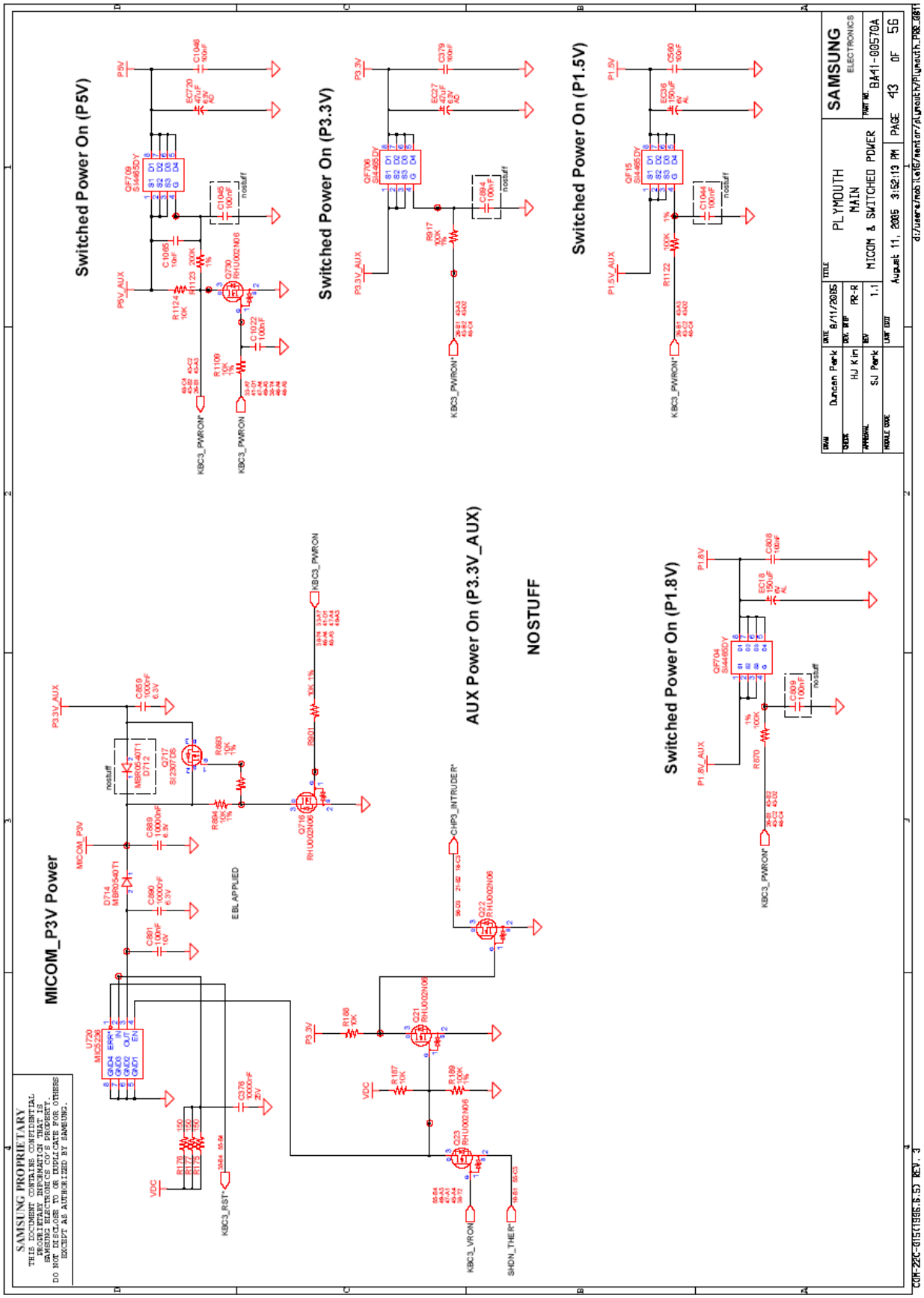
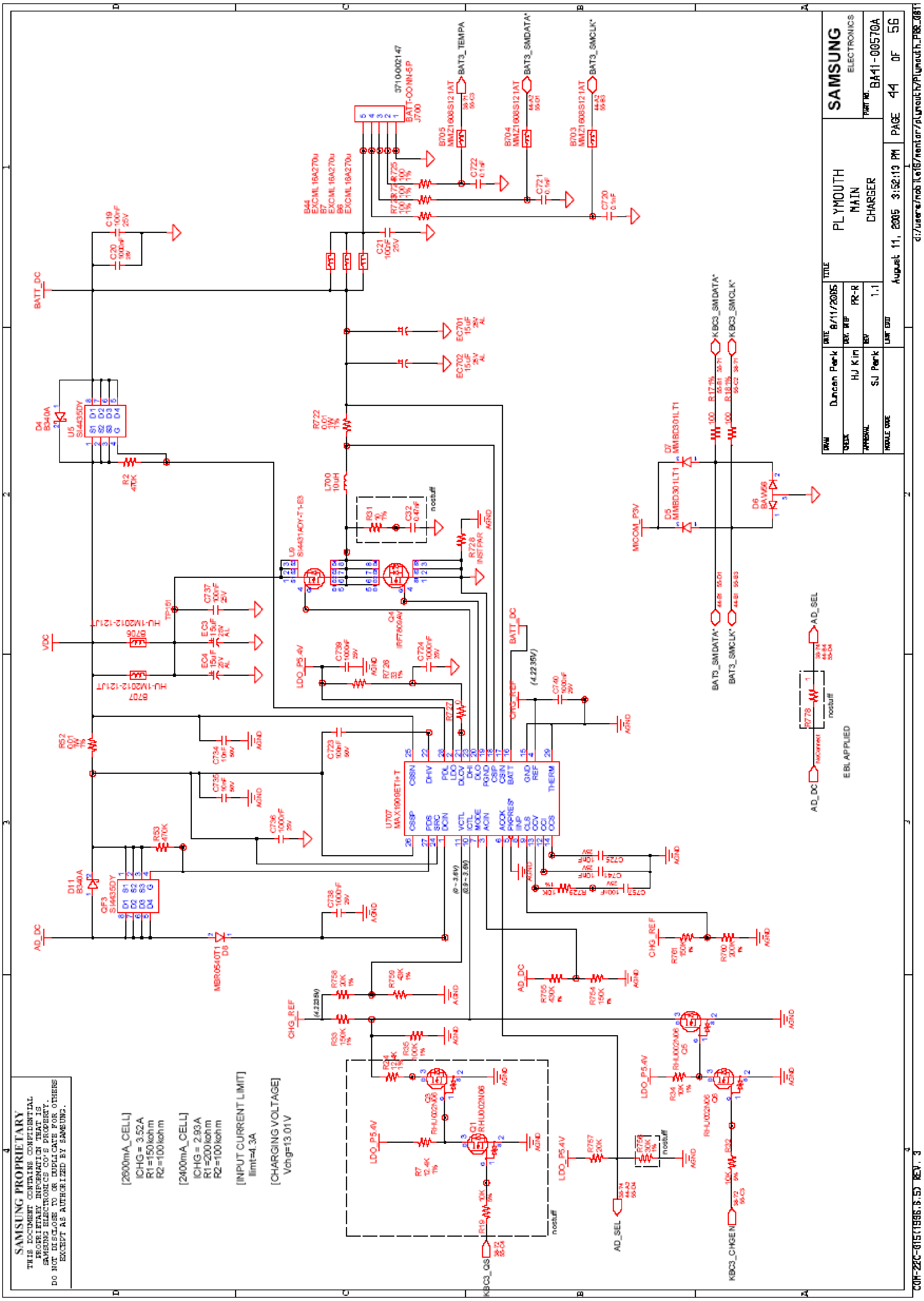
SAMSUNG ELECTRONICS
PLYMOUTH
MAIN
DDR2 POWER
BA41-00570A
PAGE 42 OF 56
August 11, 2005 3:52:13 PM
d:/users/mobile16/kentar/plymouth/Plymouth_PBR.dsn
Duncan Park 8/11/2005
HJ Kim PR-R
SJ Park 1.1
P0.9V (301 ~ 362K(Hz) (2A)
P1.8V_AUX (8A) (253 ~ 272K(Hz)
P3.3V_AUX
P5V
P5V_AUX
VDC
MEM1_VREF
DDR2_FBK1
KBC3_SUSPWR
DCDC3_PWRGD

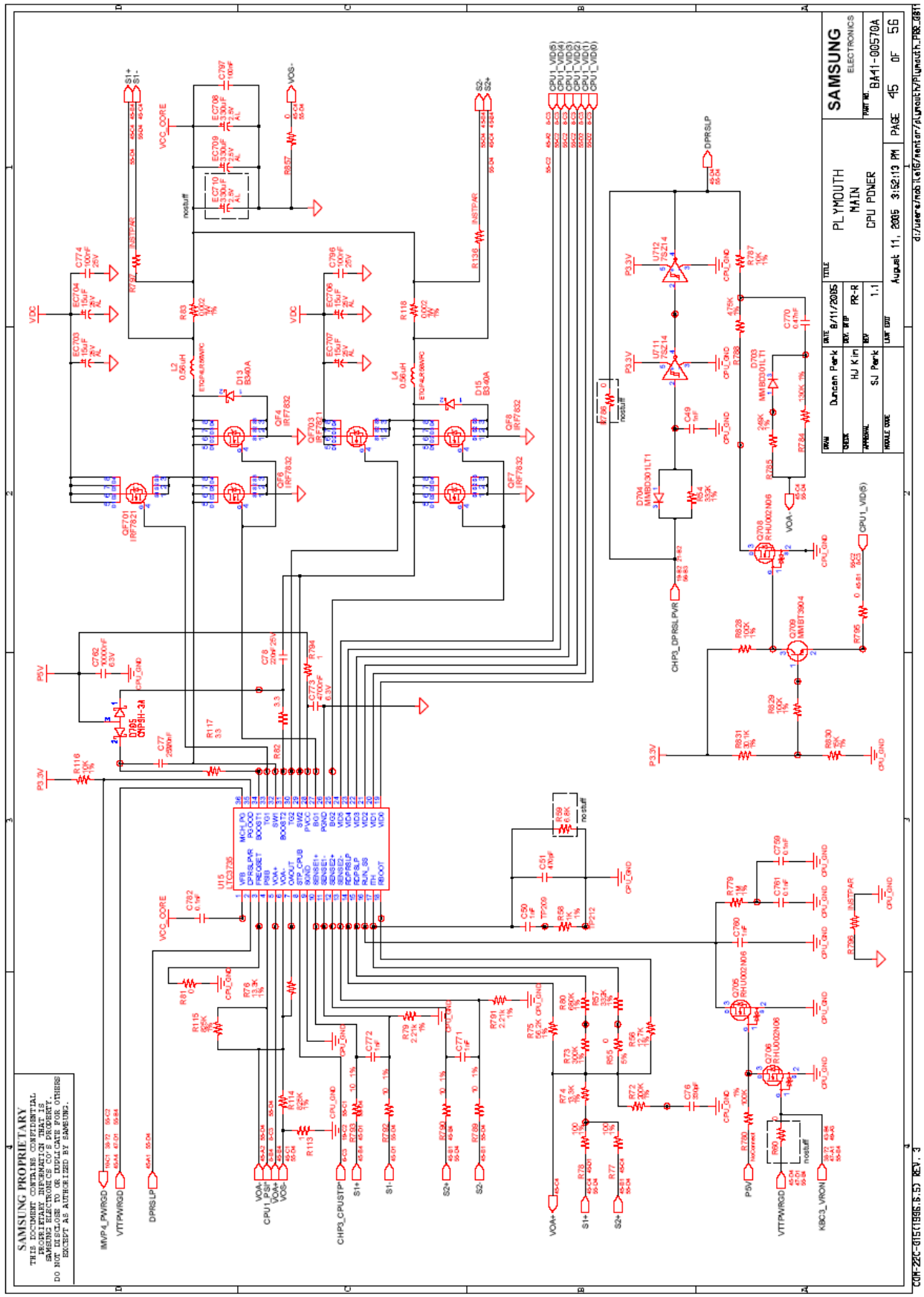
7. 회로도


Switched Power On (P5V)
Switched Power On (P3.3V)
Switched Power On (P1.5V)
Switched Power On (P1.8V)
AUX Power On (P3.3V_AUX)
MICOM_P3V Power
NOSTUFF
EBL APPLIED
SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
MICOM & SWITCHED POWER
BA41-00570A
PAGE 43 OF 56
August 11, 2005 3:52:13 PM

7. 회로도


SAMSUNG PROPRIETARY
SAMSUNG ELECTRONICS
PLYMOUTH MAIN CHARGER
BA41-00570A
MAX1909ETI+T
[2600mA_CELL]
ICHG = 3.52A
R1=150kohm
R2=100kohm
[2400mA_CELL]
ICHG = 2.93A
R1=200kohm
R2=100kohm
[INPUT CURRENT LIMIT]
Ilimit=4.3A
[CHARGING VOLTAGE]
Vchg=13.01V

7. 회로도


SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
CPU POWER
BA41-00570A
PAGE 45 OF 56
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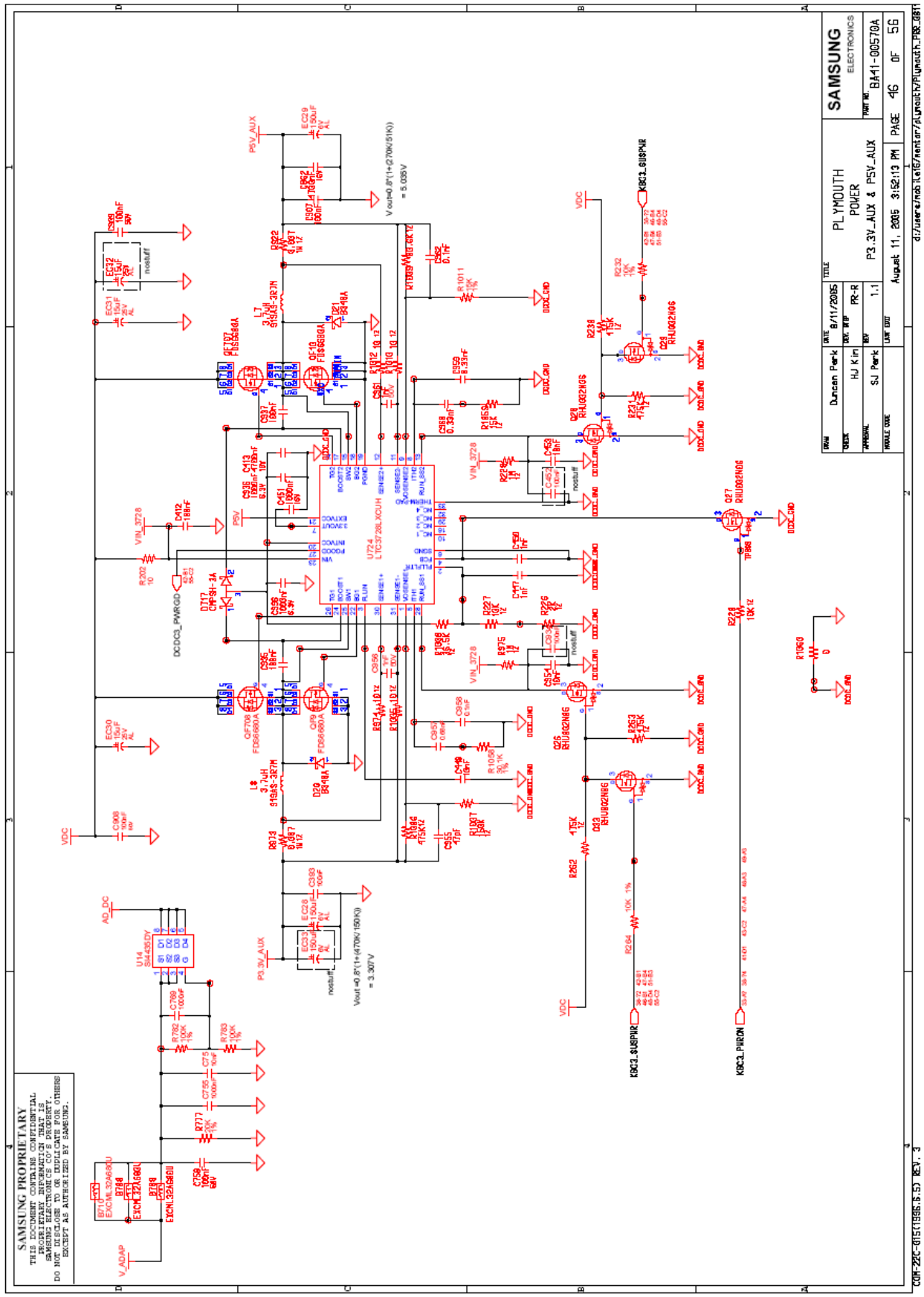
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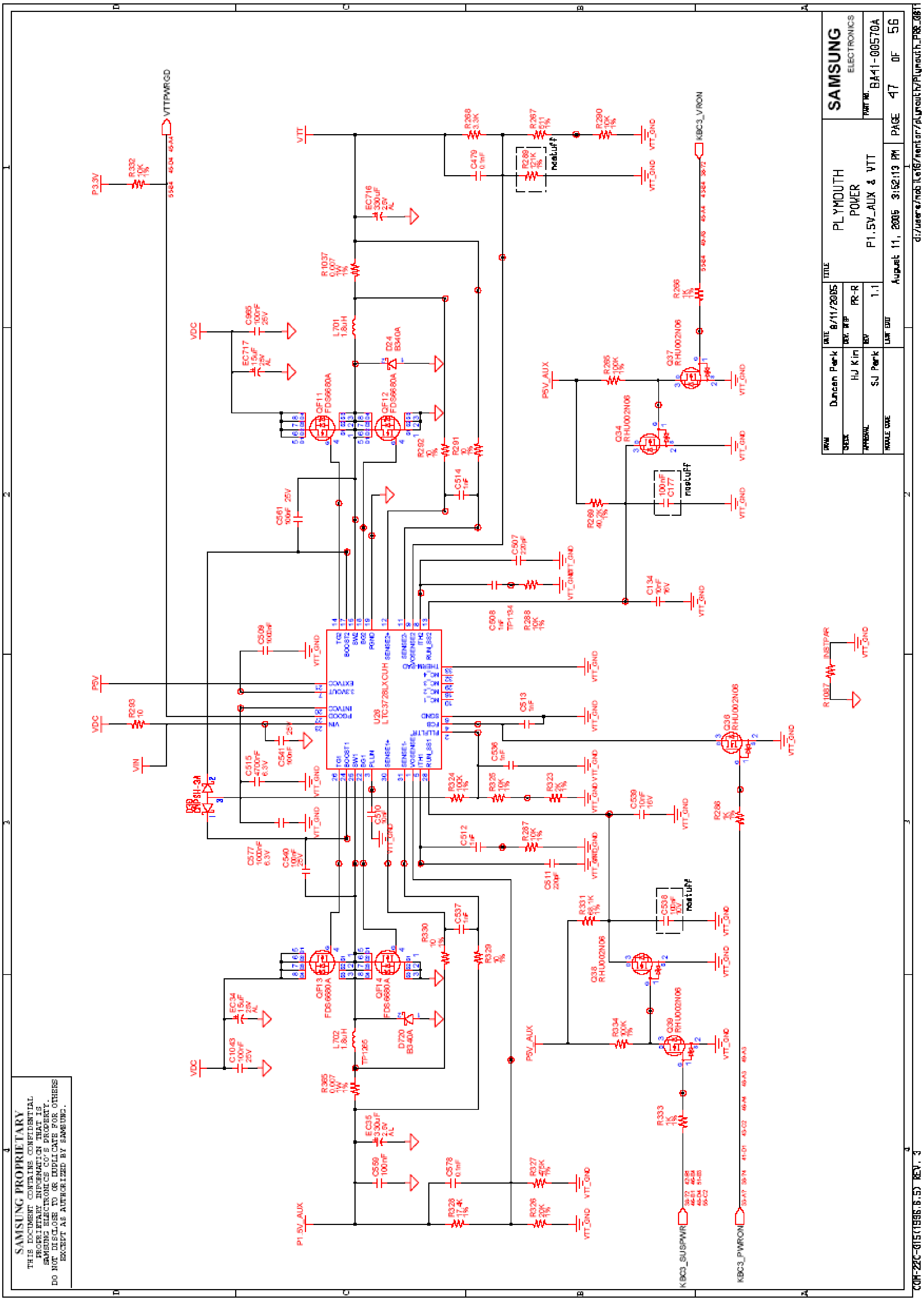
ELECTRONICS
PLYMOUTH
POWER
P3.3V_AUX & P5V_AUX
BA41-00570A
PAGE 46 OF 56
August 11, 2005 3:52:13 PM
d:/users/mobile6/mentor/plymouth/Plymouth.PRJ

7. 회로도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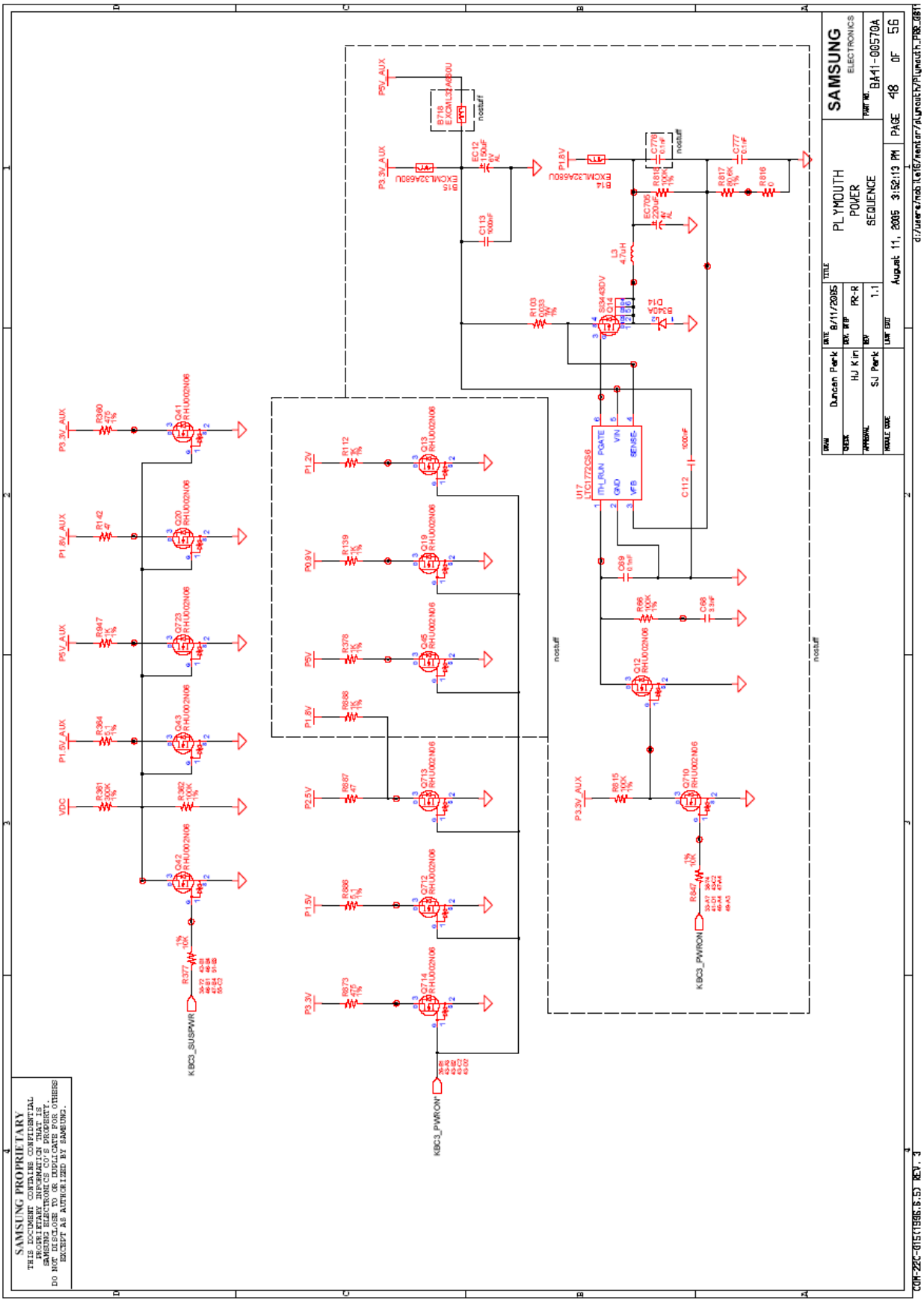
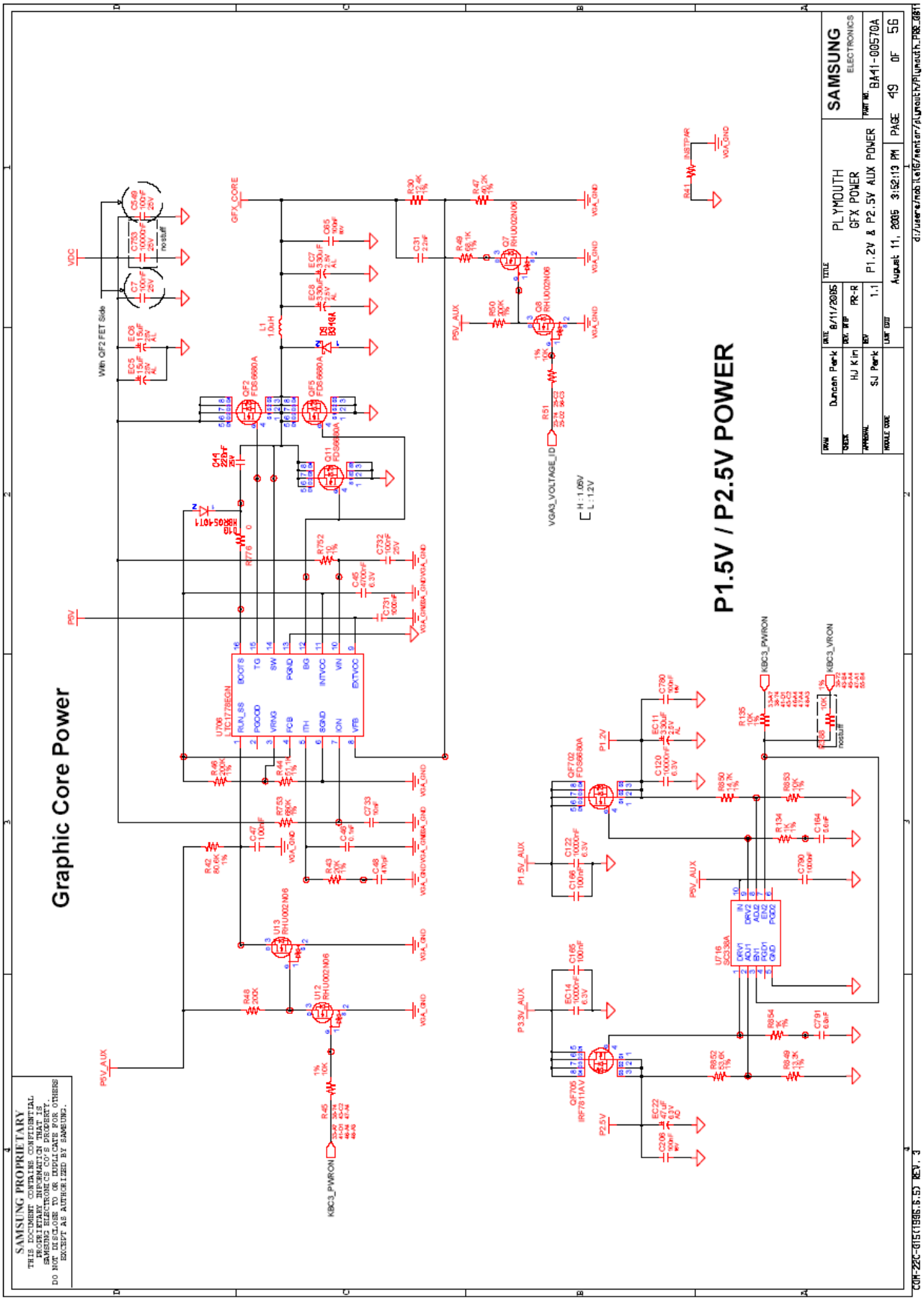
SAMSUNG ELECTRONICS
PLYMOUTH
POWER
P1.5V_AUX & VTT
BA41-00570A
PAGE 47 OF 56
Duncan Park
HJ Kim
SJ Park
8/11/2005
PR-R
1.1
August 11, 2005 3:52:13 PM
U26
LTC3728LXCUH
VTT
VDC
P5V
VIN
P3.3V
VTTPWRGD
P5V_AUX
P1.5V_AUX
KBC3_VRON
KBC3_SUSPWR
KBC3_PWRON
VTT_GND

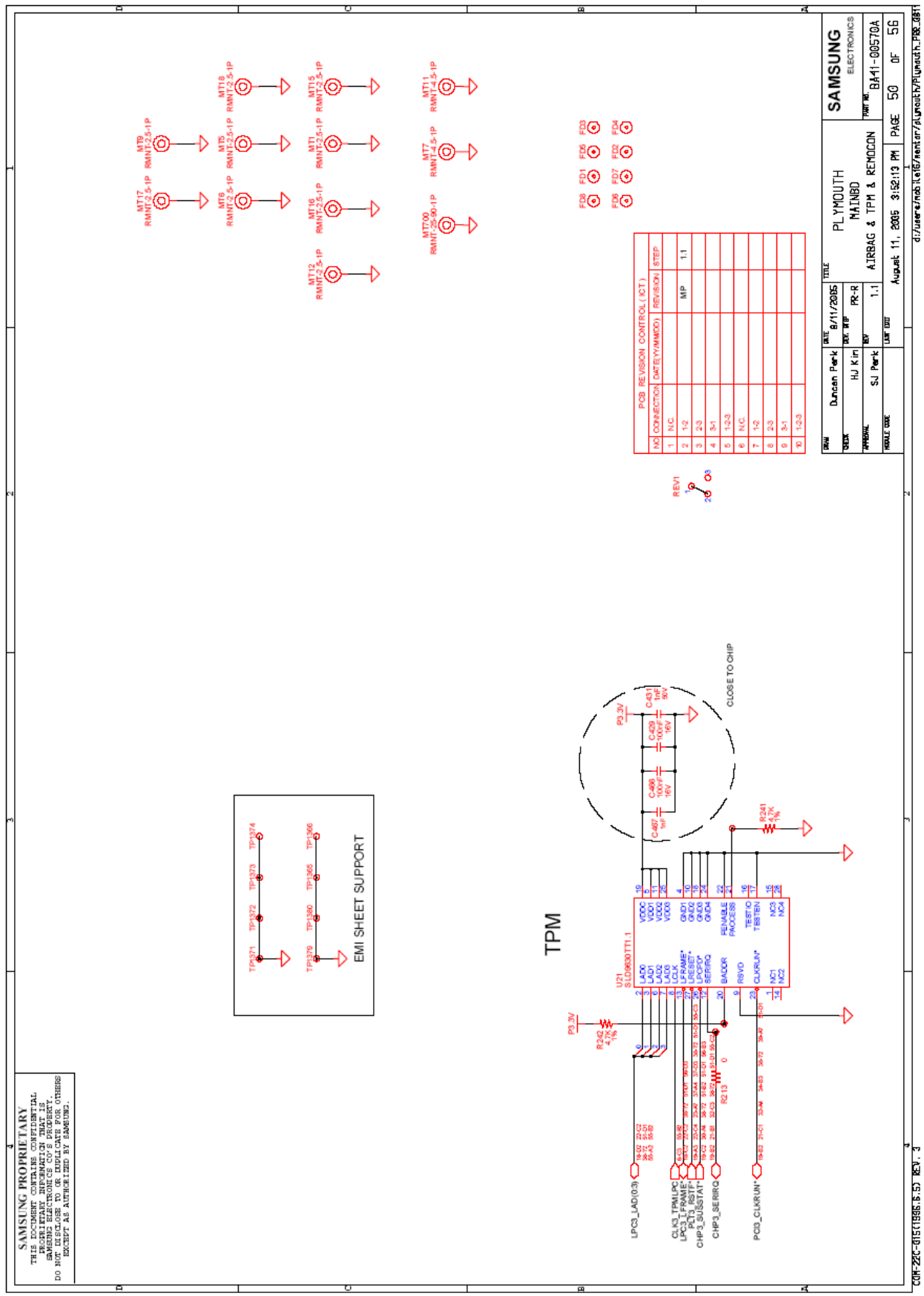
7. 회로도


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
POWER
SEQUENCE
BA41-00570A
PAGE 48 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
PR-R
1.1
U17
LTC1772CS6
Q41
Q20
Q723
Q43
Q42
Q13
Q19
Q45
Q712
Q714
Q710
Q12
RHU002N06
KBC3_SUSPWR
KBC3_PWRON
KBC3_PWRON

7. 회로도


Graphic Core Power
P1.5V / P2.5V POWER
SAMSUNG PROPRIETARY
SAMSUNG
PLYMOUTH
GFX POWER
P1.2V & P2.5V AUX POWER
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 49 OF 56

7. 회로도


SAMSUNG PROPRIETARY
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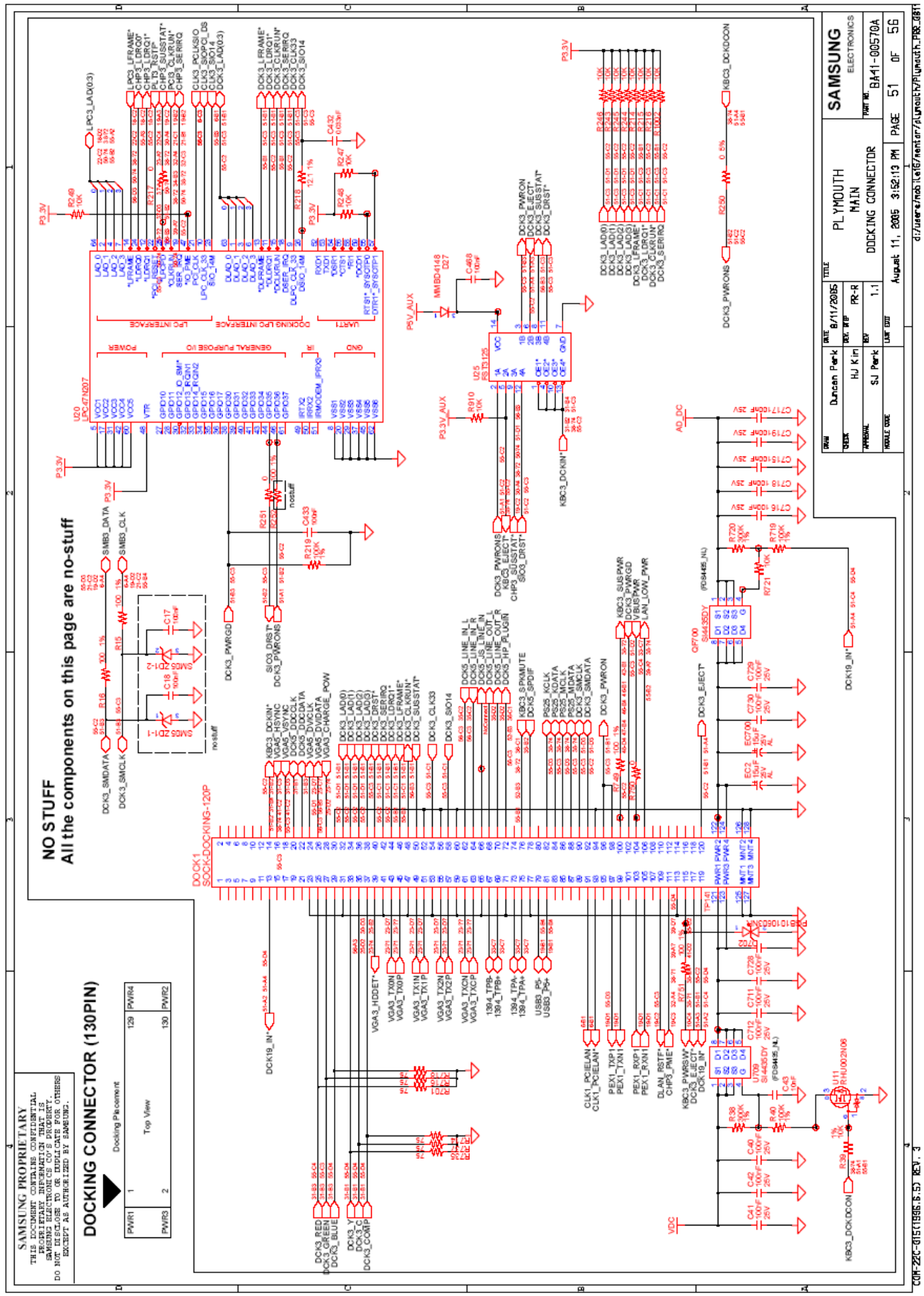
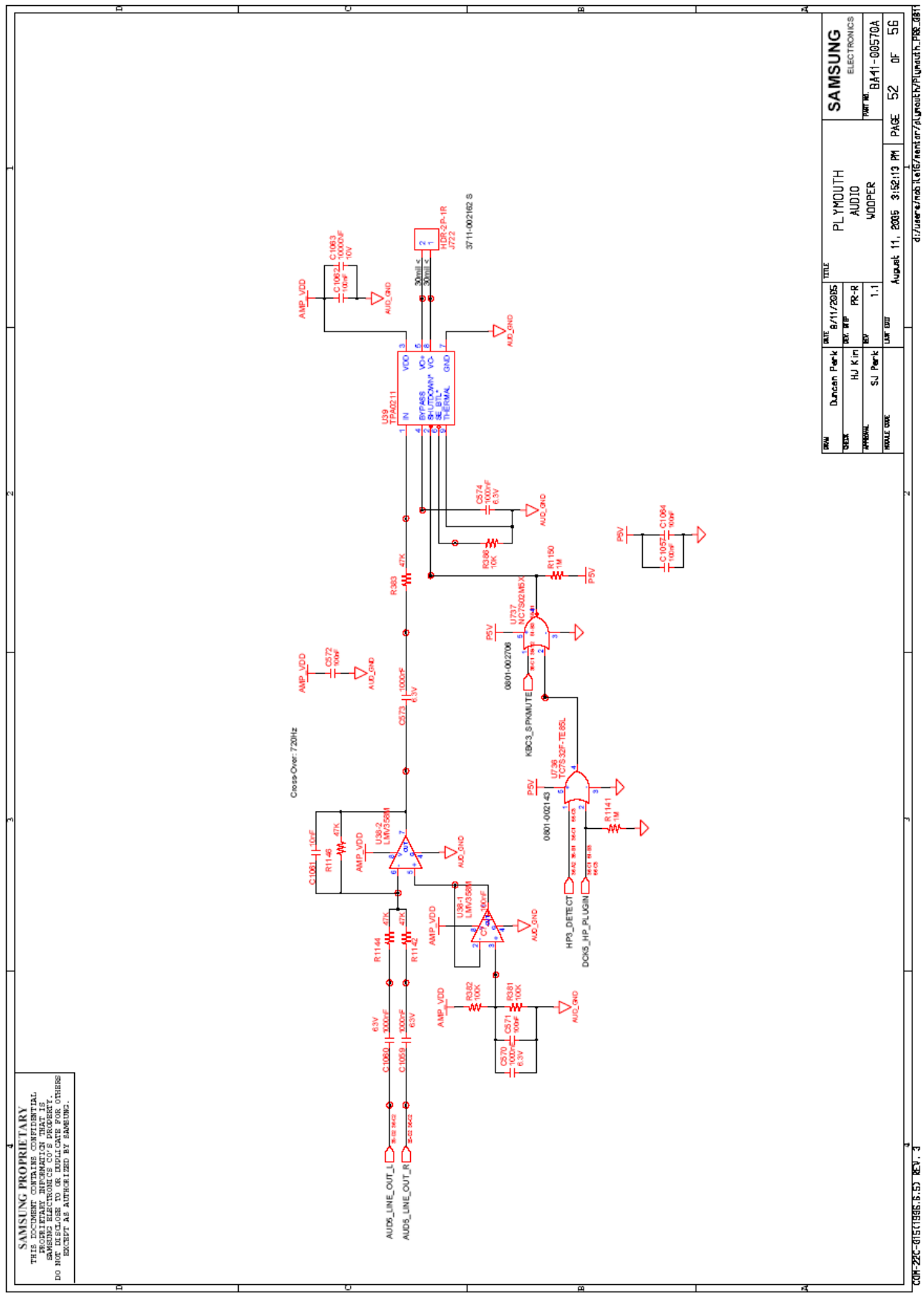
EMI SHEET SUPPORT
TPM
CLOSE TO CHIP
PLYMOUTH
MAINBD
AIRBAG & TPM & REMOCON
SAMSUNG
ELECTRONICS
BA41-00570A
PAGE 50 OF 56
August 11, 2005 3:52:13 PM
d:/users/mobile6/mentor/plymouth/Plymouth.PRJ

7. 회로도


NO STUFF
All the components on this page are no-stuff
DOCKING CONNECTOR (130PIN)
SAMSUNG PROPRIETARY
SAMSUNG
PLYMOUTH
MAIN
DOCKING CONNECTOR
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 51 OF 56

7. 회로도


SAMSUNG PROPRIETARY
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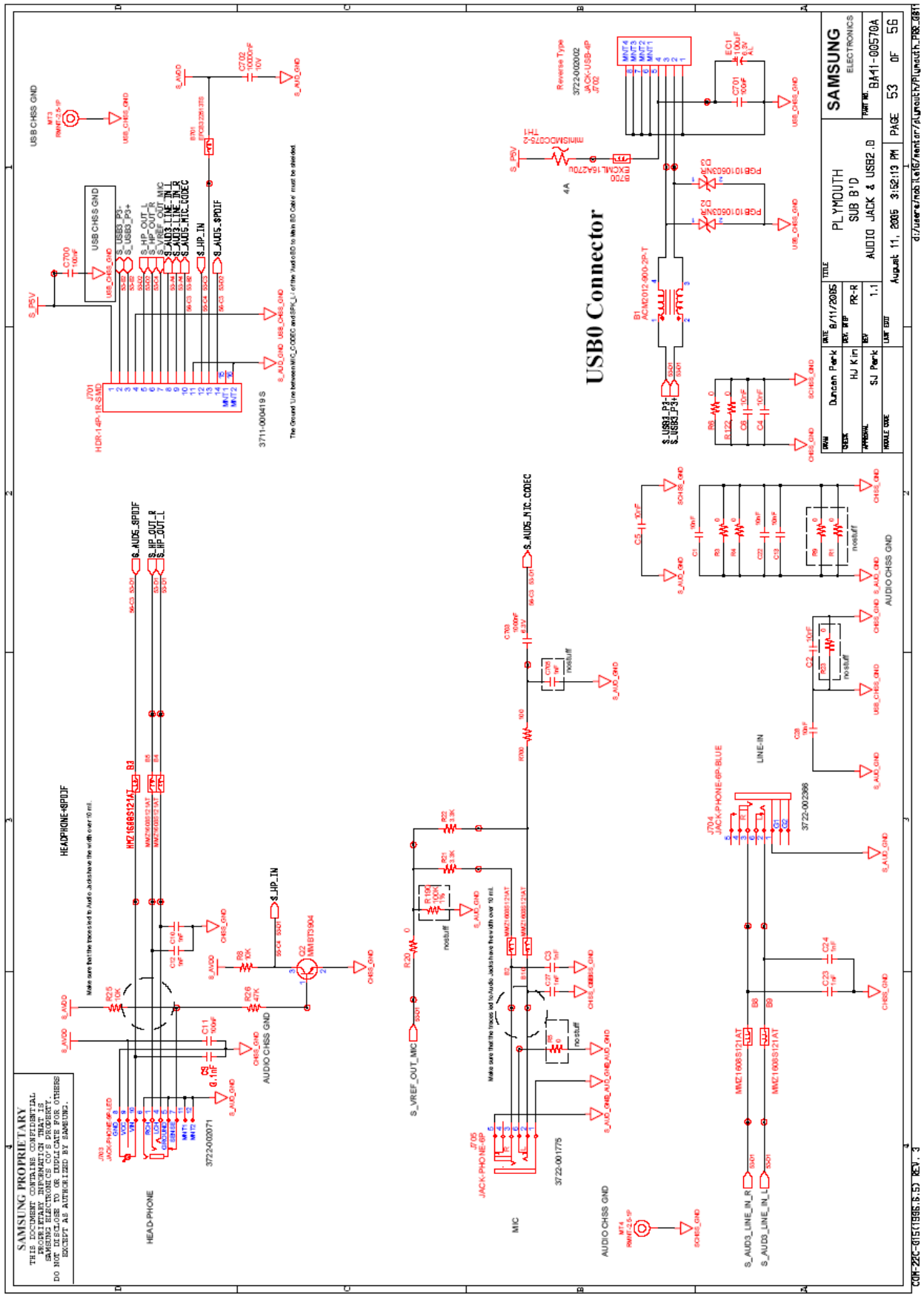
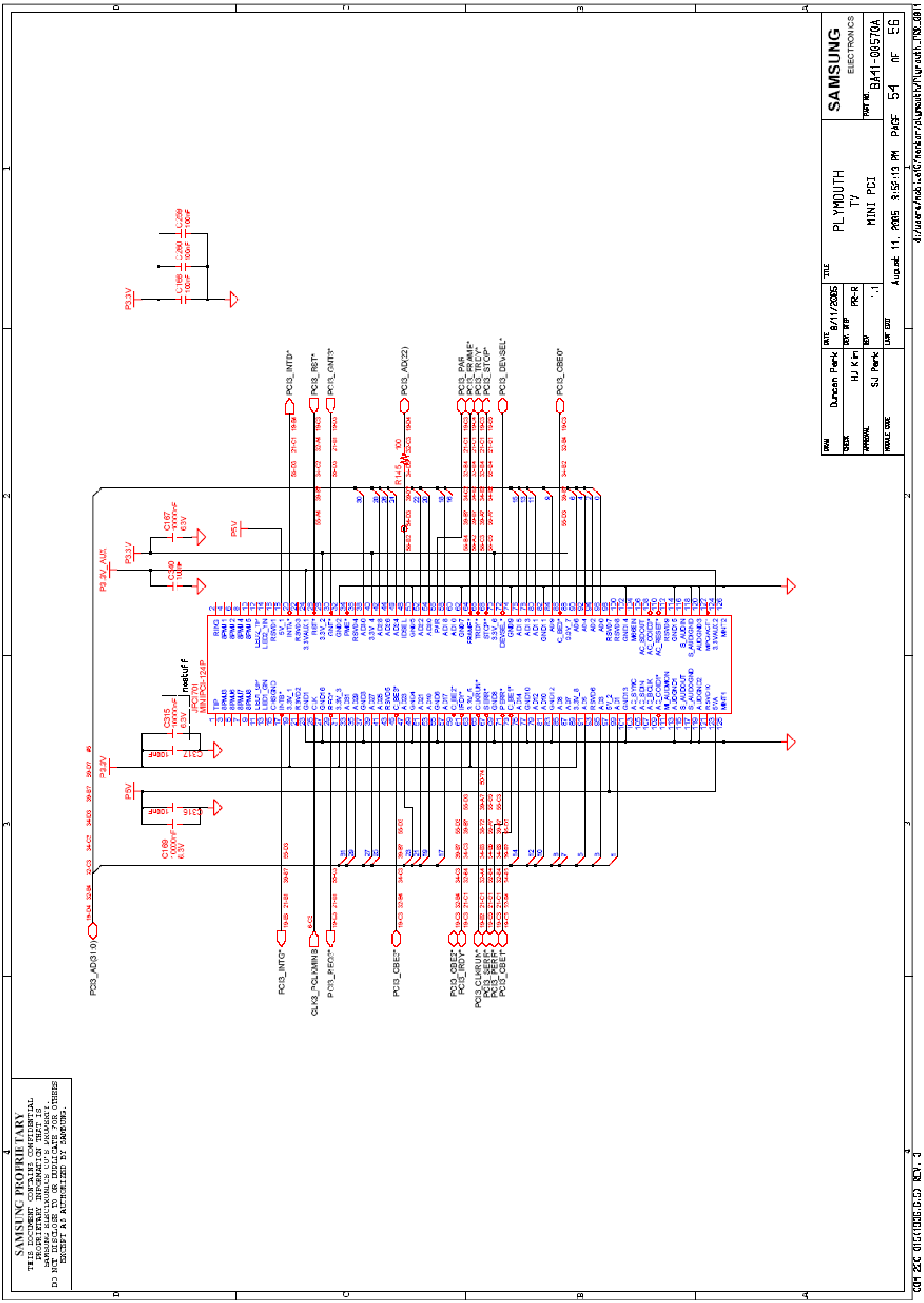
SAMSUNG ELECTRONICS
PLYMOUTH
AUDIO
WOOPER
BA41-00570A
PAGE 52 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
PR-R
1.1
Cross-Over: 720Hz
AUDS_LINE_OUT_L
AUDS_LINE_OUT_R
HP3_DETECT
DOKS_HP_PLUGIN
KBC3_SPKMUTE
AMP_VDD
AUD_GND
P5V

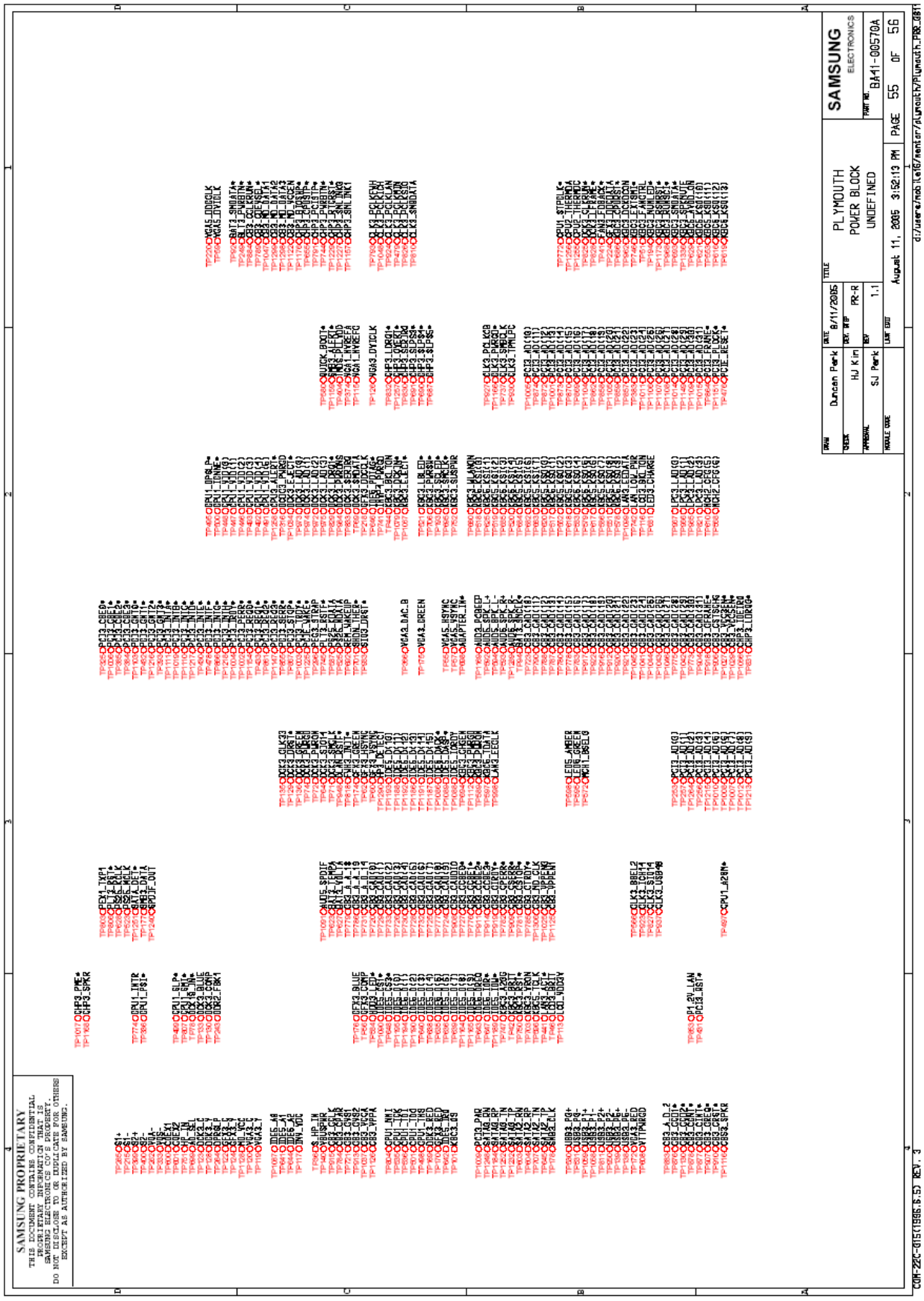
7. 회로도


USB0 Connector
SAMSUNG PROPRIETARY
SAMSUNG ELECTRONICS
PLYMOUTH
SUB B'D
AUDIO JACK & USB2.0
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 53 OF 56
HEADPHONE-6PDIF
HEAD-PHONE
MIC
LINE-IN
AUDIO CHSS GND
USB CHSS GND

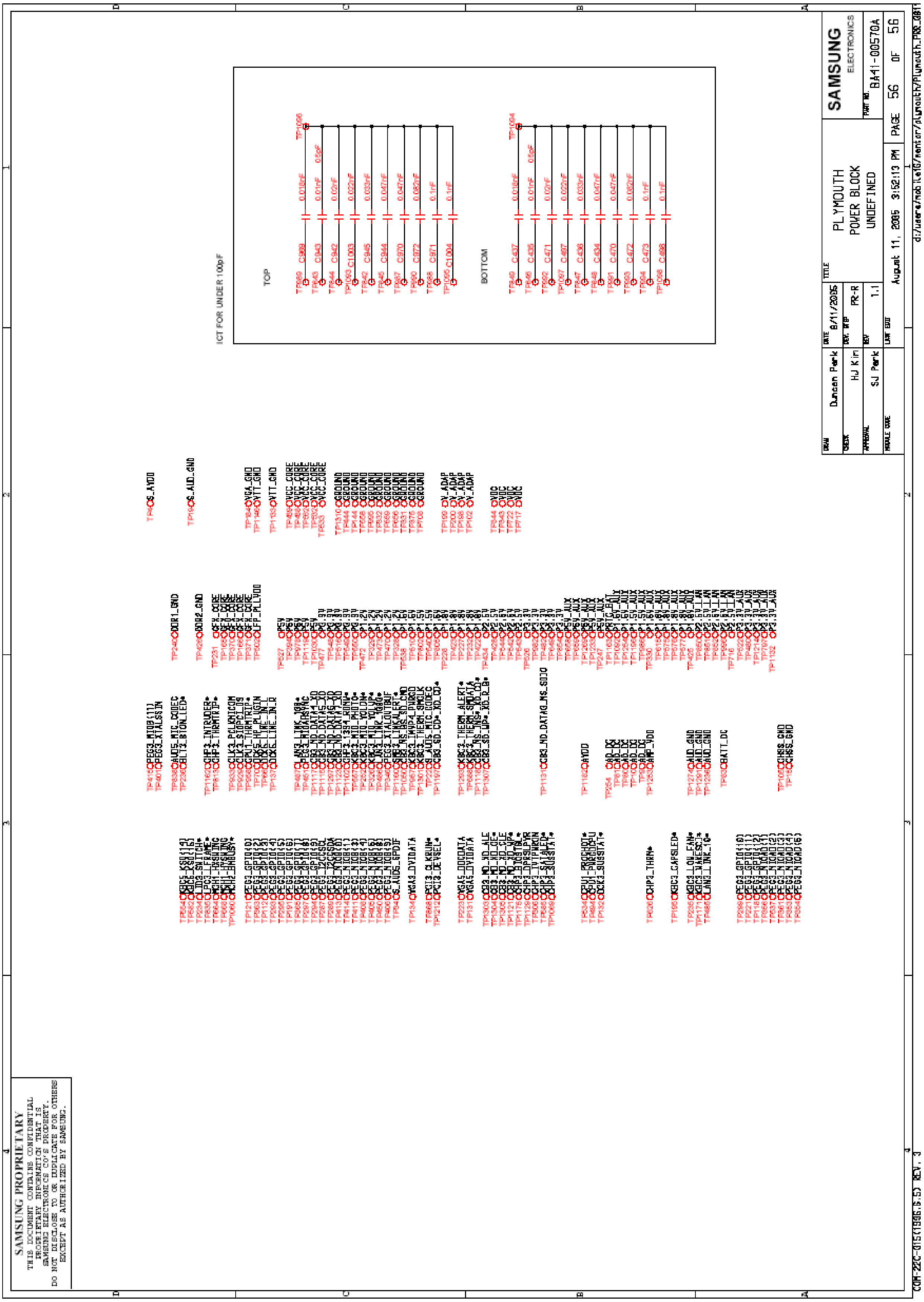
7. 회로도


SAMSUNG
ELECTRONICS
PLYMOUTH
TV
MINI PCI
BA41-00570A
PAGE 54 OF 56
SAMSUNG PROPRIETARY

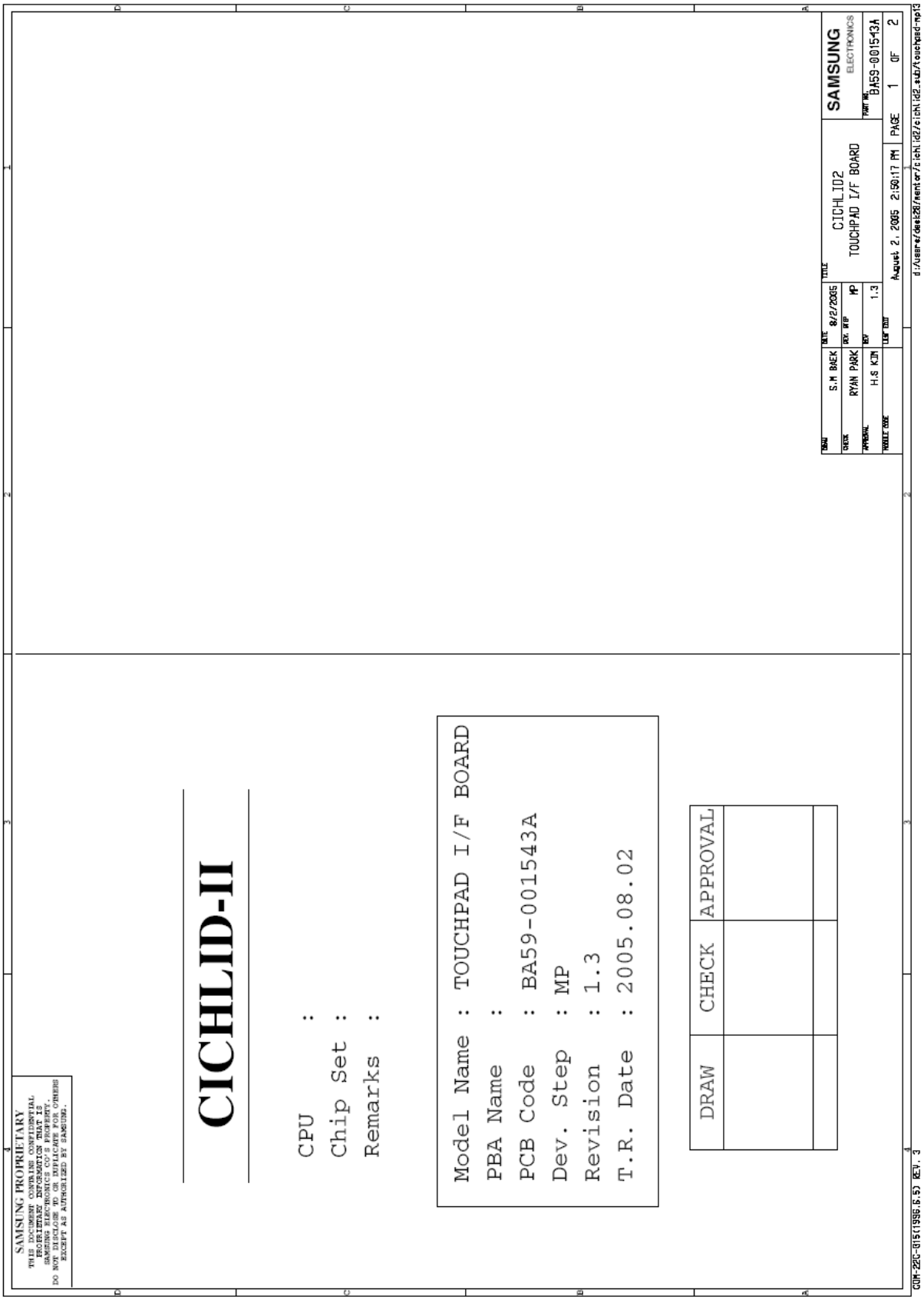
7. 회로도



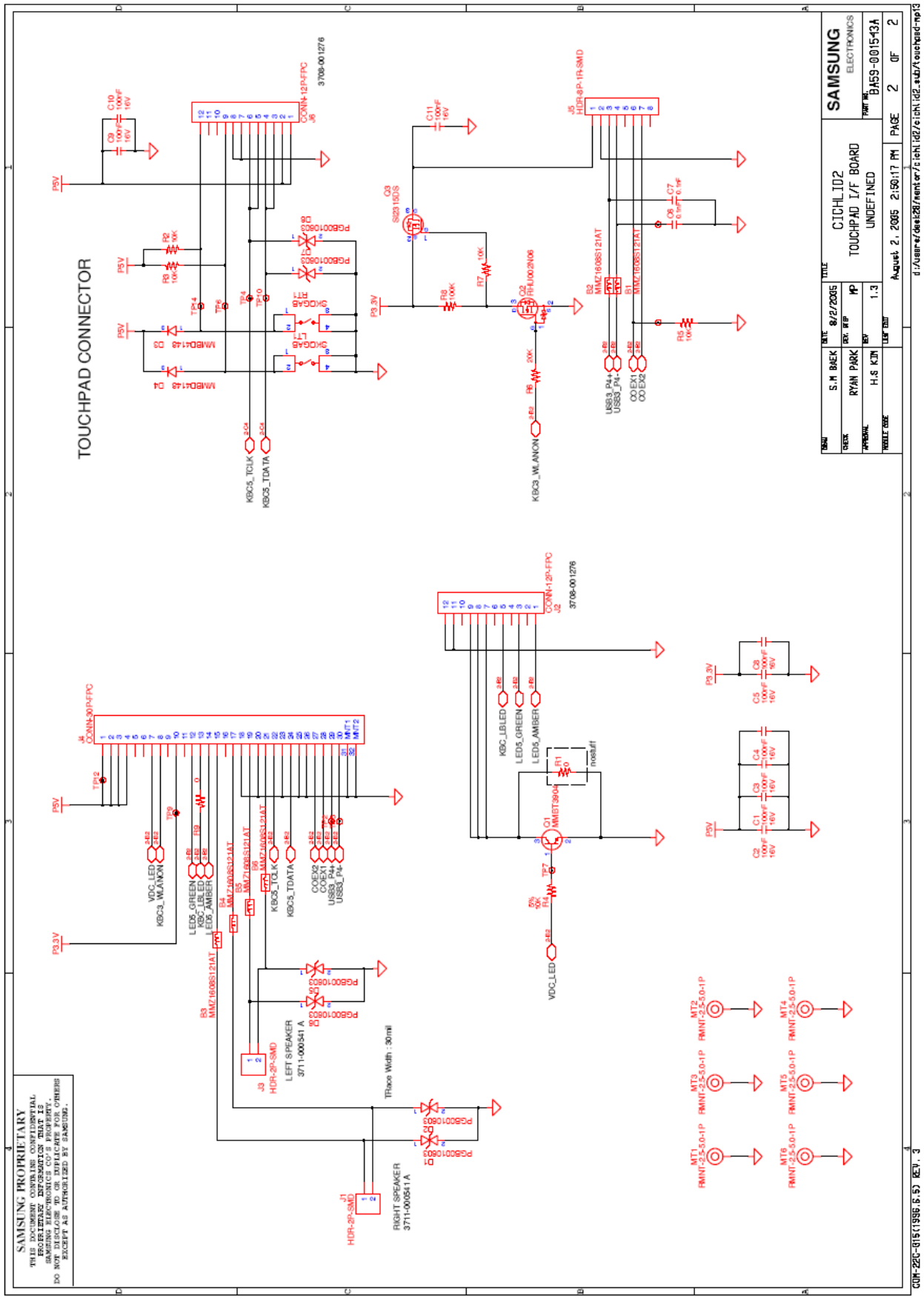
7. 회로도


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
POWER BLOCK
UNDEFINED
BA41-00570A
ICT FOR UNDER 100pF
TOP
BOTTOM

2) Touchpad I/F Board



7. 회로도


TOUCHPAD CONNECTOR
SAMSUNG
ELECTRONICS
CICHLID2
TOUCHPAD I/F BOARD
UNDEFINED
BA59-00154A
August 2, 2005 2:50:17 PM
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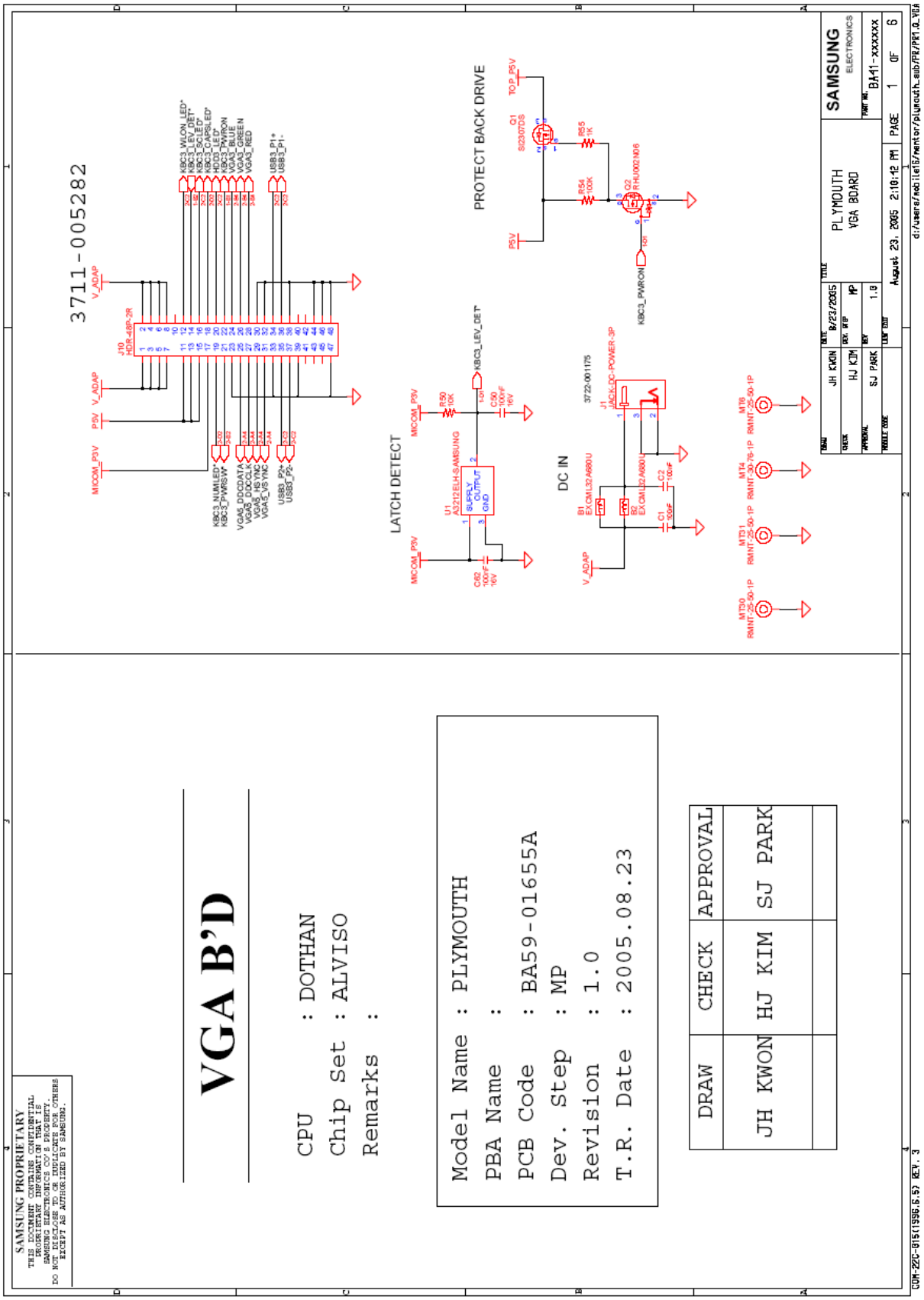
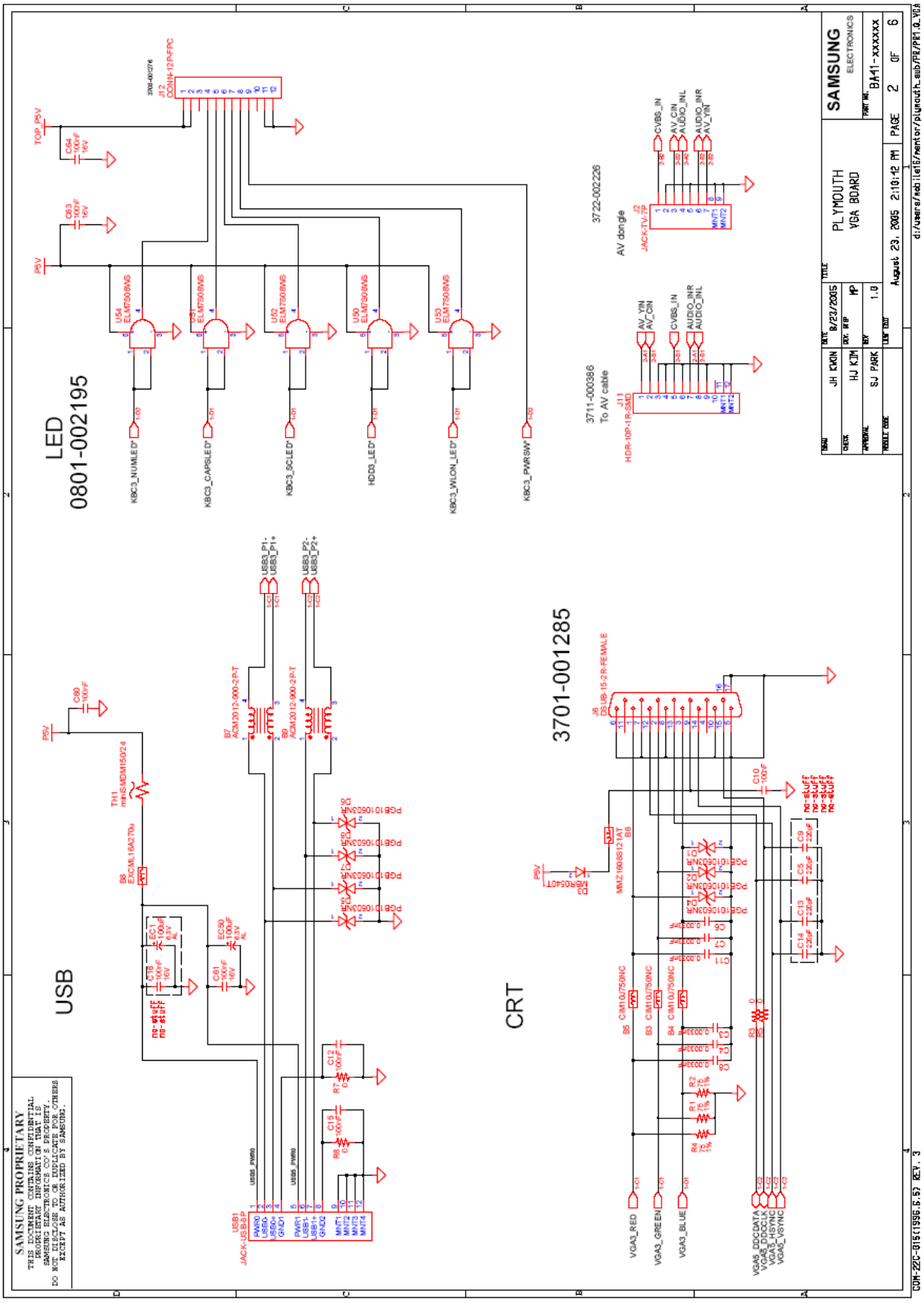
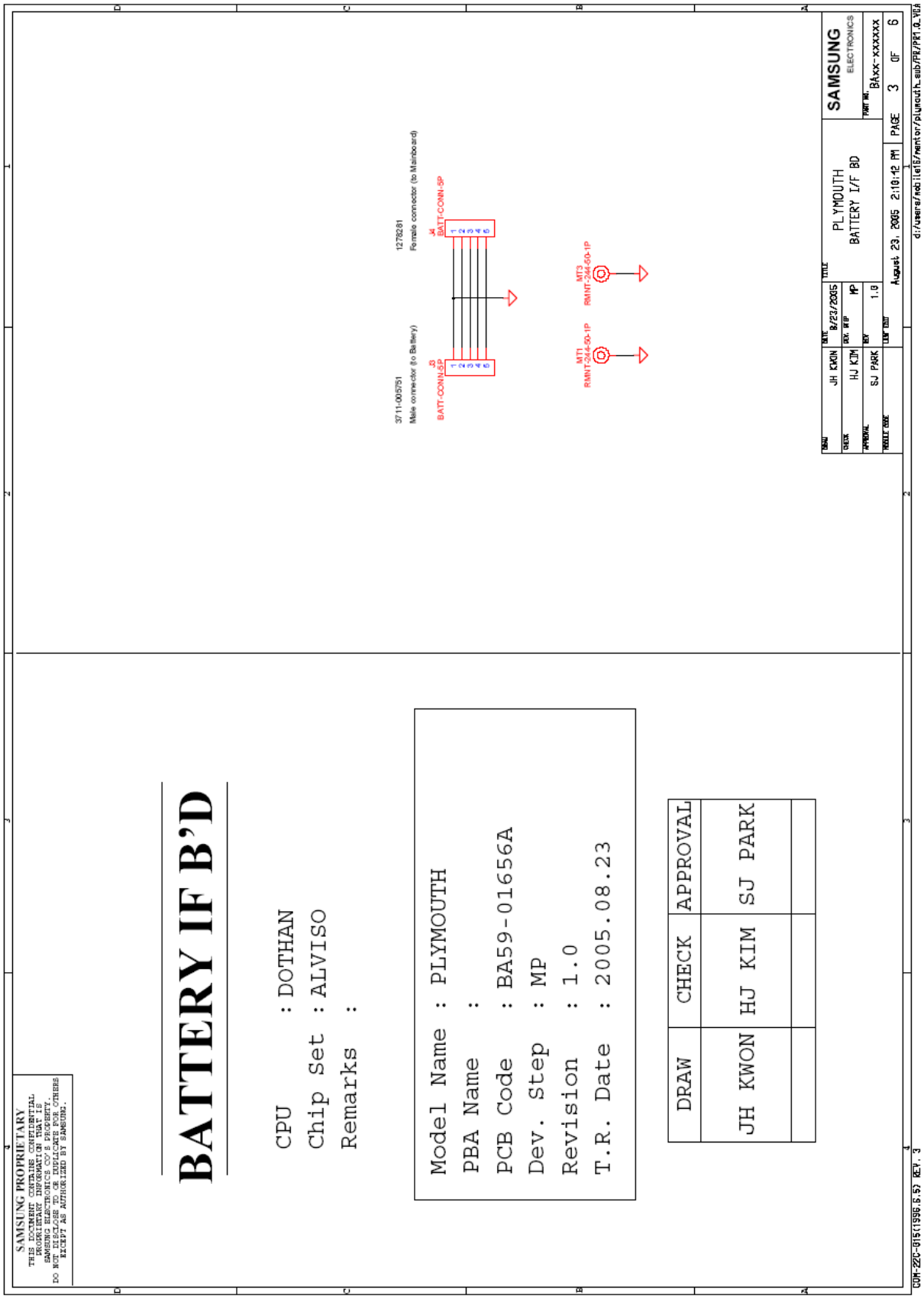
3) VGA Board


VGA B'D
CPU : DOTHAN
Chip Set : ALVISO
Remarks :
Model Name : PLYMOUTH
PBA Name :
PCB Code : BA59-01655A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2005.08.23
DRAW
CHECK
APPROVAL
JH KWON
HJ KIM
SJ PARK
3711-005282
PROTECT BACK DRIVE
LATCH DETECT
DC IN
PLYMOUTH
VGA BOARD
SAMSUNG
ELECTRONICS
BA41-XXXXXX
August 23, 2005 2:10:42 PM
SAMSUNG PROPRIETARY

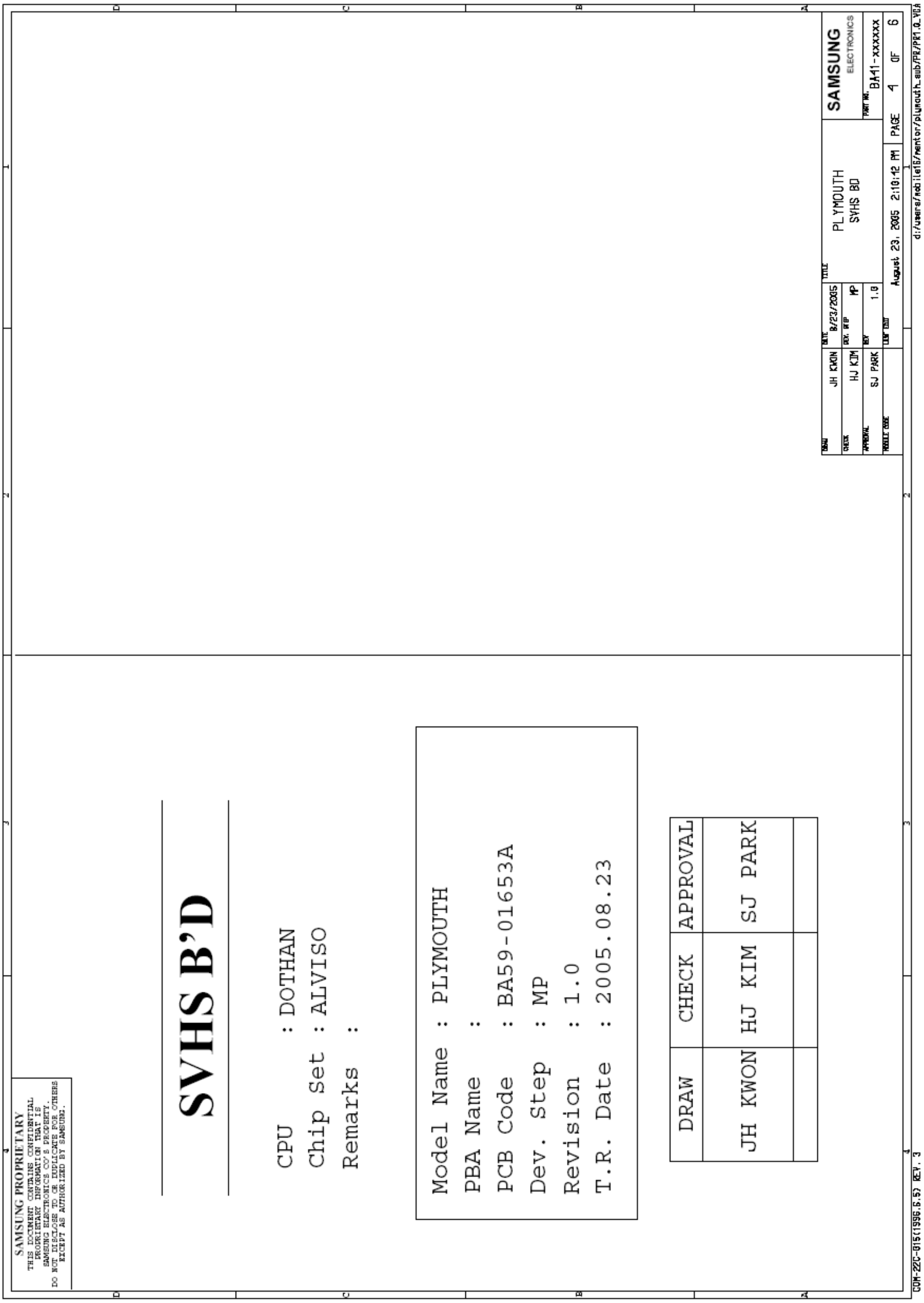
7. 회로도


LED
0801-002195
USB
CRT
3701-001285
PLYMOUTH
VGA BOARD
SAMSUNG
ELECTRONICS
SAMSUNG PROPRIETARY
August 23, 2005 2:10:12 PM
PAGE 2 OF 6

4) Battery I/F Board



5) SVHS Board


SVHS B'D
CPU : DOTHAN
Chip Set : ALVISO
Remarks :
Model Name : PLYMOUTH
PBA Name :
PCB Code : BA59-01653A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2005.08.23
DRAW
CHECK
APPROVAL
JH KWON
HJ KIM
SJ PARK
SAMSUNG PROPRIETARY
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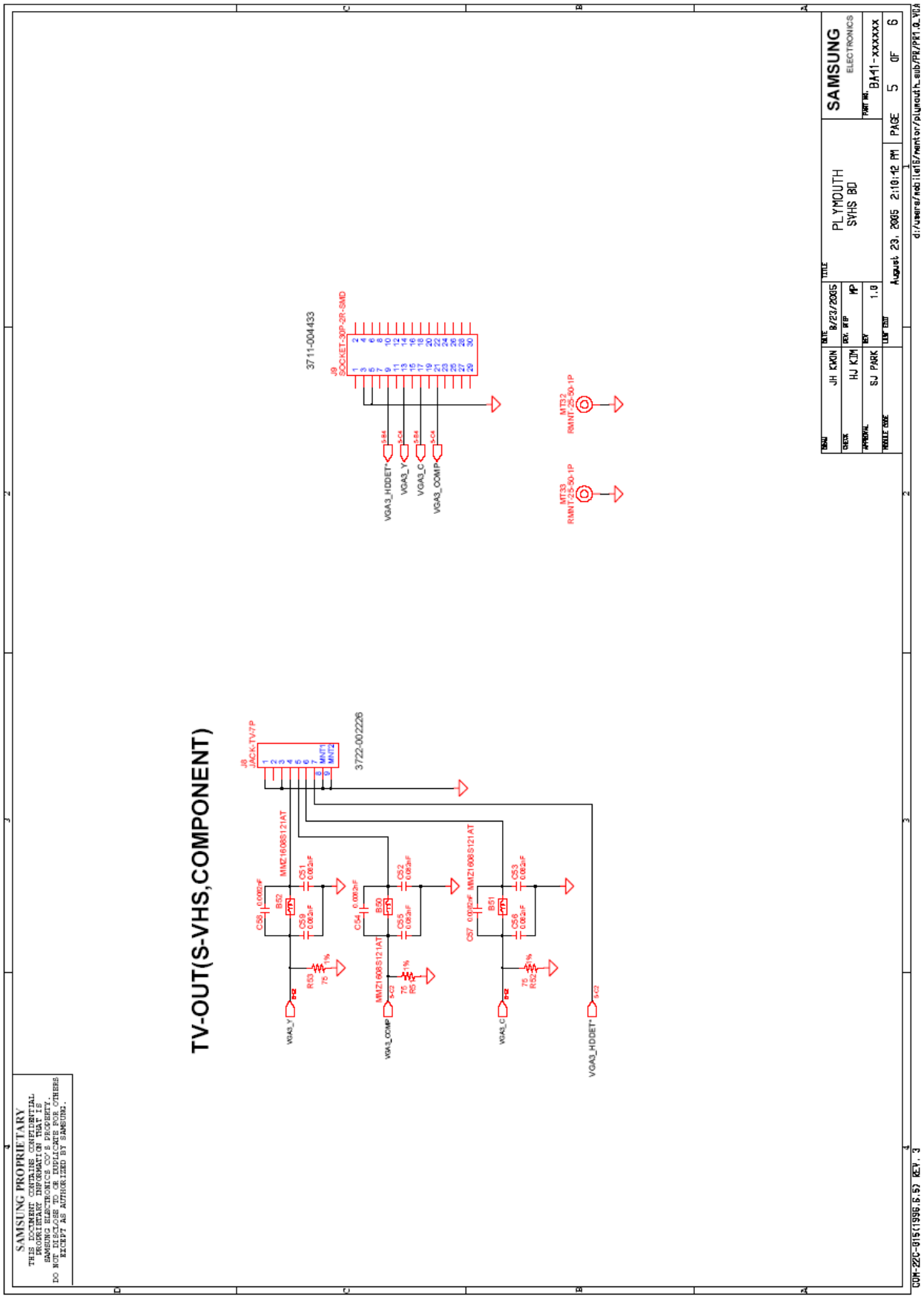
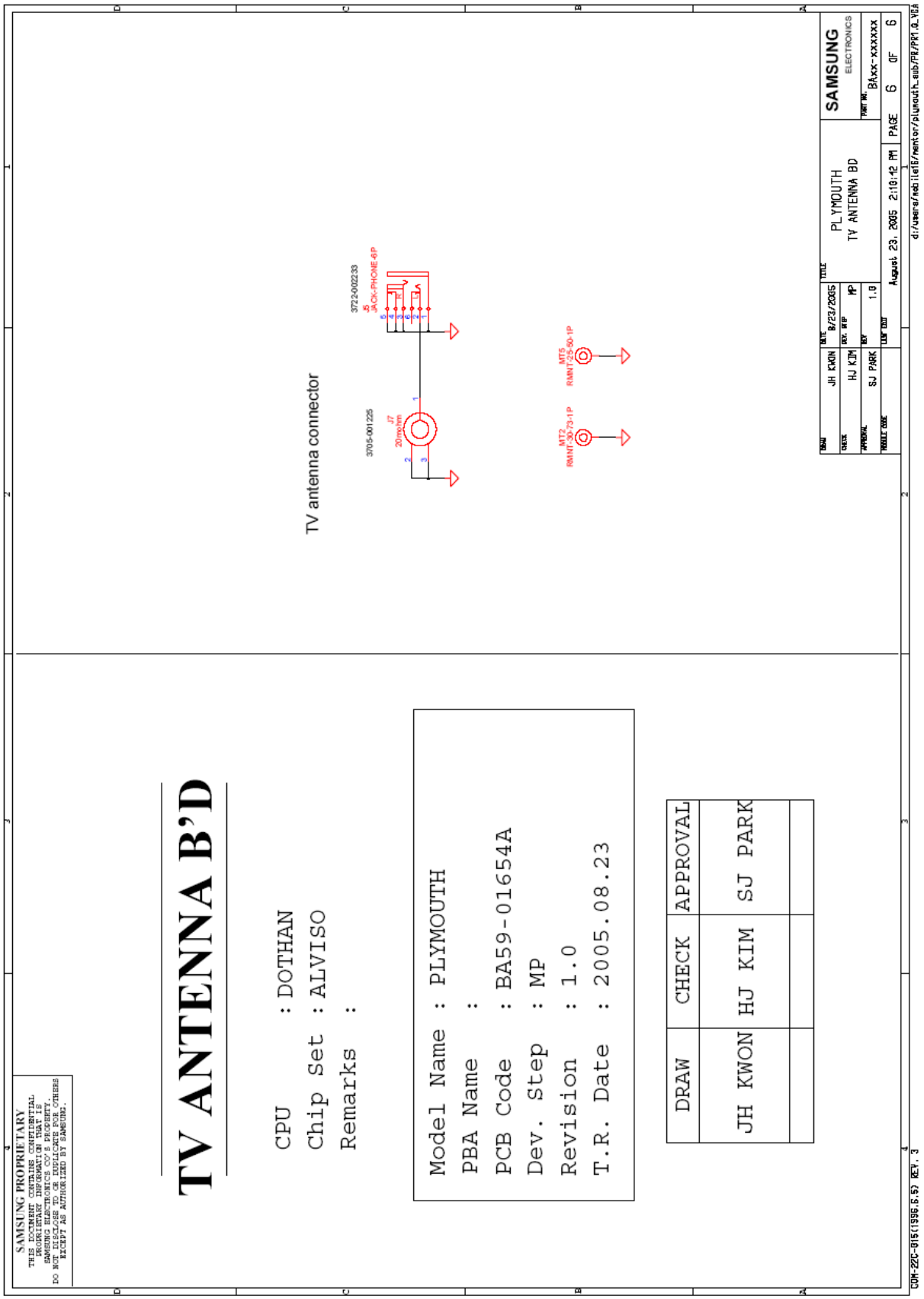
DRAW JH KWON
DATE 8/23/2005
CHECK HJ KIM
DEV. STEP MP
APPROVAL SJ PARK
REV 1.0
TITLE
PLYMOUTH
SVHS BD
SAMSUNG
ELECTRONICS
PART NO. BA41-xxxxxx
August 23, 2005 2:10:12 PM
PAGE 4 OF 6
COM-22C-015(1996.6.5) REV. 3

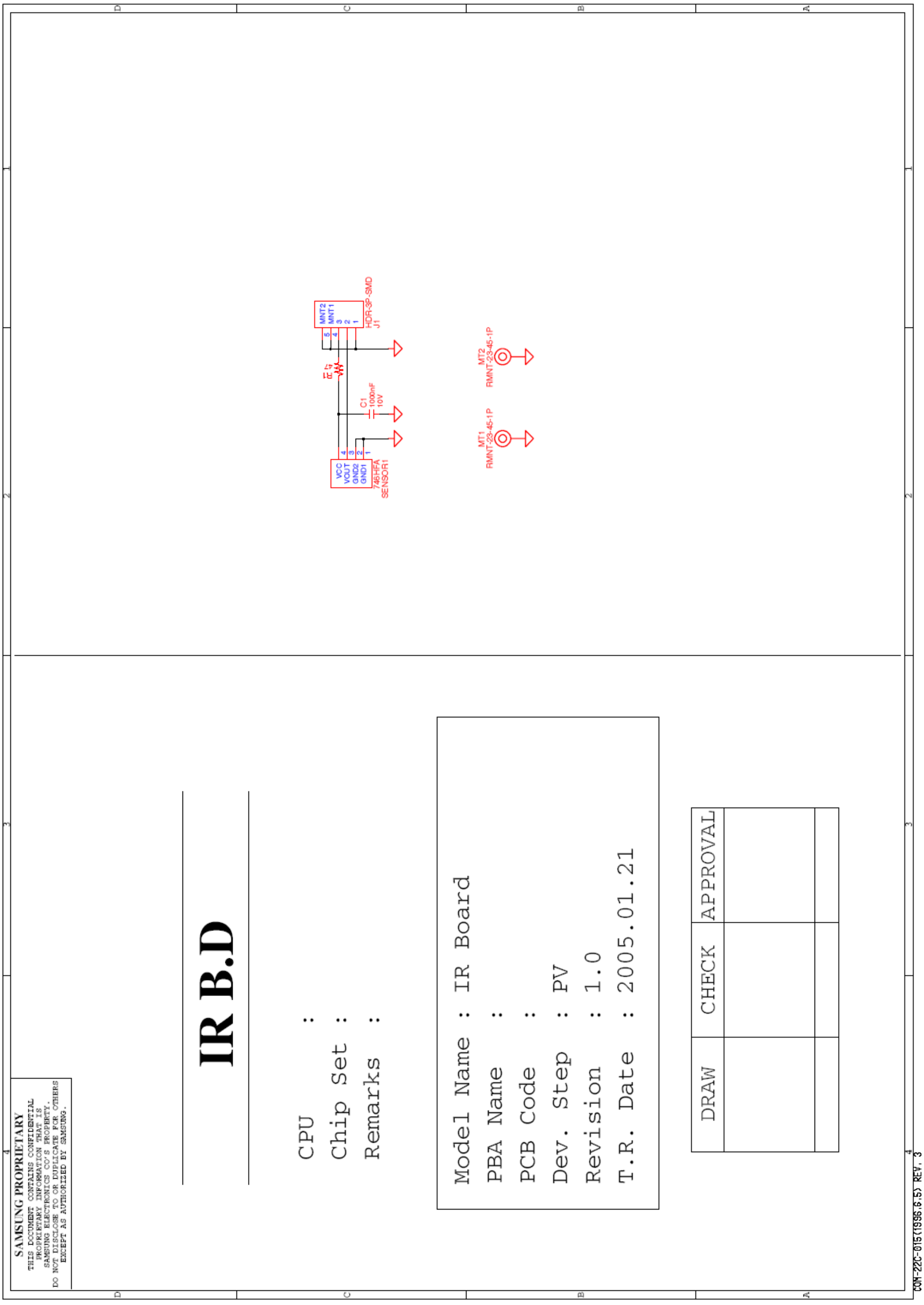
7. 회로도


TV-OUT(S-VHS,COMPONENT)
SAMSUNG PROPRIETARY
SAMSUNG
PLYMOUTH
SVHS BD
JH KWON
HJ KIM
SJ PARK
August 23, 2005 2:10:42 PM
PAGE 5 OF 6
BA41-xxxxxx
VGA3_HDDET
VGA3_Y
VGA3_C
VGA3_COMP

6) TV Antenna Board



7) IR Board


HDR-3P-SMD
J1
MNT2
MNT1
C1
1000nF
10V
746HFA
SENSOR1
VCC
VOUT
GND2
GND1
MT1
RMNT-23-45-1P
MT2
RMNT-23-45-1P
SAMSUNG PROPRIETARY
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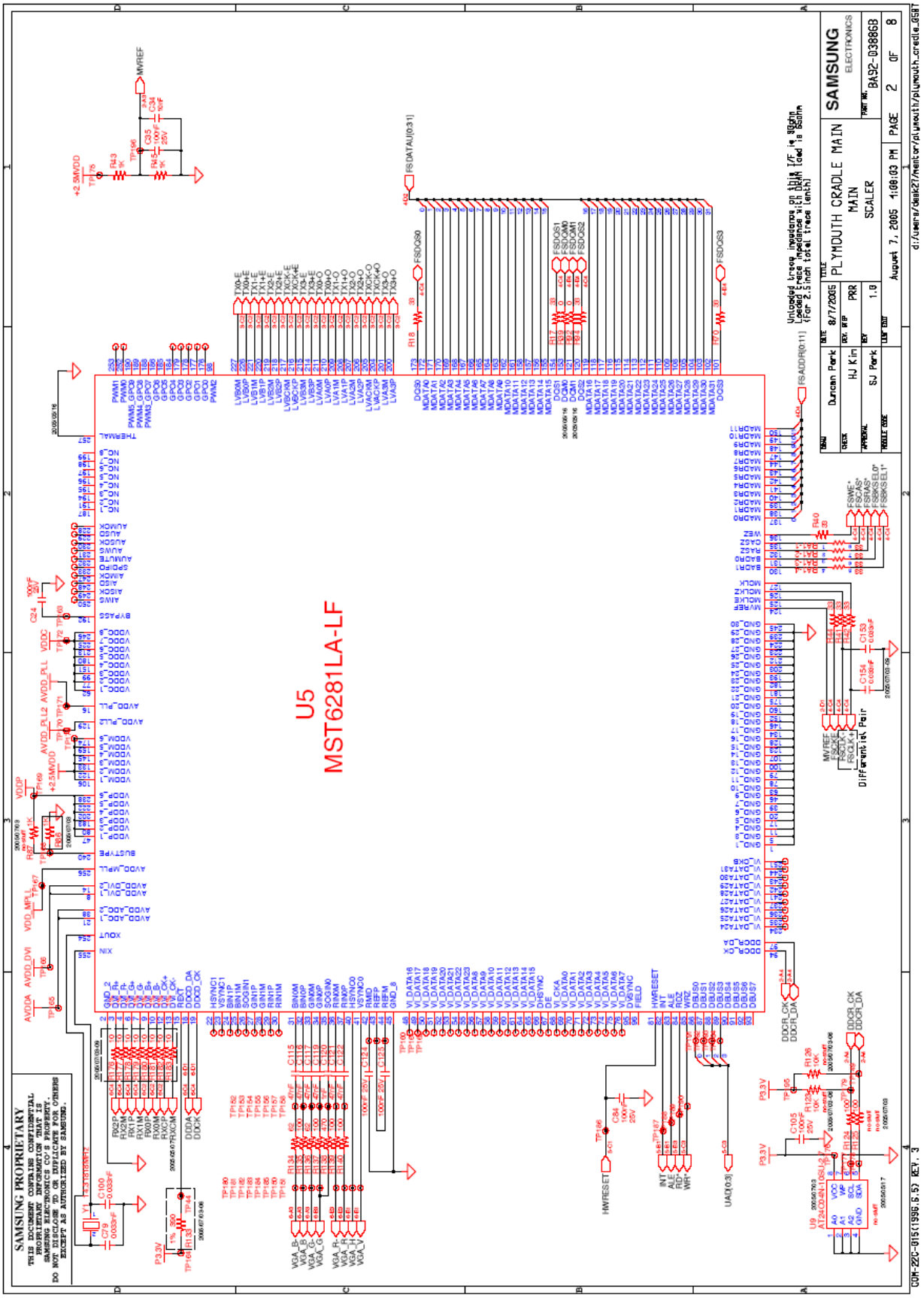
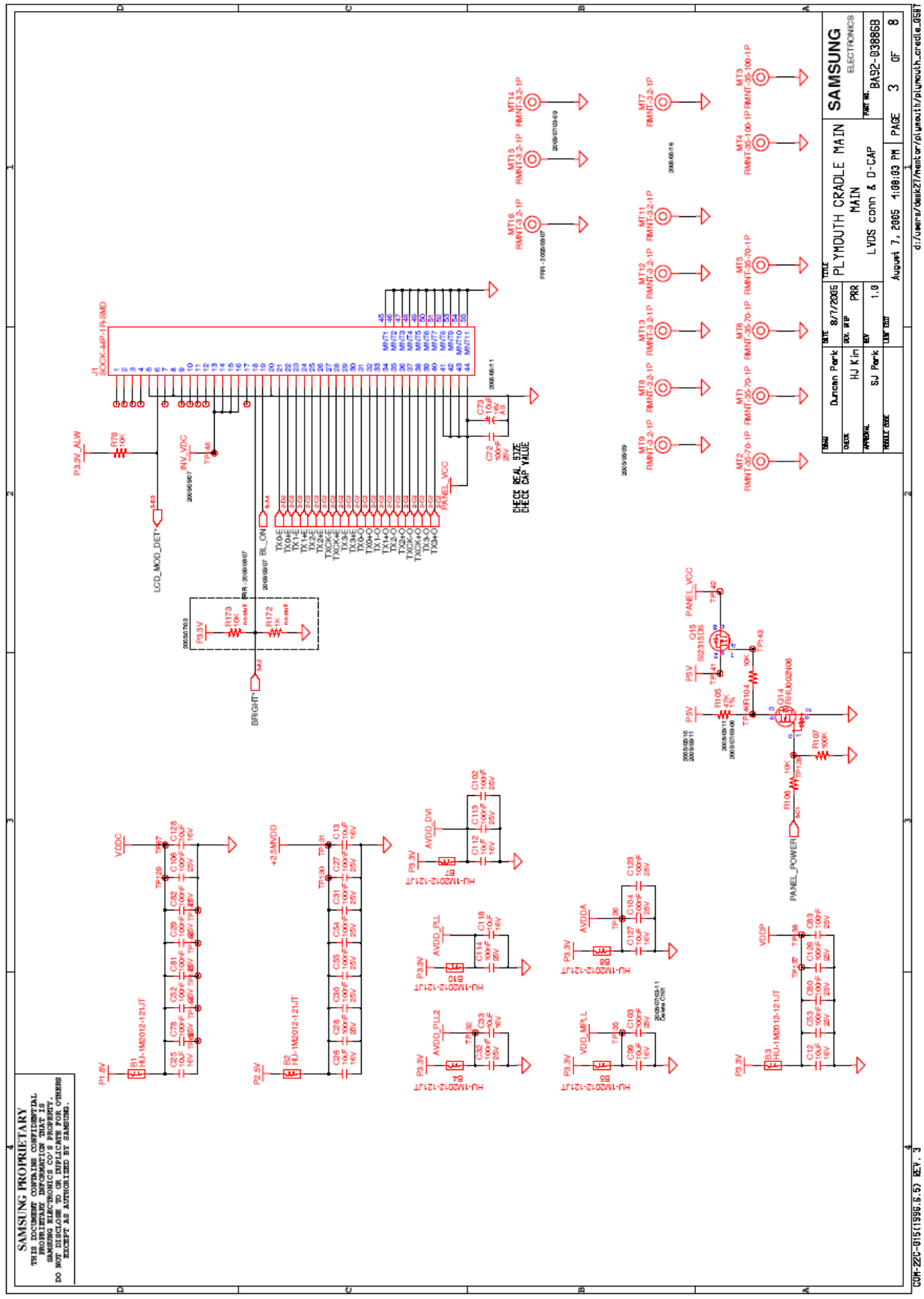
IR B.D
CPU :
Chip Set :
Remarks :
Model Name : IR Board
PBA Name :
PCB Code :
Dev. Step : PV
Revision : 1.0
T.R. Date : 2005.01.21
DRAW
CHECK
APPROVAL

8) Cradle Main Board

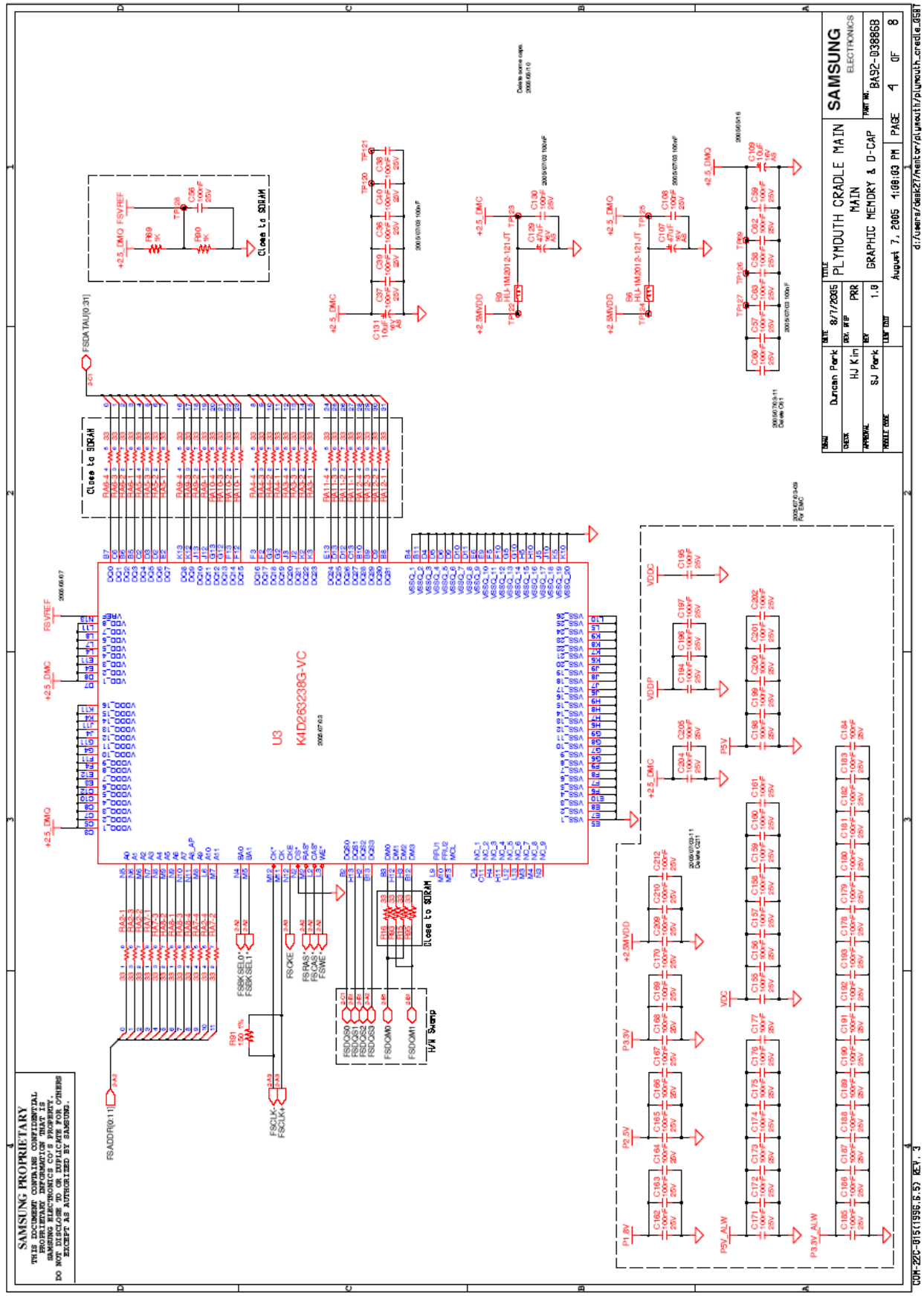
7. 회로도


U5
MST6281LA-LF
SAMSUNG PROPRIETARY
PLYMOUTH CRADLE MAIN
MAIN
SCALER
SAMSUNG
ELECTRONICS
BA92-03886B
August 7, 2005 1:08:03 PM
PAGE 2 OF 8
Duncan Park
HJ Kim
SJ Park
8/7/2005
PRR
1.0
Unloaded trace impedance on this IF is 90ohm
Loaded trace impedance with DRAM load is 50ohm
(For 2.5inch total trace length)
Differential Pair
d:/users/desk27/mentor/plymouth/plymouth_cradle.dsn

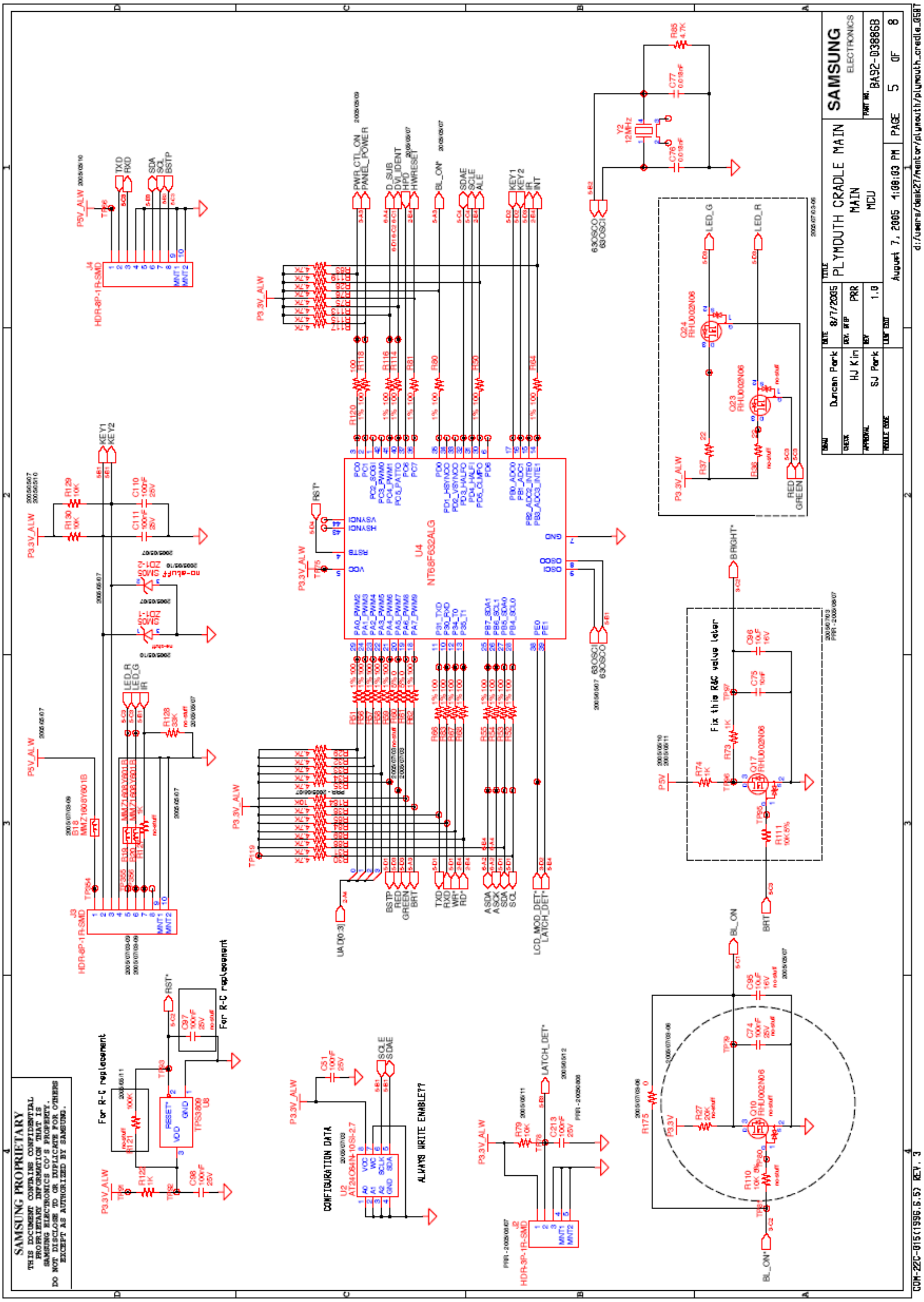
7. 회로도


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH CRADLE MAIN
MAIN
LVDS conn & D-CAP
BA32-03886B
August 7, 2005 4:08:03 PM
PAGE 3 OF 8
Duncan Park
HJ Kim
SJ Park
8/17/2005
PRR
1.0
J1
SOCK-44P-1R-SMD
LCD_MOD_DET*
INV_VDC
PANEL_VCC
BRIGHT*
BL_ON
P3.3V_ALW
P3.3V
P5V
P1.8V
P2.5V
VDDC
+2.5MVDD
AVDD_DVI
AVDD_PLL
AVDDA
VDD_MPLL
VDDP
PANEL_POWER
CHECK REAL SIZE
CHECK CAP VALUE

7. 회로도

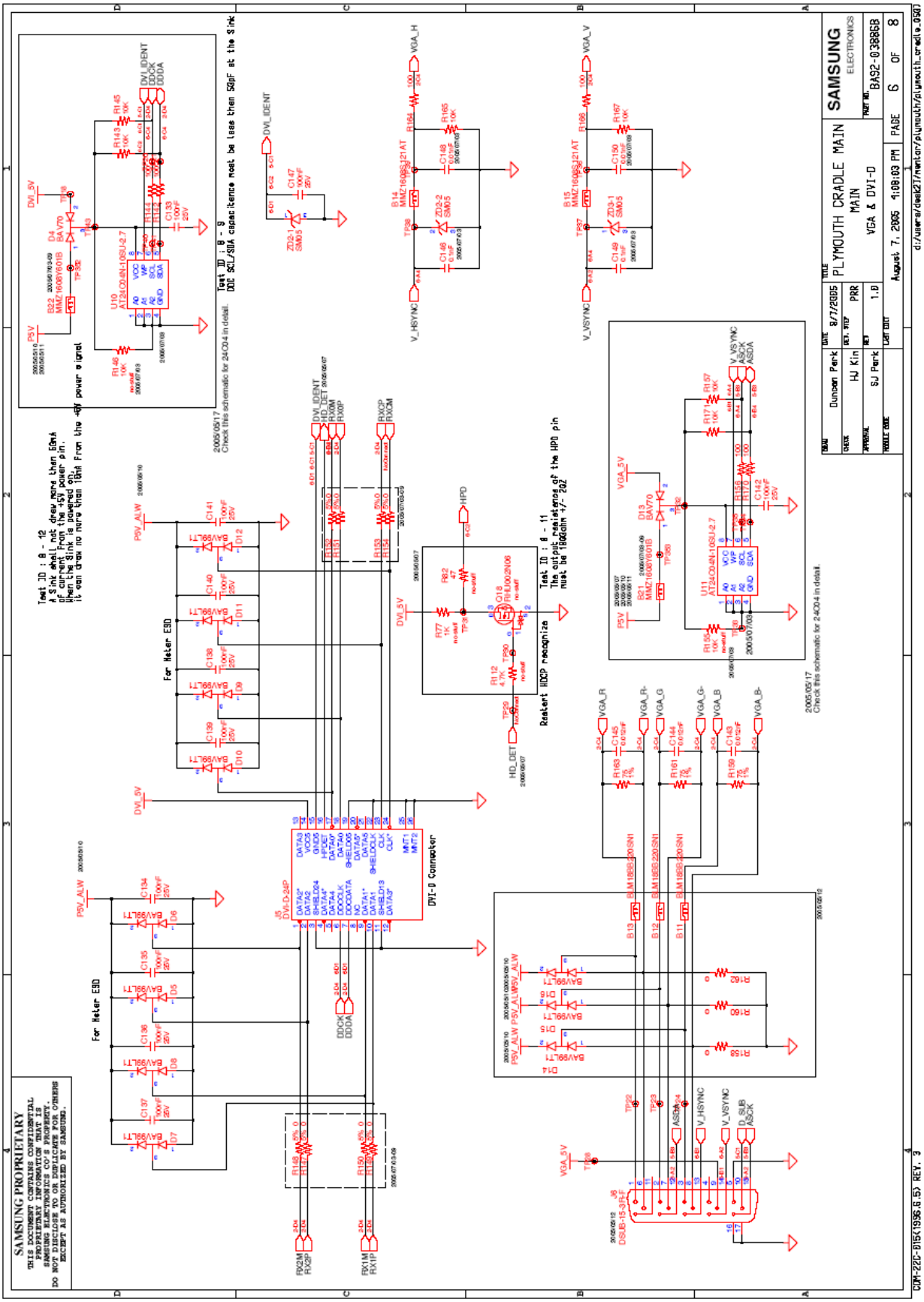

SAMSUNG PROPRIETARY
SAMSUNG ELECTRONICS
TITLE
PLYMOUTH CRADLE MAIN
MAIN
GRAPHIC MEMORY & D-CAP
PART NO
BA92-03886B
August 7, 2005 4:08:03 PM
PAGE 4 OF 8
d:/users/desk27/mentor/plymouth/plymouth_cradle.dsn
U3
K4D263238G-VC
Close to SDRAM

7. 회로도

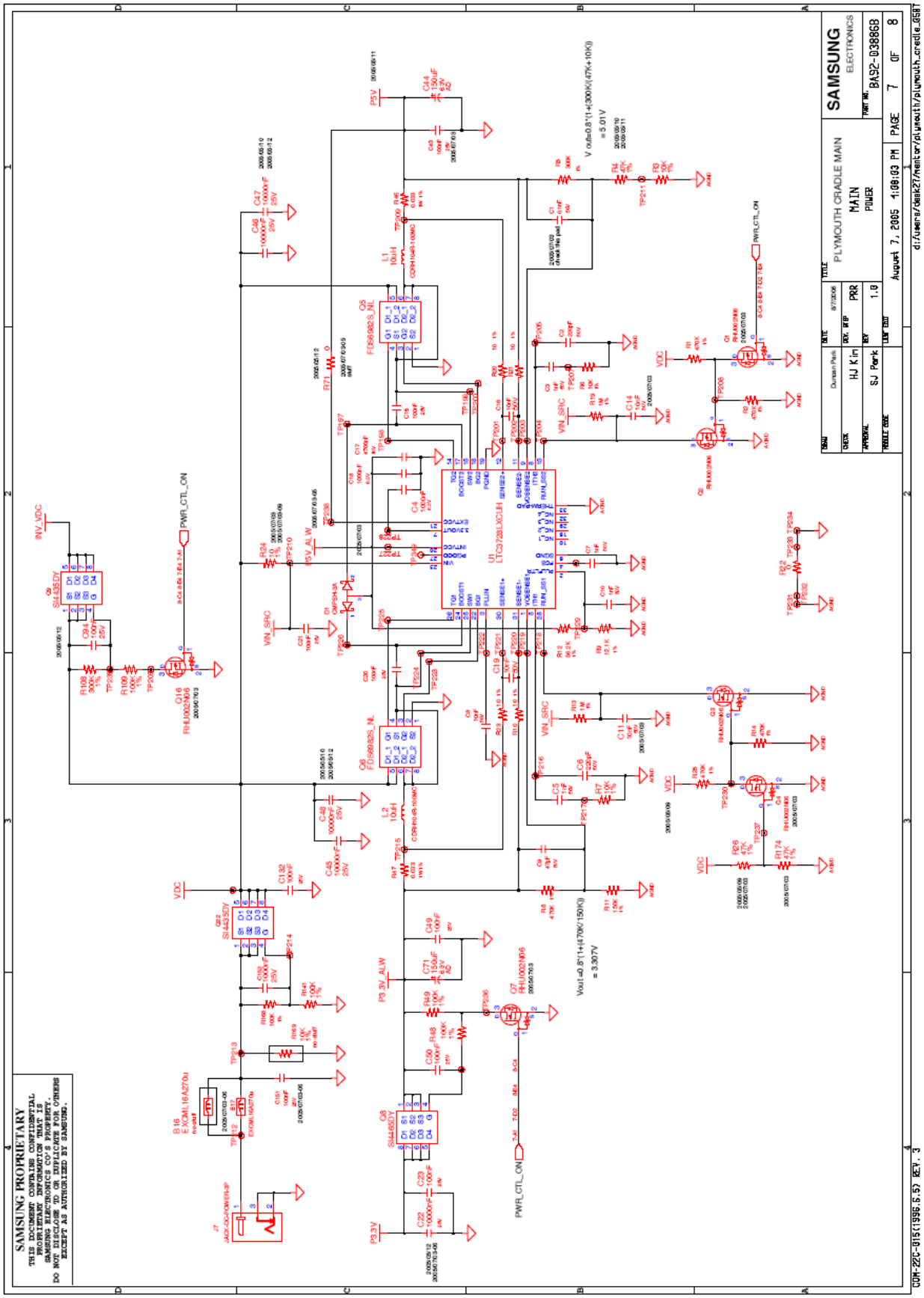


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH CRADLE MAIN
MAIN
MCU
BA92-03886B
U4
NT68F632ALG

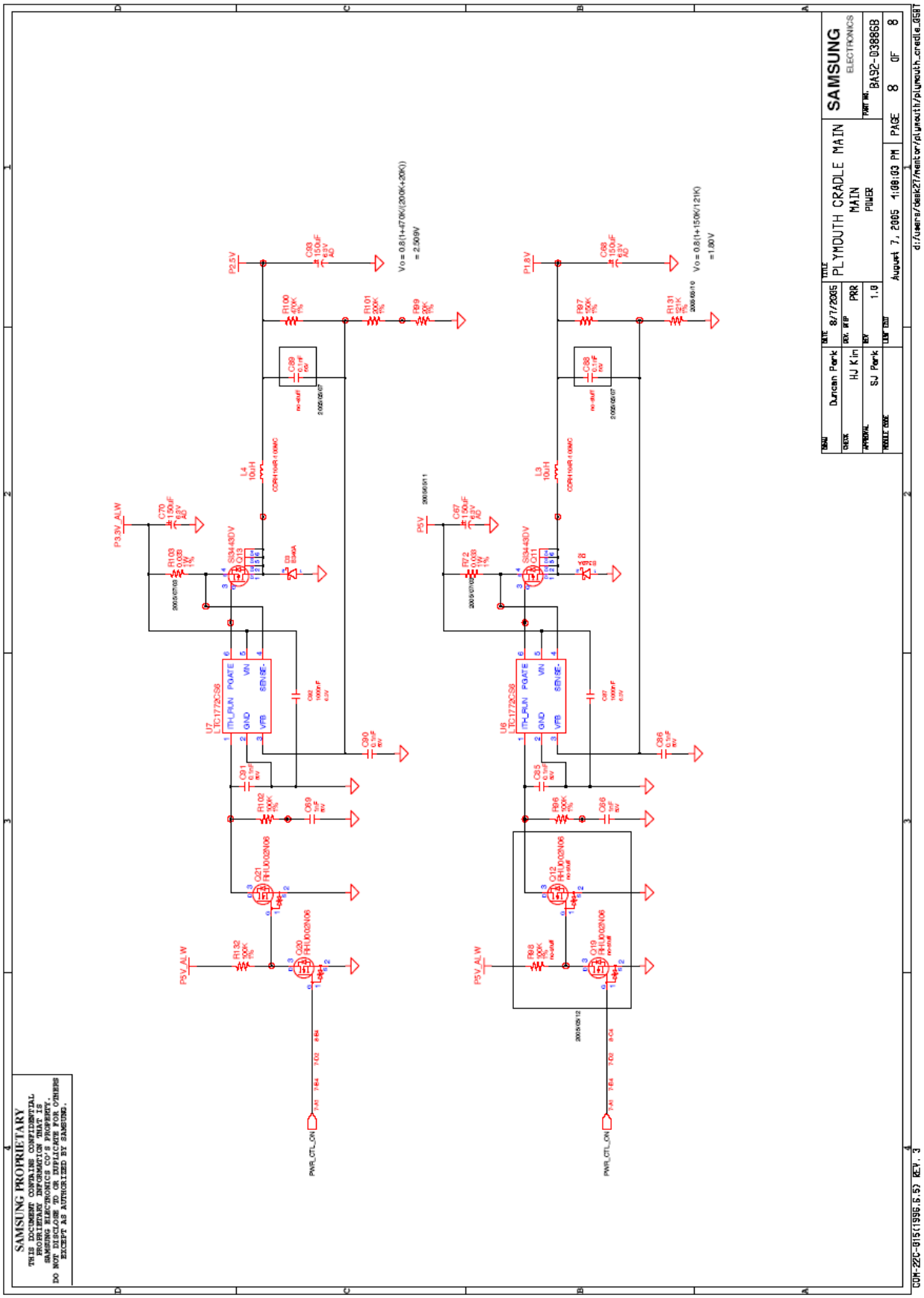
7. 회로도



7. 회로도


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH CRADLE MAIN
MAIN
POWER
BA92-03886B
August 7, 2005 1:08:03 PM
PAGE 7 OF 8
d:/users/desk27/mentor/plymouth/plymouth_cradle.dsn
COM-22C-01(1996.6.5) REV. 3

7. 회로도


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH CRADLE MAIN
MAIN
POWER
BA92-03886B
PAGE 8 OF 8
August 7, 2005 4:08:03 PM
d:/users/desk27/mentor/plymouth/plymouth_cradle.dsn
COM-22C-015(1996.5.5) REV. 3

9) Cradle Switch Board