9. Schematic Diagram

9-1 MIAN BOARD

9-1-1 Schematic Diagram

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OSCAR-G

CPU : Intel P-M DOTHAN
Chip Set : ATI RC300MD + SB150
Remarks : Additional USB Controller Used

Model Name :	Oscar-G
PBA Name :	
PCB Code :	BA41-00478A
Dev. Step :	MP
Revision :	1.1
T.R. Date :	2004-12-11

DRAW	CHECK	APPROVAL

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CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	COVER SHEET	PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 1 OF 51	

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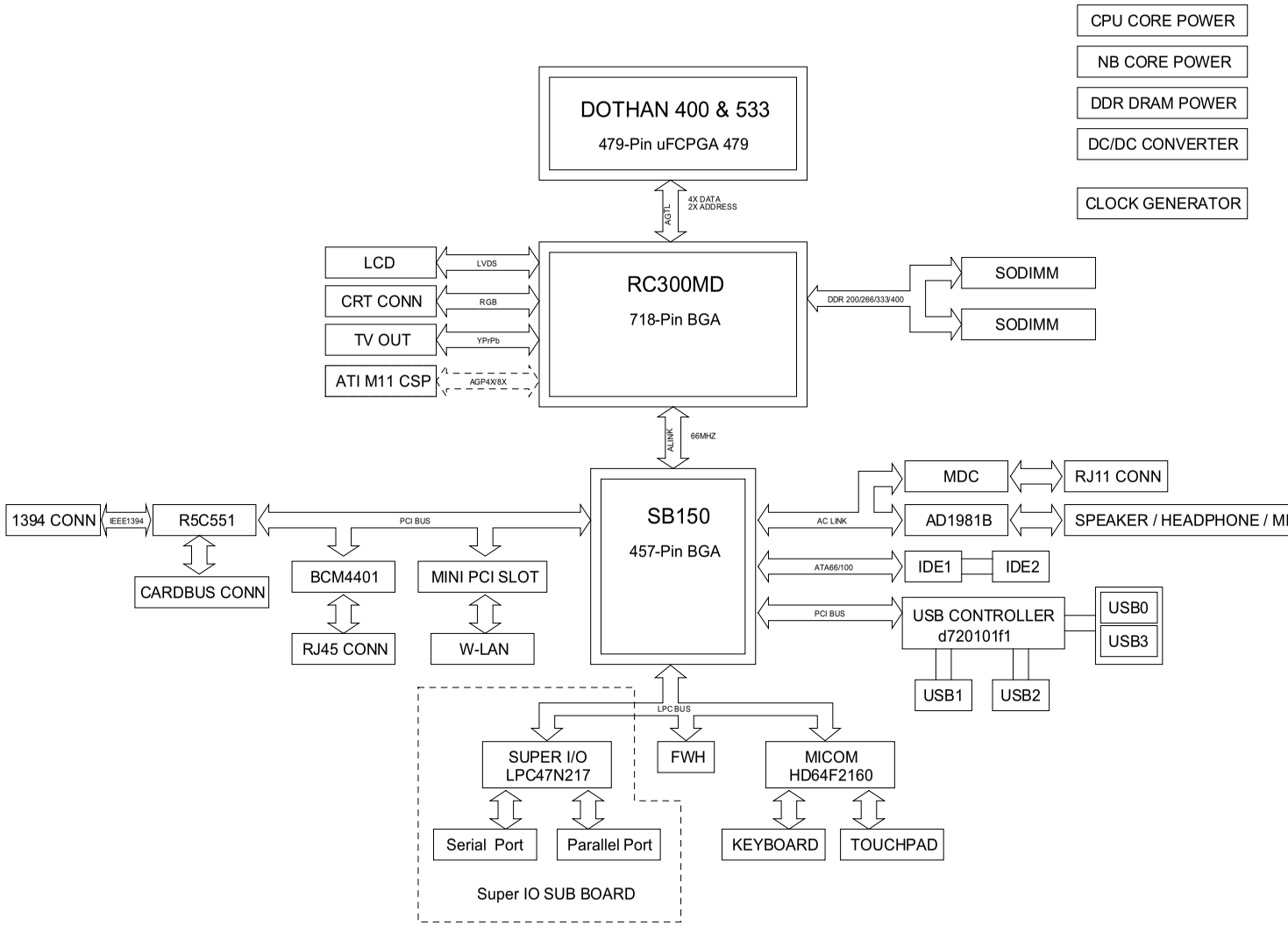

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI DEVICES

DEVICES	IDSEL#	REQ/GNT#	INTERRUPTS
MINIPCI	AD19	0	C, A
CARDBUS CONTROLLER	AD20	1	A, B
LAN CONTROLLER	AD21	2	C
USB CONTROLLER	AD22	3	D, C, B

VOLTAGE RAILS

	POWER	VOLTAGE	ACTIVE SCOPE	PAGE	REMARKS
SYSTEM	VDC	8-19V	S0-S5	49	
	P5V	5V	OFF IN S3-S5	49	
	P5V_ALW	5V	S0-S5	45	SWITCHED FROM VDC
	P3.3V	3.3V	OFF IN S3-S5	45	SWITCHED FROM P3.3V_AUX
	P3V_MICOM	3.3V	S0-S5	45	SWITCHED FROM VDC
	P3.3V_AUX	3.3V	S0-S3	49	
	P1.5V_AUX	1.5V	S0-S3	48	
	P1.25V	1.25V	S0-S3	43	
CPU	VCC_CORE	VID[5:0]	OFF IN S3-S5	46	
	VCCP	1.05V	OFF IN S3-S5	47	
RC300MD	AVDD_NB	2.5V	OFF IN S3-S5	15	SWITCHED FROM P2.5V
	P2.5V_AUX	2.5V	S0-S3	43	
	P1.8V	1.8V	OFF IN S3-S5	48	
	AVDDQ	1.8V	OFF IN S3-S5	15	SWITCHED FROM P1.8V
	PLVDD	1.8V	OFF IN S3-S5	15	SWITCHED FROM P1.8V
	VCC_NB	1.5V	OFF IN S3-S5	47	
	P1.5V	1.5V	OFF IN S3-S5	45	SWITCHED FROM P1.5V_AUX
SB150	P3.3V_AVDDC	3.3V	S0-S3	29	SWITCHED FROM P3.3V_AUX
	USB_AVDD	3.3V	S0-S3	29	SWITCHED FROM P3.3V_AUX
	V_BAT	3.0V	S0-S5	27	
	P2.5V	2.5V	OFF IN S3-S5	45	SWITCHED FROM P2.5V_AUX
	AVDD_CK	2.5V	OFF IN S3-S5	29	SWITCHED FROM P2.5V
	P2.5V_AUX_SB	2.5V	S0-S3	29	SWITCHED FROM P2.5V_AUX
	P2.5V_ALW	2.5V	S0-S5	45	SWITCHED FROM P5V_ALW / VDC
GFX	VGA_CORE	1.0/1.2V	OFF IN S3-S5	43	
	P1.8V_VGA	1.8V	OFF IN S3-S5	48	SWITCHED FROM P2.5V_AUX
ETC	VCC_CB	3.3V/5V	OFF IN S3-S5	34	
	VPP_CB	VAR	OFF IN S3-S5	34	
	AVDD	5V	OFF IN S3-S5	36	SWITCHED FROM P5V

I2C / SMB ADDRESS

DEVICES	ADDRESS	HEX	BUS
SOUTH BRIDGE	MASTER	-	SMBUS MASTER
ADM1032(CPU THERMAL SENSOR)	1001 110X	9Ch	THERMAL SENSOR
ADM1032(GFX THERMAL SENSOR)	1001 110X	9Ch	THERMAL SENSOR
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-

USB PORT ASSIGN

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1	SYSTEM PORT B
2	SYSTEM PORT C
3	SYSTEM PORT D
4	RESERVED

CPU CORE VOLTAGE TABLE

VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE		VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE	
0	0	0	0	0	0	1.708V		1	0	0	0	0	0	1.196V	
0	0	0	0	0	1	1.692V		1	0	0	0	0	1	1.180V	
0	0	0	0	1	0	1.676V		1	0	0	0	1	0	1.164V	
0	0	0	0	1	1	1.660V		1	0	0	0	1	1	1.148V	
0	0	0	1	0	0	1.644V		1	0	0	1	0	0	1.132V	
0	0	0	1	0	1	1.628V		1	0	0	1	0	1	1.116V	
0	0	0	1	1	0	1.612V		1	0	0	1	1	0	1.100V	
0	0	0	1	1	1	1.596V		1	0	0	1	1	1	1.084V	
0	0	1	0	0	0	1.580V		1	0	1	0	0	0	1.068V	
0	0	1	0	0	1	1.564V		1	0	1	0	0	1	1.052V	
0	0	1	0	1	0	1.548V		1	0	1	0	1	0	1.036V	
0	0	1	0	1	1	1.532V		1	0	1	0	1	1	1.020V	
0	0	1	1	0	0	1.516V		1	0	1	1	0	0	1.004V	
0	0	1	1	0	1	1.500V		1	0	1	1	0	1	0.988V	
0	0	1	1	1	0	1.484V		1	0	1	1	1	0	0.972V	
0	0	1	1	1	1	1.468V		1	0	1	1	1	1	0.956V	
0	1	0	0	0	0	1.452V		1	1	0	0	0	0	0.940V	
0	1	0	0	0	1	1.436V		1	1	0	0	0	1	0.924V	
0	1	0	0	1	0	1.420V		1	1	0	0	1	0	0.908V	
0	1	0	0	1	1	1.404V		1	1	0	0	1	1	0.892V	
0	1	0	1	0	0	1.388V		1	1	0	1	0	0	0.876V	
0	1	0	1	0	1	1.372V		1	1	0	1	0	1	0.860V	
0	1	0	1	1	0	1.356V	DOTHAN@400MHz HIGHEST FREQ.	1	1	0	1	1	0	0.844V	LOWEST FREQ.
0	1	0	1	1	1	1.340V		1	1	0	1	1	1	0.828V	
0	1	1	0	0	0	1.324V		1	1	1	0	0	0	0.812V	
0	1	1	0	0	1	1.308V	DOTHAN@533MHz HIGHEST FREQ.	1	1	1	0	0	1	0.796V	
0	1	1	0	1	0	1.292V		1	1	1	0	1	0	0.780V	
0	1	1	0	1	1	1.276V		1	1	1	0	1	1	0.764V	
0	1	1	1	0	0	1.260V		1	1	1	1	0	0	0.748V	DEEPER SLEEP
0	1	1	1	0	1	1.244V		1	1	1	1	0	1	0.732V	
0	1	1	1	1	0	1.228V		1	1	1	1	1	0	0.716V	
0	1	1	1	1	1	1.212V		1	1	1	1	1	1	0.700V	

CPU STRAPS

		Intel© Pentium-M		Intel© Celeron-M
		DOTHAN FSB 533MHz	DOTHAN/BANIAS FSB 400MHz	DOTHAN/BANIAS FSB 400MHz
Sheet 7	R888	NO STUFF	STUFF	STUFF
	R889	STUFF	NO STUFF	NO STUFF
Sheet 9	B16	STUFF	NO STUFF	NO STUFF
	B17	NO STUFF	STUFF	STUFF
Sheet 17	R252	NO STUFF	STUFF	STUFF

REVISION HISTORY

SEE REVISION CHANGE NOTE FOR MORE INFORMATION.

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CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1		PART NO.: BA41-00478A
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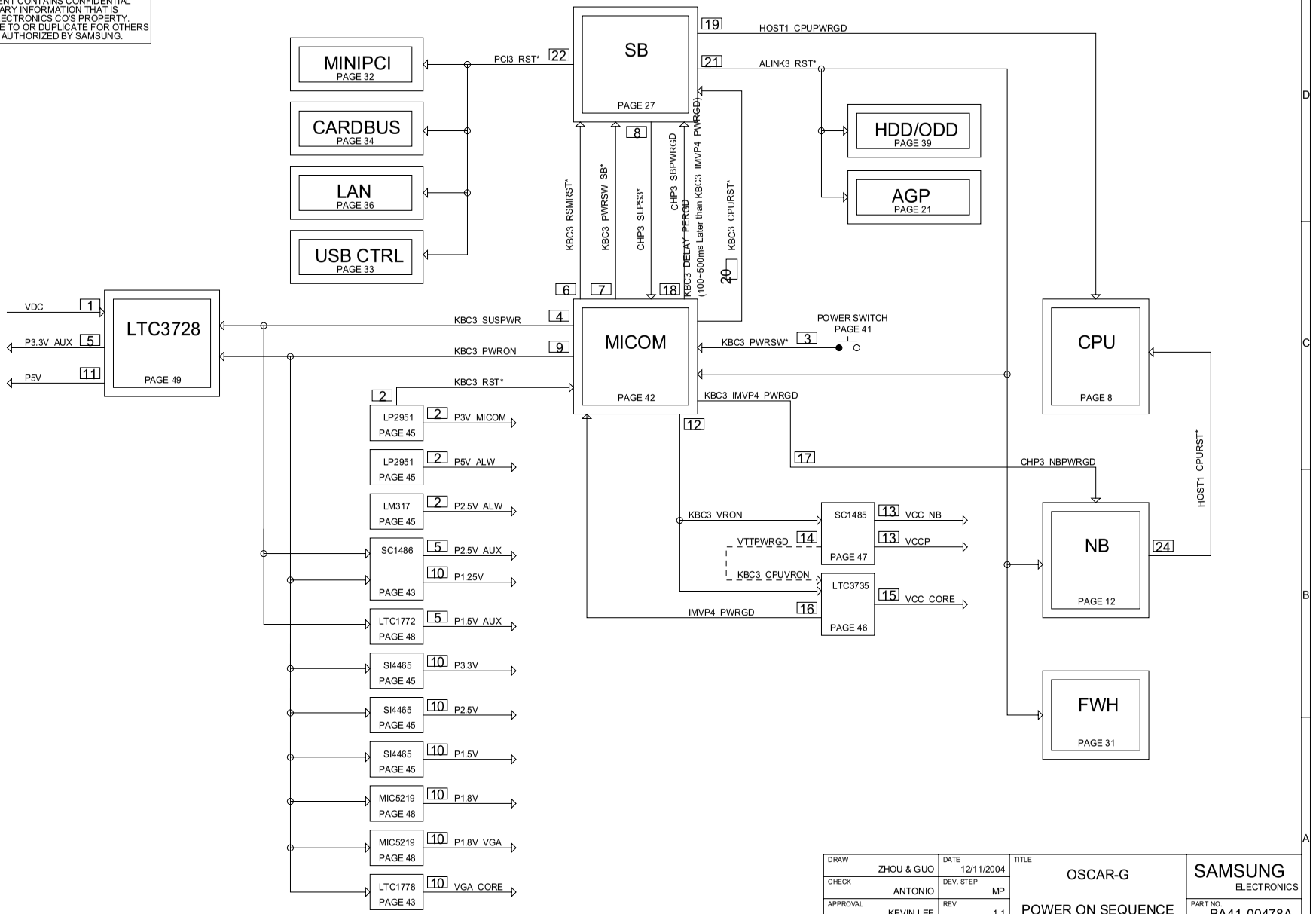

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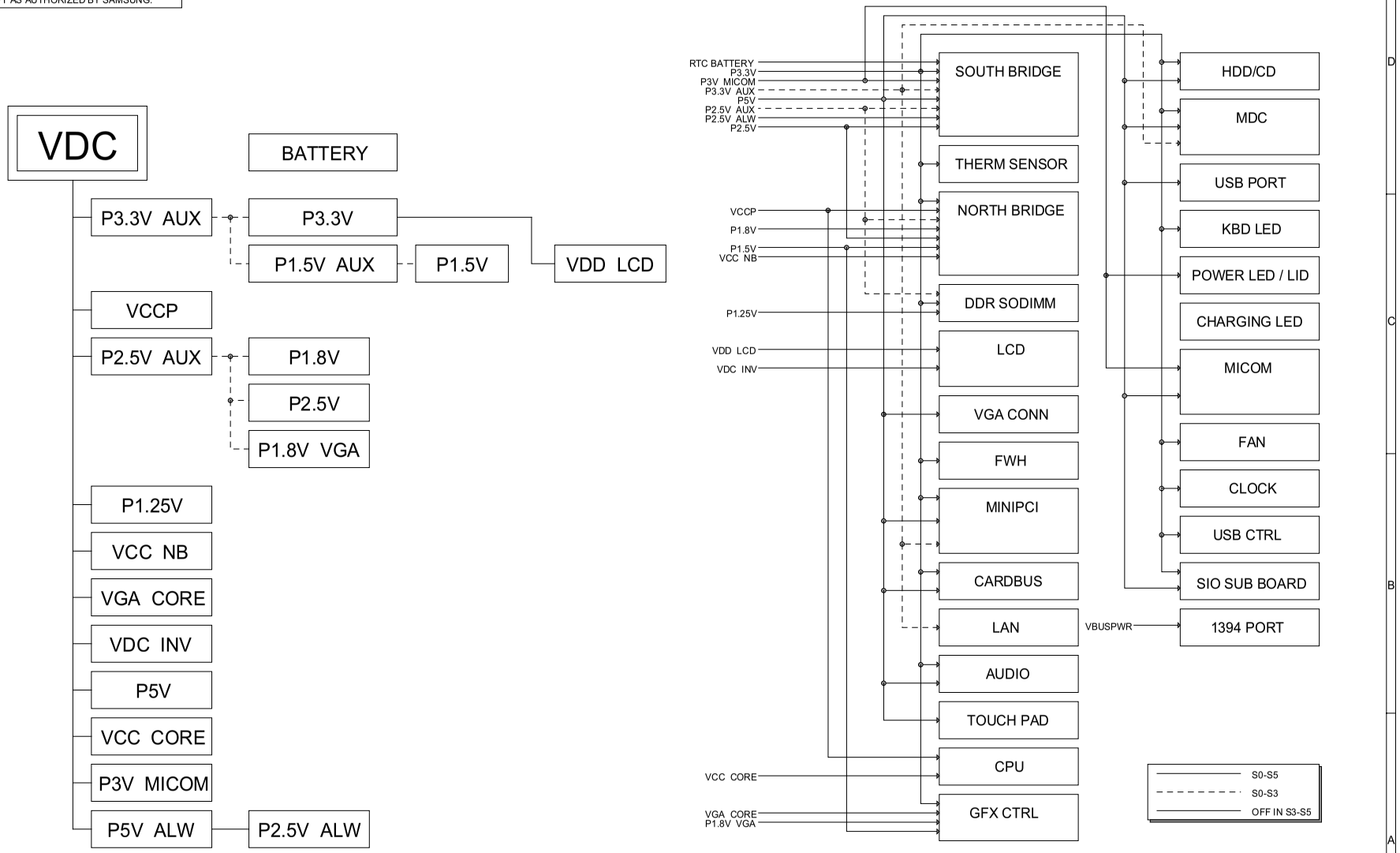

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CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	POWER DIAGRAM	PART NO.: BA41-00478A
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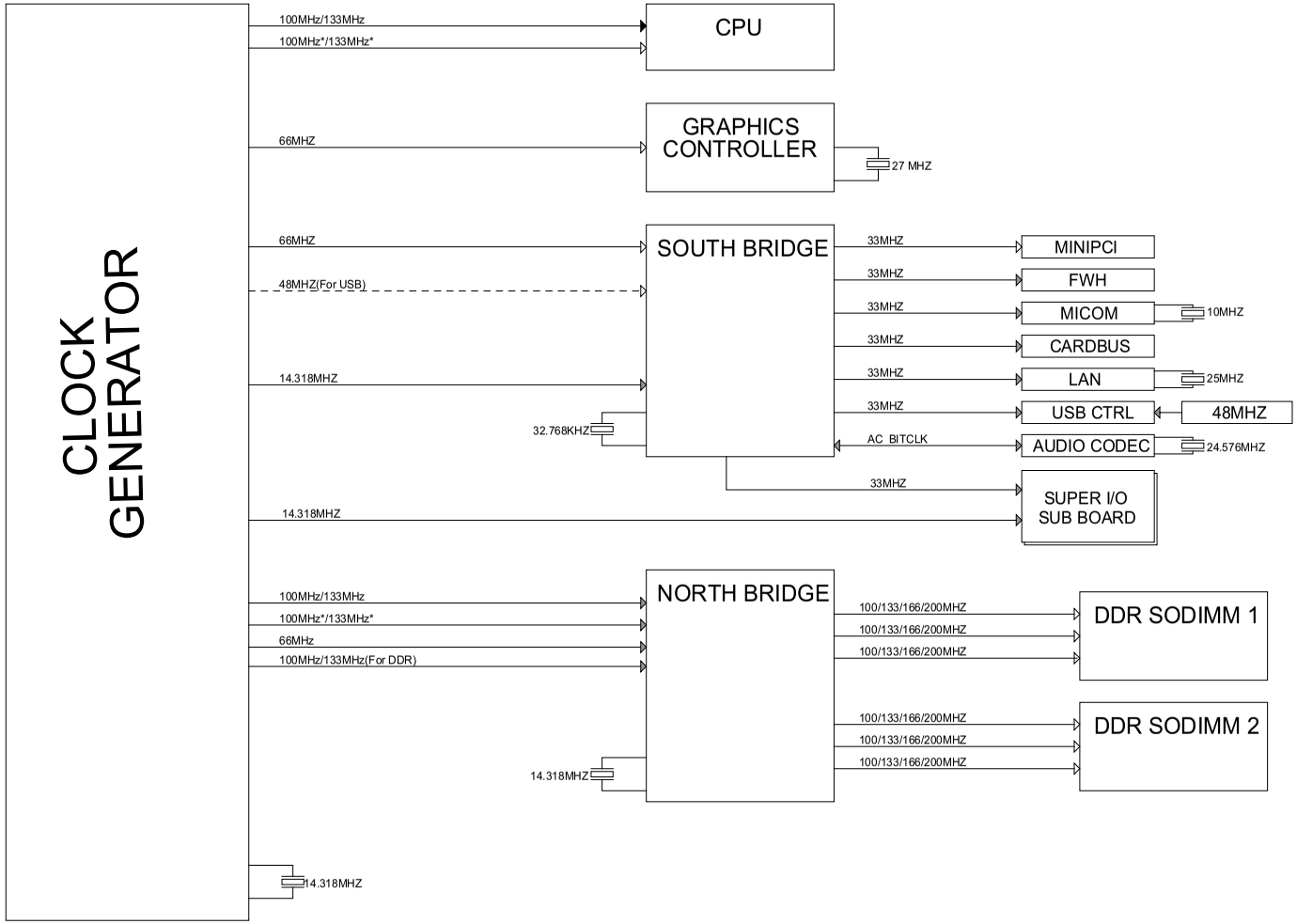

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CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	CLOCK DIAGRAM	PART NO.: BA41-00478A
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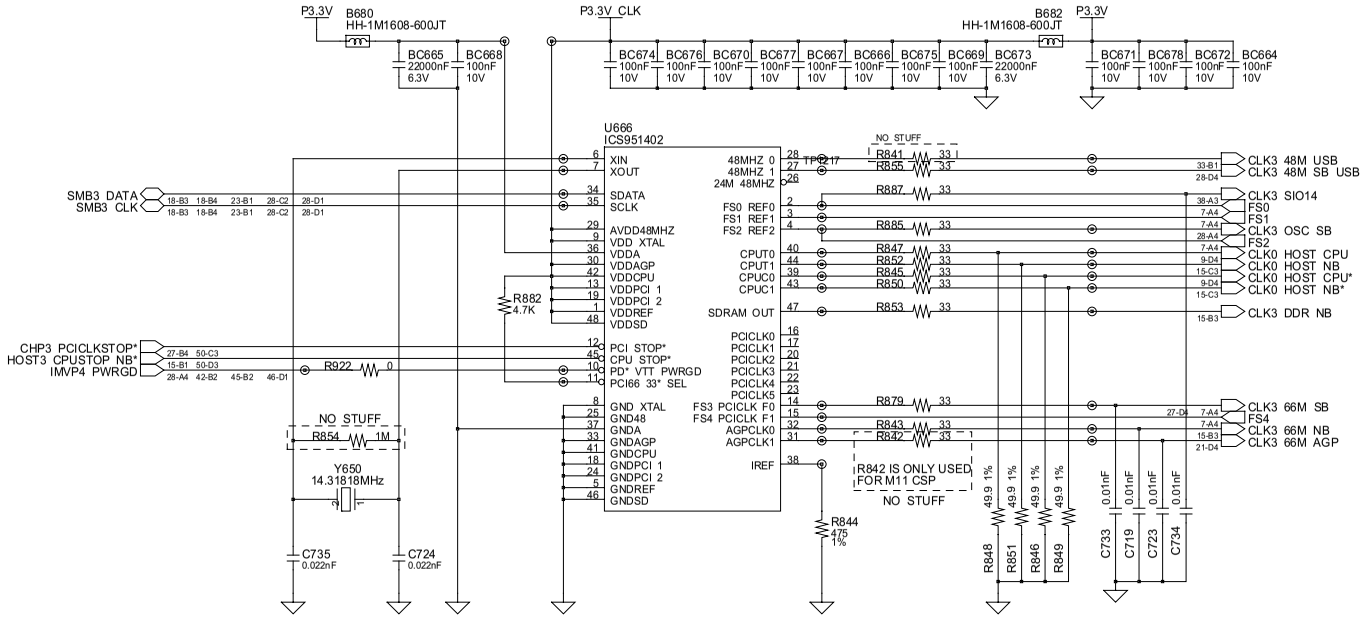
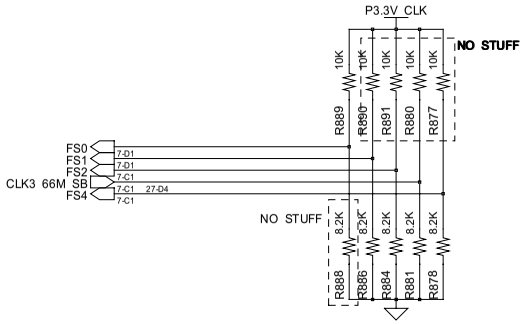


LAYOUT NOTE

- PLACE ALL THE SERIES TERMINATION RESISTORS CLOSE TO CLOCK GENERATOR.
- ROUTE ALL CLK0 HOST CPU/* AND CLK0 HOST NB/* AS DIFFERENTIAL PAIR RULE.
- PUT DECOUPLING CAPS CLOSE TO CLOCK GENERATOR.

CLOCK FREQUENCY SELECTION



CLOCK FREQUENCY SELECT TABLE (MHZ)

FS4	FS3	FS2	FS1	FS0	CPU	MEM	AGP	PCI	FS4	FS3	FS2	FS1	FS0	CPU	MEM	AGP	PCI
0	0	0	0	0	100.01	100.01	66.66	66.66	1	0	0	0	0	99.51	99.51	66.66	66.66
0	0	0	0	1	133.33	133.33	66.66	66.66	1	0	0	0	1	132.69	132.69	66.66	66.66
0	0	0	1	0	200.01	200.01	66.66	66.66	1	0	0	1	0	199.02	199.02	66.66	66.66
0	0	0	1	1	166.64	166.64	66.66	66.66	1	0	0	1	1	165.85	165.85	66.66	66.66
0	0	1	0	0	100.01	133.34	66.66	66.66	1	0	1	0	0	99.51	99.51	66.66	66.66
0	0	1	0	1	133.34	100.01	66.66	66.66	1	0	1	0	1	132.68	132.68	66.66	66.66
0	0	1	1	0	133.16	166.45	66.66	66.66	1	0	1	1	0	132.59	132.59	66.66	66.66
0	0	1	1	1	166.45	133.16	66.66	66.66	1	0	1	1	1	165.73	165.73	66.66	66.66
0	1	0	0	0	105.00	105.00	66.66	66.66	1	1	0	0	0	99.38	99.38	66.66	66.66
0	1	0	0	1	140.00	140.00	66.66	66.66	1	1	0	0	1	132.52	132.52	66.66	66.66
0	1	0	1	0	66.67	66.67	66.66	66.66	1	1	0	1	0	198.77	198.77	66.66	66.66
0	1	0	1	1	175.00	175.00	66.66	66.66	1	1	0	1	1	165.64	165.64	66.66	66.66
0	1	1	0	0	109.99	109.99	66.66	66.66	1	1	1	0	0	99.38	132.51	66.66	66.66
0	1	1	0	1	146.66	146.66	66.66	66.66	1	1	1	0	1	132.51	99.38	66.66	66.66
0	1	1	1	0	210.00	210.00	66.66	66.66	1	1	1	1	0	132.36	165.45	66.66	66.66
0	1	1	1	1	183.27	183.27	66.66	66.66	1	1	1	1	1	165.45	132.36	66.66	66.66

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CHECK: ANTONIO	DEV. STEP: MP	CLOCK GENERATOR	
APPROVAL: KEVIN LEE	REV: 1.1		PART NO.: BA41-00478A
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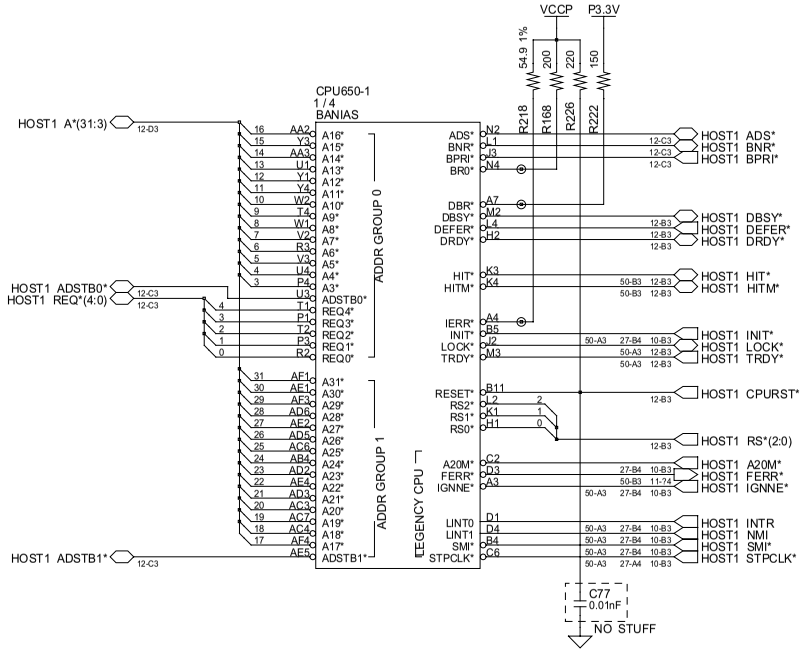

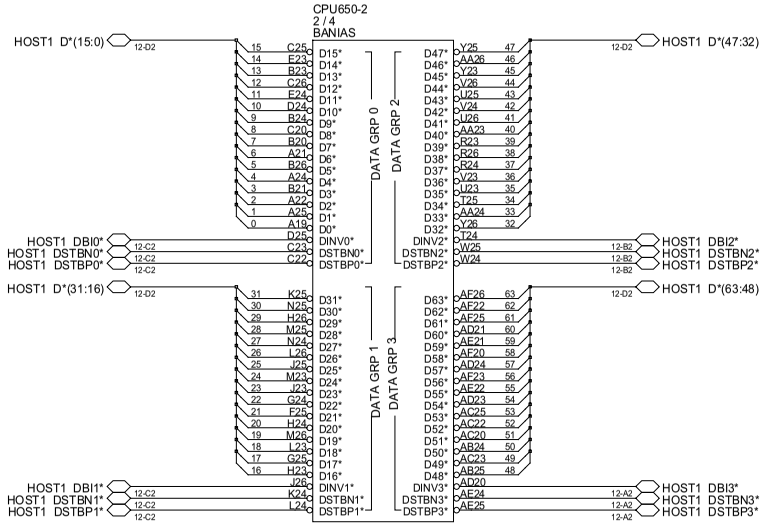

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CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	CPU (1/2)	PART NO.: BA41-00478A
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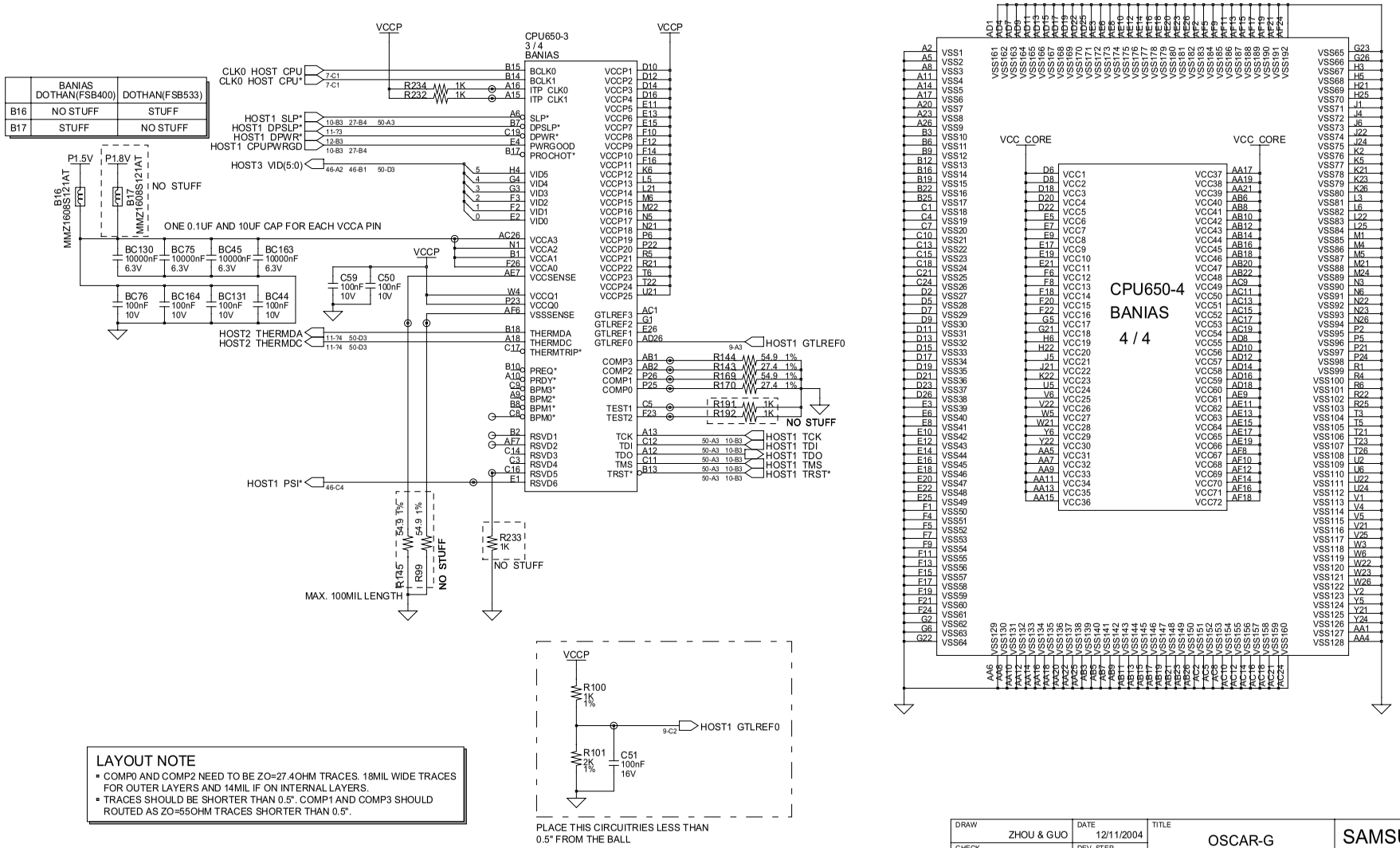

	BANIAS DOTHAN(FSB400)	DOTHAN(FSB533)
B16	NO STUFF	STUFF
B17	STUFF	NO STUFF

LAYOUT NOTE

- COMP0 AND COMP2 NEED TO BE ZO=27.4OHM TRACES. 18MIL WIDE TRACES FOR OUTER LAYERS AND 14MIL IF ON INTERNAL LAYERS.
- TRACES SHOULD BE SHORTER THAN 0.5". COMP1 AND COMP3 SHOULD ROUTED AS ZO=55OHM TRACES SHORTER THAN 0.5".

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CHECK: ANTONIO	DEV. STEP: MP	CPU (2/2)	
APPROVAL: KEVIN LEE	REV: 1.1		PART NO.: BA41-00478A
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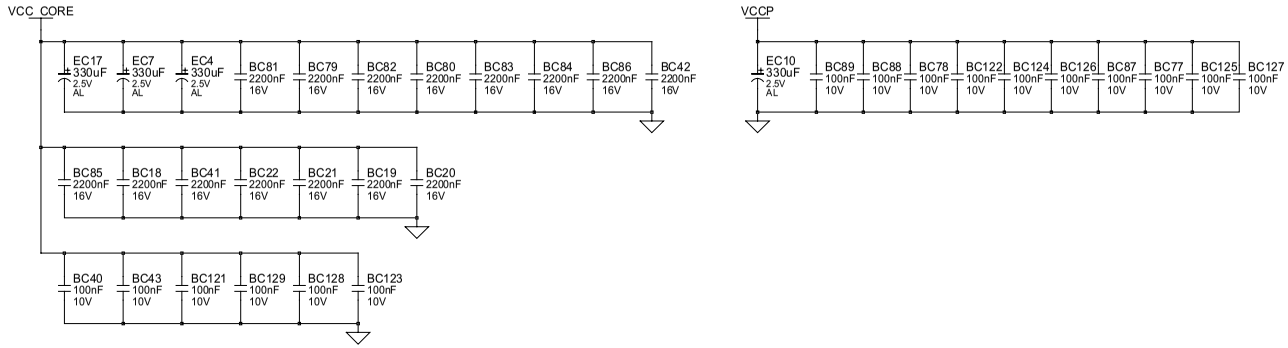

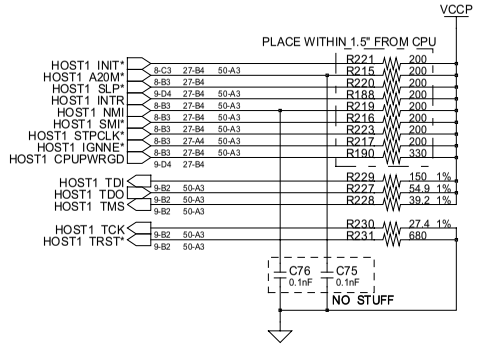

HOST1 TDI & HOST1 TDO PULLUPS MUST BE PLACED WITHIN 300PS OF CPU TDI PIN (WITHIN 2")

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APPROVAL: KEVIN LEE	REV: 1.1	PULLUPS / DECOUPLINGS	PART NO.: BA41-00478A
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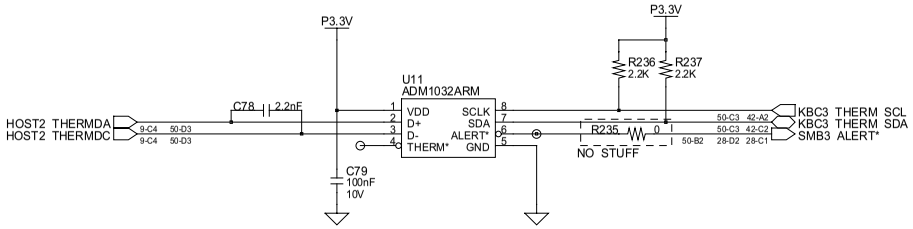
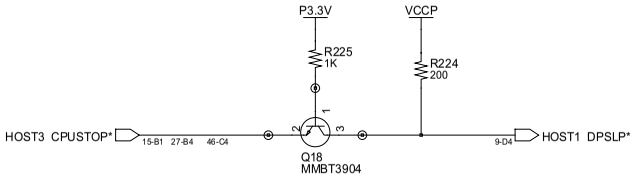
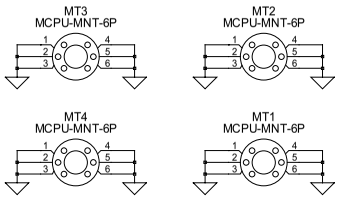
THERMAL SENSOR

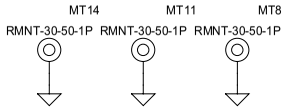


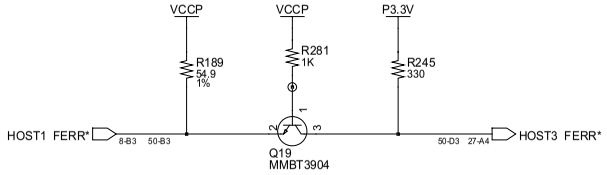
LAYOUT NOTE

- PLACE THERMAL SENSOR CLOSE TO A REMOTE DIODE.
- KEEP TRACES AWAY FROM HIGH VOLTAGE (+12V).
- KEEP TRACES AWAY FROM FAST DATA BUSES AND CRT SIGNAL.
- ROUTE USING RECOMMENDED TRACE WIDTHS AND SPACINGS (10MIL/10MIL).
- PLACE A GROUND PLANE UNDER THE TRACES.
- USE GUARD TRACES FLANKING DXP AND DXN AND CONNECTING TO GND.
- ROUTE CPU2 THERMDA AND CPU2 THERMDC ON SAME LAYER.









DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	THERMAL SENSOR	PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM		PAGE 11 OF 51

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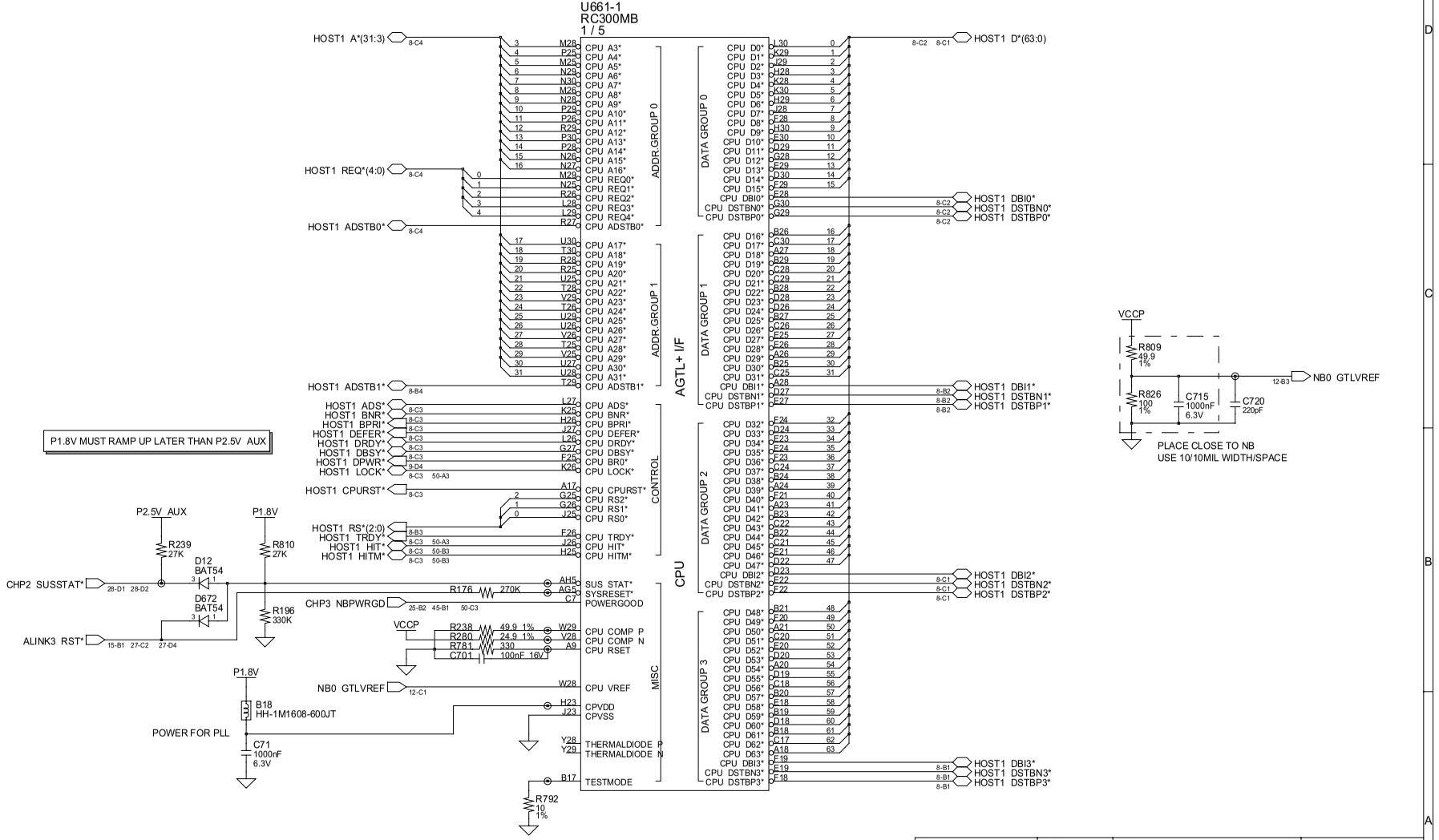

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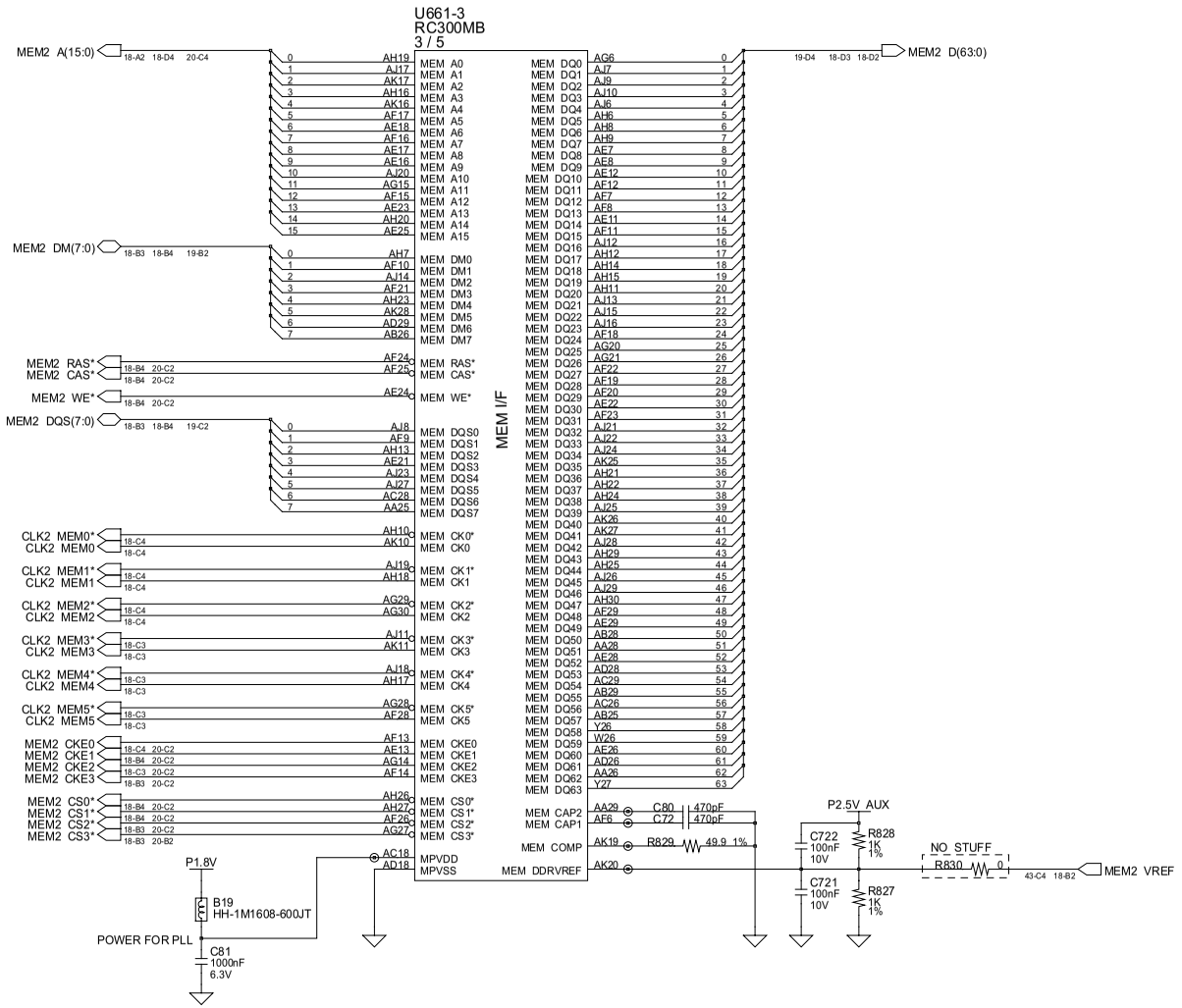

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APPROVAL: KEVIN LEE	REV: 1.1	NORTH BRIDGE (2/5)	PART NO.: BA41-00478A
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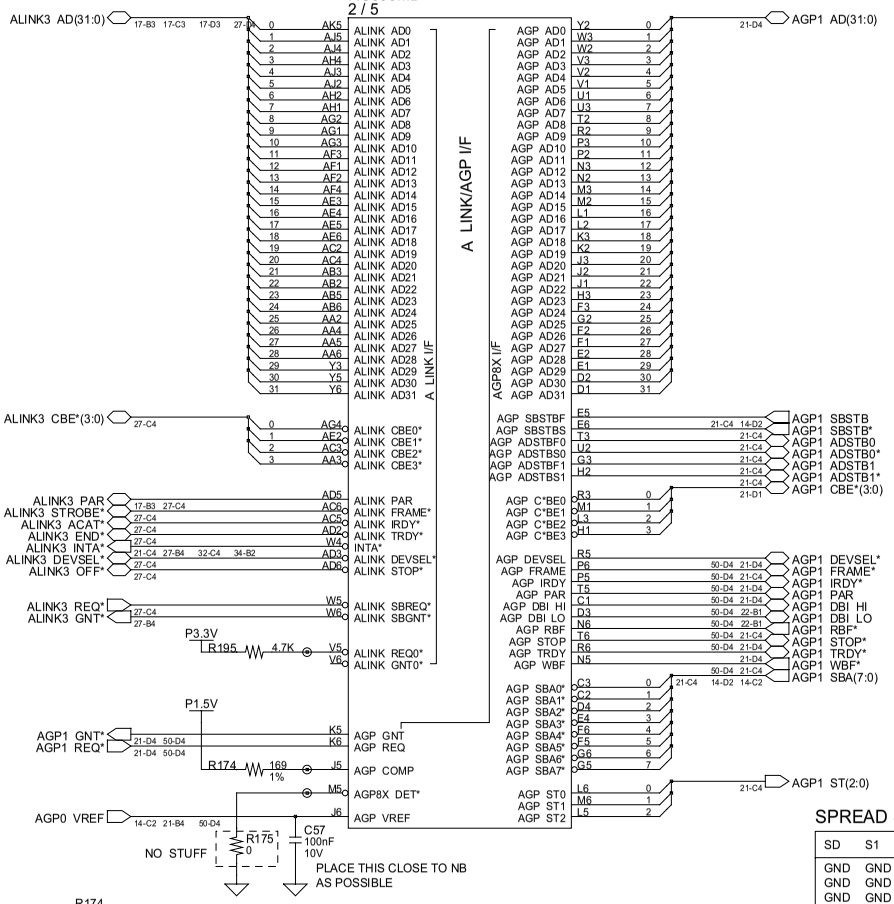
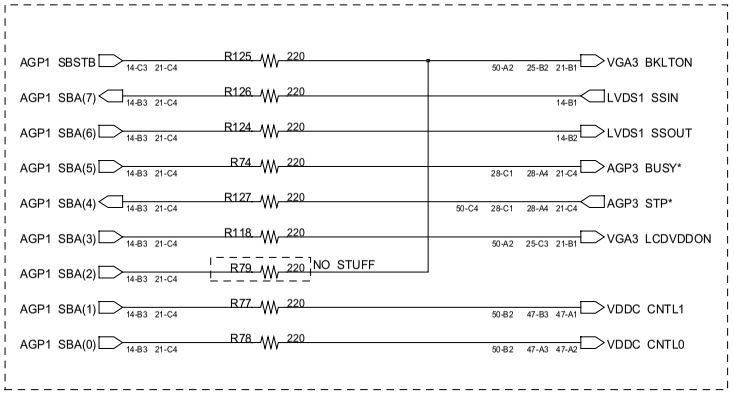
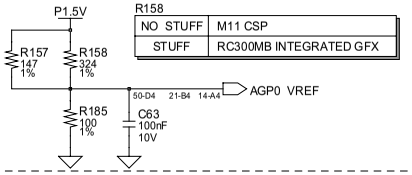


R174

169OHM	M11 CSP
NO STUFF	RC300MB INTEGRATED GFX

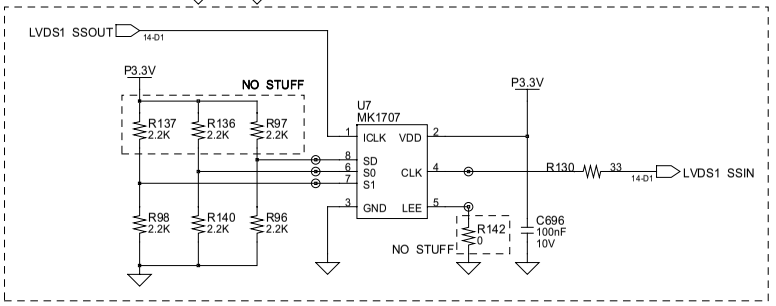


USED ONLY FOR RC300MB INTEGRATED GFX



R158

NO STUFF	M11 CSP
STUFF	RC300MB INTEGRATED GFX



USED ONLY FOR RC300MB INTEGRATED GFX

R142

NO STUFF	LOW EMI ENABLE
STUFF	DISABLE SPREAD SPECTRUM

SPREAD SPECTRUM TABLE

SD	S1	S0	DIRECTION	% SPREAD
GND	GND	GND	DOWN	0.6
GND	GND	NS	DOWN	0.8
GND	GND	3.3V	DOWN	1.25
GND	NS	GND	DOWN / CENTER	0.5 / -1.5
GND	NS	NS	DOWN	2
GND	NS	3.3V	DOWN / CENTER	0.5 / -2.5
GND	3.3V	GND	DOWN / CENTER	0.5 / -3
GND	3.3V	NS	DOWN	5
3.3V	GND	GND	CENTER	+/-0.35
3.3V	GND	NS	CENTER	+/-0.5
3.3V	GND	3.3V	CENTER	+/-0.7
3.3V	NS	GND	CENTER	+/-0.8
3.3V	NS	NS	CENTER	+/-1.1
3.3V	NS	3.3V	CENTER	+/-1.4
3.3V	3.3V	NS	CENTER	+/-2.5

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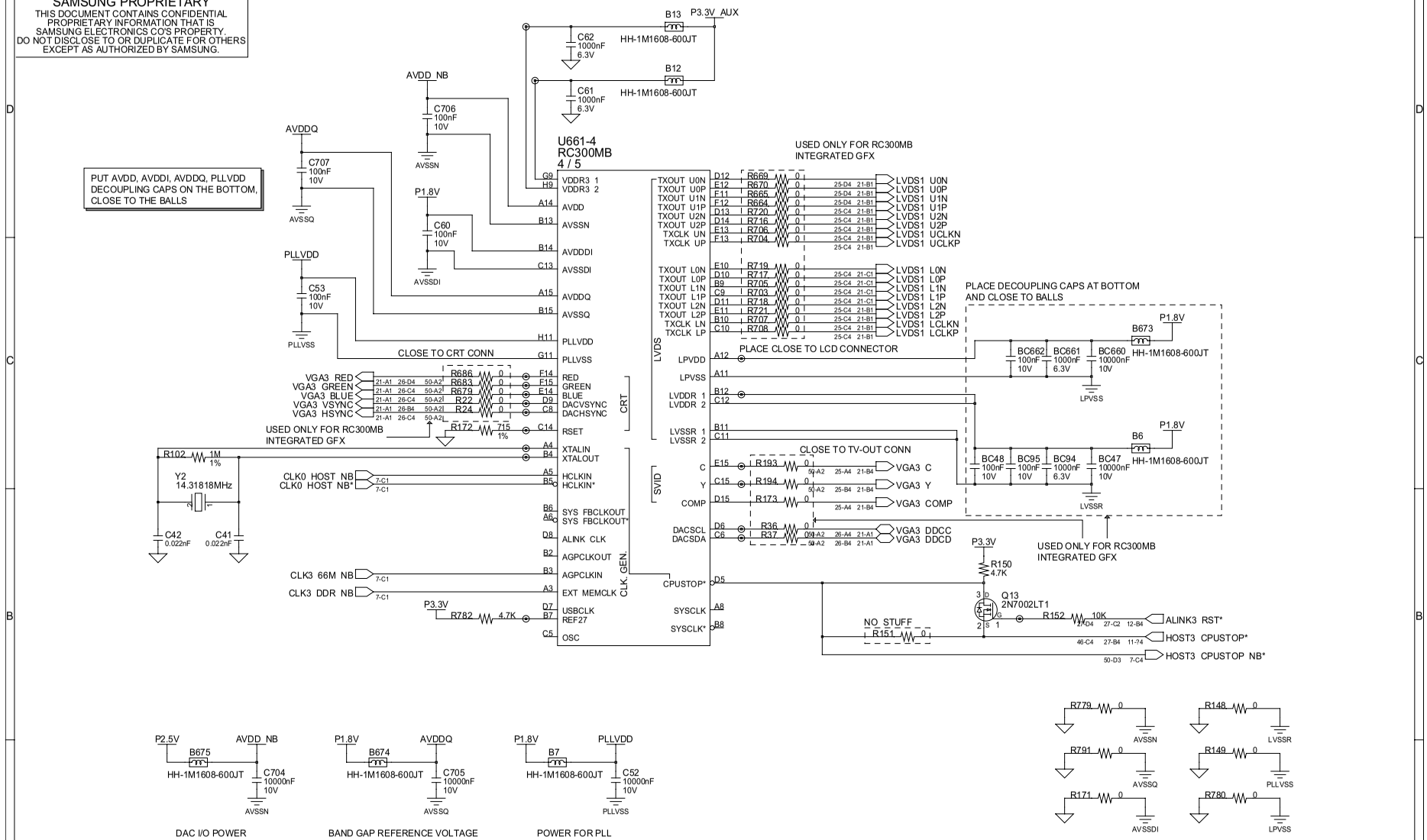

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CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	NORTH BRIDGE (4/5)	PART NO.: BA41-00478A
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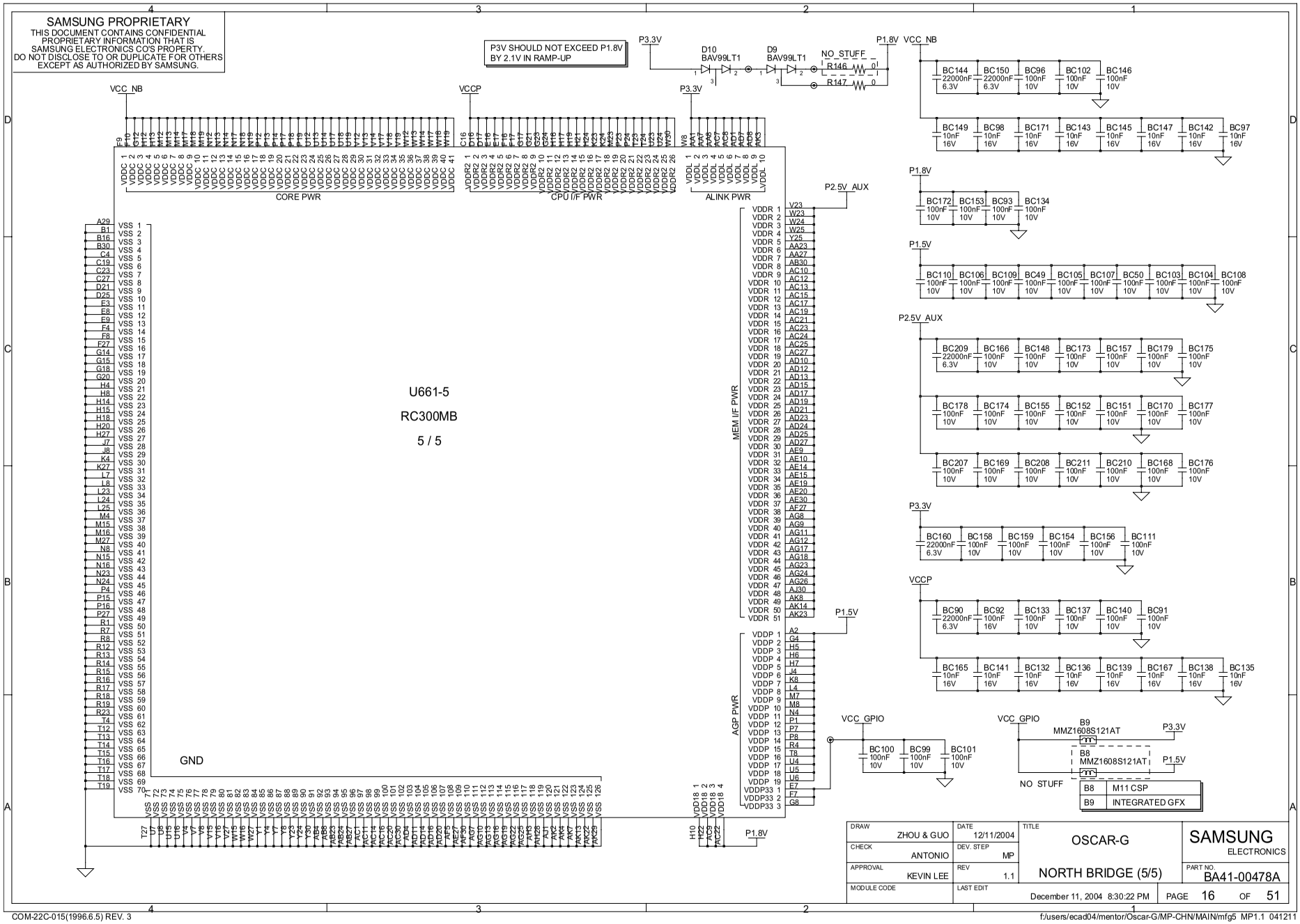

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CHECK: ANTONIO	DEV. STEP: MP	NORTH BRIDGE (5/5)	
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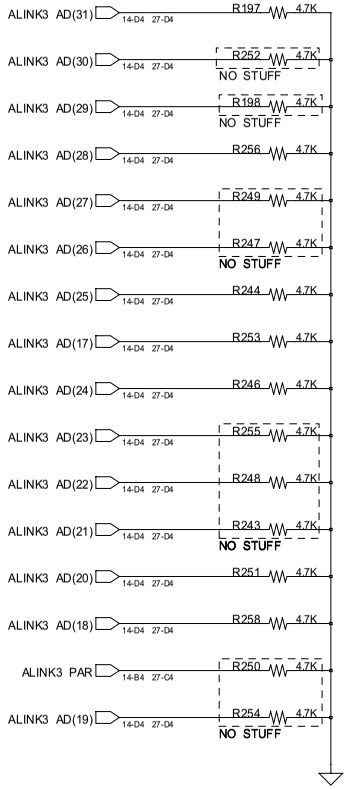

FSB CLK SPEED ALINK3 AD(31:30)	00 : 100 MHZ 01 : 133 MHZ (DEFAULT) 10 : 200 MHZ 11 : 166 MHZ
STRAP CONFIGURATION ALINK3 AD(29)	0 : REDUCED SET 1 : FULL SET (DEFAULT)
SPREAD SPECTRUM ENABLE ALINK3 AD(28)	0 : DISABLE (DEFAULT) 1 : ENABLE
FRC SHORT RESET# ALINK3 AD(27)	0 : TEST MODE 1 : NORMAL MODE (DEFAULT)
ENABLE IOQ ALINK3 AD(26)	0 : IOQ=1 1 : IOQ=12 (DEFAULT)
CPU VOLTAGE ALINK3 AD(25, 17)	00 : 1.05V (DEFAULT) 01 : 1.35V 10 : 1.75V 11 : 1.45V
MOBILE CPU SELECT ALINK3 AD(24)	0 : BANIAS & DOTHAN(DEFAULT) 1 : OTHER CPU
CLOCK BYPASS DISABLE ALINK3 AD(23)	0 : TEST MODE 1 : NORMAL (DEFAULT)
OSC PAD OUTPUT PCICLK ALINK3 AD(22)	0 : OSC CLK OUT 1 : PCICLK OUT (DEFAULT)
AUTO CALIBRATION ENABLE ALINK3 AD(21)	0 : DISABLE 1 : ENABLE (DEFAULT)
INTERNAL CLK GEN ENABLE ALINK3 AD(20)	0 : DISABLE (DEFAULT) 1 : ENABLE
ENABLE PHASE CALIBRATION ALINK3 AD(18)	0 : DISABLE 1 : ENABLE (DEFAULT)
EXTENDED DEBUG MODE ALINK3 PAR	0 : DEBUG MODE 1 : NOMAL (DEFAULT)
MEMORY IO VOLTAGE ALINK3 AD(19)	0 : 1.8V 1 : 2.5V (DEFAULT)

ALINK SIGNALS HAVE INTERNAL PULL-UPS
NO EXTERNAL PULL-UPS ARE NEEDED

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CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	NORTH BRIDGE STRAPS	PART NO.: BA41-00478A
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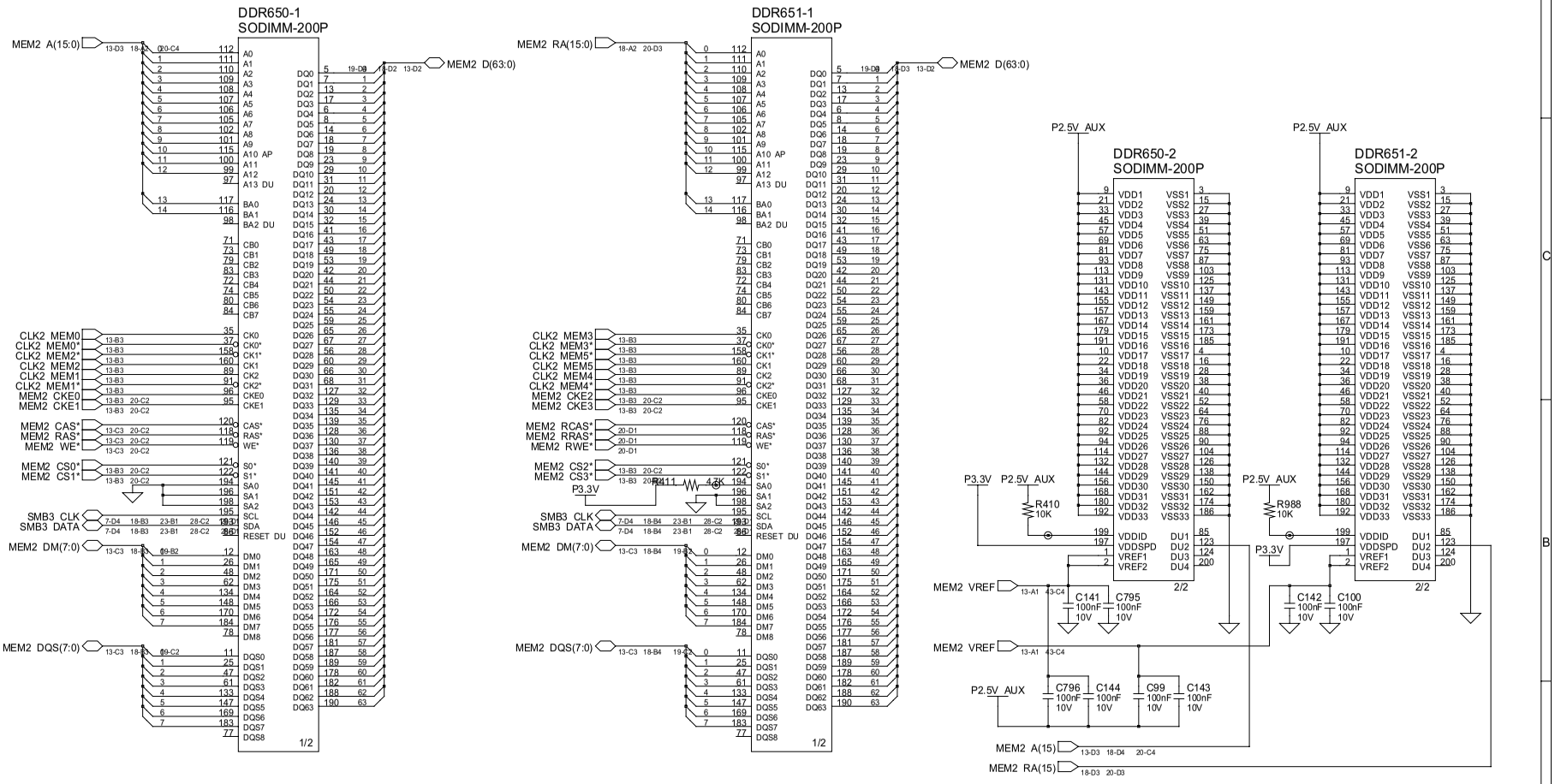

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CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	DDR SODIMM	PART NO.: BA41-00478A
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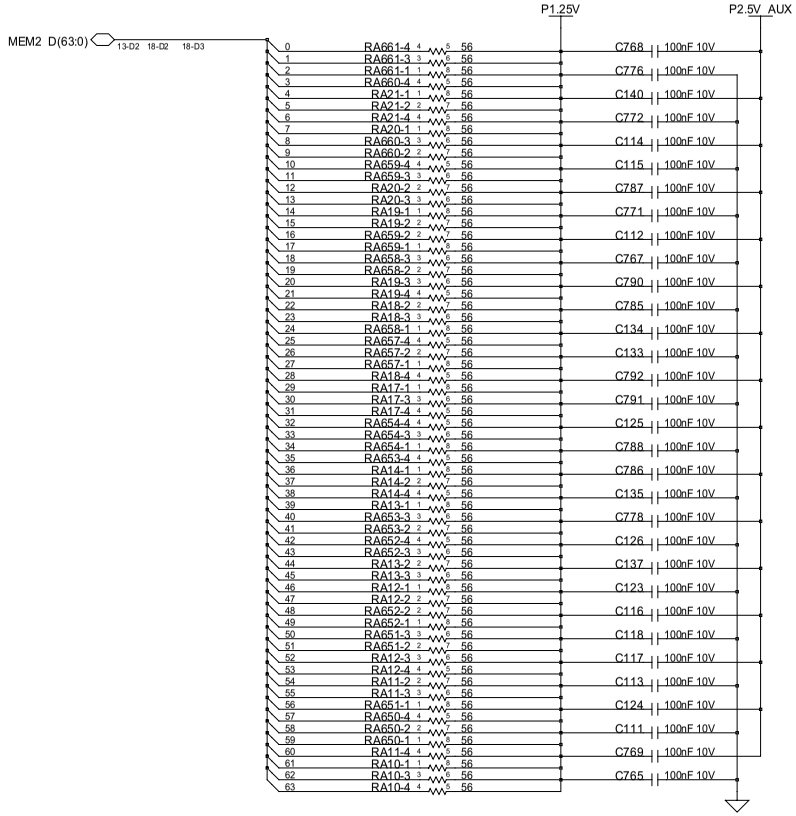

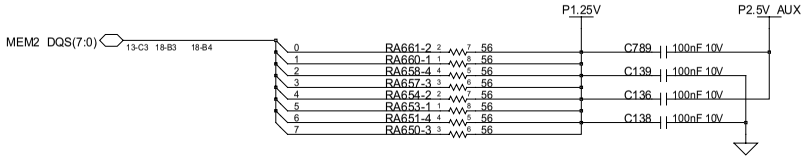

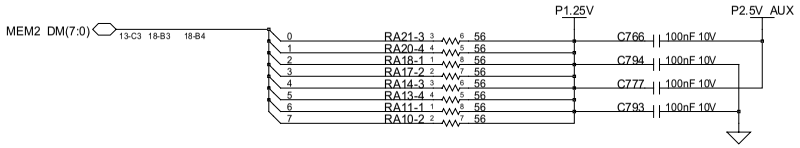

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CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	DDR TERMINATION (1/2)	PART NO.: BA41-00478A
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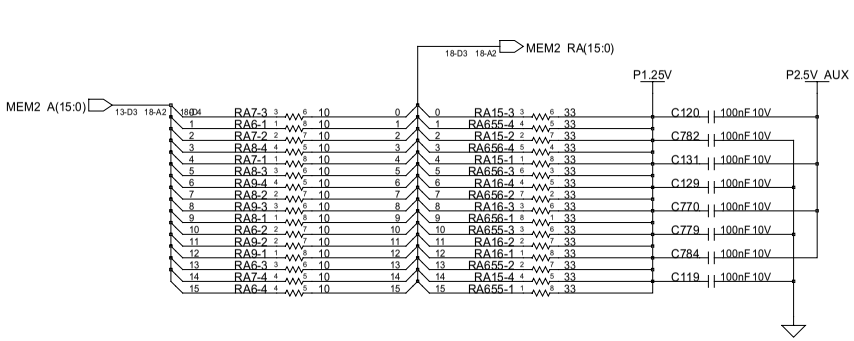

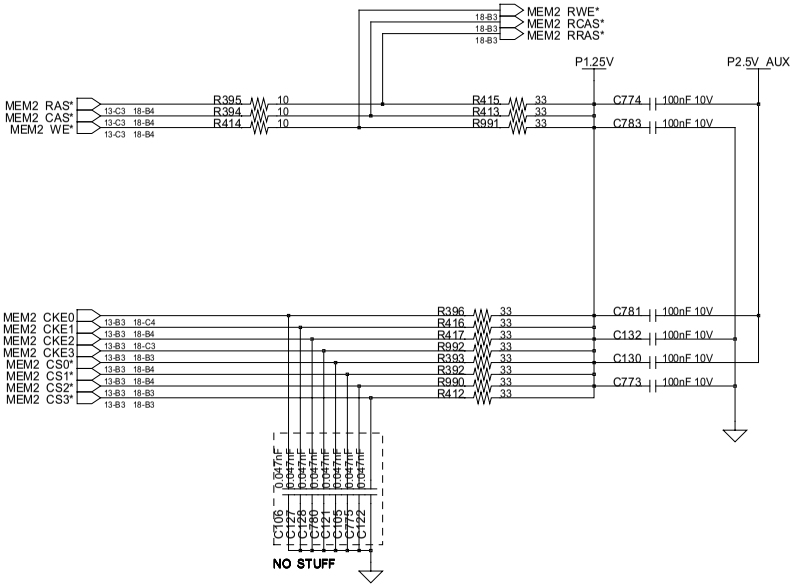

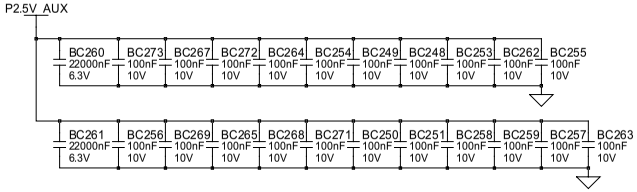

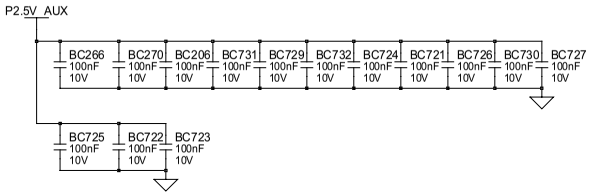

- 2 DECOUPLING CAPS PER RESISTOR PAK
- PLACE RPACKS & RESISTORS AFTER THE LAST DIMM

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CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	DDR TERMINATION (2/2)	PART NO.: BA41-00478A
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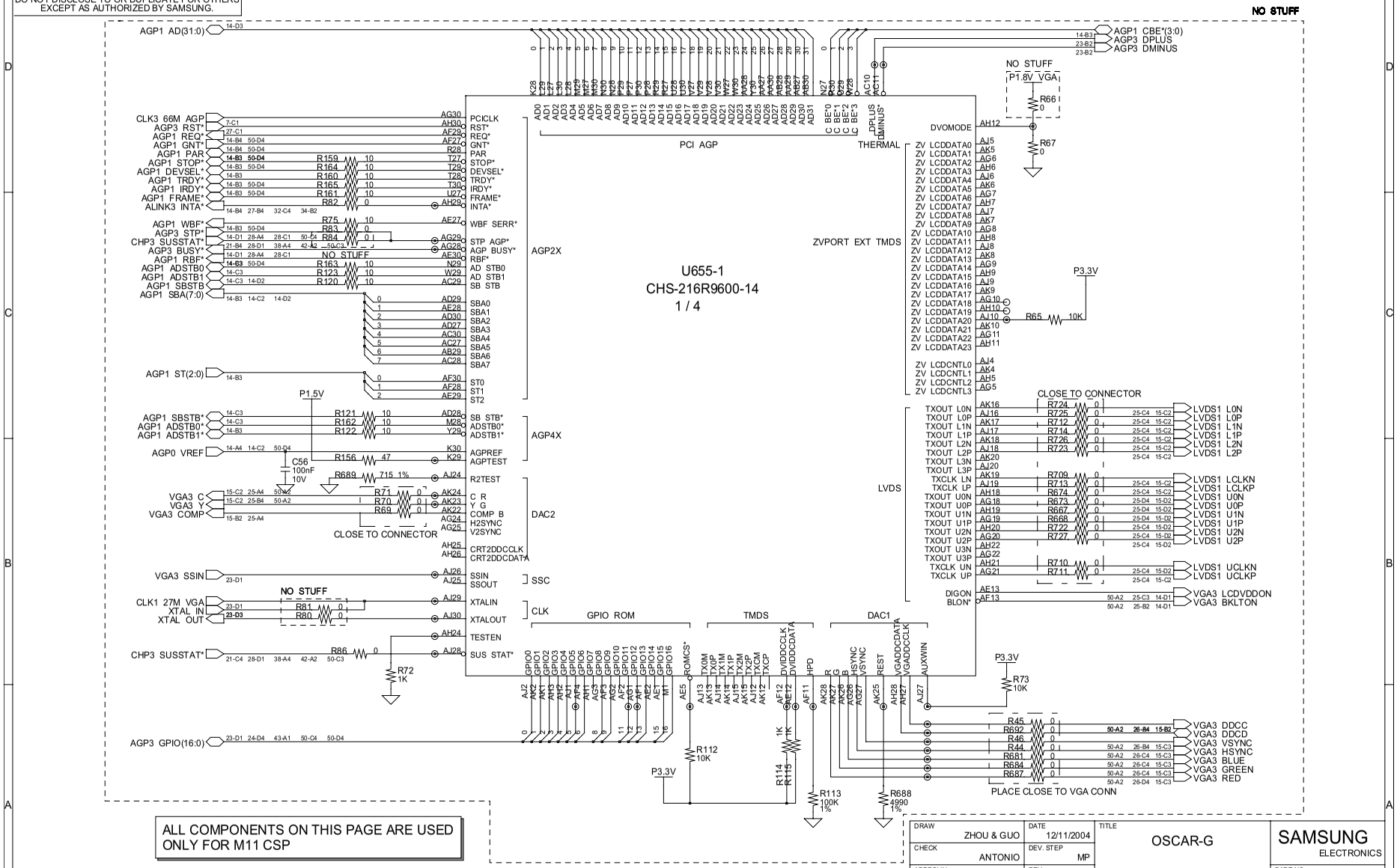

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CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	GFX CONTROLLER (1/3)	PART NO.: BA41-00478A
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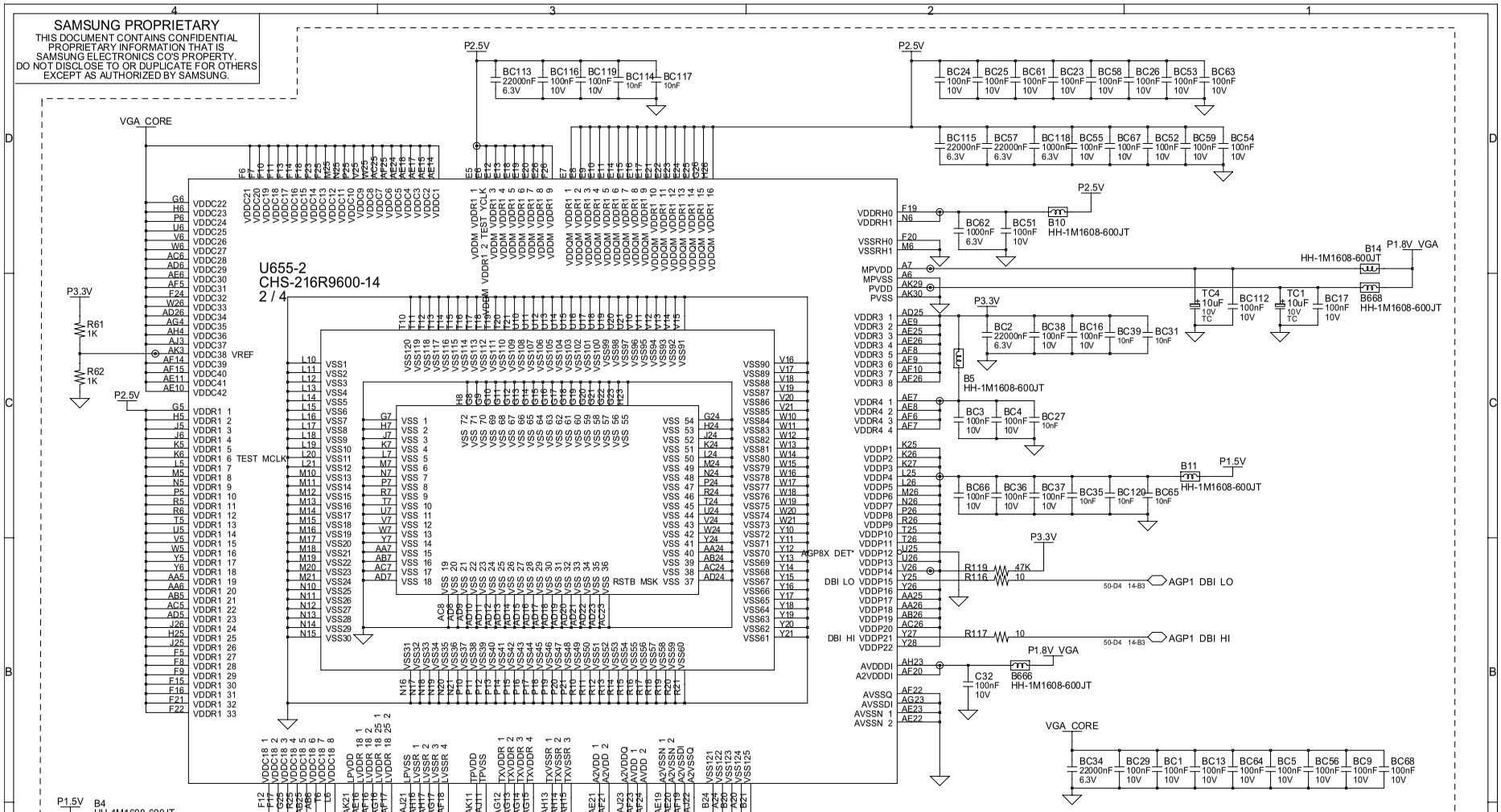

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP	GFX CONTROLLER (2/3)	
APPROVAL: KEVIN LEE	REV: 1.1		PART NO. BA41-00478A
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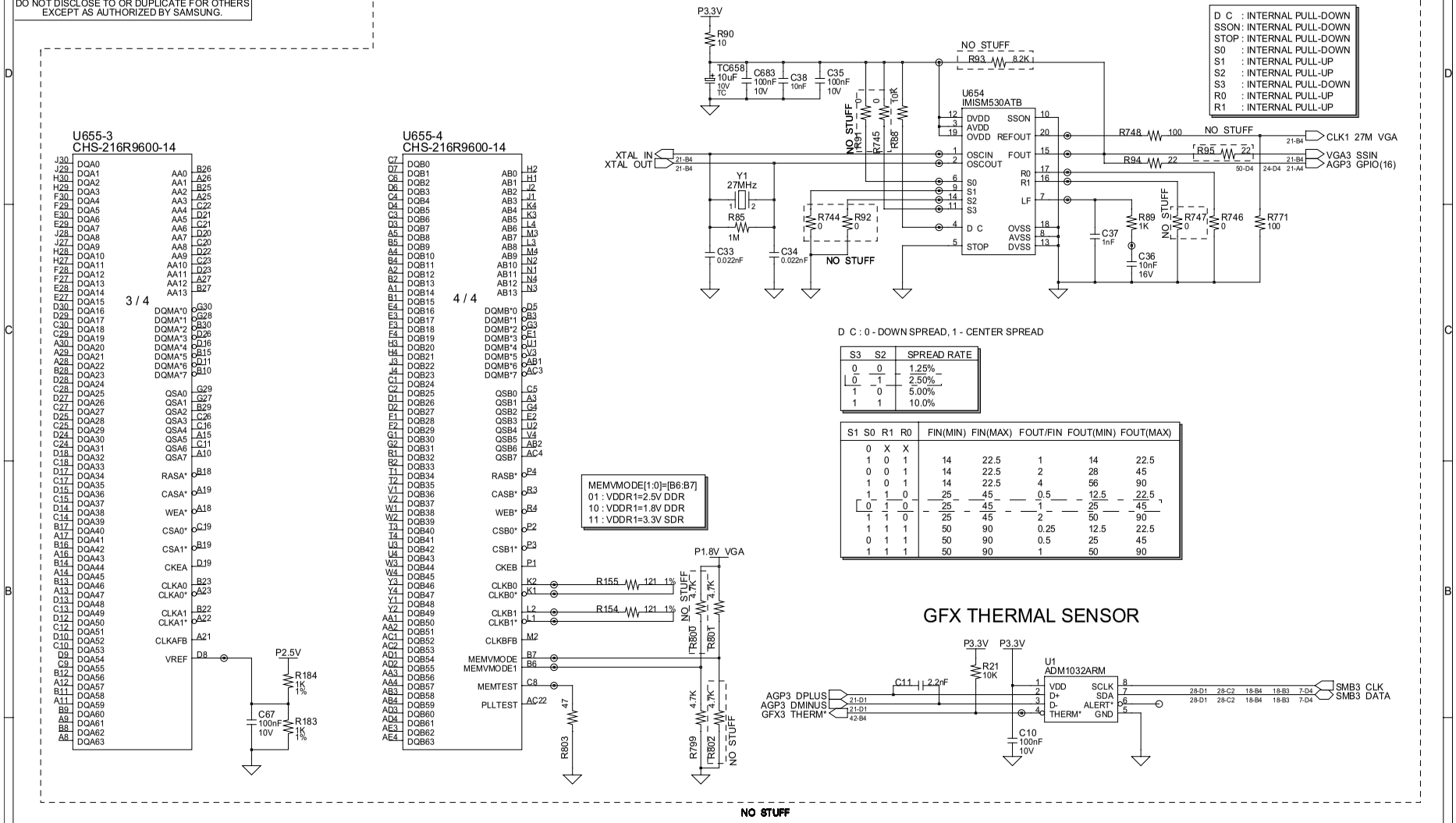

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	GFX CONTROLLER (3/3)	PART NO.: BA41-00478A
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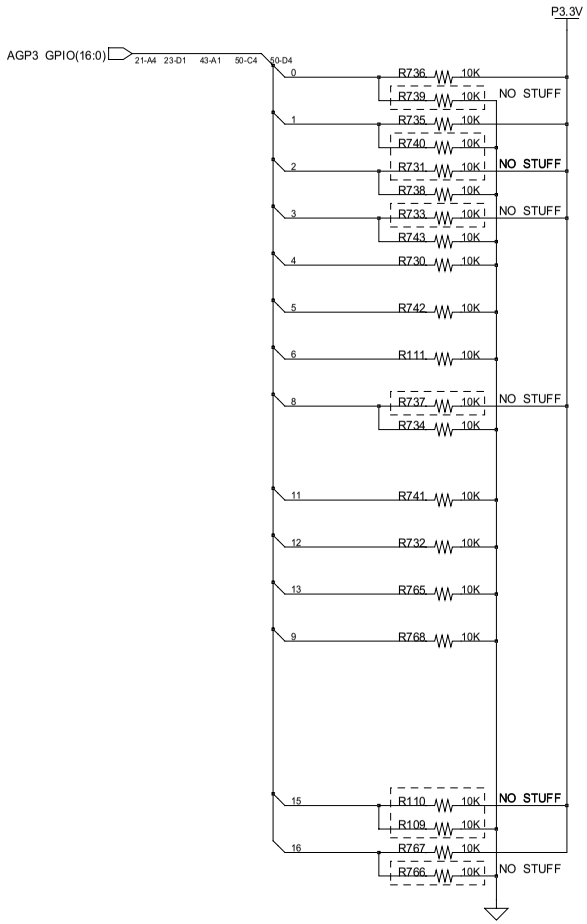

AGPFBSKEW [1:0]	AGP 1X CLOCK FEEDBACK PHASE ADJUSTMENT WRT REFCLK (CPU CLK) 00 : REFCLK SLIGHTLY EARLIER THAN FEEDBACK 01 : REFCLK 1 TAP LATER THAN FEEDBACK 10 : REFCLK 1 TAP EARLIER THAN FEEDBACK 11 : REFCLK 2 TAPS EARLIER THAN FEEDBACK CLOCK (DEFAULT)
X1CLK SKEQ [3:2]	CLOCK PHASE ADJUSTMENT BETWEEN X1CLK AND X2CLK 00 : 0 TAP DELAY (DEFAULT) 01 : 1 TAP DELAY 10 : 2 TAPS DELAY 11 : 3 TAPS DELAY
BUSCFG [6:4]	CONTROLS BUS TYPE, CLK PLL SELECT, AND IDSEL AGP8X_DETb / BUSCFG[2:0] / AGPMODE / SIGNALING / IDESEL 0 / 000 / AGP8X / 0.8V / AD16 (DEFAULT) 0 / 001 / AGP8X / 0.8V / AD17 0 / 010 / AGP4X / 0.8V / AD16 0 / 011 / AGP4X / 0.8V / AD17 1 / 000 / AGP4X / 1.5V / AD16 1 / 001 / AGP4X / 1.5V / AD17
ID DISABLE [8]	IN A SYSTEM WITH TWO GRAPHICS CHIPS, ONE ON THE MOTHERBOARD, THE OTHER ON ADD-IN CARD, THIS STRAP CAN BE USED TO DISABLE ONE OF THE TWO THROUGH A JUMPER. 0 : NOMAL OPERATION (DEFALULT) 1 : SHUTS THE CHIP DOWN BY NOT RESPONDING TO ANY CONFIG CYCLES.
ROMIDCFG [9, 13:11]	IF NO ROM ATTACHED, CONTROLSS CHIP ID'S. IF ROM ATTACHED, IDENTIFIES ROM TYPE. 0X0X : NO ROM, CHG ID=0 (NOTE : X=DON'T CARE) (DEFAULT) 0X1X : NO ROM, CHG ID=1 (NOTE : X=DON'T CARE) 1000 : PARALLEL ROM, CHIP ID'S FROM ROM 1001 : 1M SERIAL AT25F1024 ROM (ATMEL) 1010 : 1M SERIAL AT45DB011 ROM (ATMEL) 1011 : 1M SERIAL M25P10 ROM (ST) 1100 : 512K SERIAL M25P05 ROM (ST) 1101 : 1M SERIAL SST45LF010 ROM (SST) 1M SERIAL W45B512 ROM (WINBOND) 512K SERIAL W45B012 ROM (WINBOND) 1110 : 1M SERIAL SST25VF010 ROM (SST) 512K SERIAL SST25VF512 ROM (SST) 1111 : 1M NX25F011B ROM (NEXFLASH) CHIP IDS CHIP ID IS BASED ON THE BONDING OPTION AND CHG ID STRAP CHG ID=ROMIDCFG(0)=GPIO(12) 0 : DEFAULT SETTINGS 1 : CHANGE ID
POWERPLAY [15]	SWITCH EXTERNAL REGULATOR BETWEEN HIGH AND LOW CORE VOLTAGE 0 : SET HIGHER CORE VOLTAGE (VDDC=1.2V) (DEFAULT) 1 : SET LOWER CORE VOLTAGE (VDDC=1.0V)
EXTERNAL SPREAD SPECTRUM [16]	SPREAD SPECTRUM CLOCK INPUT FOR MEMORY CLOCK AND/OR ENGINE CLOCK REQUIRES SPREAD VERSION OF 27MHZ

NO STUFF

ALL COMPONENTS ON THIS PAGE
ARE USED ONLY FOR M11 CSP

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	GFX STRAPS	PART NO.: BA41-00478A
MODULE CODE:	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 24 OF 51	

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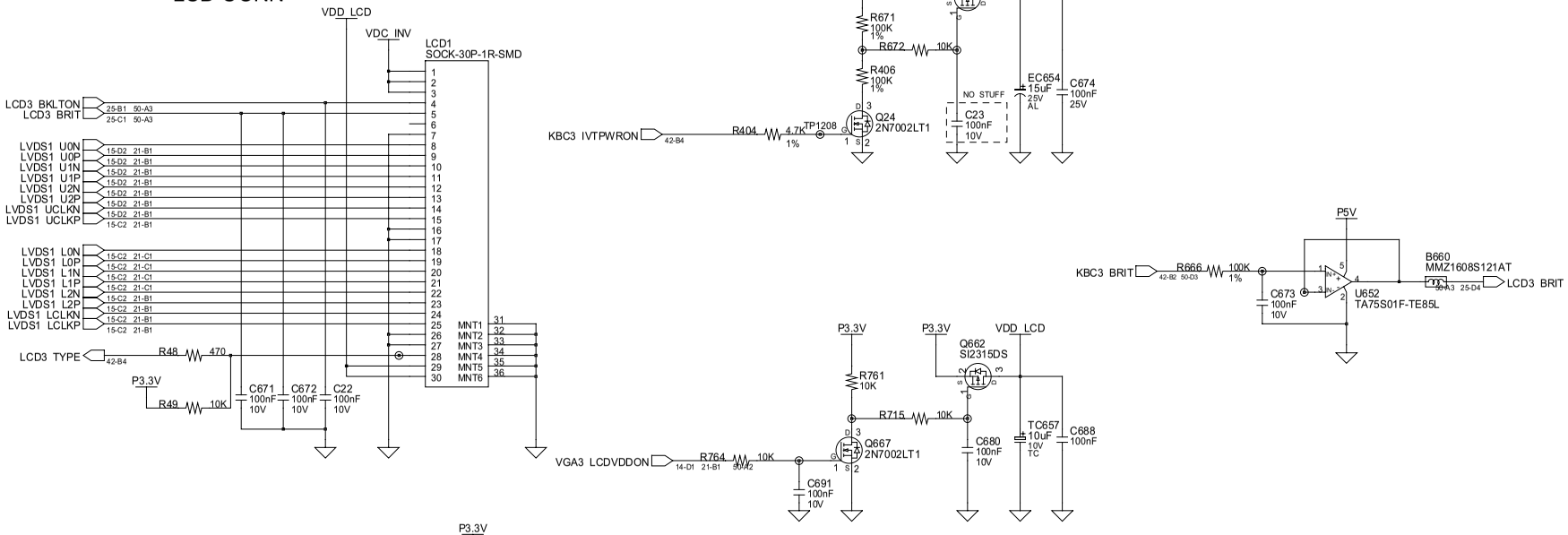
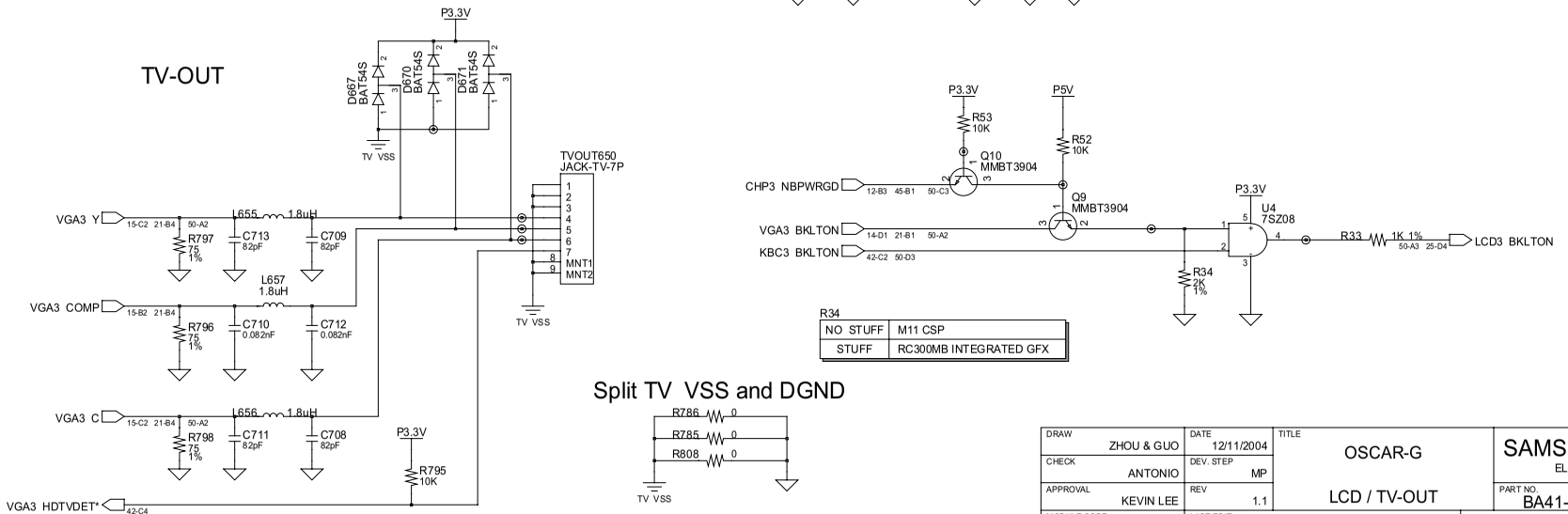
LCD CONN



TV-OUT



R34	
NO STUFF	M11 CSP
STUFF	RC300MB INTEGRATED GFX

Split TV VSS and DGND

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	LCD / TV-OUT	PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 25 OF 51	

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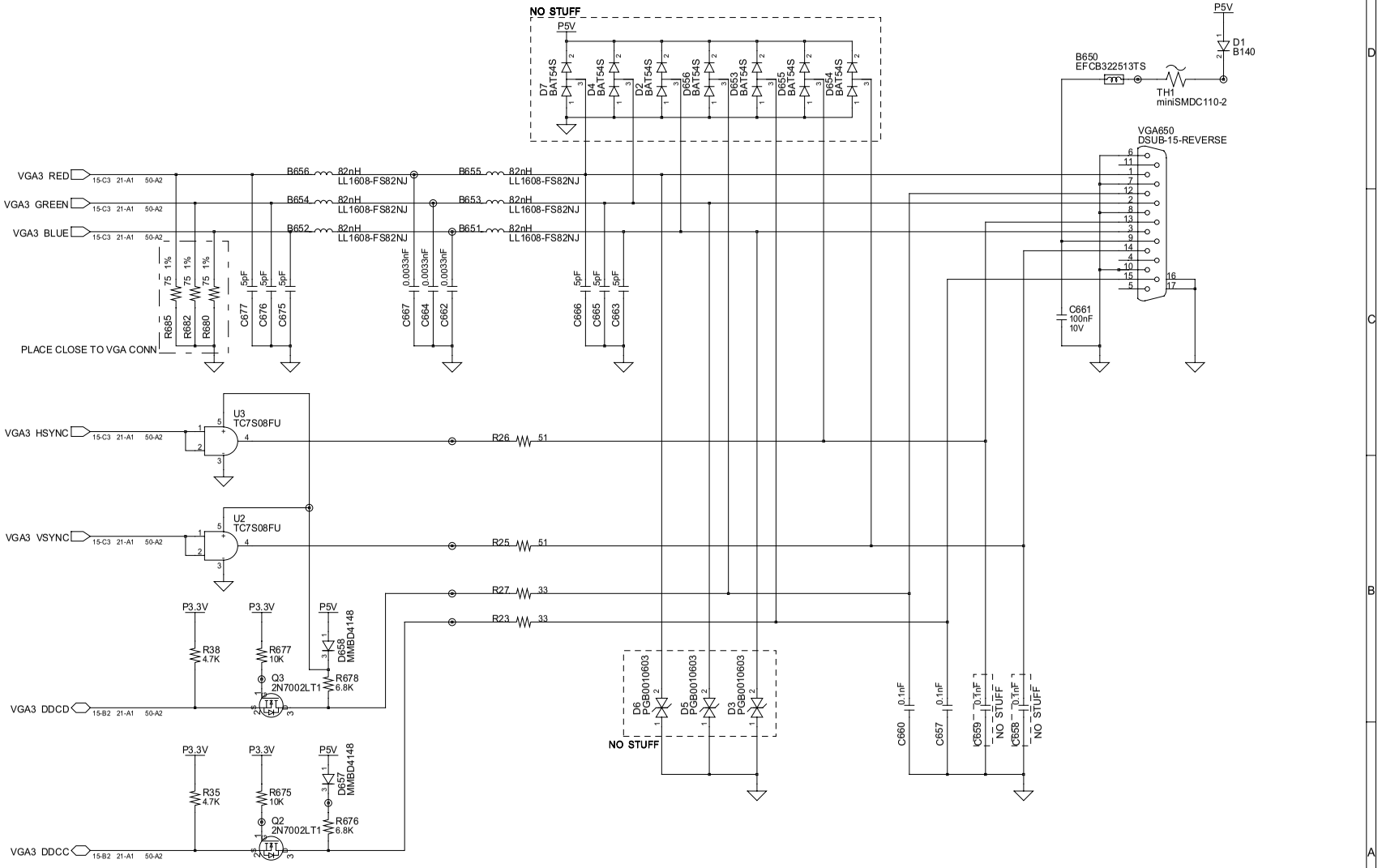

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP	CRT CONNECTOR	
APPROVAL: KEVIN LEE	REV: 1.1		PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 26 OF 51	

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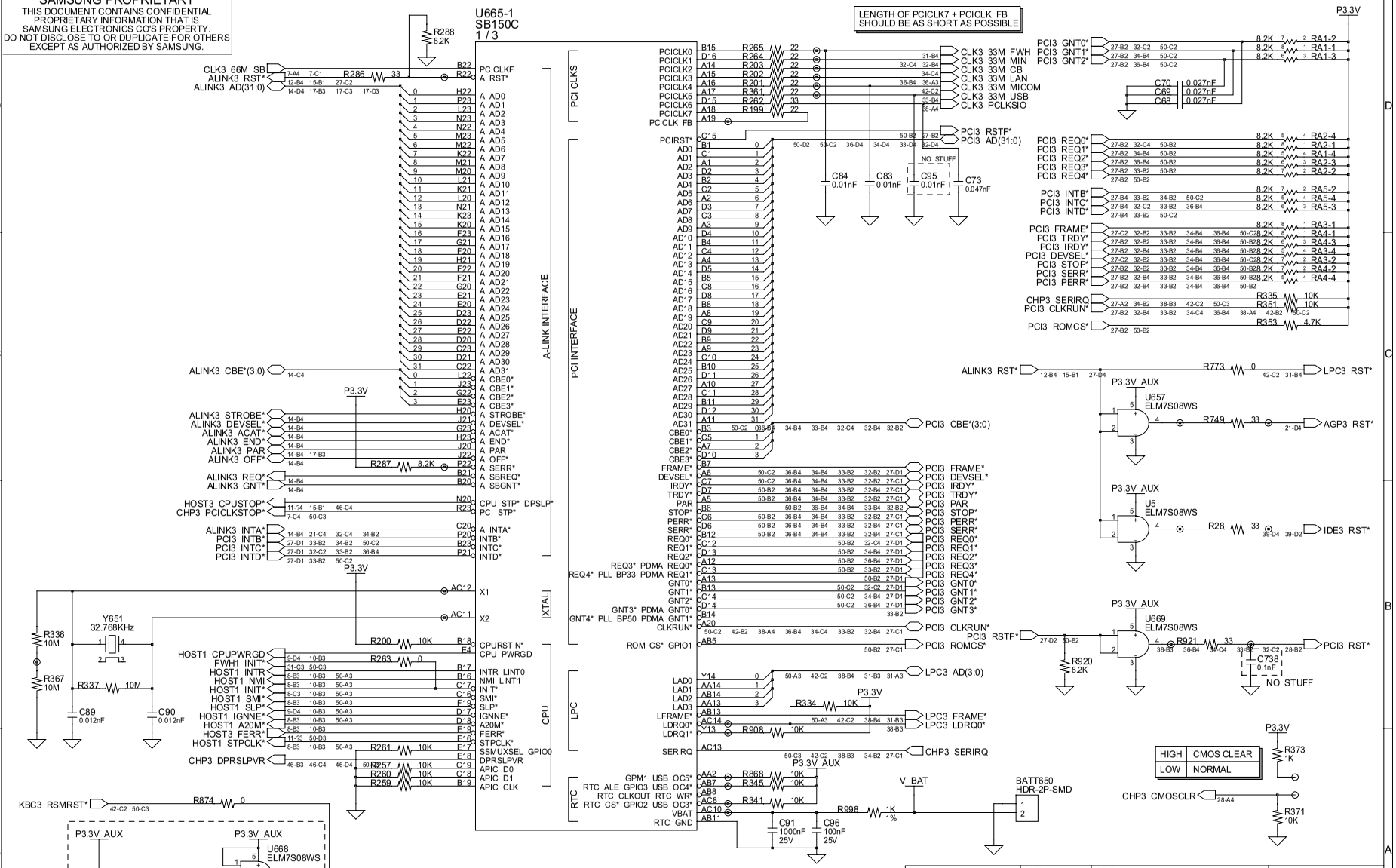

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP	SOUTH BRIDGE (1/3)	
APPROVAL: KEVIN LEE	REV: 1.1		PART NO. BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM		PAGE 27 OF 51

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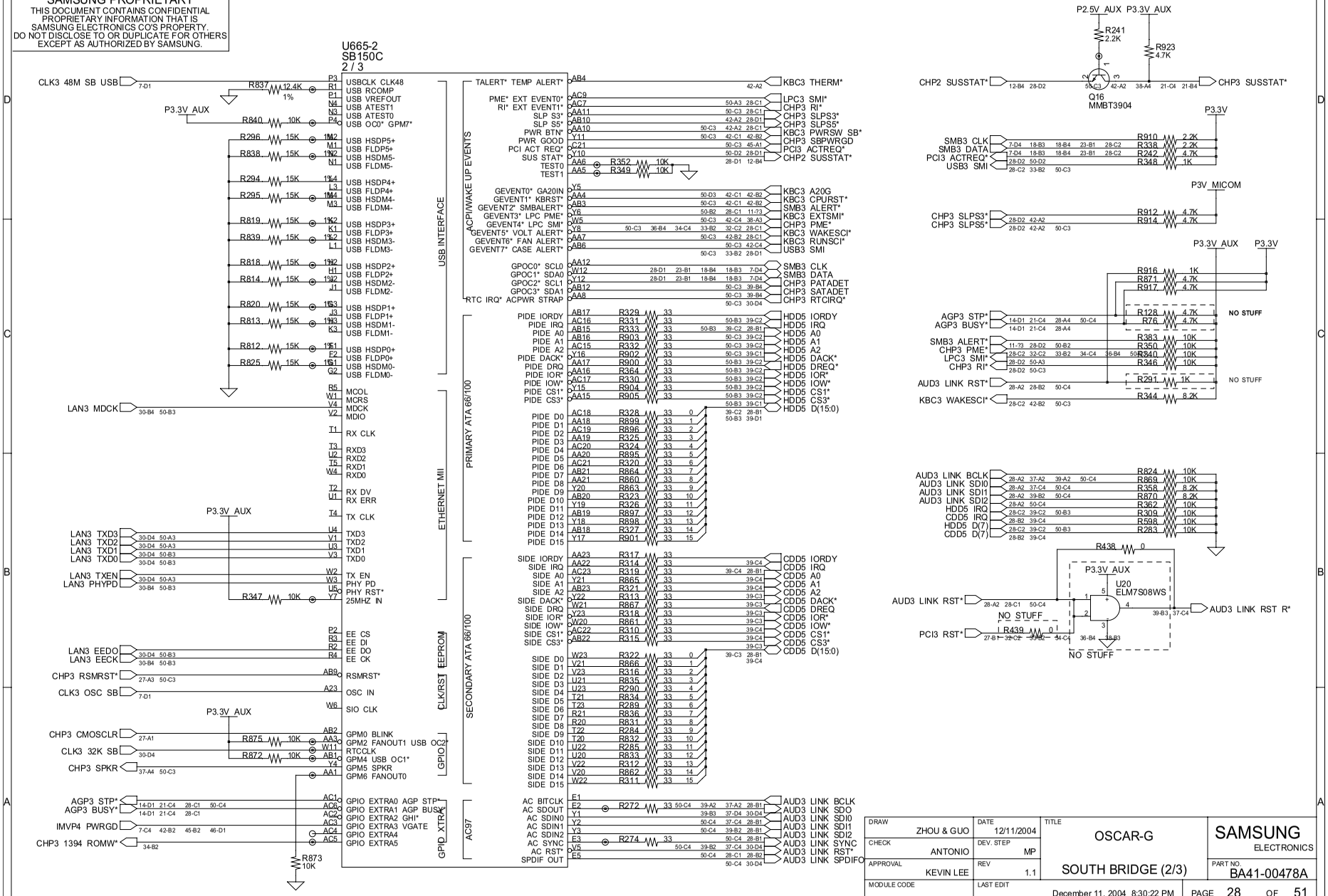

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP	SOUTH BRIDGE (2/3)	
APPROVAL: KEVIN LEE	REV: 1.1		PART NO. BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 28 OF 51	

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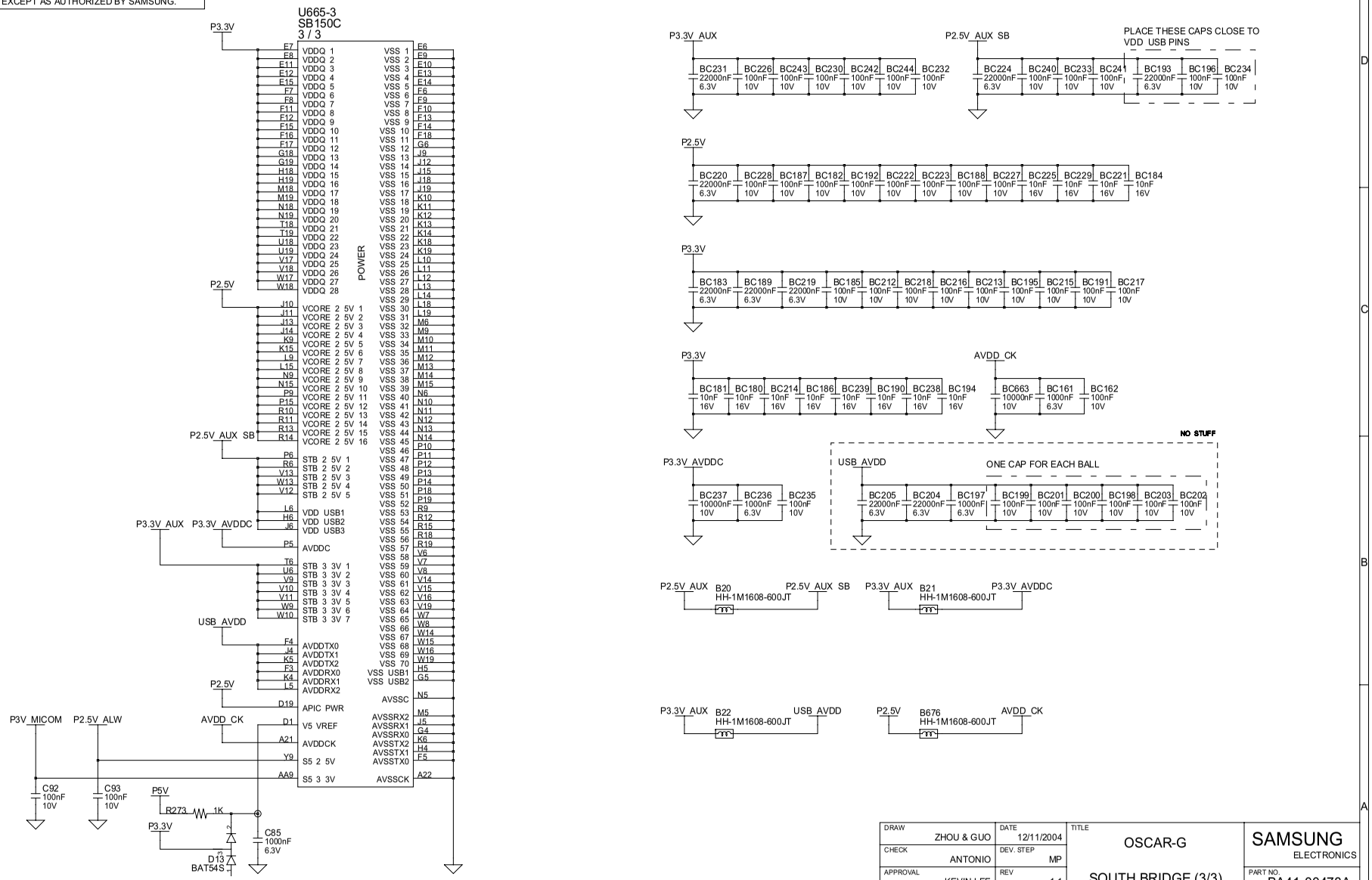

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	SOUTH BRIDGE (3/3)	PART NO.: BA41-00478A
MODULE CODE:	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 29 OF 51	

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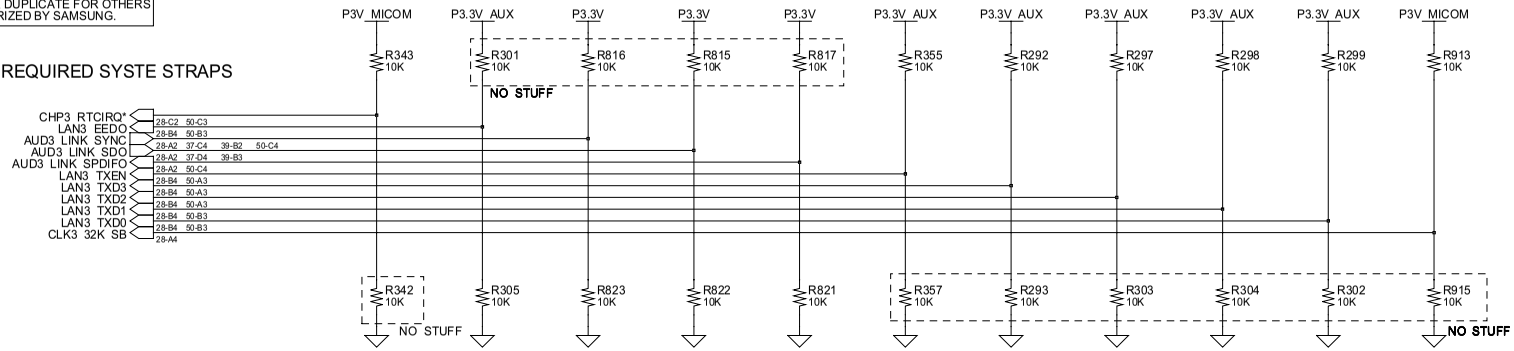
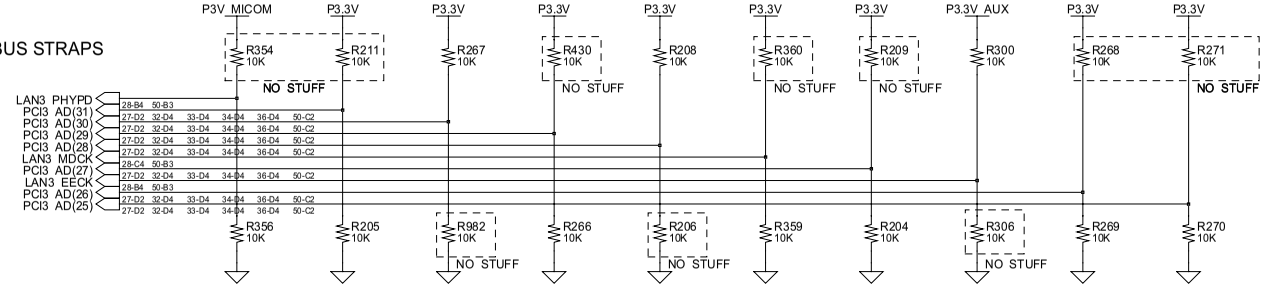
REQUIRED SYSTE STRAPS



	RTCIRQ	EEDO	AC_SYNC	AC_SDOUT	SPDIF_OUT	TX_EN	ETHERNET TXD[3:0]	32KHZ_S5
STRAP HIGH	MANUAL PWR ON (DEFAULT)	USE DEBUG STRAPS	INIT ACTIVE HIGH (AMD)	33MHZ NB BUS	SIO 24MHZ	DISABLE CPU FREQ SETTING (DEFAULT)	PROCESSOR FREQUENCY MULTIPLIER	32KHZ OUTPUT FROM SB200 (INT RTC) (DEFAULT)
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS (DEFAULT)	INIT ACTIVE LOW (PIII) (DEFAULT)	HI SPEED ALINK (DEFAULT)	SIO 48MHZ (DEFAULT)	ENABLE CPU FREQ SETTING		32KHZ INPUT TO SB200 (EXT RTC)

DEBUS STRAPS



	PHY_PD	PCI_AD(31)	PCI_AD(30)	PCI_AD(29)	PCI_AD(28)	MDCK	PCI_AD(27)	EECK	PCI_AD(26)	PCI_AD(25)
STRAP HIGH	USE SHORT RESET	PLL CHARGE PUMP CTRL BIT 1 HI	PLL CHARGE PUMP CTRL BIT 0 HI (DEFAULT)	PLL VCO CTRL BIT 1 HI	PLL VCO CTRL BIT 0 HI (DEFAULT)	USE 4K EEPROM	BYPASS PCI PLL	0 0 : FWH 0 1 : LPC ROM * 1 0 : LPC ROM II (PMC LPC TYPE) 1 1 : XBUS PCI ROM		BYPASS IDE PLL A11/A12 ONLY
STRAP LOW	USE LONG RESET (DEFAULT)	PLL CHARGE PUMP CTRL BIT 1 LO (DEFAULT)	PLL CHARGE PUMP CTRL BIT 0 LO	PLL VCO CTRL BIT 1 LO (DEFAULT)	PLL VCO CTRL BIT 0 LO	USE 16K EEPROM (DEFAULT)	USE PCI PLL (DEFAULT)			USE IDE PLL FOR A21+SB (DEFAULT)

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	SOUTH BRIDGE STRAPS	PART NO.: BA41-00478A
MODULE CODE:	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 30 OF 51	

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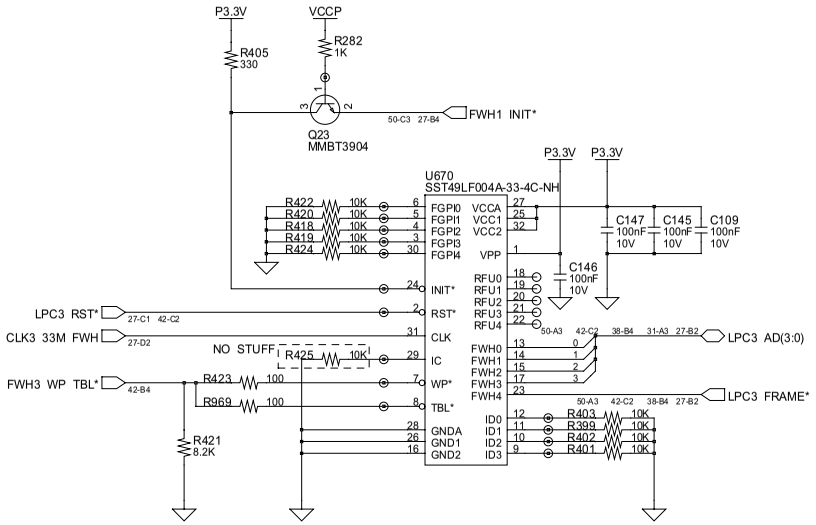
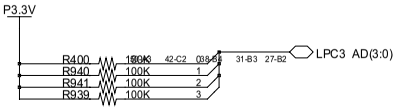
NOTE:
SST49LF004A support FWH operational mode
SST49LF040 support LPC operational mode



Use PMC Pm49FL004 LPC Flash ROM, P/N 1107-001288



02 VERIFY REAL MODE	66 CONFIGURE ADVANCE CACHE REGISTERS
03 DISABLE NMI	6A DISPLAY EXTERNAL CACHE SIZE
04 GET CPU TYPE	6C DISPLAY SHADOW MESSAGE
06 INITIALIZE SYSTEM H/W	6E DISPLAY NON-DISPOSABLE SEGMENT
08 INITIALIZE CHIPSET REGISTERS	70 DISPLAY ERROR MESSAGE
09 SET IN POST FLAG	72 CHECK FOR CONFIGURATION ERROR
0A INIT CPU REGISTERS	74 TEST REAL-TIME CLOCK
0B CPU CACHE ON	76 CHECK FOR KEYBOARD EERROR
0C INITIALIZE CACHE TO POST	7C SETUP HARDWARE INTERRUPT VECTOR
0E INITIALIZE I/O VALUE	7E TEST COPROCESSER IF PRESENT
0F ENABLE THE L-BUS IDE	80 DISABLE ON-BOARD I/O PORT
10 INITIALIZE POWER MANAGER	82 DETECT AND INSTALL EXT. RS232C
11 LOAD ALTERNATE REGISTERS	84 DETECT AND INSTALL EXT. PARALLEL
13 PCI BUS MASTER RESET WITH INITIAL POST VALUE	86 RE-INITIALIZE ON-BOARD I/O PORT
14 INITIALIZE KEYBOARD CONTROLLER	88 INITIALIZE BIOS DATA ROM
16 CHECK CHECKSUM	8A INITIALIZE EXTENDED BIOS DATA AREA
18 INITIALIZE 8254 TIMER	8C INITIALIZE FDD CONTROLLER
1A INITIALIZE 8237 DMA CONTROLLER	9A SHADOW OPTION ROMS
1C RESET INTERRUP CONTROLLER	9C SETUP POWER MANAGEMENT
20 TEST DRAM REFRESH	9E ENABLE H/W INTERRUPT
22 TEST 8742 KEYBOARD CONTROLLER	A0 SET TIME OF DAY
24 SET ES SEGMENT REGISTERS TO 4GB	A4 INITIALIZE TYPEMATIC RATE
26 ENABLE A20	A8 ERASE F2 PROMPT
28 AUTO SIZING DRAM	AA SCAN FOR F2 KEY STROKE
32 COMPUTE THE CPU SPEED	AC ENTER SETUP
34 TEST CMOS RAM	AE CLEAR IN POST FLAG
38 SHADOW SYSTEM BIOS ROM	B0 CHECK FOR ERRORS
3A AUTO SIZING CACHE	B2 POST DONE-PREPARE TO BOOT O/S
3C CONFIGURE ADVANCED CHIPSET REGISTERS	B4 ONE BEEP
3D LOAD ALTER REG. WITH CMOS VALUE	B6 CHECK PASSWORD (OPTION)
42 INITIALIZE INTERRUPT VECTOR	B7 ACPI INIT
44 INITIALIZE BIOS INTERRUPT	BA DMI INIT
46 CHECK ROM COPYRIGHT NOTICE	BE CLEAR SCREEN
47 INITIALIZE I20 SUPPORT IF INSTALLED	C0 TRY BOOT WITH INT19
48 CHECK VIDEO CONFIGURE AGAINST CMOS	D0 INTERRUPT HANDLER ERROR
49 INITIALIZE PCI BUS AND DEVICE	D2 UNKNOWN INTERRUPT ERROR
4A INITIALIZE ALL VIDEO BIOS ROM	D4 PENDING INTERRUPT ERROR
4C SHADOW VIDEO BIOS ROM	D6 SHUTDOWN 5
50 DISPLAY CPU TYPE AND SPEED	D8 SHUTDOWN ERROR
52 TEST KEYBOARD	DA EXTENDED BLOCK MOVE
54 SET KEYCLICK IF ENABLED	DC SHUTDOWN 10
56 ENABLE KEYBOARD	89 ENABLE NMI
58 TEST FOR UNEXPECTED INTERRUPTS	90 INITIALIZE HDD CONTROLLER
5A DISPLAY " PRESS ..... SETUP"	91 INITIALIZE LOCAL BUS HDD CONTROLLER
5C TEST RAM BETWEEN 512K AND 640K	92 JUMP TO USER PATCH 2
60 TEST EXTENDED MEMORY	94 DISABLE A20 ADDRESS LINE
62 TEST EXTENDED MEMORY ADDRESS LINE	96 CLEAR HUGE ES SEGMENT REG.
64 JUMP TO USER PATCH 1	98 SEARCH FOR OPTION ROMS

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	FWH	PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 31 OF 51	

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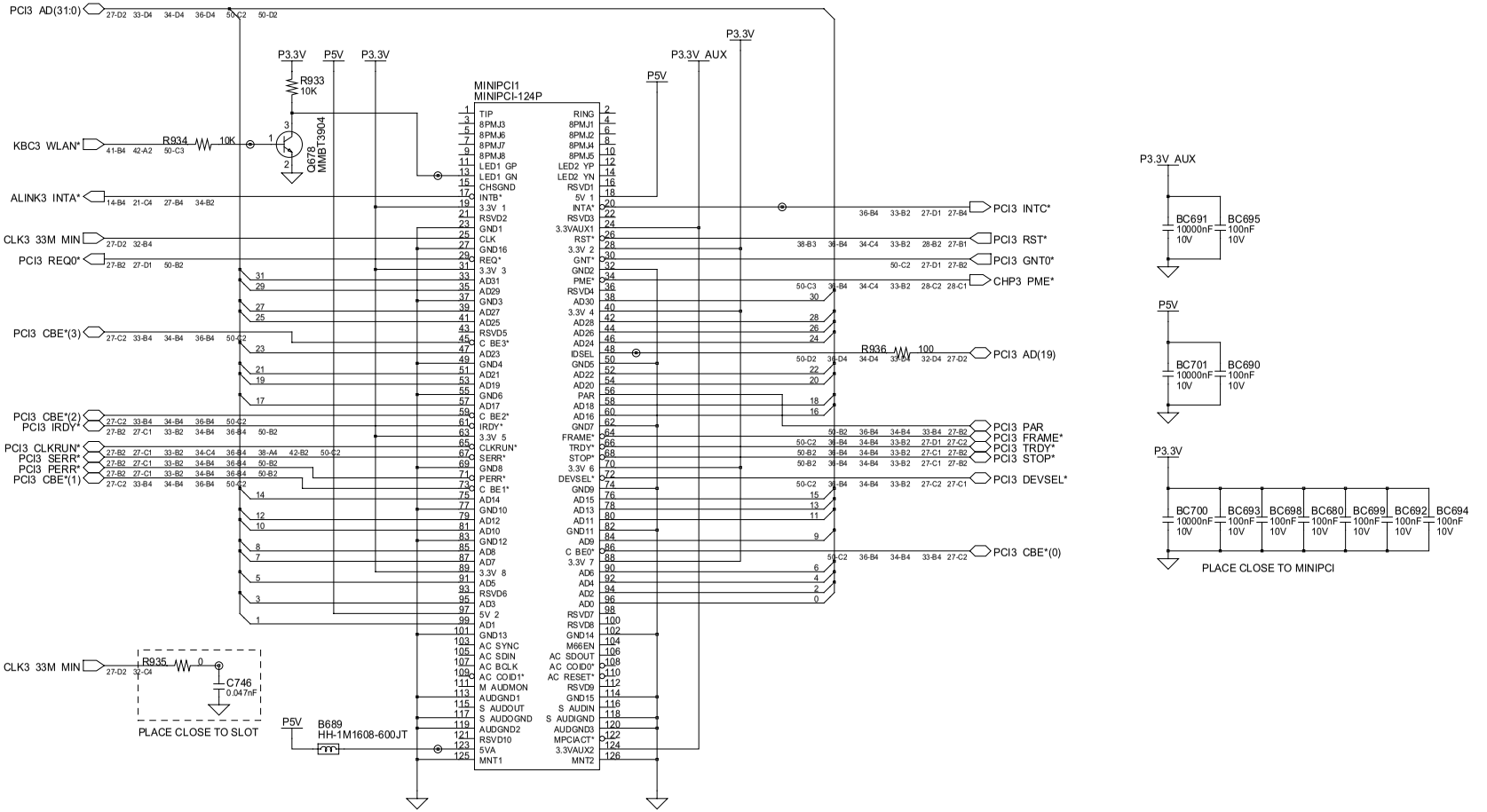

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	MINIPCI	PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 32 OF 51	

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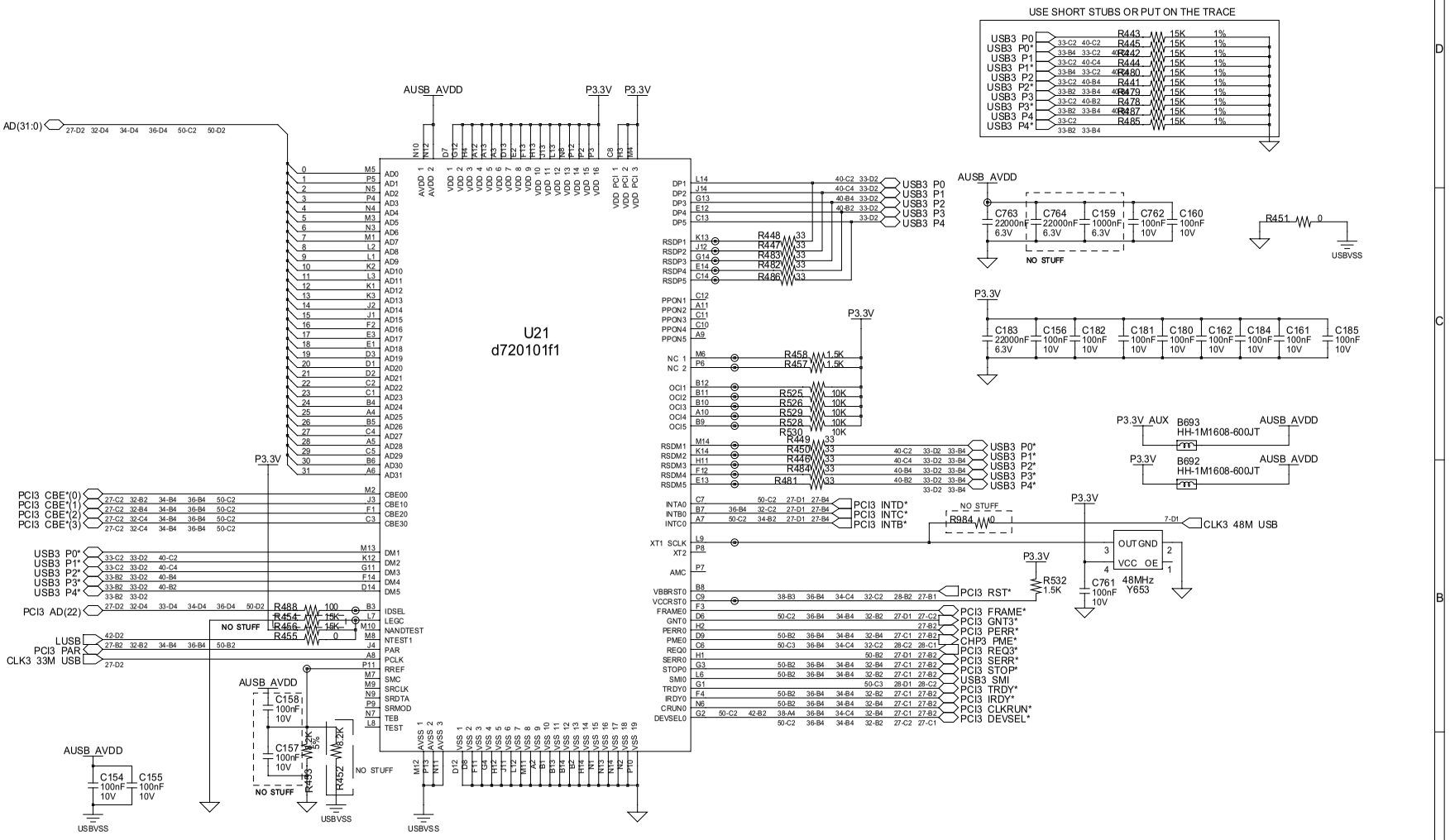

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	USB CONTROLLER	PART NO.: BA41-00478A
MODULE CODE:	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 33 OF 51	

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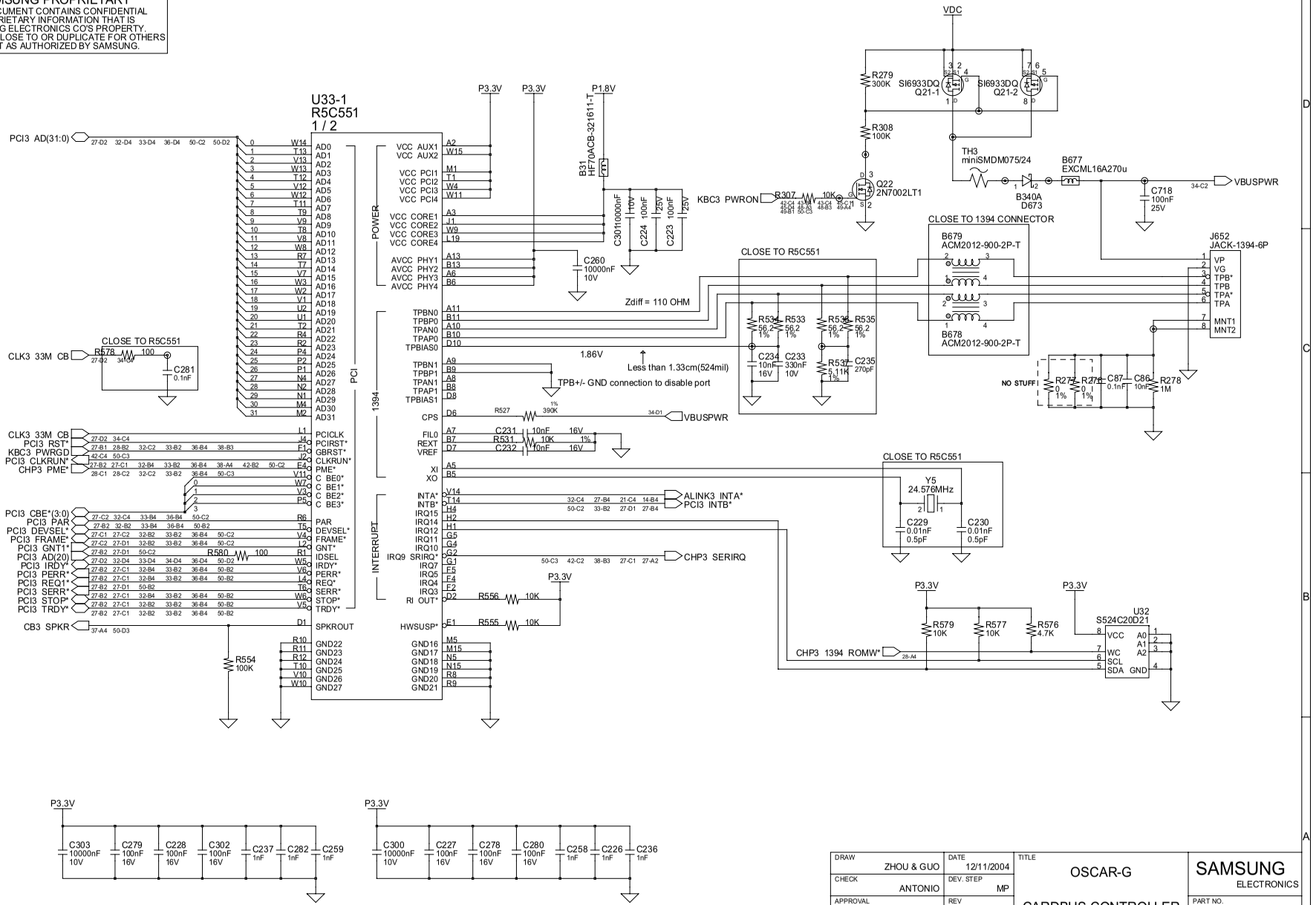

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	CARDBUS CONTROLLER	PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 34 OF 51	

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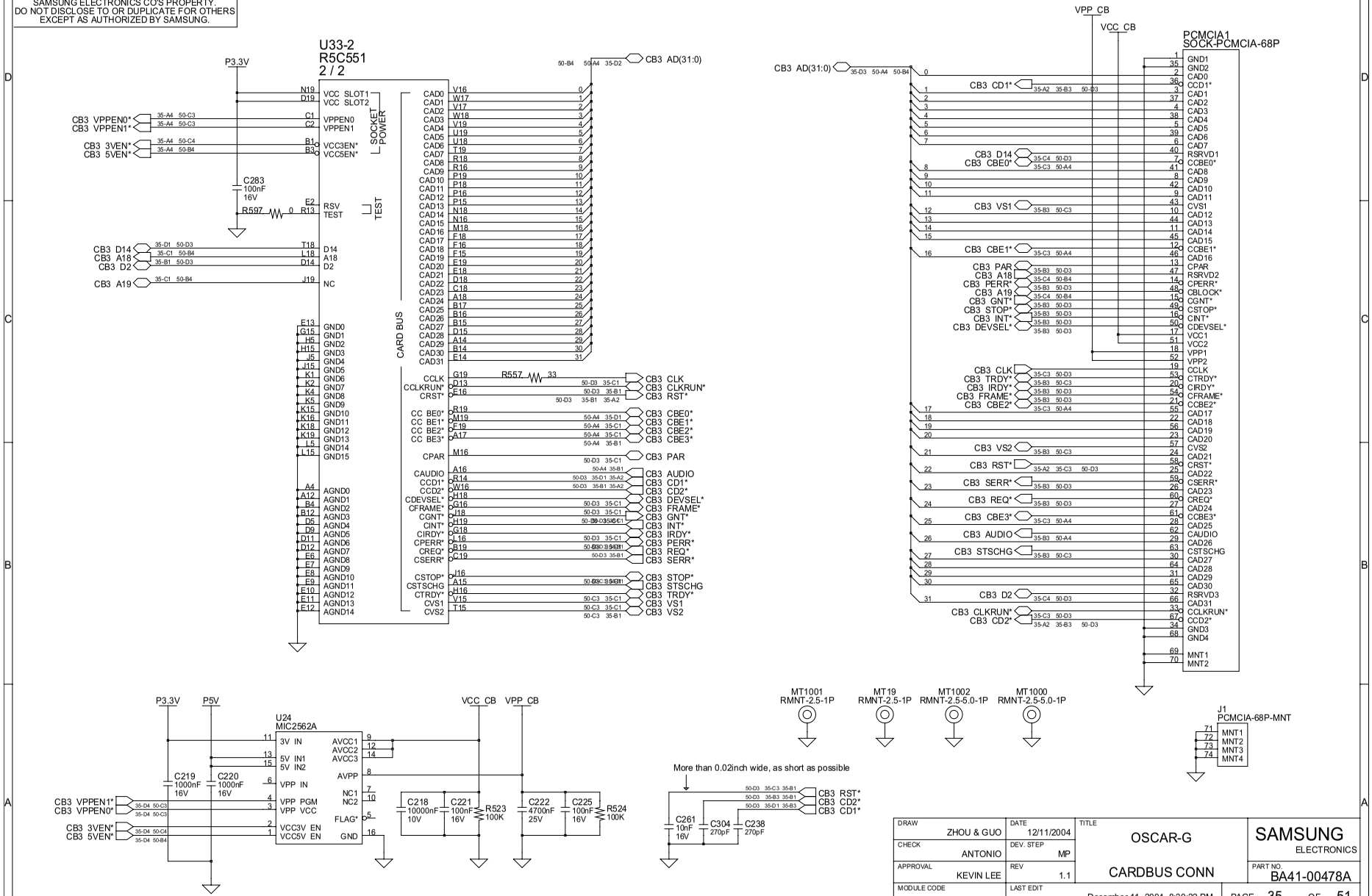

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	CARDBUS CONN	PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 35 OF 51	

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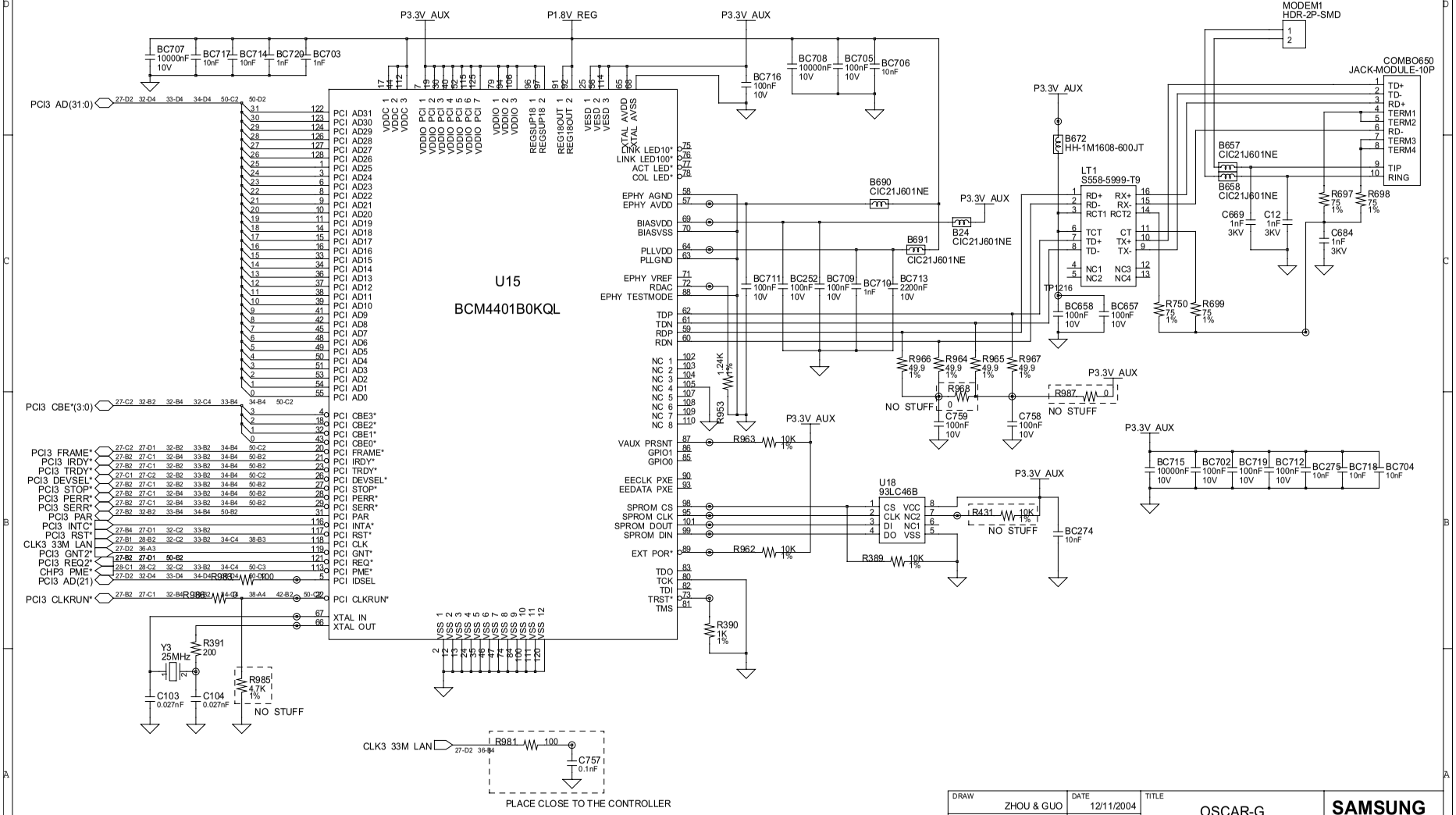

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP	LAN CONTROLLER	
APPROVAL: KEVIN LEE	REV: 1.1		PART NO. BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 36 OF 51	

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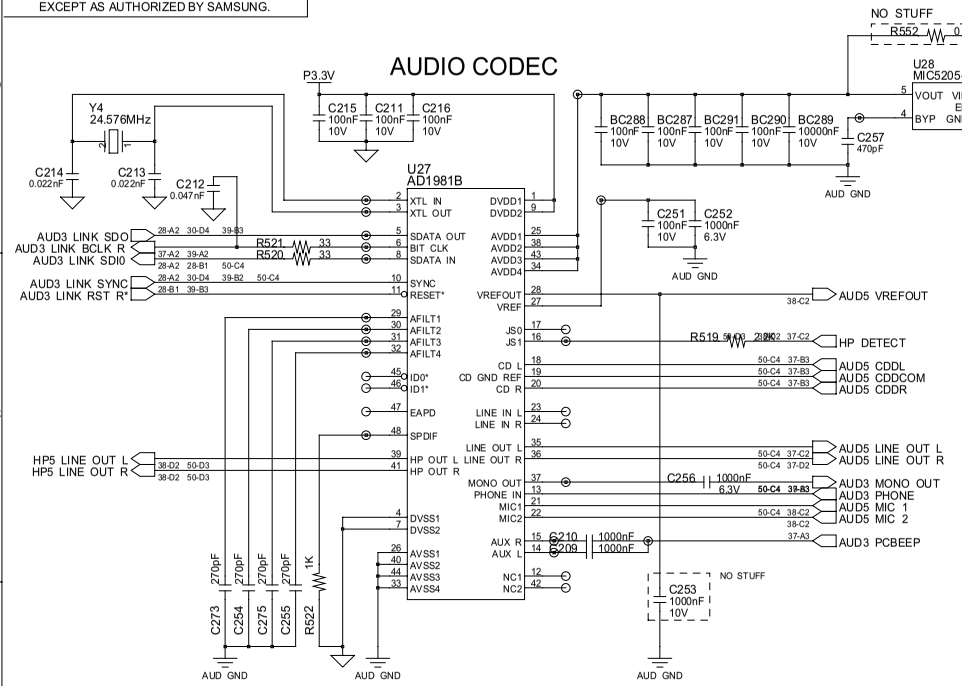
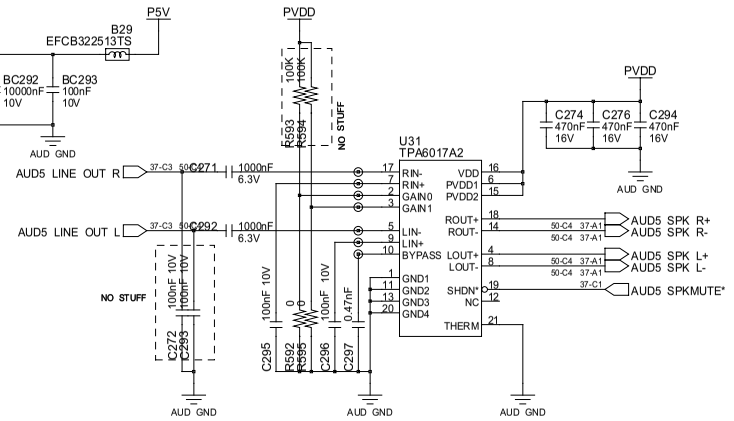
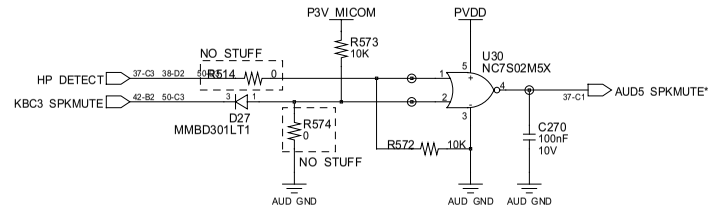
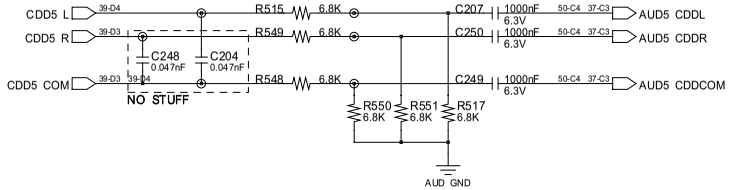
AUDIO CODEC

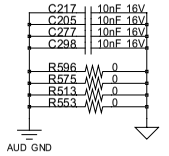


AUDIO AMP









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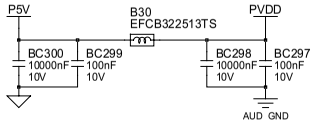
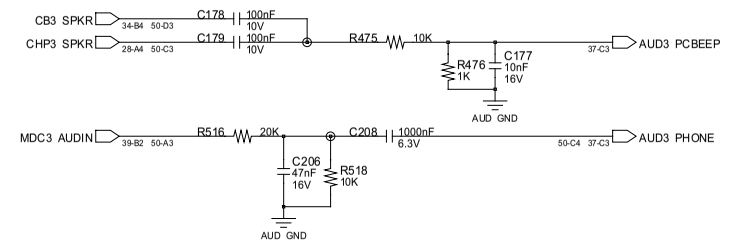
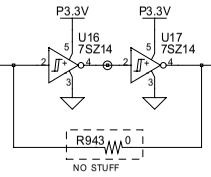
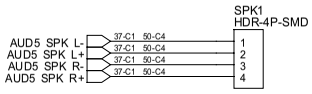






SPEAKER CONN



DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	AUDIO CODEC	PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 37 OF 51	

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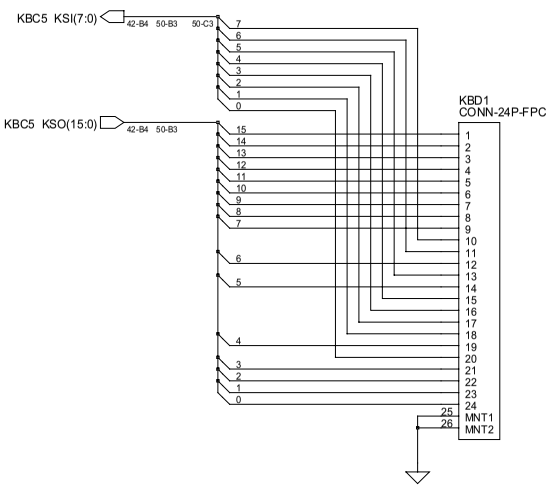
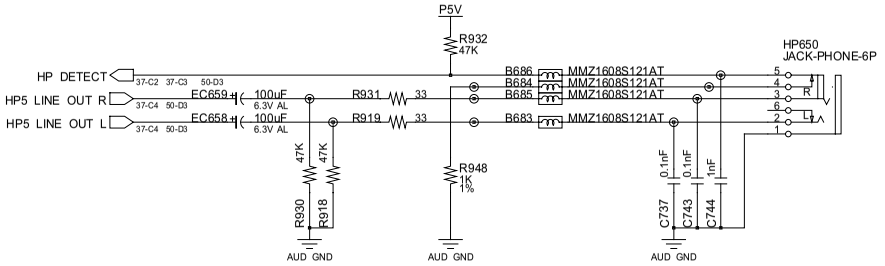
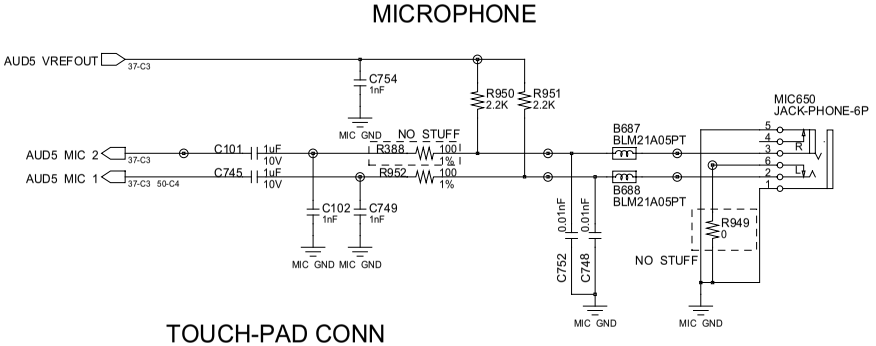
KBD CONN



HEADPHONE



MICROPHONE



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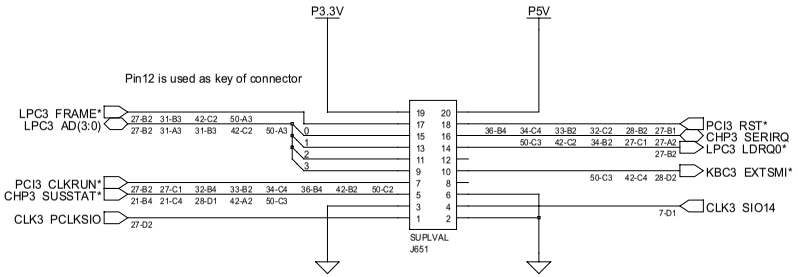
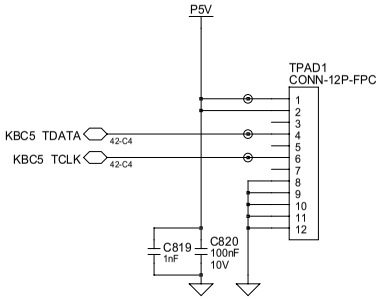
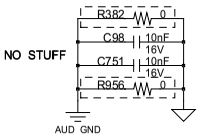
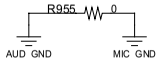


TOUCH-PAD CONN







DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	HP/MIC/KBD/TPUCH-PAD	PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 38 OF 51	

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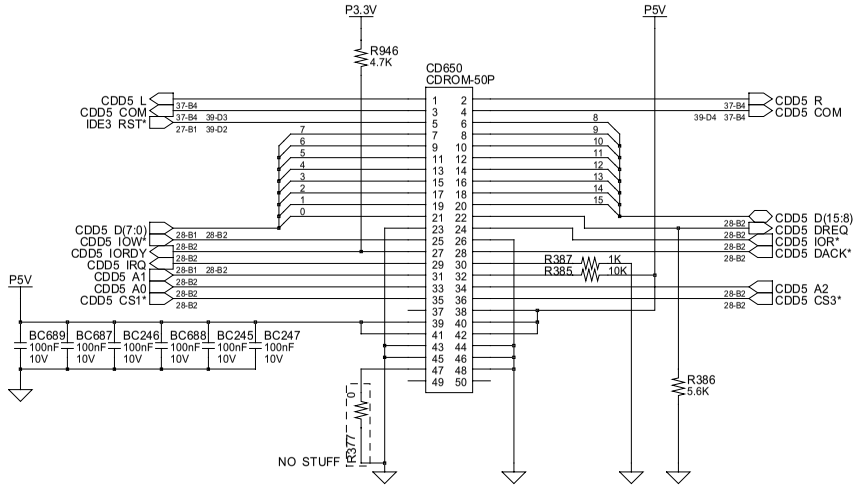
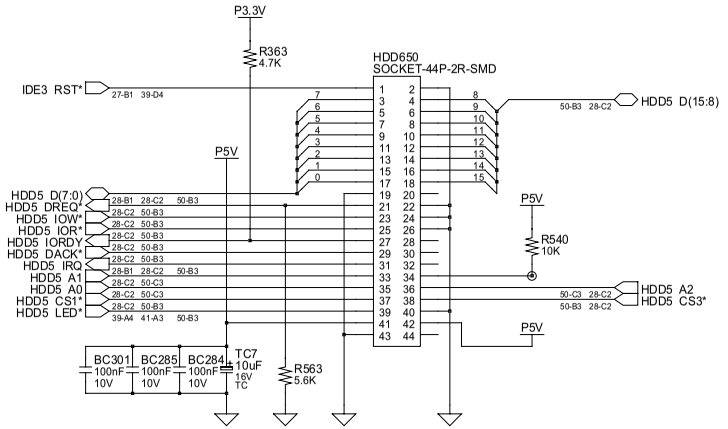
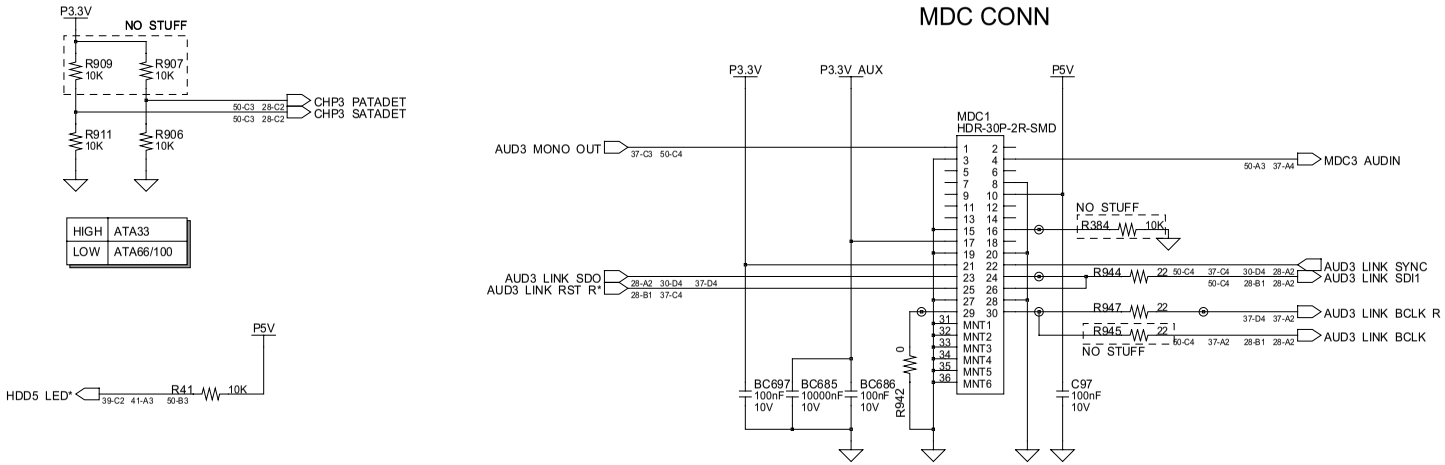
CD CONN



HDD CONN



MDC CONN



DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP	HDD / CD / MDC CONN	
APPROVAL: KEVIN LEE	REV: 1.1		PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM		PAGE 39 OF 51

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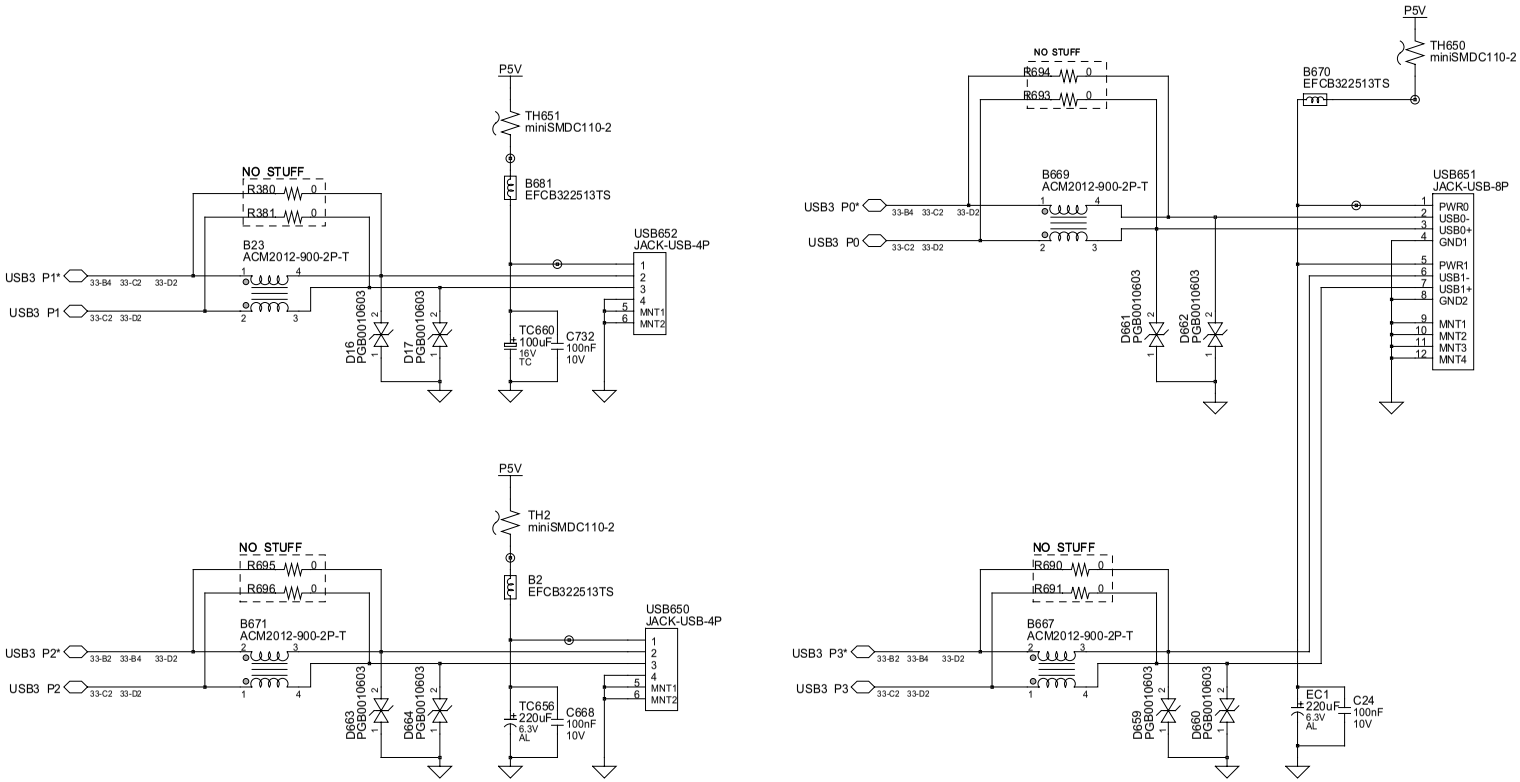

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	USB PORTS	PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM		PAGE 40 OF 51

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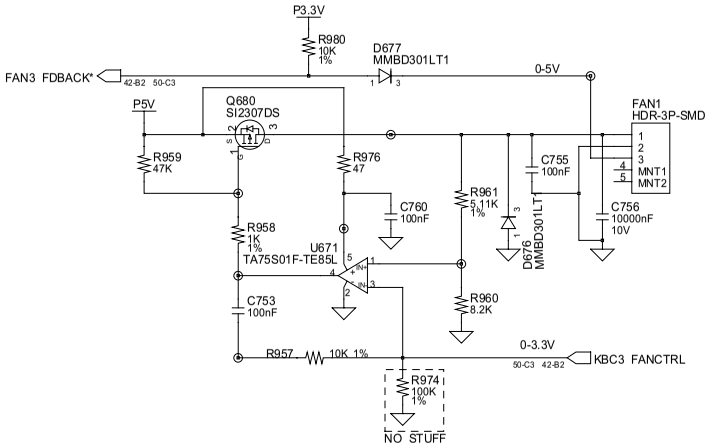
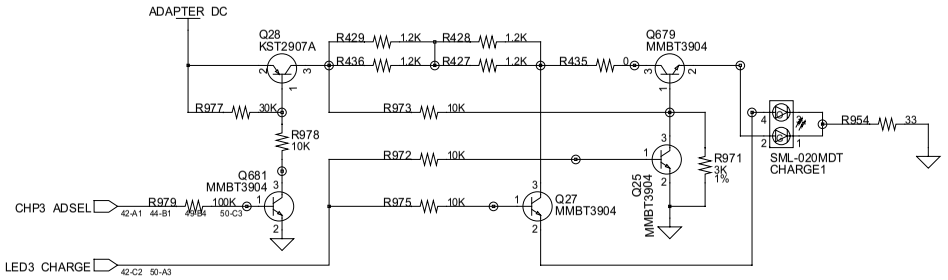
FAN HEADER

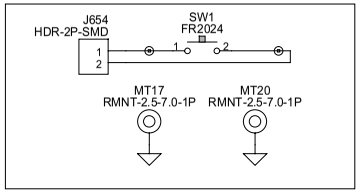


ADAPTER IN / CHARGER LED

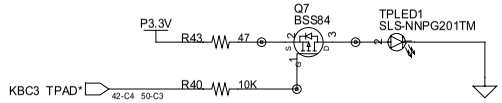


POWER SWITCH

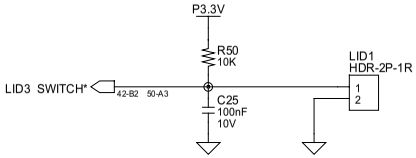
LID SWITCH B/D



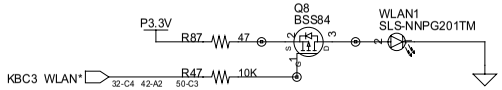
TOUCH-PAD ON/OFF LED



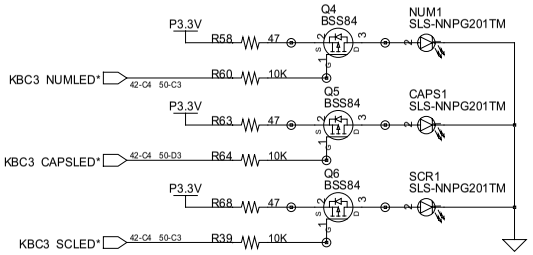
LID SIWTCH



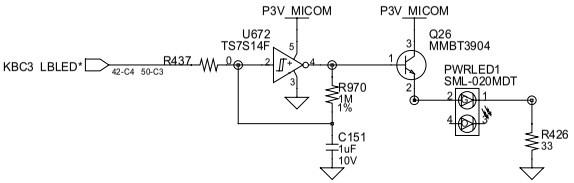
W-LAN ON/OFF LED



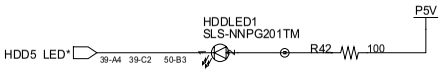
NUM / CAPS / SCROLL LOCK LED



POWER ON / LB LED



HDD LED



DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	FAN / LED / SWITCH	PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 41 OF 51	

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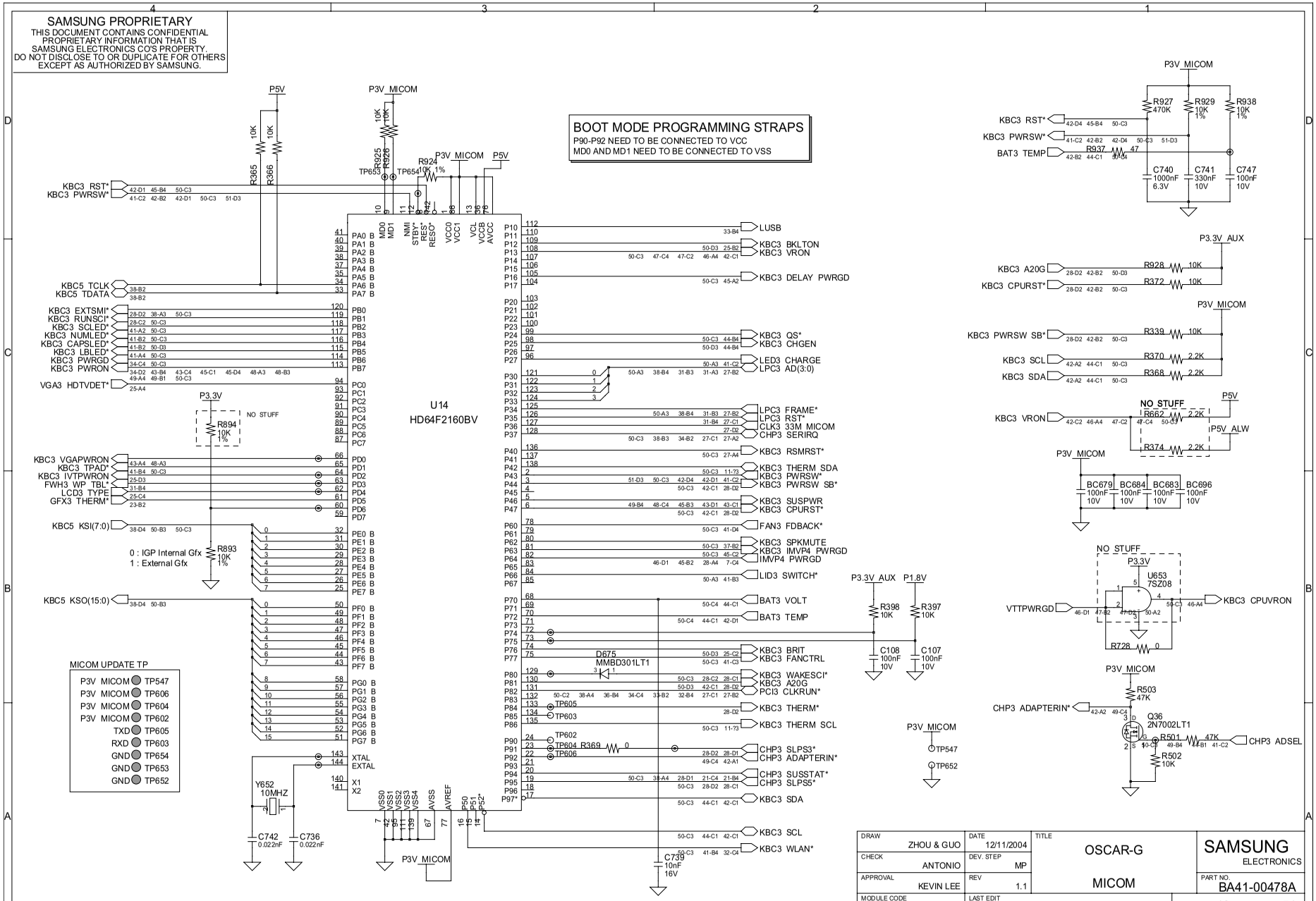

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G MICOM	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1		PART NO. BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM		PAGE 42 OF 51

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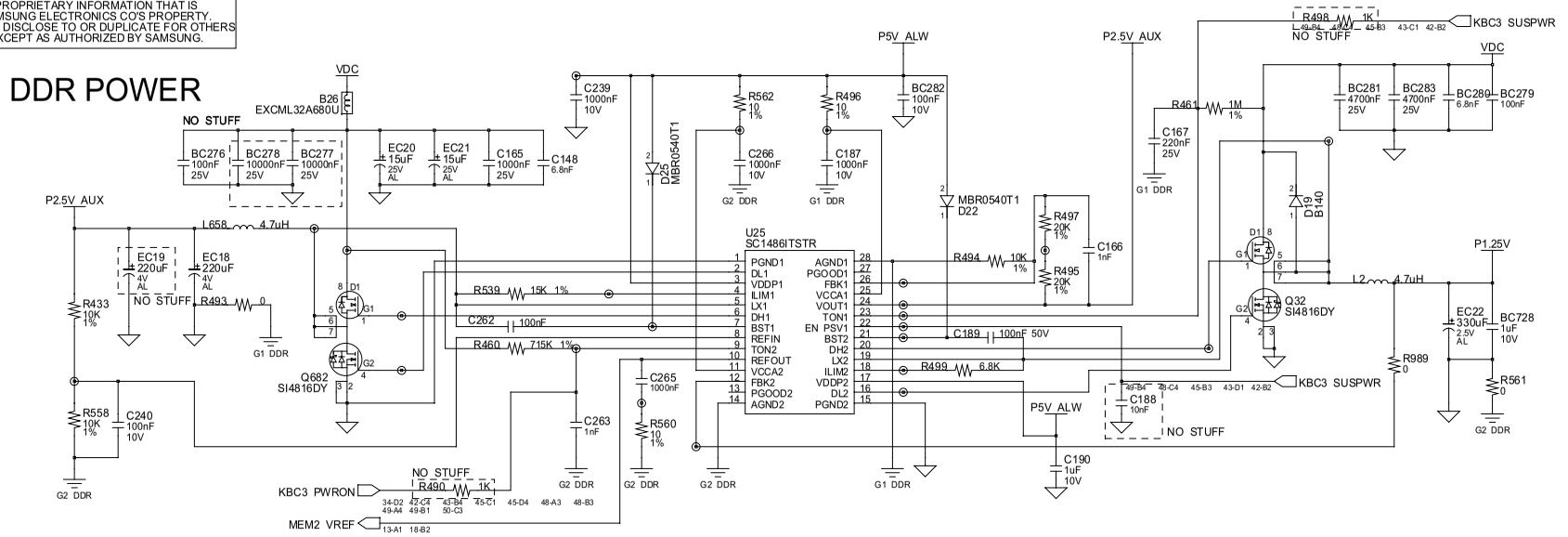
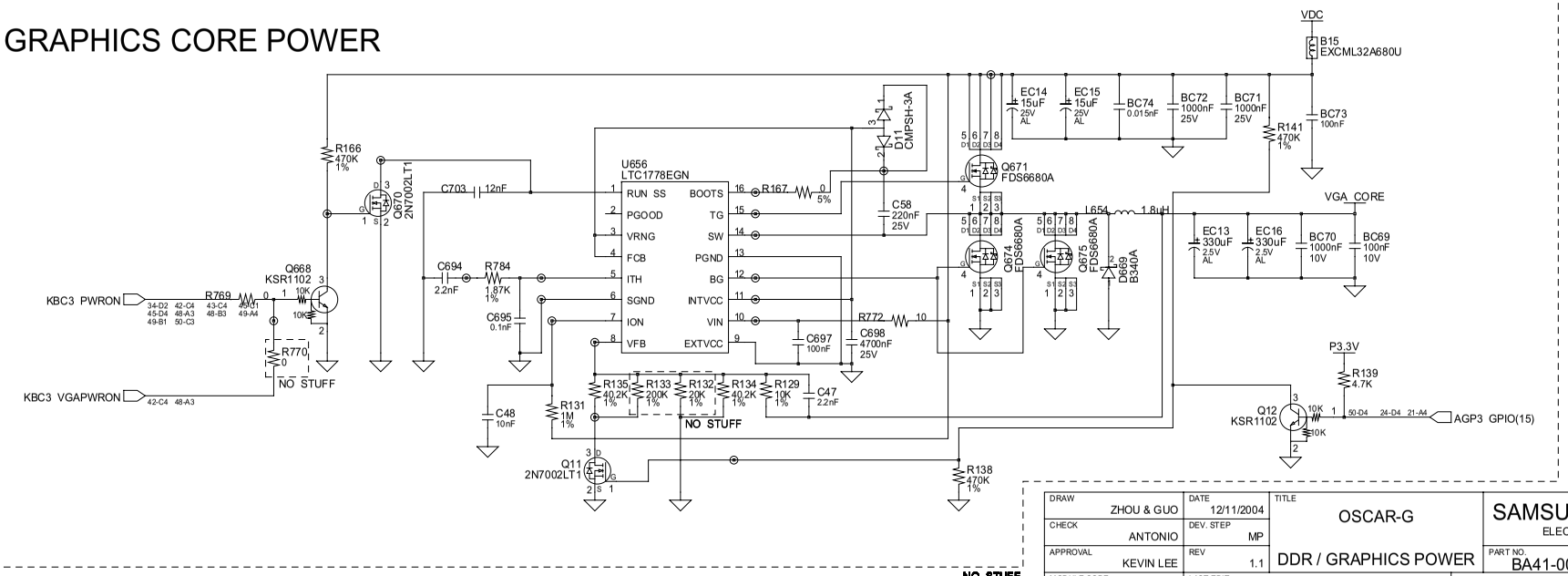
DDR POWER



GRAPHICS CORE POWER



DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	DDR / GRAPHICS POWER	PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 43 OF 51	

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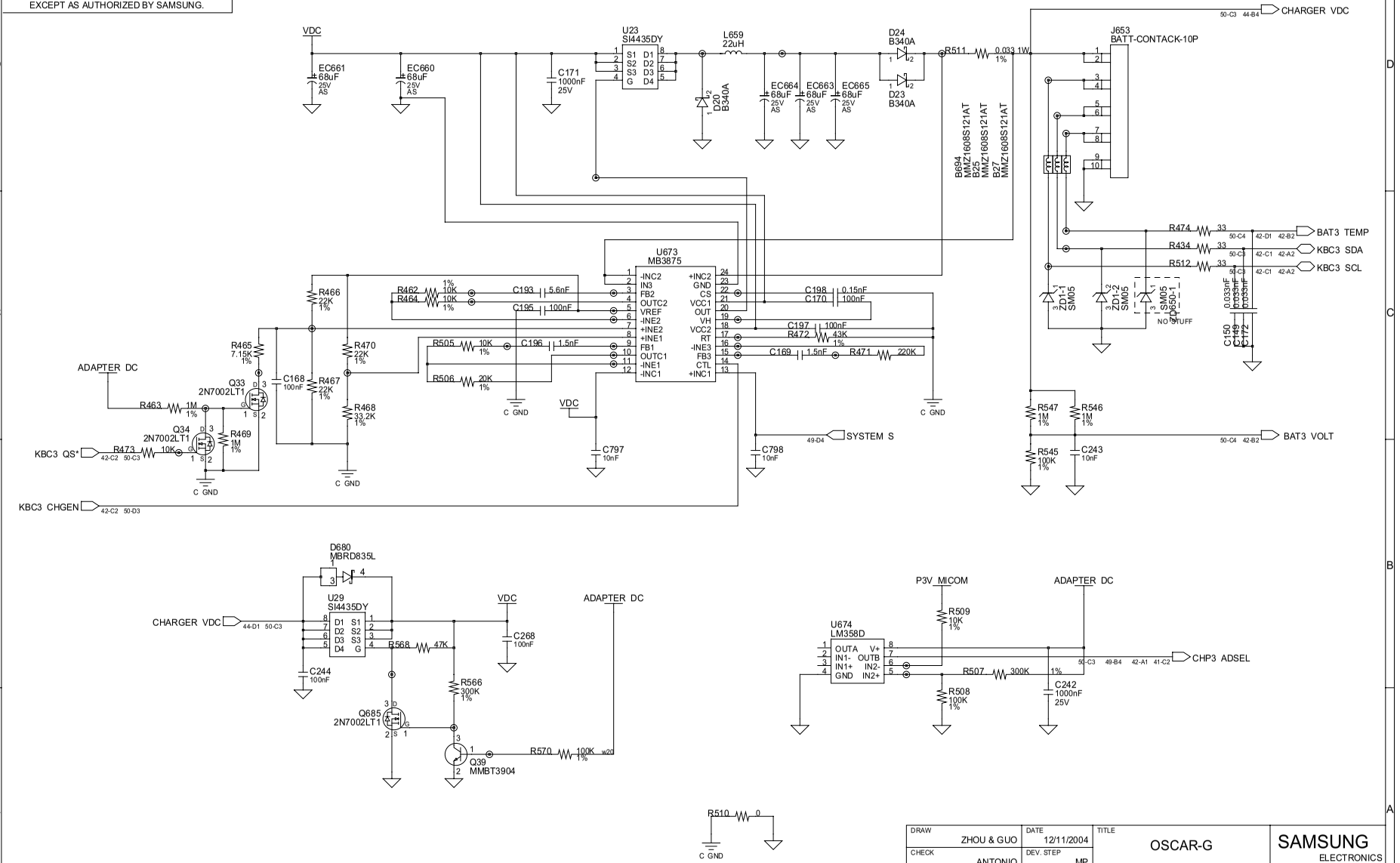

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G CHARGER	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1		PART NO. BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 44 OF 51	

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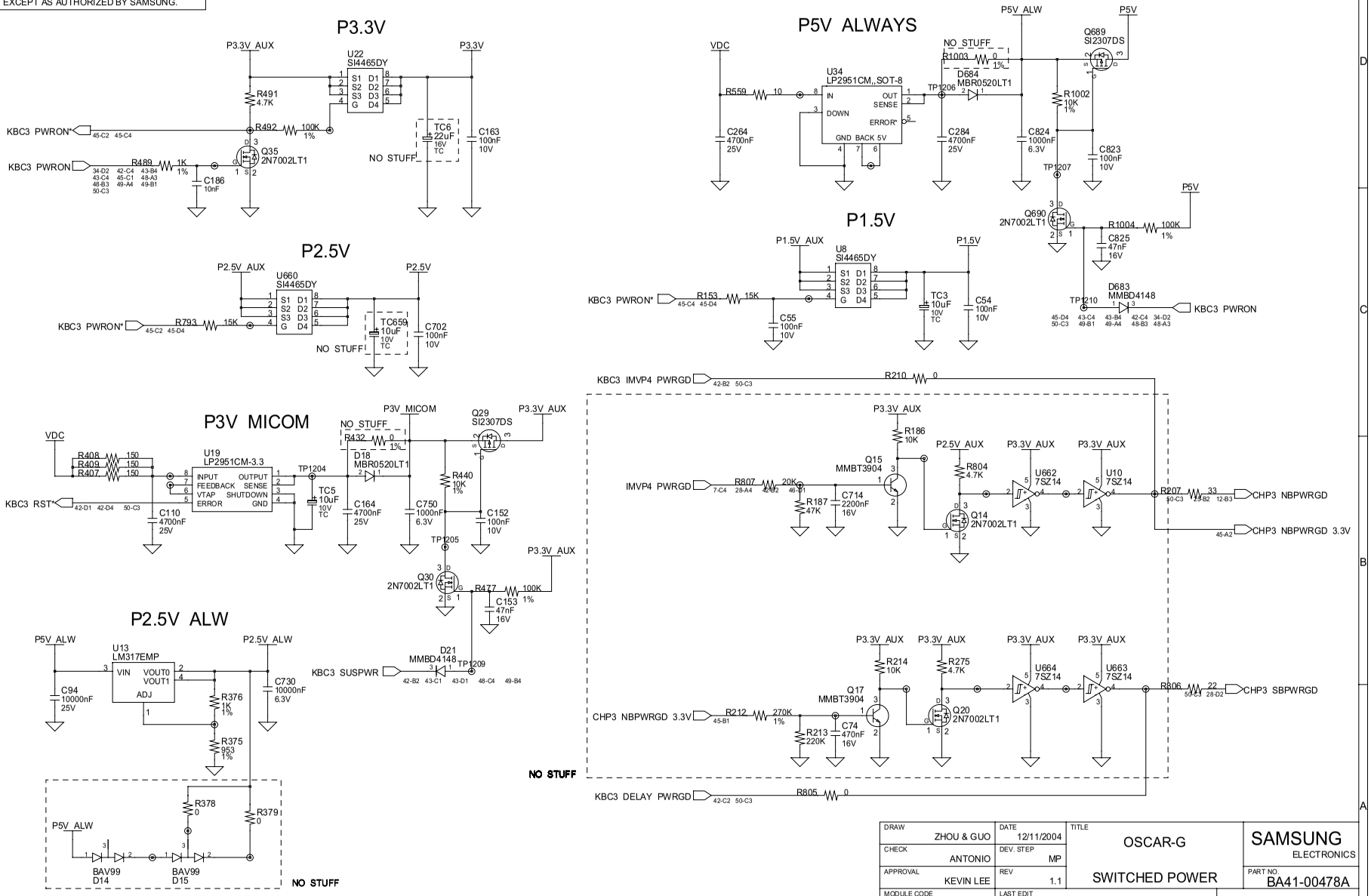

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	SWITCHED POWER	PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 45 OF 51	

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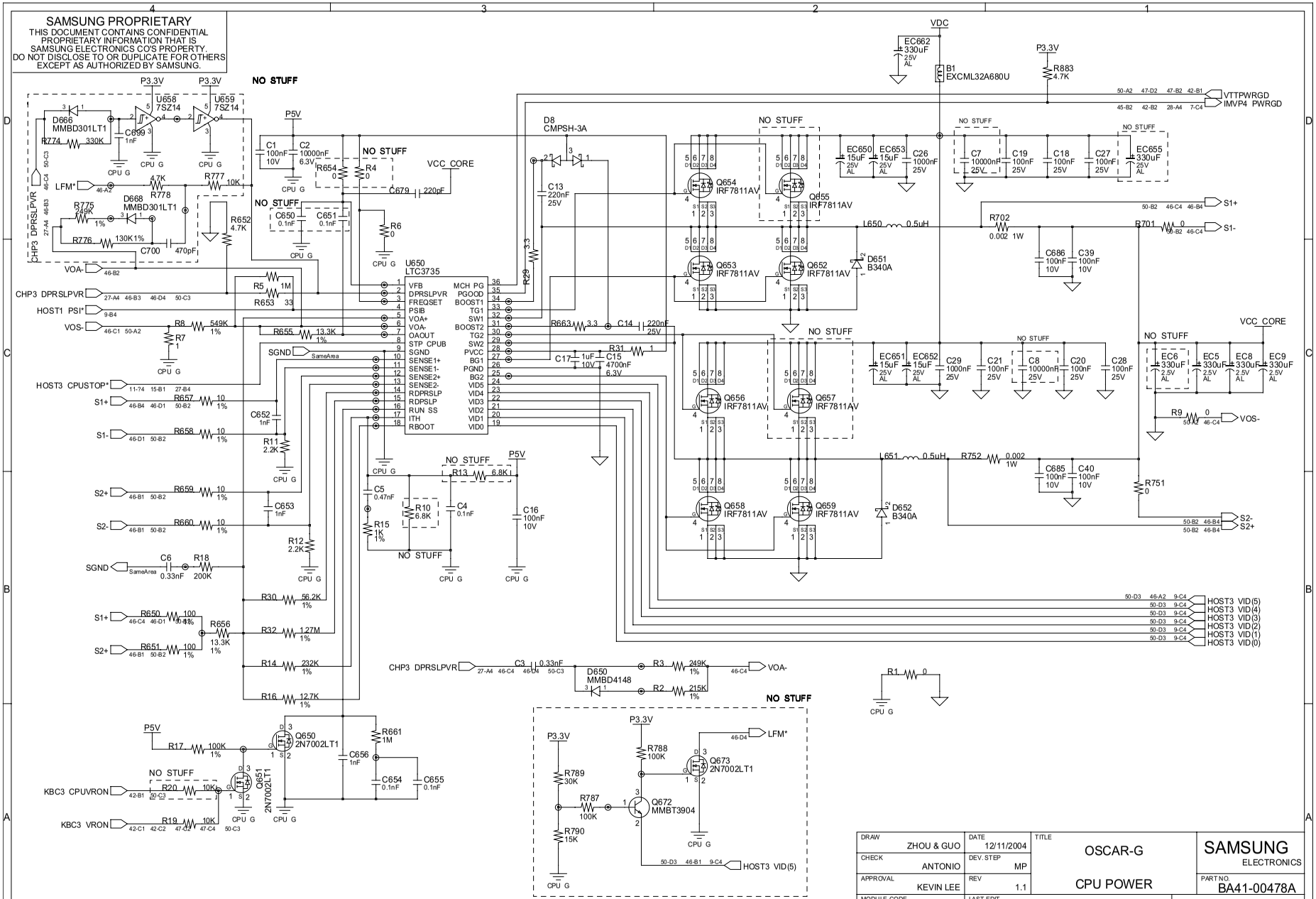

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	CPU POWER	PART NO. BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 46 OF 51	

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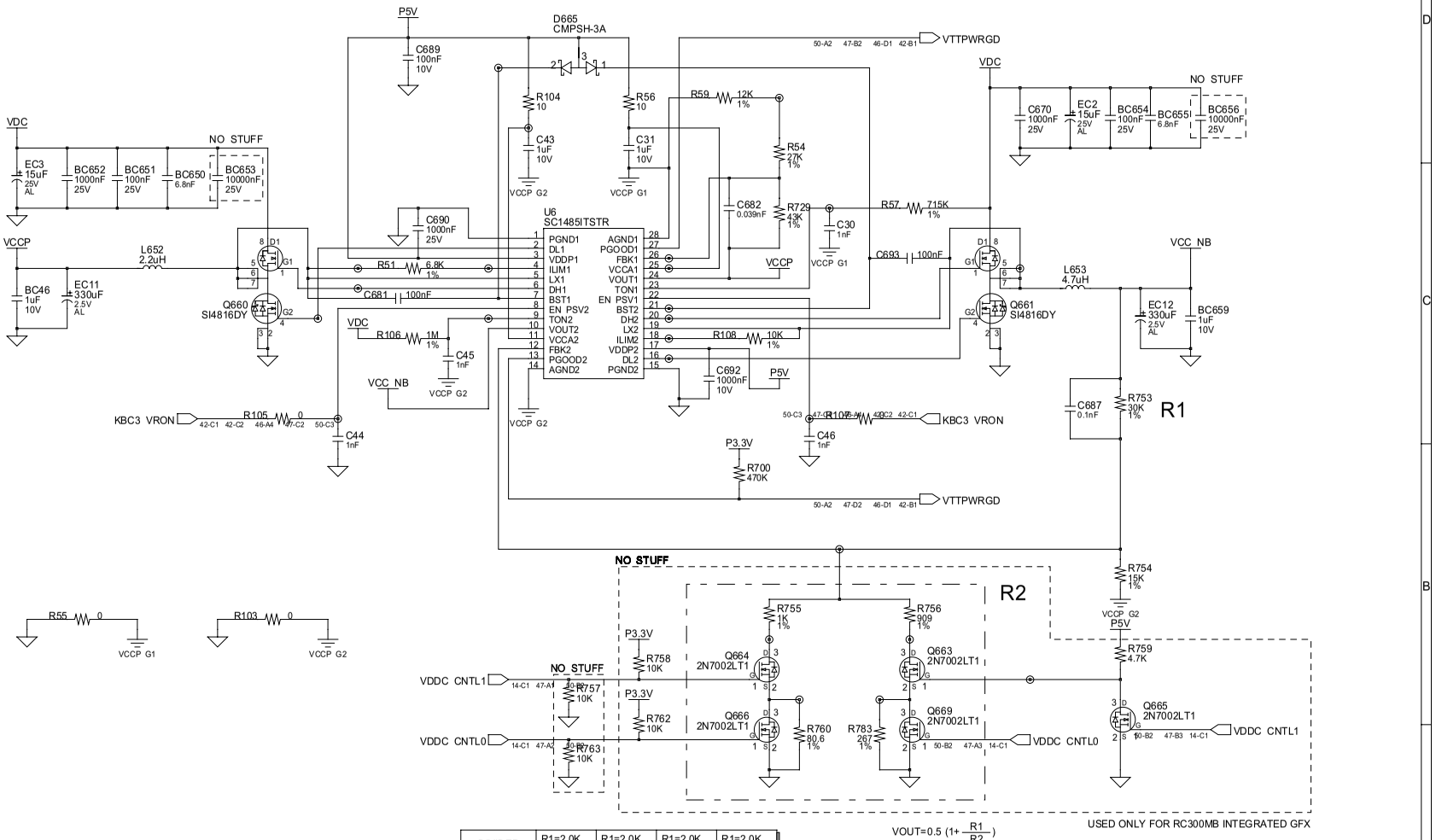

DIVIDER	R1=2.0K R2=1.0K	R1=2.0K R2=1.081K	R1=2.0K R2=0.91K	R1=2.0K R2=1.177K
VDDC CNTL1	1	1	0	0
VDDC CNTL0	1	0	1	0
VCC NB	1.5V	1.425V	1.6V	1.35V

$$VOUT = 0.5\ (1 + \frac{R1}{R2})$$

USED ONLY FOR RC300MB INTEGRATED GFX

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	VCCP / NB POWER	PART NO.: BA41-00478A
MODULE CODE:	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 47 OF 51	

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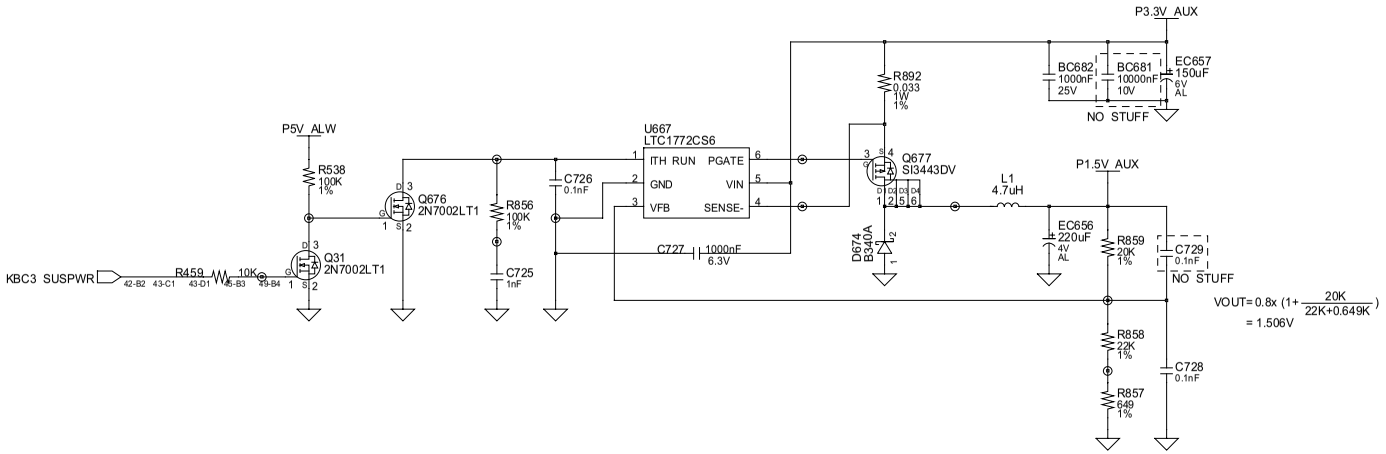

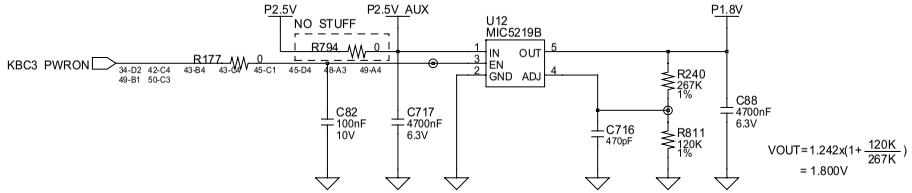

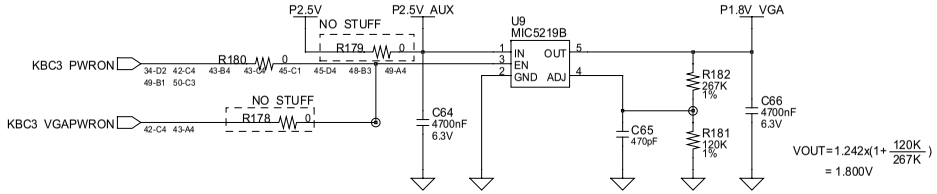

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	1.5V AUX / 1.8V / 1.8V VGA	PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 48 OF 51	

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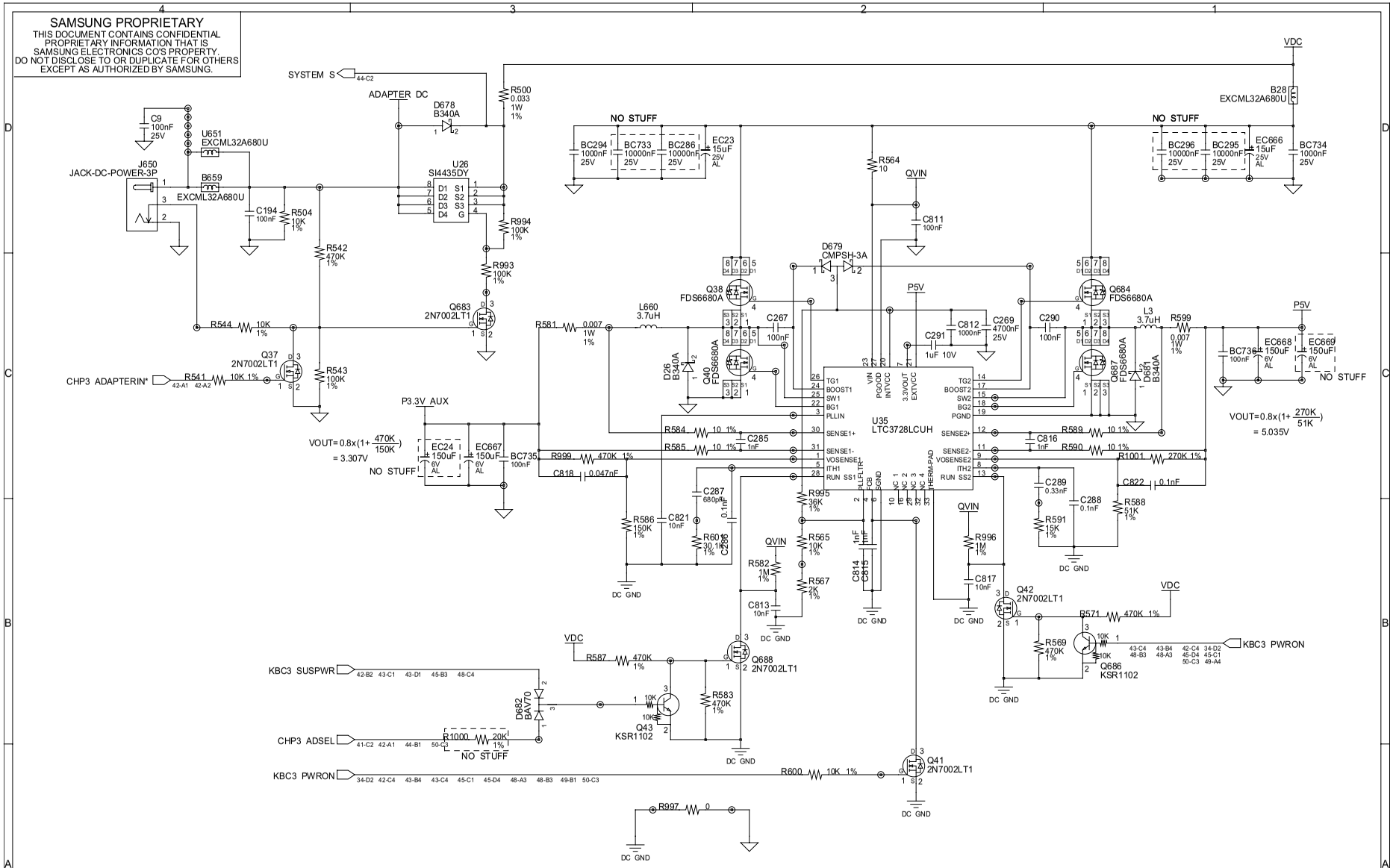

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP	P3.3V AUX / 5V	
APPROVAL: KEVIN LEE	REV: 1.1		PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 49 OF 51	

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- AGP0 VREF
- AGP1 DBI HI
- AGP1 DBI LO
- AGP1 DEVSEL*
- AGP1 FRAME*
- AGP1 GNT*
- AGP1 IRDY*
- AGP1 PAR
- AGP1 RBF*
- AGP1 REQ*
- AGP1 STOP*
- AGP1 WBF*
- AGP3 GPIO(0)
- AGP3 GPIO(1)
- AGP3 GPIO(13)
- AGP3 GPIO(15)
- AGP3 GPIO(16)
- AGP3 GPIO(2)
- AGP3 GPIO(3)
- AGP3 GPIO(4)
- AGP3 GPIO(6)
- AGP3 GPIO(8)
- AGP3 GPIO(9)
- AGP3 STP*
- AUD3 LINK BCLK
- AUD3 LINK RST*
- AUD3 LINK SDI0
- AUD3 LINK SDI1
- AUD3 LINK SDI2
- AUD3 LINK SPDIFO
- AUD3 LINK SYNC
- AUD3 MONO OUT
- AUD3 PHONE
- AUD5 CDDCOM
- AUD5 CDDL
- AUD5 CDDR
- AUD5 LINE OUT L
- AUD5 LINE OUT R
- AUD5 MIC 1
- AUD5 SPK L+
- AUD5 SPK L-
- AUD5 SPK R+
- AUD5 SPK R-
- BAT3 TEMP
- BAT3 VOLT
- CB3 3VEN*
- CB3 5VEN*
- CB3 A18
- CB3 A19
- CB3 AD(0)
- CB3 AD(1)
- CB3 AD(10)
- CB3 AD(11)
- CB3 AD(12)
- CB3 AD(13)
- CB3 AD(14)
- CB3 AD(15)
- CB3 AD(16)
- CB3 AD(17)
- CB3 AD(18)
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- CB3 AD(6)
- CB3 AD(7)
- CB3 AD(8)
- CB3 AD(9)
- CB3 AUDIO
- CB3 CBE0*
- CB3 CBE1*
- CB3 CBE2*
- CB3 CBE3*
- CB3 CD1*
- CB3 CD2*
- CB3 CLK
- CB3 CLKRUN*
- CB3 D14
- CB3 D2
- CB3 DEVSEL*
- CB3 FRAME*
- CB3 GNT*
- CB3 INT*
- CB3 IRDY*
- CB3 PAR
- CB3 PERR*
- CB3 REQ*
- CB3 RST*
- CB3 SERR*
- CB3 SPKR
- CB3 STOP*
- CB3 STSCHG
- CB3 TRDY*
- CB3 VPPEN0*
- CB3 VPPEN1*
- CB3 VS1
- CB3 VS2
- CHARGER VDC
- CHP3 ADSEL
- USB3 SMI
- CHP3 DPRSLPVR
- CHP3 NBPWRGD
- CHP3 PATADET
- CHP3 PCICLKSTOP*
- CHP3 PME*
- CHP3 RI*
- CHP3 RSMRST*
- CHP3 RTCIRQ*
- CHP3 SATADET
- CHP3 SBPWRGD
- CHP3 SERIRQ
- CHP3 SLPS5*
- CHP3 SPKR
- CHP3 SUSSTAT*
- FAN3 FDBACK*
- FWH1 INIT*
- HDD5 A0
- HDD5 A1
- HDD5 A2
- HDD5 CS1*
- HDD5 CS3*
- HDD5 D(0)
- HDD5 D(1)
- HDD5 D(10)
- HDD5 D(11)
- HDD5 D(12)
- HDD5 D(13)
- HDD5 D(14)
- HDD5 D(15)
- HDD5 D(2)
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- HDD5 D(4)
- HDD5 D(5)
- HDD5 D(6)
- HDD5 D(7)
- HDD5 D(8)
- HDD5 D(9)
- HDD5 DACK*
- HDD5 DREQ*
- HDD5 IOR*
- HDD5 IORDY
- HDD5 IOW*
- HDD5 IRQ
- HDD5 LED*
- HOST1 FERR*
- HOST1 HIT*
- HOST1 HITM*
- HOST1 IGNNE*
- HOST1 INIT*
- HOST1 INTR
- HOST1 LOCK*
- HOST1 NMI
- HOST1 SLP*
- HOST1 SMI*
- HOST1 STPCLK*
- HOST1 TCK
- HOST1 TDI
- HOST1 TDO
- HOST1 TMS
- HOST1 TRDY*
- HOST1 TRST*
- HOST2 THERMDA
- HOST2 THERMDC
- HOST3 CPUSTOP NB*
- HOST3 FERR*
- HOST3 VID(0)
- HOST3 VID(1)
- HOST3 VID(2)
- HOST3 VID(3)
- HOST3 VID(4)
- HOST3 VID(5)
- HP5 LINE OUT L
- HP5 LINE OUT R
- HP DETECT
- KBC3 A20G
- KBC3 BKLTON
- KBC3 BRIT
- KBC3 CAPSLED*
- KBC3 CHGEN
- KBC3 CPURST*
- KBC3 CPUVRON
- KBC3 DELAY PWRGD
- KBC3 EXTSMI*
- KBC3 FANCTRL
- KBC3 IMVP4 PWRGD
- KBC3 LBLED*
- KBC3 NUMLED*
- KBC3 PWRGD
- KBC3 PWRON
- KBC3 PWRSW/*
- KBC3 PWRSW SB*
- KBC3 QS*
- KBC3 RSMRST*
- KBC3 RST*
- KBC3 RUNSCI*
- KBC3 SCL
- KBC3 SCLED*
- KBC3 SDA
- KBC3 SPKMUTE
- KBC3 THERM SCL
- KBC3 THERM SDA
- KBC3 TPAD*
- KBC3 VRON
- KBC3 WAKESCI*
- KBC3 WLAN*
- KBC5 KSI(0)
- KBC5 KSI(1)
- KBC5 KSI(2)
- KBC5 KSI(3)
- KBC5 KSI(4)
- KBC5 KSI(5)
- KBC5 KSI(6)
- KBC5 KSI(7)
- KBC5 KSO(0)
- KBC5 KSO(1)
- KBC5 KSO(10)
- KBC5 KSO(11)
- KBC5 KSO(12)
- KBC5 KSO(13)
- KBC5 KSO(14)
- KBC5 KSO(15)
- KBC5 KSO(2)
- KBC5 KSO(3)
- KBC5 KSO(4)
- KBC5 KSO(5)
- KBC5 KSO(6)
- KBC5 KSO(7)
- KBC5 KSO(8)
- KBC5 KSO(9)
- LAN3 EECK
- LAN3 EEDO
- LAN3 MDCK
- LAN3 PHYPD
- LAN3 TXD0
- LAN3 TXD1
- LAN3 TXD2
- LAN3 TXD3
- LAN3 TXEN
- LCD3 BKLTON
- LCD3 BRIT
- LED3 CHARGE
- LID3 SWITCH*
- LPC3 AD(0)
- LPC3 AD(1)
- LPC3 AD(2)
- LPC3 AD(3)
- LPC3 FRAME*
- LPC3 SMI*
- MDC3 AUDIN
- PCI3 ACTREQ*
- PCI3 AD(0)
- PCI3 AD(1)
- PCI3 AD(10)
- PCI3 AD(11)
- PCI3 AD(12)
- PCI3 AD(13)
- PCI3 AD(14)
- PCI3 AD(15)
- PCI3 AD(16)
- PCI3 AD(17)
- PCI3 AD(18)
- PCI3 AD(19)
- PCI3 AD(2)
- PCI3 AD(20)
- PCI3 AD(21)
- PCI3 AD(22)
- PCI3 AD(23)
- PCI3 AD(24)
- PCI3 AD(25)
- PCI3 AD(26)
- PCI3 AD(27)
- PCI3 AD(28)
- PCI3 AD(29)
- PCI3 AD(3)
- PCI3 AD(30)
- PCI3 AD(31)
- PCI3 AD(4)
- PCI3 AD(5)
- PCI3 AD(6)
- PCI3 AD(7)
- PCI3 AD(8)
- PCI3 AD(9)
- PCI3 CBE*(0)
- PCI3 CBE*(1)
- PCI3 CBE*(2)
- PCI3 CBE*(3)
- PCI3 CLKRUN*
- PCI3 DEVSEL*
- PCI3 FRAME*
- PCI3 GNT0*
- PCI3 GNT1*
- PCI3 GNT2*
- PCI3 INTB*
- PCI3 INTD*
- PCI3 IRDY*
- PCI3 PAR
- PCI3 PERR*
- PCI3 REQ0*
- PCI3 REQ1*
- PCI3 REQ2*
- PCI3 REQ3*
- PCI3 REQ4*
- PCI3 ROMCS*
- PCI3 RSTF*
- PCI3 SERR*
- PCI3 STOP*
- PCI3 TRDY*
- PS1+
- PS1-
- PS2+
- PS2-
- SMB3 ALERT*
- VDDC CNTL0
- VDDC CNTL1
- VGA3 BKLTON
- VGA3 BLUE
- VGA3 C
- VGA3 DDCC
- VGA3 DDCD
- VGA3 GREEN
- VGA3 HSYNC
- VGA3 LCDVDDON
- VGA3 RED
- VGA3 VSYNC
- VGA3 Y
- VGS-
- VTTPWRGD
- AUD GND
- AUD GND
- AUD GND
- AVDDQ
- AVDD CK
- AVDD CK
- AVDD NB
- AVSSDI
- AVSSN
- AVSSQ
- CPU G
- CPU G
- C GND
- C GND
- G1 DDR
- G1 DDR
- G2 DDR
- LPVSS
- LVSSR
- MIC GND
- MIC GND
- P1.25V
- P1.25V
- P1.25V
- P1.25V
- P1.5V
- P1.5V
- P1.5V
- P1.5V
- P1.5V AUX
- P1.5V AUX
- P1.5V AUX
- P1.5V AUX
- P1.8V
- P1.8V
- P1.8V
- P1.8V
- P1.8V REG
- P1.8V REG
- P1.8V REG
- P1.8V REG
- P1.8V VGA
- P1.8V VGA
- P2.5V ALW
- P2.5V AUX SB
- P3.3V
- P3.3V
- P3.3V
- P3.3V
- P3.3V AVDDC
- PLLVDD
- PLLVSS
- PLLVSS
- PVDD
- PVDD
- PVDD
- PVDD
- USB AVDD
- VCCP
- VCCP
- VCCP
- VCCP
- VCCP G1
- VCCP G2
- VCC CB
- VCC CB
- VCC CORE
- VCC CORE
- VCC CORE
- VCC CORE
- VCC GPIO
- VCC NB
- VCC NB
- VCC NB
- VCC NB
- VDC
- VDC
- VDC
- VDC
- VDC INV
- VDD LCD
- VGA CORE
- VGA CORE
- VGA CORE
- VGA CORE
- VPP CB
- V BAT

DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	TEST POINT	PART NO.: BA41-00478A
MODULE CODE	LAST EDIT: December 11, 2004 8:30:22 PM	PAGE 50 OF 51	

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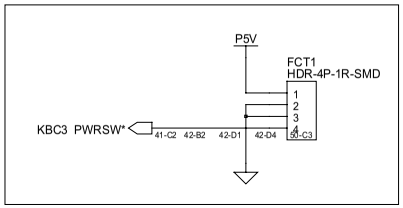
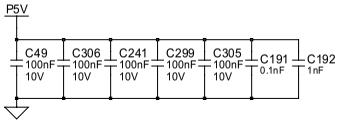
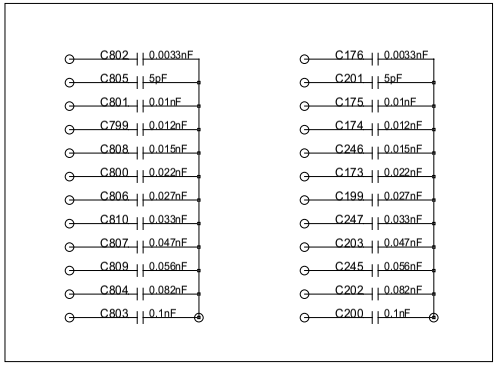
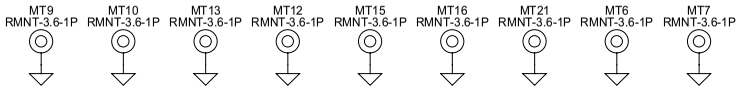




CAPS FOR ICT TEST



PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.	04/12/11	MP	1.1
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.	04/11/08	PR	1.1
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			



DRAW: ZHOU & GUO	DATE: 12/11/2004	TITLE: OSCAR-G	SAMSUNG ELECTRONICS
CHECK: ANTONIO	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.1	PCB STUFFS	PART NO.: BA41-00478A
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9. Schematic Diagram

9-1 MIAN BOARD

9-1-2 Signal Location

9-1-2 Signal Location

Signal Name	Sheet Number - Location
AGP0 VREF	14-A4, 14-C2, 21-B4, 50-D4
AGP1 AD(31)	14-D3, 21-D4
AGP1 AD(2)	14-D3, 21-D4
AGP1 AD(17)	14-D3, 21-D4
AGP1 AD(14)	14-D3, 21-D4
AGP1 AD(21)	14-D3, 21-D4
AGP1 AD(1)	14-D3, 21-D4
AGP1 AD(12)	14-D3, 21-D4
AGP1 AD(19)	14-D3, 21-D4
AGP1 AD(8)	14-D3, 21-D4
AGP1 AD(28)	14-D3, 21-D4
AGP1 AD(4)	14-D3, 21-D4
AGP1 AD(10)	14-D3, 21-D4
AGP1 AD(23)	14-D3, 21-D4
AGP1 AD(13)	14-D3, 21-D4
AGP1 AD(11)	14-D3, 21-D4
AGP1 AD(3)	14-D3, 21-D4
AGP1 AD(6)	14-D3, 21-D4
AGP1 AD(18)	14-D3, 21-D4
AGP1 AD(30)	14-D3, 21-D4
AGP1 AD(9)	14-D3, 21-D4
AGP1 AD(5)	14-D3, 21-D4
AGP1 AD(15)	14-D3, 21-D4
AGP1 AD(20)	14-D3, 21-D4
AGP1 AD(16)	14-D3, 21-D4
AGP1 AD(29)	14-D3, 21-D4
AGP1 AD(27)	14-D3, 21-D4
AGP1 AD(25)	14-D3, 21-D4
AGP1 AD(22)	14-D3, 21-D4
AGP1 AD(24)	14-D3, 21-D4
AGP1 AD(7)	14-D3, 21-D4
AGP1 AD(0)	14-D3, 21-D4
AGP1 AD(26)	14-D3, 21-D4
AGP1 AD(31:0)	14-D3, 21-D4
AGP1 ADSTB0	14-C3, 21-C4
AGP1 ADSTB0*	14-C3, 21-C4
AGP1 ADSTB1	14-C3, 21-C4
AGP1 ADSTB1*	14-B3, 21-C4
AGP1 CBE*(2)	14-B3, 21-D1
AGP1 CBE*(0)	14-B3, 21-D1

Signal Name	Sheet Number - Location
AGP1 CBE*(3)	14-B3, 21-D1
AGP1 CBE*(1)	14-B3, 21-D1
AGP1 CBE*(3:0)	14-B3, 21-D1
AGP1 DBI HI	14-B3, 22-B1, 50-D4
AGP1 DBI LO	14-B3, 22-B1, 50-D4
AGP1 DEVSEL*	14-B3, 21-D4, 50-D4
AGP1 FRAME*	14-B3, 21-C4, 50-D4
AGP1 GNT*	14-B4, 21-D4, 50-D4
AGP1 IRDY*	14-B3, 21-D4, 50-D4
AGP1 PAR	14-B3, 21-D4, 50-D4
AGP1 RBF*	14-B3, 21-C4, 50-D4
AGP1 REQ*	14-B4, 21-D4, 50-D4
AGP1 SBA(0)	14-B3, 14-C2, 21-C4
AGP1 SBA(6)	14-B3, 14-D2, 21-C4
AGP1 SBA(2)	14-B3, 14-D2, 21-C4
AGP1 SBA(3)	14-B3, 14-D2, 21-C4
AGP1 SBA(5)	14-B3, 14-D2, 21-C4
AGP1 SBA(7)	14-B3, 14-D2, 21-C4
AGP1 SBA(4)	14-B3, 14-D2, 21-C4
AGP1 SBA(1)	14-B3, 14-C2, 21-C4
AGP1 SBA(7:0)	14-B3, 21-C4
AGP1 SBSTB	14-C3, 14-D2, 21-C4
AGP1 SBSTB*	14-C3, 21-C4
AGP1 ST(1)	14-B3, 21-C4
AGP1 ST(0)	14-B3, 21-C4
AGP1 ST(2)	14-B3, 21-C4
AGP1 ST(2:0)	14-B3, 21-C4
AGP1 STOP*	14-B3, 21-D4, 50-D4
AGP1 TRDY*	14-B3, 21-D4
AGP1 WBF*	14-B3, 21-C4, 50-D4
AGP3 BUSY*	14-D1, 21-C4, 28-A4, 28-C1
AGP3 DMINUS	21-D1, 23-B2
AGP3 DPLUS	21-D1, 23-B2
AGP3 GPIO(13)	21-A4, 24-D4, 50-D4
AGP3 GPIO(12)	21-A4, 24-D4
AGP3 GPIO(8)	21-A4, 24-D4, 50-C4
AGP3 GPIO(6)	21-A4, 24-D4, 50-C4
AGP3 GPIO(5)	21-A4, 24-D4
AGP3 GPIO(4)	21-A4, 24-D4, 50-C4
AGP3 GPIO(3)	21-A4, 24-D4, 50-C4

Signal Name	Sheet Number - Location
AGP3 GPIO(2)	21-A4, 24-D4, 50-D4
AGP3 GPIO(1)	21-A4, 24-D4, 50-D4
AGP3 GPIO(0)	21-A4, 24-D4, 50-D4
AGP3 GPIO(15)	21-A4, 24-D4, 43-A1, 50-D4
AGP3 GPIO(16)	21-A4, 23-D1, 24-D4, 50-D4
AGP3 GPIO(11)	21-A4, 24-D4
AGP3 GPIO(9)	21-A4, 24-D4, 50-C4
AGP3 GPIO(7)	21-A4, 24-D4
AGP3 GPIO(10)	21-A4, 24-D4
AGP3 GPIO(14)	21-A4, 24-D4
AGP3 GPIO(16:0)	21-A4, 24-D4
AGP3 RST*	21-D4, 27-C1
AGP3 STP*	14-D1, 21-C4, 28-A4, 28-C1, 50-C4
ALINK3 ACAT*	14-B4, 27-C4
ALINK3 AD(28)	14-D4, 17-C3, 27-D4
ALINK3 AD(19)	14-D4, 17-B3, 27-D4
ALINK3 AD(27)	14-D4, 17-C3, 27-D4
ALINK3 AD(26)	14-D4, 17-C3, 27-D4
ALINK3 AD(13)	14-D4, 27-D4
ALINK3 AD(16)	14-D4, 27-D4
ALINK3 AD(17)	14-D4, 17-C3, 27-D4
ALINK3 AD(5)	14-D4, 27-D4
ALINK3 AD(7)	14-D4, 27-D4
ALINK3 AD(0)	14-D4, 27-D4
ALINK3 AD(3)	14-D4, 27-D4
ALINK3 AD(22)	14-D4, 17-B3, 27-D4
ALINK3 AD(6)	14-D4, 27-D4
ALINK3 AD(14)	14-D4, 27-D4
ALINK3 AD(4)	14-D4, 27-D4
ALINK3 AD(9)	14-D4, 27-D4
ALINK3 AD(20)	14-D4, 17-B3, 27-D4
ALINK3 AD(15)	14-D4, 27-D4
ALINK3 AD(8)	14-D4, 27-D4
ALINK3 AD(29)	14-D4, 17-C3, 27-D4
ALINK3 AD(24)	14-D4, 17-C3, 27-D4
ALINK3 AD(1)	14-D4, 27-D4
ALINK3 AD(25)	14-D4, 17-C3, 27-D4
ALINK3 AD(18)	14-D4, 17-B3, 27-D4
ALINK3 AD(2)	14-D4, 27-D4
ALINK3 AD(23)	14-D4, 17-B3, 27-D4
ALINK3 AD(10)	14-D4, 27-D4
ALINK3 AD(12)	14-D4, 27-D4
ALINK3 AD(21)	14-D4, 17-B3, 27-D4

Signal Name	Sheet Number - Location
ALINK3 AD(31)	14-D4, 17-D3, 27-D4
ALINK3 AD(11)	14-D4, 27-D4
ALINK3 AD(30)	14-D4, 17-D3, 27-D4
ALINK3 AD(31:0)	14-D4, 27-D4
ALINK3 CBE*(3)	14-C4, 27-C4
ALINK3 CBE*(1)	14-C4, 27-C4
ALINK3 CBE*(2)	14-C4, 27-C4
ALINK3 CBE*(0)	14-C4, 27-C4
ALINK3 CBE*(3:0)	14-C4, 27-C4
ALINK3 DEVSEL*	14-B4, 27-C4
ALINK3 END*	14-B4, 27-C4
ALINK3 GNT*	14-B4, 27-B4
ALINK3 INTA*	14-B4, 21-C4, 27-B4, 32-C4, 34-B2
ALINK3 OFF*	14-B4, 27-C4
ALINK3 PAR	14-B4, 17-B3, 27-C4
ALINK3 REQ*	14-B4, 27-C4
ALINK3 RST*	12-B4, 15-B1, 27-C2, 27-D4
ALINK3 STROBE*	14-B4, 27-C4
AUD3 LINK BCLK	28-A2, 28-B1, 37-A2, 39-A2, 50-C4
AUD3 LINK BCLK R	37-A2, 37-D4, 39-A2
AUD3 LINK RST*	28-A2, 28-B2, 28-C1, 50-C4
AUD3 LINK RST R*	28-B1, 37-C4, 39-B3
AUD3 LINK SDI0	28-A2, 28-B1, 37-C4, 50-C4
AUD3 LINK SDI1	28-A2, 28-B1, 39-B2, 50-C4
AUD3 LINK SDI2	28-A2, 28-B1, 50-C4
AUD3 LINK SDO	28-A2, 30-D4, 37-D4, 39-B3
AUD3 LINK SPDIFO	28-A2, 30-D4, 50-C4
AUD3 LINK SYNC	28-A2, 30-D4, 37-C4, 39-B2, 50-C4
AUD3 MONO OUT	37-C3, 39-B3, 50-C4
AUD3 PCBEEP	37-A3, 37-C3
AUD3 PHONE	37-A3, 37-C3, 50-C4
AUD5 CDDCOM	37-B3, 37-C3, 50-C4
AUD5 CDDL	37-B3, 37-C3, 50-C4
AUD5 CDDR	37-B3, 37-C3, 50-C4
AUD5 LINE OUT L	37-C2, 37-C3, 50-C4
AUD5 LINE OUT R	37-C3, 37-D2, 50-C4
AUD5 MIC 1	37-C3, 38-C2, 50-C4
AUD5 MIC 2	37-C3, 38-C2
AUD5 SPKMUTE*	37-C1, 37-C1
AUD5 SPK L+	37-A1, 37-C1, 50-C4
AUD5 SPK L-	37-A1, 37-C1, 50-C4

Signal Name	Sheet Number - Location
AUD5 SPK R+	37-A1, 37-C1, 50-C4
AUD5 SPK R-	37-A1, 37-C1, 50-C4
AUD5 VREFOUT	37-C3, 38-C2
BAT3 TEMP	42-B2, 42-D1, 44-C1, 50-C4
BAT3 VOLT	42-B2, 44-C1, 50-C4
CB3 3VEN*	35-A4, 35-D4, 50-C4
CB3 5VEN*	35-A4, 35-D4, 50-B4
CB3 A18	35-C1, 35-C4, 50-B4
CB3 A19	35-C1, 35-C4, 50-B4
CB3 AD(20)	35-D2, 35-D3, 50-B4
CB3 AD(19)	35-D2, 35-D3, 50-B4
CB3 AD(18)	35-D2, 35-D3, 50-B4
CB3 AD(6)	35-D2, 35-D3, 50-A4
CB3 AD(25)	35-D2, 35-D3, 50-B4
CB3 AD(24)	35-D2, 35-D3, 50-B4
CB3 AD(2)	35-D2, 35-D3, 50-B4
CB3 AD(11)	35-D2, 35-D3, 50-B4
CB3 AD(14)	35-D2, 35-D3, 50-B4
CB3 AD(31)	35-D2, 35-D3, 50-A4
CB3 AD(8)	35-D2, 35-D3, 50-A4
CB3 AD(7)	35-D2, 35-D3, 50-A4
CB3 AD(27)	35-D2, 35-D3, 50-B4
CB3 AD(21)	35-D2, 35-D3, 50-B4
CB3 AD(29)	35-D2, 35-D3, 50-B4
CB3 AD(12)	35-D2, 35-D3, 50-B4
CB3 AD(1)	35-D2, 35-D3, 50-B4
CB3 AD(0)	35-D2, 35-D3, 50-B4
CB3 AD(13)	35-D2, 35-D3, 50-B4
CB3 AD(23)	35-D2, 35-D3, 50-B4
CB3 AD(22)	35-D2, 35-D3, 50-B4
CB3 AD(10)	35-D2, 35-D3, 50-B4
CB3 AD(9)	35-D2, 35-D3, 50-A4
CB3 AD(26)	35-D2, 35-D3, 50-B4
CB3 AD(17)	35-D2, 35-D3, 50-B4
CB3 AD(16)	35-D2, 35-D3, 50-B4
CB3 AD(4)	35-D2, 35-D3, 50-A4
CB3 AD(3)	35-D2, 35-D3, 50-B4
CB3 AD(15)	35-D2, 35-D3, 50-B4
CB3 AD(30)	35-D2, 35-D3, 50-B4
CB3 AD(5)	35-D2, 35-D3, 50-A4
CB3 AD(28)	35-D2, 35-D3, 50-B4
CB3 AD(31:0)	35-D2, 35-D3
CB3 AUDIO	35-B1, 35-B3, 50-A4
CB3 CBE0*	35-C3, 35-D1, 50-A4

Signal Name	Sheet Number - Location
CB3 CBE1*	35-C1, 35-C3, 50-A4
CB3 CBE2*	35-C1, 35-C3, 50-A4
CB3 CBE3*	35-B1, 35-C3, 50-A4
CB3 CD1*	35-A2, 35-B3, 35-D1, 50-D3
CB3 CD2*	35-A2, 35-B1, 35-B3, 50-D3
CB3 CLK	35-C1, 35-C3, 50-D3
CB3 CLKRUN*	35-B1, 35-C3, 50-D3
CB3 D14	35-C4, 35-D1, 50-D3
CB3 D2	35-B1, 35-C4, 50-D3
CB3 DEVSEL*	35-B3, 35-C1, 50-D3
CB3 FRAME*	35-B3, 35-C1, 50-D3
CB3 GNT*	35-B3, 35-C1, 50-D3
CB3 INT*	35-B3, 35-C1, 50-D3
CB3 IRDY*	35-B3, 35-C1, 50-D3
CB3 PAR	35-B3, 35-C1, 50-D3
CB3 PERR*	35-B3, 35-C1, 50-D3
CB3 REQ*	35-B1, 35-B3, 50-D3
CB3 RST*	35-A2, 35-B1, 35-C3, 50-D3
CB3 SERR*	35-B1, 35-B3, 50-D3
CB3 SPKR	34-B4, 37-A4, 50-D3
CB3 STOP*	35-B3, 35-C1, 50-D3
CB3 STSCHG	35-B1, 35-B3, 50-C3
CB3 TRDY*	35-B3, 35-C1, 50-C3
CB3 VPPEN0*	35-A4, 35-D4, 50-C3
CB3 VPPEN1*	35-A4, 35-D4, 50-C3
CB3 VS1	35-B3, 35-C1, 50-C3
CB3 VS2	35-B1, 35-B3, 50-C3
CDD5 A0	28-B2, 39-C4
CDD5 A1	28-B2, 39-C4
CDD5 A2	28-B2, 39-C3
CDD5 COM	37-B4, 39-D3, 39-D4
CDD5 CS1*	28-B2, 39-C4
CDD5 CS3*	28-B2, 39-C3
CDD5 D(14)	28-B2, 39-C3
CDD5 D(5)	28-B2, 39-C4
CDD5 D(8)	28-B2, 39-C3
CDD5 D(0)	28-B2, 39-C4
CDD5 D(9)	28-B2, 39-C3
CDD5 D(6)	28-B2, 39-C4
CDD5 D(12)	28-B2, 39-C3
CDD5 D(13)	28-B2, 39-C3
CDD5 D(2)	28-B2, 39-C4
CDD5 D(4)	28-B2, 39-C4
CDD5 D(15)	28-B2, 39-C3

Signal Name	Sheet Number - Location
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CDD5 D(11)	28-B2, 39-C3
CDD5 D(3)	28-B2, 39-C4
CDD5 D(10)	28-B2, 39-C3
CDD5 D(1)	28-B2, 39-C4
CDD5 D(15:8)	39-C3
CDD5 D(7:0)	39-C4
CDD5 D(15:0)	28-B2
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CDD5 DREQ	28-B2, 39-C3
CDD5 IOR*	28-B2, 39-C3
CDD5 IORDY	28-B2, 39-C4
CDD5 IOW*	28-B2, 39-C4
CDD5 IRQ	28-B1, 28-B2, 39-C4
CDD5 L	37-B4, 39-D4
CDD5 R	37-B4, 39-D3
CHARGER VDC	44-B4, 44-D1, 50-C3
CHP2 SUSSTAT*	12-B4, 28-D1, 28-D2
CHP3 1394 ROMW*	28-A4, 34-B2
CHP3 ADAPTERIN*	42-A1, 42-A2, 49-C4
CHP3 ADSEL	41-C2, 42-A1, 44-B1, 49-B4, 50-C3
CHP3 CMOSCLR	27-A1, 28-A4
CHP3 DPRSLPVR	27-A4, 46-B3, 46-C4, 46-D4, 50-C3
CHP3 NBPWRGD	12-B3, 25-B2, 45-B1, 50-C3
CHP3 NBPWRGD 3.3V	45-A2, 45-B1
CHP3 PATADET	28-C2, 39-B4, 50-C3
CHP3 PCICLKSTOP*	7-C4, 27-B4, 50-C3
CHP3 PME*	28-C1, 28-C2, 32-C2, 33-B2, 34-C4, 36-B4, 50-C3
CHP3 RI*	28-C1, 28-D2, 50-C3
CHP3 RSMRST*	27-A3, 28-B4, 50-C3
CHP3 RTCIRQ*	28-C2, 30-D4, 50-C3
CHP3 SATADET	28-C2, 39-B4, 50-C3
CHP3 SBPWRGD	28-D2, 45-A1, 50-C3
CHP3 SERIRQ	27-A2, 27-C1, 34-B2, 38-B3, 42-C2, 50-C3
CHP3 SLPS3*	28-D1, 28-D2, 42-A2
CHP3 SLPS5*	28-C1, 28-D2, 42-A2, 50-C3
CHP3 SPKR	28-A4, 37-A4, 50-C3
CHP3 SUSSTAT*	21-B4, 21-C4, 28-D1, 38-A4, 42-A2, 50-C3
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Signal Name	Sheet Number - Location
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CLK0 HOST NB*	7-C1, 15-C3
CLK1 27M VGA	21-B4, 23-D1
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CLK2 MEM0*	13-B3, 18-C4
CLK2 MEM1	13-B3, 18-C4
CLK2 MEM1*	13-B3, 18-C4
CLK2 MEM2	13-B3, 18-C4
CLK2 MEM2*	13-B3, 18-C4
CLK2 MEM3	13-B3, 18-C3
CLK2 MEM3*	13-B3, 18-C3
CLK2 MEM4	13-B3, 18-C3
CLK2 MEM4*	13-B3, 18-C3
CLK2 MEM5	13-B3, 18-C3
CLK2 MEM5*	13-B3, 18-C3
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CLK3 33M CB	27-D2, 34-C4, 34-C4
CLK3 33M FWH	27-D2, 31-B4
CLK3 33M LAN	27-D2, 36-A3, 36-B4
CLK3 33M MICOM	27-D2, 42-C2
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CLK3 66M NB	7-C1, 15-B3
CLK3 66M SB	7-A4, 7-C1, 27-D4
CLK3 DDR NB	7-C1, 15-B3
CLK3 OSC SB	7-D1, 28-A4
CLK3 PCLKSIO	27-D2, 38-A4
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FWH1 INIT*	27-B4, 31-C3, 50-C3
FWH3 WP TBL*	31-B4, 42-B4
GFX3 THERM*	23-B2, 42-B4
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HDD5 A1	28-C2, 39-C2, 50-C3
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HDD5 D(9)	28-C2, 39-D1, 50-B3
HDD5 D(12)	28-C2, 39-D1, 50-B3
HDD5 D(11)	28-C2, 39-D1, 50-B3
HDD5 D(4)	28-C2, 39-C2, 50-B3
HDD5 D(15)	28-C2, 39-D1, 50-B3
HDD5 D(13)	28-C2, 39-D1, 50-B3
HDD5 D(6)	28-C2, 39-C2, 50-B3
HDD5 D(7)	28-B1, 28-C2, 39-C2, 50-B3
HDD5 D(14)	28-C2, 39-D1, 50-B3
HDD5 D(5)	28-C2, 39-C2, 50-B3
HDD5 D(0)	28-C2, 39-C2, 50-B3
HDD5 D(10)	28-C2, 39-D1, 50-B3
HDD5 D(1)	28-C2, 39-C2, 50-B3
HDD5 D(2)	28-C2, 39-C2, 50-B3
HDD5 D(8)	28-C2, 39-D1, 50-B3
HDD5 D(7:0)	39-C2
HDD5 D(15:8)	39-D1
HDD5 D(15:0)	28-C2
HDD5 DACK*	28-C2, 39-C2, 50-B3
HDD5 DREQ*	28-C2, 39-C2, 50-B3
HDD5 IOR*	28-C2, 39-C2, 50-B3
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HDD5 IOW*	28-C2, 39-C2, 50-B3
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HOST1 A*(15)	8-C4, 12-D3
HOST1 A*(5)	8-C4, 12-D3
HOST1 A*(6)	8-C4, 12-D3
HOST1 A*(3)	8-C4, 12-D3
HOST1 A*(12)	8-C4, 12-D3
HOST1 A*(19)	8-C4, 12-D3
HOST1 A*(20)	8-C4, 12-D3
HOST1 A*(9)	8-C4, 12-D3
HOST1 A*(14)	8-C4, 12-D3
HOST1 A*(7)	8-C4, 12-D3
HOST1 A*(16)	8-C4, 12-D3
HOST1 A*(18)	8-C4, 12-D3
HOST1 A*(29)	8-C4, 12-D3
HOST1 A*(8)	8-C4, 12-D3
HOST1 A*(11)	8-C4, 12-D3
HOST1 A*(27)	8-C4, 12-D3

Signal Name	Sheet Number - Location
HOST1 A*(31)	8-C4, 12-D3
HOST1 A*(28)	8-C4, 12-D3
HOST1 A*(17)	8-C4, 12-D3
HOST1 A*(4)	8-C4, 12-D3
HOST1 A*(26)	8-C4, 12-D3
HOST1 A*(10)	8-C4, 12-D3
HOST1 A*(23)	8-C4, 12-D3
HOST1 A*(22)	8-C4, 12-D3
HOST1 A*(13)	8-C4, 12-D3
HOST1 A*(25)	8-C4, 12-D3
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HOST1 A*(31:3)	8-C4, 12-D3
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HOST1 ADS*	8-C3, 12-C3
HOST1 ADSTB0*	8-C4, 12-C3
HOST1 ADSTB1*	8-B4, 12-C3
HOST1 BNR*	8-C3, 12-C3
HOST1 BPRI*	8-C3, 12-C3
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HOST1 CPURST*	8-C3, 12-B3
HOST1 D*(3)	8-C2, 12-D2
HOST1 D*(35)	8-C1, 12-D2
HOST1 D*(2)	8-C2, 12-D2
HOST1 D*(21)	8-C2, 12-D2
HOST1 D*(32)	8-C1, 12-D2
HOST1 D*(27)	8-C2, 12-D2
HOST1 D*(26)	8-C2, 12-D2
HOST1 D*(11)	8-C2, 12-D2
HOST1 D*(57)	8-C1, 12-D2
HOST1 D*(53)	8-C1, 12-D2
HOST1 D*(38)	8-C1, 12-D2
HOST1 D*(25)	8-C2, 12-D2
HOST1 D*(24)	8-C2, 12-D2
HOST1 D*(28)	8-C2, 12-D2
HOST1 D*(59)	8-C1, 12-D2
HOST1 D*(46)	8-C1, 12-D2
HOST1 D*(6)	8-C2, 12-D2
HOST1 D*(42)	8-C1, 12-D2
HOST1 D*(41)	8-C1, 12-D2
HOST1 D*(40)	8-C1, 12-D2
HOST1 D*(16)	8-C2, 12-D2
HOST1 D*(55)	8-C1, 12-D2
HOST1 D*(54)	8-C1, 12-D2

Signal Name	Sheet Number - Location
HOST1 D*(39)	8-C1, 12-D2
HOST1 D*(31)	8-C2, 12-D2
HOST1 D*(10)	8-C2, 12-D2
HOST1 D*(19)	8-C2, 12-D2
HOST1 D*(50)	8-C1, 12-D2
HOST1 D*(49)	8-C1, 12-D2
HOST1 D*(34)	8-C1, 12-D2
HOST1 D*(8)	8-C2, 12-D2
HOST1 D*(7)	8-C2, 12-D2
HOST1 D*(36)	8-C1, 12-D2
HOST1 D*(4)	8-C2, 12-D2
HOST1 D*(1)	8-C2, 12-D2
HOST1 D*(5)	8-C2, 12-D2
HOST1 D*(17)	8-C2, 12-D2
HOST1 D*(58)	8-C1, 12-D2
HOST1 D*(37)	8-C1, 12-D2
HOST1 D*(63)	8-C1, 12-D2
HOST1 D*(61)	8-C1, 12-D2
HOST1 D*(47)	8-C1, 12-D2
HOST1 D*(15)	8-C2, 12-D2
HOST1 D*(22)	8-C2, 12-D2
HOST1 D*(20)	8-C2, 12-D2
HOST1 D*(62)	8-C1, 12-D2
HOST1 D*(14)	8-C2, 12-D2
HOST1 D*(44)	8-C1, 12-D2
HOST1 D*(0)	8-C2, 12-D2
HOST1 D*(43)	8-C1, 12-D2
HOST1 D*(51)	8-C1, 12-D2
HOST1 D*(56)	8-C1, 12-D2
HOST1 D*(48)	8-C1, 12-D2
HOST1 D*(45)	8-C1, 12-D2
HOST1 D*(18)	8-C2, 12-D2
HOST1 D*(29)	8-C2, 12-D2
HOST1 D*(12)	8-C2, 12-D2
HOST1 D*(60)	8-C1, 12-D2
HOST1 D*(13)	8-C2, 12-D2
HOST1 D*(52)	8-C1, 12-D2
HOST1 D*(23)	8-C2, 12-D2
HOST1 D*(33)	8-C1, 12-D2
HOST1 D*(9)	8-C2, 12-D2
HOST1 D*(30)	8-C2, 12-D2
HOST1 D*(63:0)	12-D2
HOST1 D*(63:48)	8-C1
HOST1 D*(31:16)	8-C2

Signal Name	Sheet Number - Location
HOST1 D*(15:0)	8-C2
HOST1 D*(47:32)	8-C1
HOST1 DBI0*	8-C2, 12-C2
HOST1 DBI1*	8-B2, 12-C2
HOST1 DBI2*	8-C1, 12-B2
HOST1 DBI3*	8-B1, 12-A2
HOST1 DBSY*	8-C3, 12-B3
HOST1 DEFER*	8-C3, 12-B3
HOST1 DPSLP*	9-D4, 11-?3
HOST1 DPWR*	9-D4, 12-B3
HOST1 DRDY*	8-C3, 12-B3
HOST1 DSTBN0*	8-C2, 12-C2
HOST1 DSTBN1*	8-B2, 12-C2
HOST1 DSTBN2*	8-C1, 12-B2
HOST1 DSTBN3*	8-B1, 12-A2
HOST1 DSTBP0*	8-C2, 12-C2
HOST1 DSTBP1*	8-B2, 12-C2
HOST1 DSTBP2*	8-C1, 12-B2
HOST1 DSTBP3*	8-B1, 12-A2
HOST1 FERR*	8-B3, 11-?4, 50-B3
HOST1 GTLREF0	9-A3, 9-C2
HOST1 HIT*	8-C3, 12-B3, 50-B3
HOST1 HITM*	8-C3, 12-B3, 50-B3
HOST1 IGNNE*	8-B3, 10-B3, 27-B4, 50-A3
HOST1 INIT*	8-C3, 10-B3, 27-B4, 50-A3
HOST1 INTR	8-B3, 10-B3, 27-B4, 50-A3
HOST1 LOCK*	8-C3, 12-B3, 50-A3
HOST1 NMI	8-B3, 10-B3, 27-B4, 50-A3
HOST1 PSI*	9-B4, 46-C4
HOST1 REQ*(4)	8-C4, 12-C3
HOST1 REQ*(2)	8-C4, 12-C3
HOST1 REQ*(1)	8-C4, 12-C3
HOST1 REQ*(0)	8-C4, 12-C3
HOST1 REQ*(3)	8-C4, 12-C3
HOST1 REQ*(4:0)	8-C4, 12-C3
HOST1 RS*(0)	8-B3, 12-B3
HOST1 RS*(1)	8-B3, 12-B3
HOST1 RS*(2)	8-B3, 12-B3
HOST1 RS*(2:0)	8-B3, 12-B3
HOST1 SLP*	9-D4, 10-B3, 27-B4, 50-A3
HOST1 SMI*	8-B3, 10-B3, 27-B4, 50-A3
HOST1 STPCLK*	8-B3, 10-B3, 27-A4, 50-A3
HOST1 TCK	9-B2, 10-B3, 50-A3
HOST1 TDI	9-B2, 10-B3, 50-A3

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HOST1 TMS	9-B2, 10-B3, 50-A3
HOST1 TRDY*	8-C3, 12-B3, 50-A3
HOST1 TRST*	9-B2, 10-B3, 50-A3
HOST2 THERMDA	9-C4, 11-?4, 50-D3
HOST2 THERMDC	9-C4, 11-?4, 50-D3
HOST3 CPUSTOP*	11-?4, 15-B1, 27-B4, 46-C4
HOST3 CPUSTOP NB*	7-C4, 15-B1, 50-D3
HOST3 FERR*	11-?3, 27-A4, 50-D3
HOST3 VID(5)	9-C4, 46-A2, 46-B1, 50-D3
HOST3 VID(2)	9-C4, 46-B1, 50-D3
HOST3 VID(0)	9-C4, 46-B1, 50-D3
HOST3 VID(3)	9-C4, 46-B1, 50-D3
HOST3 VID(4)	9-C4, 46-B1, 50-D3
HOST3 VID(1)	9-C4, 46-B1, 50-D3
HOST3 VID(5:0)	9-C4
HP5 LINE OUT L	37-C4, 38-D2, 50-D3
HP5 LINE OUT R	37-C4, 38-D2, 50-D3
HP DETECT	37-C2, 37-C3, 38-D2, 50-D3
IDE3 RST*	27-B1, 39-D2, 39-D4
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KBC3 A20G	28-D2, 42-B2, 42-C1, 50-D3
KBC3 BKLTON	25-B2, 42-C2, 50-D3
KBC3 BRIT	25-C2, 42-B2, 50-D3
KBC3 CAPSLED*	41-B2, 42-C4, 50-D3
KBC3 CHGEN	42-C2, 44-B4, 50-D3
KBC3 CPURST*	28-D2, 42-B2, 42-C1, 50-C3
KBC3 CPUVRON	42-B1, 46-A4, 50-C3
KBC3 DELAY PWRGD	42-C2, 45-A2, 50-C3
KBC3 EXTSMI*	28-D2, 38-A3, 42-C4, 50-C3
KBC3 FANCTRL	41-C3, 42-B2, 50-C3
KBC3 IMVP4 PWRGD	42-B2, 45-C2, 50-C3
KBC3 IVTPWRON	25-D3, 42-B4
KBC3 LBLED*	41-A4, 42-C4, 50-C3
KBC3 NUMLED*	41-B2, 42-C4, 50-C3
KBC3 PWRGD	34-C4, 42-C4, 50-C3
KBC3 PWRON	34-D2, 42-C4, 43-B4, 43-C4, 45-C1, 45-D4, 48-A3, 48-B3, 49-A4, 49-B1, 50-C3
KBC3 PWRON*	45-C2, 45-C4, 45-D4
KBC3 PWRSW*	41-C2, 42-B2, 42-D1, 42-D4, 50-C3, 51-D3

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KBC3 PWRSW SB*	28-D2, 42-B2, 42-C1, 50-C3
KBC3 QS*	42-C2, 44-B4, 50-C3
KBC3 RSMRST*	27-A4, 42-C2, 50-C3
KBC3 RST*	42-D1, 42-D4, 45-B4, 50-C3
KBC3 RUNSCI*	28-C2, 42-C4, 50-C3
KBC3 SCL	42-A2, 42-C1, 44-C1, 50-C3
KBC3 SCLED*	41-A2, 42-C4, 50-C3
KBC3 SDA	42-A2, 42-C1, 44-C1, 50-C3
KBC3 SPKMUTE	37-B2, 42-B2, 50-C3
KBC3 SUSPWR	42-B2, 43-C1, 43-D1, 45-B3, 48-C4, 49-B4
KBC3 THERM*	28-D2, 42-A2
KBC3 THERM SCL	11-?3, 42-A2, 50-C3
KBC3 THERM SDA	11-?3, 42-C2, 50-C3
KBC3 TPAD*	41-B4, 42-C4, 50-C3
KBC3 VGAPWRON	42-C4, 43-A4, 48-A3
KBC3 VRON	42-C1, 42-C2, 46-A4, 47-C2, 47-C4, 50-C3
KBC3 WAKESCI*	28-C1, 28-C2, 42-B2, 50-C3
KBC3 WLAN*	32-C4, 41-B4, 42-A2, 50-C3
KBC5 KSI(3)	38-D4, 42-B4, 50-B3
KBC5 KSI(5)	38-D4, 42-B4, 50-B3
KBC5 KSI(2)	38-D4, 42-B4, 50-B3
KBC5 KSI(0)	38-D4, 42-B4, 50-C3
KBC5 KSI(7)	38-D4, 42-B4, 50-B3
KBC5 KSI(4)	38-D4, 42-B4, 50-B3
KBC5 KSI(6)	38-D4, 42-B4, 50-B3
KBC5 KSI(1)	38-D4, 42-B4, 50-C3
KBC5 KSI(7:0)	38-D4, 42-B4
KBC5 KSO(5)	38-D4, 42-B4, 50-B3
KBC5 KSO(1)	38-D4, 42-B4, 50-B3
KBC5 KSO(2)	38-D4, 42-B4, 50-B3
KBC5 KSO(10)	38-D4, 42-B4, 50-B3
KBC5 KSO(15)	38-D4, 42-B4, 50-B3
KBC5 KSO(11)	38-D4, 42-B4, 50-B3
KBC5 KSO(9)	38-D4, 42-B4, 50-B3
KBC5 KSO(4)	38-D4, 42-B4, 50-B3
KBC5 KSO(13)	38-D4, 42-B4, 50-B3
KBC5 KSO(6)	38-D4, 42-B4, 50-B3
KBC5 KSO(7)	38-D4, 42-B4, 50-B3
KBC5 KSO(14)	38-D4, 42-B4, 50-B3
KBC5 KSO(0)	38-D4, 42-B4, 50-B3
KBC5 KSO(3)	38-D4, 42-B4, 50-B3
KBC5 KSO(8)	38-D4, 42-B4, 50-B3

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KBC5 KSO(12)	38-D4, 42-B4, 50-B3
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KBC5 TDATA	38-B2, 42-C4
LAN3 EECK	28-B4, 30-B4, 50-B3
LAN3 EEDO	28-B4, 30-D4, 50-B3
LAN3 MDCK	28-C4, 30-B4, 50-B3
LAN3 PHYPD	28-B4, 30-B4, 50-B3
LAN3 TXD0	28-B4, 30-D4, 50-B3
LAN3 TXD1	28-B4, 30-D4, 50-B3
LAN3 TXD2	28-B4, 30-D4, 50-A3
LAN3 TXD3	28-B4, 30-D4, 50-A3
LAN3 TXEN	28-B4, 30-D4, 50-A3
LCD3 BKLTON	25-B1, 25-D4, 50-A3
LCD3 BRIT	25-C1, 25-D4, 50-A3
LCD3 TYPE	25-C4, 42-B4
LED3 CHARGE	41-C2, 42-C2, 50-A3
LFM*	46-A2, 46-D4
LID3 SWITCH*	41-B3, 42-B2, 50-A3
LPC3 AD(2)	27-B2, 31-A3, 31-B3, 38-B4, 42-C2, 50-A3
LPC3 AD(3)	27-B2, 31-A3, 31-B3, 38-B4, 42-C2, 50-A3
LPC3 AD(1)	27-B2, 31-A3, 31-B3, 38-B4, 42-C2, 50-A3
LPC3 AD(0)	27-B2, 31-A3, 31-B3, 38-B4, 42-C2, 50-A3
LPC3 AD(3:0)	27-B2, 31-A3, 31-B3, 38-B4, 42-C2
LPC3 FRAME*	27-B2, 31-B3, 38-B4, 42-C2, 50-A3
LPC3 LDRQ0*	27-B2, 38-B3
LPC3 RST*	27-C1, 31-B4, 42-C2
LPC3 SMI*	28-C1, 28-D2, 50-A3
LUSB	33-B4, 42-D2
LVDS1 L0N	15-C2, 21-C1, 25-C4
LVDS1 L0P	15-C2, 21-C1, 25-C4
LVDS1 L1N	15-C2, 21-C1, 25-C4
LVDS1 L1P	15-C2, 21-C1, 25-C4
LVDS1 L2N	15-C2, 21-B1, 25-C4
LVDS1 L2P	15-C2, 21-B1, 25-C4
LVDS1 LCLKN	15-C2, 21-B1, 25-C4
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Signal Name	Sheet Number - Location
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MEM2 A(7)	13-D3, 18-D4, 20-C4
MEM2 A(5)	13-D3, 18-D4, 20-C4
MEM2 A(1)	13-D3, 18-D4, 20-C4
MEM2 A(6)	13-D3, 18-D4, 20-C4
MEM2 A(13)	13-D3, 18-D4, 20-C4
MEM2 A(9)	13-D3, 18-D4, 20-C4
MEM2 A(15)	13-D3, 18-A2, 18-D4, 20-C4
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MEM2 CKE2	13-B3, 18-C3, 20-C2
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Signal Name	Sheet Number - Location
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MEM2 D(2)	13-D2, 18-D2, 18-D3, 19-D4
MEM2 D(51)	13-D2, 18-D2, 18-D3, 19-D4
MEM2 D(18)	13-D2, 18-D2, 18-D3, 19-D4
MEM2 D(8)	13-D2, 18-D2, 18-D3, 19-D4
MEM2 D(6)	13-D2, 18-D2, 18-D3, 19-D4
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MEM2 D(58)	13-D2, 18-D2, 18-D3, 19-D4
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MEM2 D(13)	13-D2, 18-D2, 18-D3, 19-D4
MEM2 D(29)	13-D2, 18-D2, 18-D3, 19-D4
MEM2 D(11)	13-D2, 18-D2, 18-D3, 19-D4
MEM2 D(14)	13-D2, 18-D2, 18-D3, 19-D4
MEM2 D(43)	13-D2, 18-D2, 18-D3, 19-D4
MEM2 D(50)	13-D2, 18-D2, 18-D3, 19-D4
MEM2 D(28)	13-D2, 18-D2, 18-D3, 19-D4
MEM2 D(38)	13-D2, 18-D2, 18-D3, 19-D4
MEM2 D(36)	13-D2, 18-D2, 18-D3, 19-D4
MEM2 D(63)	13-D2, 18-D2, 18-D3, 19-D4
MEM2 D(41)	13-D2, 18-D2, 18-D3, 19-D4
MEM2 D(1)	13-D2, 18-D2, 18-D3, 19-D4
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MEM2 D(59)	13-D2, 18-D2, 18-D3, 19-D4
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MEM2 D(60)	13-D2, 18-D2, 18-D3, 19-D4

Signal Name	Sheet Number - Location
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MEM2 D(9)	13-D2, 18-D2, 18-D3, 19-D4
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MEM2 D(10)	13-D2, 18-D2, 18-D3, 19-D4
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MEM2 DM(6)	13-C3, 18-B3, 18-B4, 19-B2
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MEM2 DQS(4)	13-C3, 18-B3, 18-B4, 19-C2
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MEM2 RA(3)	18-D3, 20-D3
MEM2 RA(6)	18-D3, 20-D3
MEM2 RA(12)	18-D3, 20-D3
MEM2 RA(9)	18-D3, 20-D3
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MEM2 RA(5)	18-D3, 20-D3
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PCI3 AD(17)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-D2
PCI3 AD(21)	27-D2, 32-D4, 33-D4, 34-D4, 36-B4, 36-D4, 50-D2
PCI3 AD(28)	27-D2, 30-B4, 32-D4, 33-D4, 34-D4, 36-D4, 50-C2
PCI3 AD(19)	27-D2, 32-C2, 32-D4, 33-D4, 34-D4, 36-D4, 50-D2
PCI3 AD(4)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-C2
PCI3 AD(6)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-C2
PCI3 AD(22)	27-D2, 32-D4, 33-B4, 33-D4, 34-D4, 36-D4, 50-D2
PCI3 AD(31)	27-D2, 30-B4, 32-D4, 33-D4, 34-D4, 36-D4, 50-C2
PCI3 AD(30)	27-D2, 30-B4, 32-D4, 33-D4, 34-D4, 36-D4, 50-C2
PCI3 AD(20)	27-D2, 32-D4, 33-D4, 34-B4, 34-D4, 36-D4, 50-D2
PCI3 AD(18)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-D2
PCI3 AD(26)	27-D2, 30-B4, 32-D4, 33-D4, 34-D4, 36-D4, 50-C2
PCI3 AD(10)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-D2
PCI3 AD(15)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-D2
PCI3 AD(29)	27-D2, 30-B4, 32-D4, 33-D4, 34-D4, 36-D4, 50-C2

Signal Name	Sheet Number - Location
PCI3 AD(25)	27-D2, 30-B4, 32-D4, 33-D4, 34-D4, 36-D4, 50-C2
PCI3 AD(7)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-C2
PCI3 AD(5)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-C2
PCI3 AD(13)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-D2
PCI3 AD(23)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-D2
PCI3 AD(11)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-D2
PCI3 AD(1)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-D2
PCI3 AD(3)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-C2
PCI3 AD(0)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-D2
PCI3 AD(14)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-D2
PCI3 AD(9)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-C2
PCI3 AD(24)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-C2
PCI3 AD(16)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-D2
PCI3 AD(12)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-D2
PCI3 AD(2)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-D2
PCI3 AD(8)	27-D2, 32-D4, 33-D4, 34-D4, 36-D4, 50-C2
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PCI3 GNT1*	27-B2, 27-D1, 34-B4, 50-C2
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9. Schematic Diagram

9-2 SIO SUB BOARD

9-2-1 Schematic Diagram

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Oscar-G

CPU : Intel P-M
Chip Set : ATI RC300MD + IXP150
Remarks : Sub system for Super I/O

Model Name : SIO sub Board
PBA Name :
PCB Code : BA41-00477A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2004-12-09

DRAW	CHECK	APPROVAL

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DRAW: Zhou & Guo	DATE: 12/9/2004	TITLE: Oscar-G SIO SUB BOARD COVER	SAMSUNG ELECTRONICS
CHECK: Antonio	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-00477A
MODULE CODE:	LAST EDIT: December 9, 2004 9:47:51 AM	PAGE 1 OF 4	

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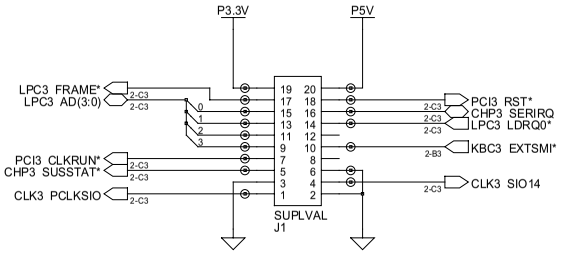
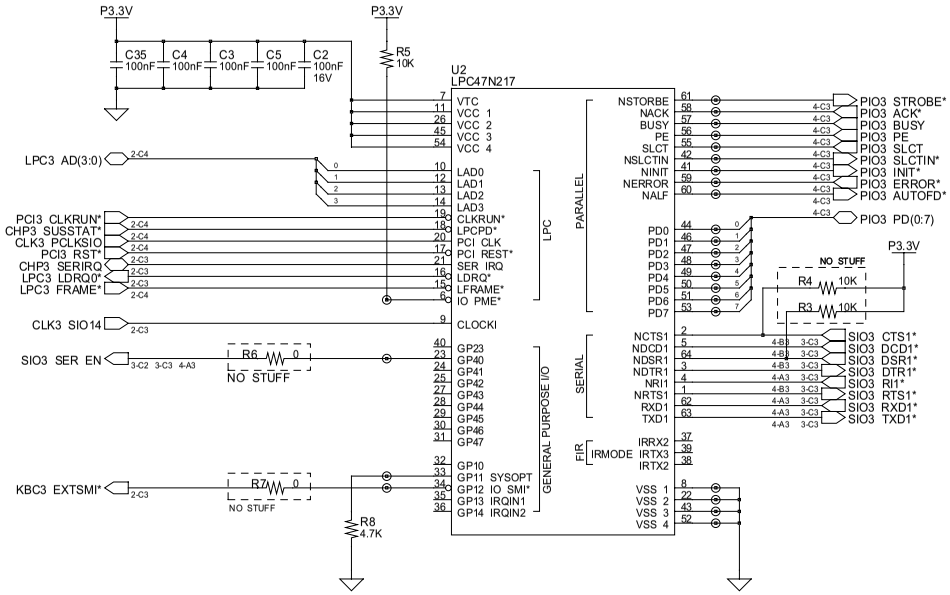
B'd to B'd CONN



Pin12 is the key of J1

Simple LPC Super I/O



DRAW: Zhou & Guo	DATE: 12/9/2004	TITLE: Oscar-G	SAMSUNG ELECTRONICS
CHECK: Antonio	DEV. STEP: MP	SIO SUB BOARD	
APPROVAL: KEVIN LEE	REV: 1.0	B'd to B'd CONN, Super I/O	PART NO.: BA41-00477A
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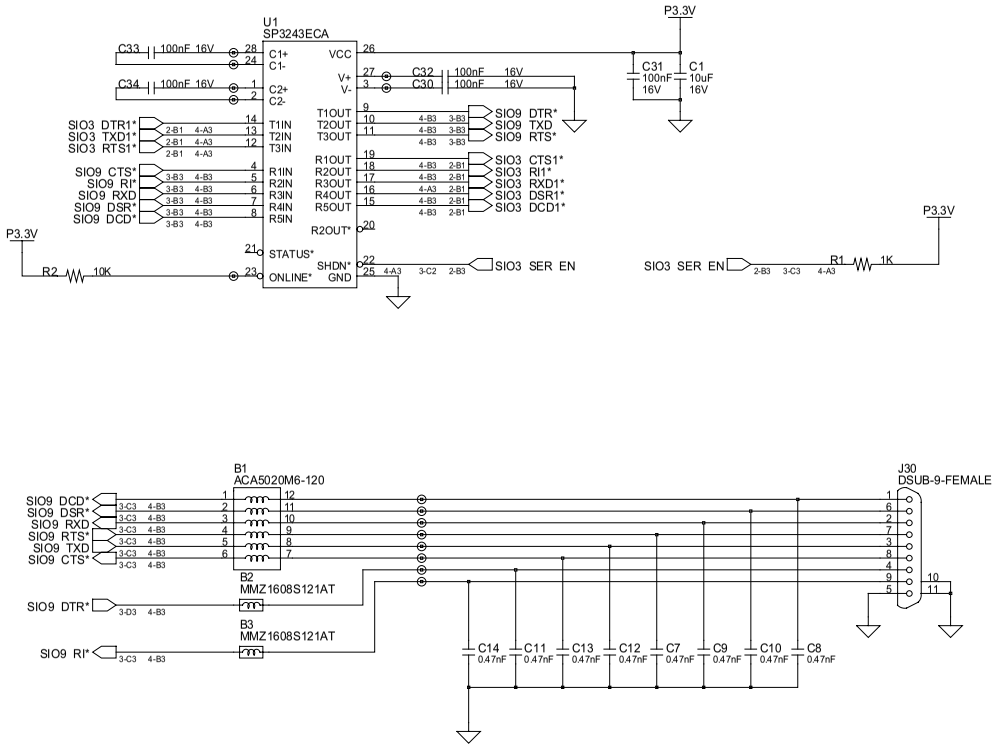

DRAW: Zhou & Guo	DATE: 12/9/2004	TITLE: Oscar-G	SAMSUNG ELECTRONICS
CHECK: Antonio	DEV. STEP: MP	SIO SUB BOARD	
APPROVAL: KEVIN LEE	REV: 1.0	Serial port	PART NO.: BA41-00477A
MODULE CODE:	LAST EDIT: December 9, 2004 9:47:51 AM	PAGE 3 OF 4	

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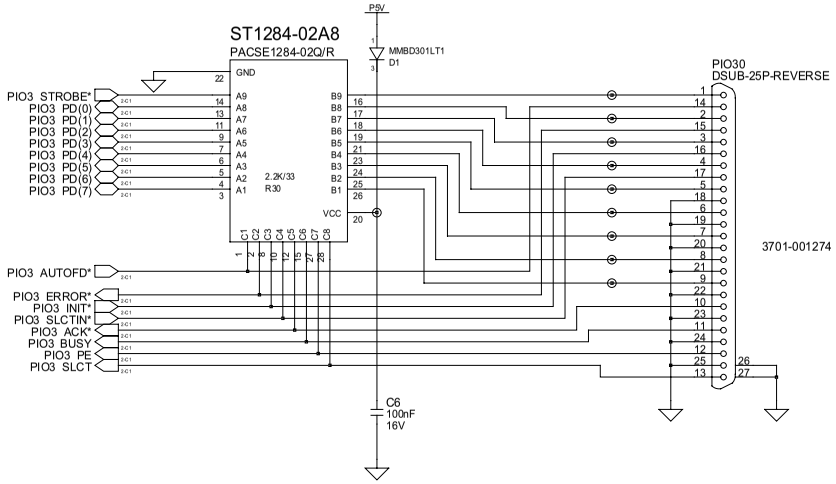
Parallel Port



TESTPOINT

TP69 SIO9 RI*
TP70 SIO9 RXD
TP71 SIO9 TXD
TP72 SIO3 RI1*
TP73 SIO9 CTS*
TP74 SIO9 DCD*
TP75 SIO9 DSR*
TP76 SIO9 DTR*
TP77 SIO9 RTS*
TP78 SIO3 CTS1*
TP79 SIO3 DCD1*
TP80 SIO3 DSR1*
TP81 SIO3 DTR1*
TP82 SIO3 RTS1*
TP83 SIO3 RXD1*
TP84 SIO3 TXD1*
TP85 SIO3 SER_EN

REV30

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.	04/12/09	1.0	MP
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.	04/11/08	1.1	PR
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

MT1
RMNT-35-60-1P

MT2
RMNT-35-60-1P

DRAW: Zhou & Guo	DATE: 12/9/2004	TITLE: Oscar-G / SIO SUB BOARD / PARALLEL PORT/Test point	SAMSUNG ELECTRONICS
CHECK: Antonio	DEV. STEP: MP		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-00477A
MODULE CODE:	LAST EDIT: December 9, 2004 9:47:51 AM	PAGE 4 OF 4	

9. Schematic Diagram

9-2 SIO SUB BOARD

9-2-2 Signal Location

9-2-2 Signal Location

Signal Name	Sheet Number - Location
CHP3 SERIRQ	2-C3, 2-C3
CHP3 SUSSTAT*	2-C3, 2-C4
CLK3 PCLKSIO	2-C3, 2-C4
CLK3 SIO14	2-C3, 2-C3
KBC3 EXTSMI*	2-B3, 2-C3
LPC3 AD(1)	2-C3, 2-C4
LPC3 AD(2)	2-C3, 2-C4
LPC3 AD(0)	2-C3, 2-C4
LPC3 AD(3)	2-C3, 2-C4
LPC3 AD(3:0)	2-C3, 2-C4
LPC3 FRAME*	2-C3, 2-C4
LPC3 LDRQ0*	2-C3, 2-C3
PCI3 CLKRUN*	2-C3, 2-C4
PCI3 RST*	2-C3, 2-C3
PIO3 ACK*	2-C1, 4-C3
PIO3 AUTOFD*	2-C1, 4-C3
PIO3 BUSY	2-C1, 4-C3
PIO3 ERROR*	2-C1, 4-C3
PIO3 INIT*	2-C1, 4-C3
PIO3 PD(7)	2-C1, 4-C3
PIO3 PD(3)	2-C1, 4-C3
PIO3 PD(5)	2-C1, 4-C3
PIO3 PD(4)	2-C1, 4-C3
PIO3 PD(0)	2-C1, 4-C3
PIO3 PD(1)	2-C1, 4-C3
PIO3 PD(2)	2-C1, 4-C3

Signal Name	Sheet Number - Location
PIO3 PD(6)	2-C1, 4-C3
PIO3 PD(0:7)	2-C1
PIO3 PE	2-C1, 4-C3
PIO3 SLCT	2-C1, 4-C3
PIO3 SLCTIN*	2-C1, 4-C3
PIO3 STROBE*	2-C1, 4-C3
SIO3 CTS1*	2-B1, 3-C3, 4-B3
SIO3 DCD1*	2-B1, 3-C3, 4-B3
SIO3 DSR1*	2-B1, 3-C3, 4-B3
SIO3 DTR1*	2-B1, 3-C3, 4-A3
SIO3 RI1*	2-B1, 3-C3, 4-B3
SIO3 RTS1*	2-B1, 3-C3, 4-A3
SIO3 RXD1*	2-B1, 3-C3, 4-A3
SIO3 SER EN	2-B3, 3-C2, 3-C3, 4-A3
SIO3 TXD1*	2-B1, 3-C3, 4-A3
SIO9 CTS*	3-B3, 3-C3, 4-B3
SIO9 DCD*	3-B3, 3-C3, 4-B3
SIO9 DSR*	3-B3, 3-C3, 4-B3
SIO9 DTR*	3-B3, 3-D3, 4-B3
SIO9 RI*	3-B3, 3-C3, 4-B3
SIO9 RTS*	3-B3, 3-C3, 4-B3
SIO9 RXD	3-B3, 3-C3, 4-B3
SIO9 TXD	3-B3, 3-C3, 4-B3