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# MACAO

CPU : STEALEY (A110)  
 Chip Set : 945GU + ICH7-U  
 Remarks : Ultra Mobile PC  
 WSVGA, HSDPA, DMB

Model Name : MACAO  
 PBA Name : BA41-00743A  
 Dev. Step : SR  
 Revision : 0.1  
 T.R. Date : 2007.03.15

DRAW	CHECK	APPROVAL
W.S. Ko	H.K.Park	J.S. Euh

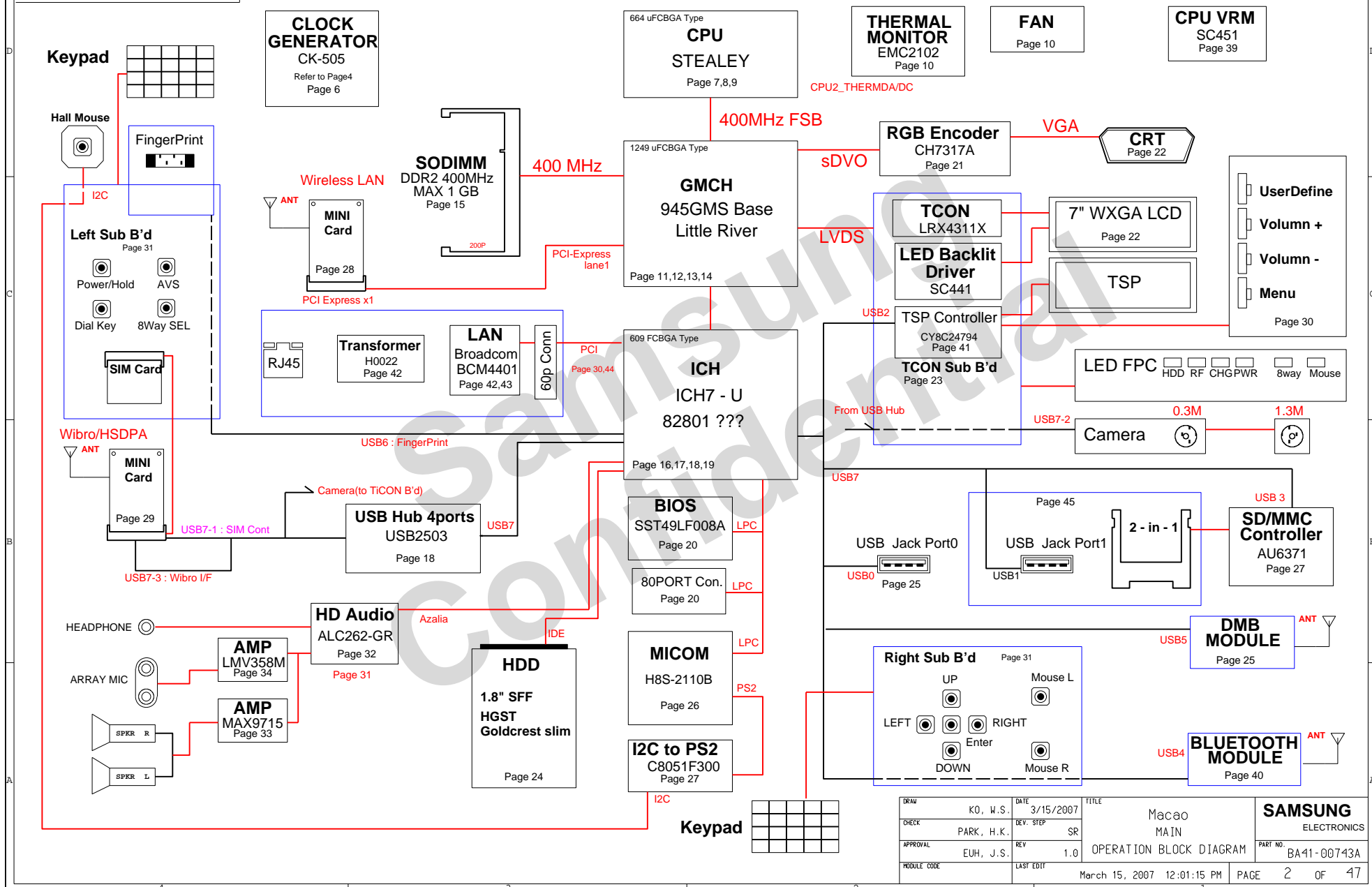
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# OPERATION BLOCK DIAGRAM

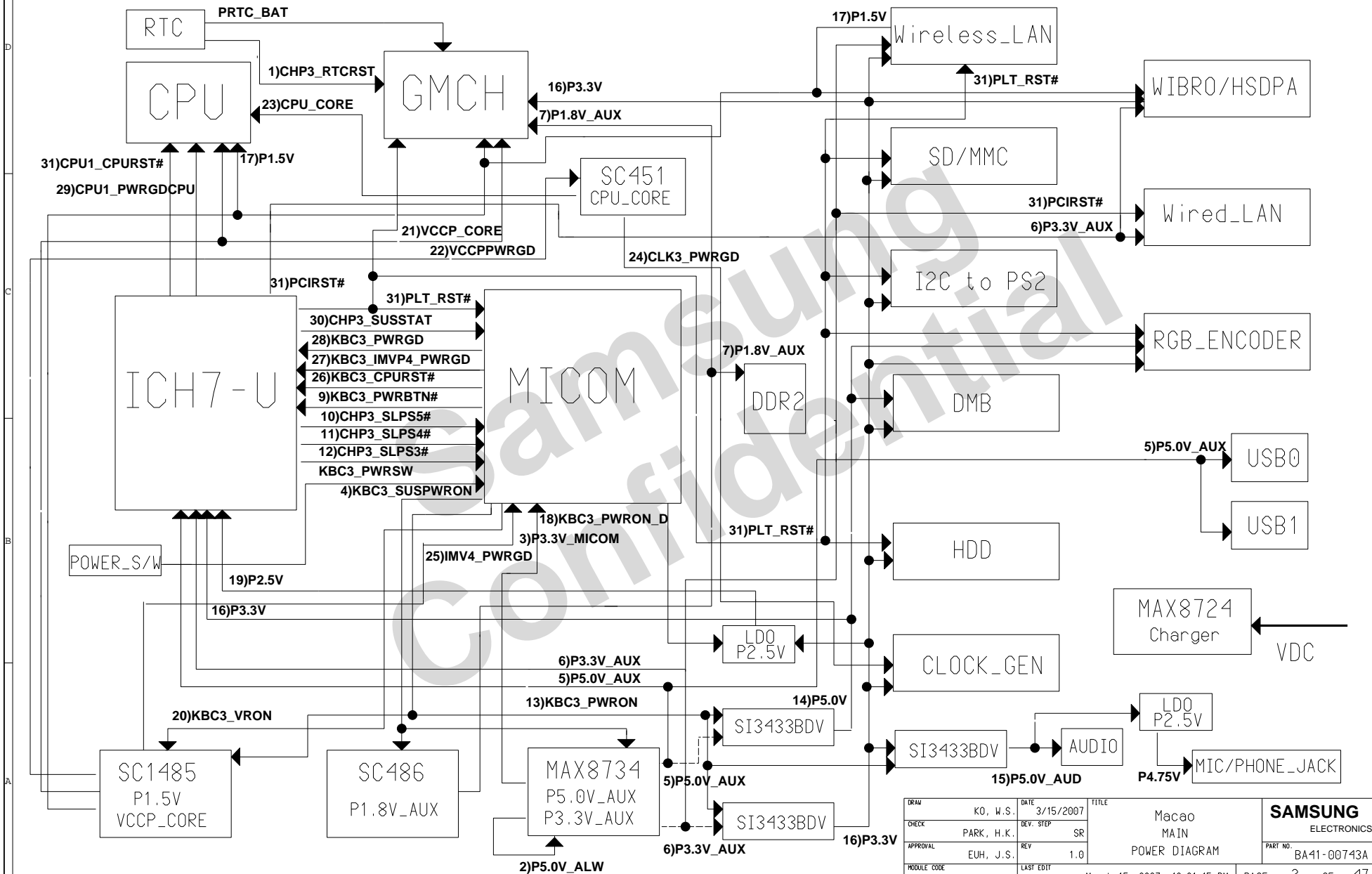


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# Power Sequence Block Diagram

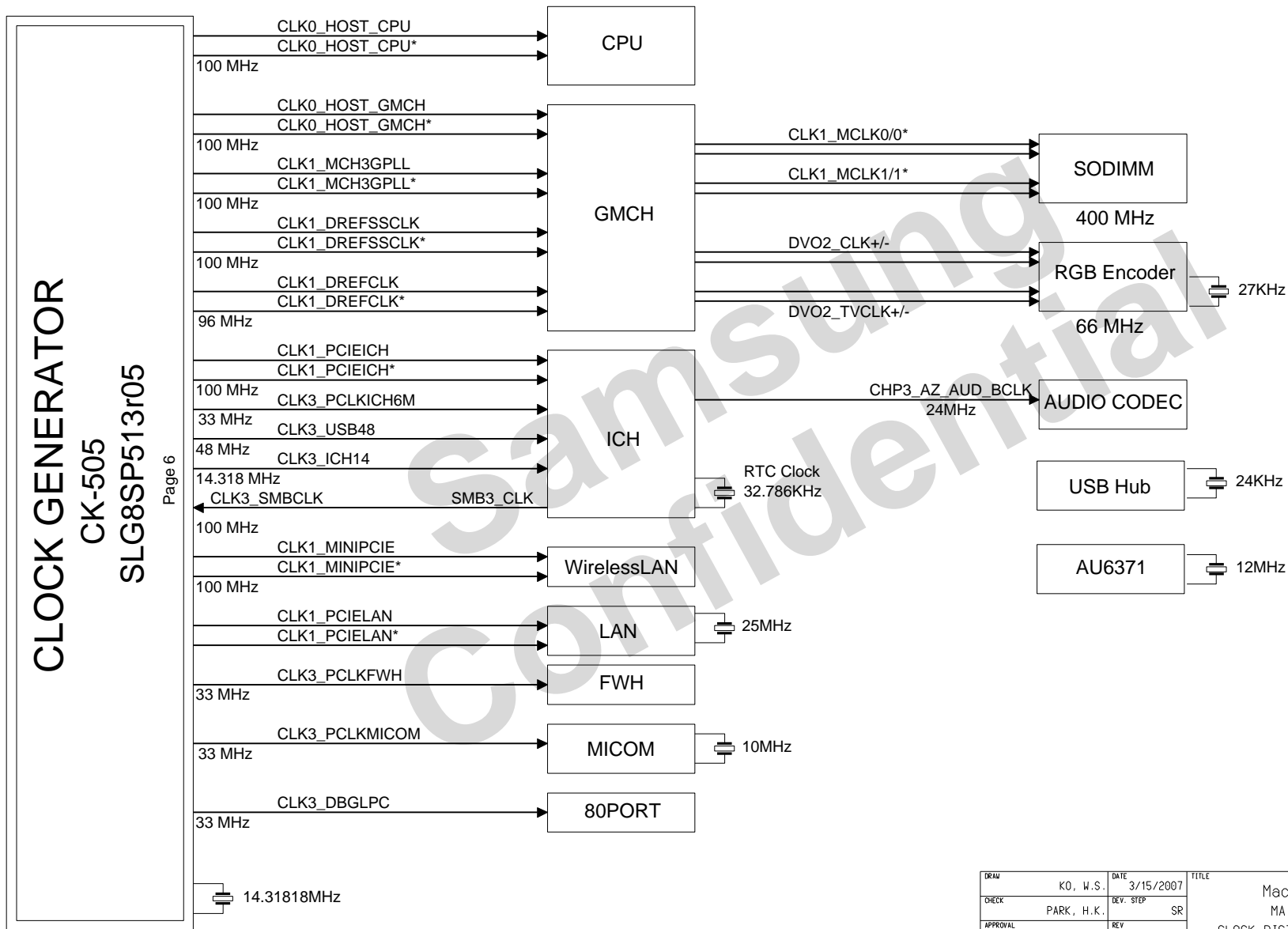


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# CLOCK DISTRIBUTION



**CLOCK GENERATOR**  
**CK-505**  
**SLG8SP513r05**

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# BOARD INFORMATION

## SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

### PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Wired LAN	AD21	3	G
USB Hub to PCI LPC Bridge/IDE/AC97/SMBUS	AD29(internal) AD30(internal) AD31(internal)	Programable	

### I<sup>2</sup>C / SMB Address

Devices	Address	Hex	Bus
<b>ICH6M</b>	<b>Master</b>	-	<b>SMBUS Master</b>
CK-510M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
SODIMMO	1010 000X	A0h	
USB Hub	1010 000X	A0h	
<b>MICOM</b>	<b>Master</b>		
BATTERY	0001 011h	16h	
THERMAL MORNORIT	x111 1010	7Ah	
HALL MOUSE	x001 1100	1Ch	

### USB PORT Assign

Port0	Right USB JACK
Port1	Left USB JACK
Port2	Touch Sensor Panel
Port3	SD/MMC Controller
Port4	Bluetooth
Port5	DMB
Port6	FingerPrint
Port7	USB Hub - 1. USIM Controller 2. Camera 3. Wibro / HSDPA

### System Power States

Power Rail	Devices (Page Number)
<b>P5V</b>	FAN(10) 80PORT(20) MICOM(25) DMB(25) RGB_ENCODER(21) AUDIO AMP(32)
<b>P3.3V</b>	CLOCK(6) Thermal sensor(10) SODIMM(15) ICH7(17) 80PORT(20) HDD(24)WIBRO/HSDPA(29)SD/MMC(27) MICOM(26) DMB(25) I2CtoPS2(24)GMCH(11)Wireless_LAN(28)
<b>P1.5V</b>	CPU(7) GMCH(11) ICH7(16) WIBRO/HSDPA(29)SC1485(37)
<b>P2.5V</b>	GMCH(11)ICH7(16)RGB_ENCODER(21)
<b>P5V_AUX</b>	ICH7(16) USB0(25)USB1(45)MAX8734(36)
<b>P3.3V_AUX</b>	ICH7(16)Wired_LAN(30) WIBRO/HSDPA(29)MAX8734(36)
<b>P1.8V_AUX</b>	GMCH(11) SODIMM(15) SC486(35)
<b>VCCP_CORE</b>	CPU(7) GMCH(11) ICH7(16) SC1485(37)
<b>VCC_CORE</b>	CPU(7)SC451(39)

### Voltage Rails

Power Rail	Descriptions
<b>PRTC_BAT VDC</b>	3.3V (can drop to 2.0V min. in G3 state) supply for the RTC well. Primary DC system power supply (6 to 19V)
<b>P5V_AUX</b> <b>P3.3V_AUX</b> <b>P1.8V_AUX</b>	5.0V power rail (off in S4-S5) 3.3V power rail (off in S4-S5) GMCH/DDR II Power Source(off in S4-S5)
<b>P5V</b> <b>P3.3V</b> <b>P1.5V</b> <b>P2.5V</b>	5.0V switched power rail (off in S3-S5) 3.3V switched power rail (off in S3-S5) 1.5V switched power rail (off in S3-S5) 2.5V LDO power rail (off in S3-S5)
<b>VCCP_CORE</b> <b>CPU_CORE</b>	1.05V power rail, GMCH core, CPU/GMCH FSB Termination. Core voltage for Stealey CPU (0.74~1.30V)
<b>P3.3V_MICOM</b> <b>P1.5V_DMI</b>	3.3V always on power rail for MICOM 1.5V (Direct Media Interface Compensation)
<b>LCD_VDD3V</b> <b>VCC_CRT</b>	3.3V (LCD) 5V (CRT)
<b>P4.75_AUD</b> <b>P5.0V_AMP</b>	4.75V (ALC262) 5V (Audio AMP)

### CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1	1.148 V
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V
0	0	0	1	0	1	1.628 V	1	0	0	0	1	1	1.116 V
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V
0	0	0	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V
0	0	1	1	0	1	1.500 V	1	0	1	1	1	0	0.988 V
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V
0	1	0	1	1	0	1.356 V	1	1	0	1	1	0	0.844 V
0	1	0	1	1	1	1.340 V	1	1	0	1	1	1	0.828 V
0	1	1	0	0	0	1.324 V	1	1	1	0	0	0	0.812 V
0	1	1	0	0	1	1.308 V	1	1	1	0	0	1	0.796 V
0	1	1	0	1	0	1.292 V	1	1	1	0	1	0	0.780 V
0	1	1	0	1	1	1.276 V	1	1	1	0	1	1	0.764 V
0	1	1	1	0	0	1.260 V	1	1	1	1	0	0	0.748 V
0	1	1	1	0	1	1.244 V	1	1	1	1	0	1	0.732 V
0	1	1	1	1	0	1.228 V	1	1	1	1	1	0	0.716 V
0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V

DOTHAN-ULV Base Stealey  
HIGH FREQUENCY MODE

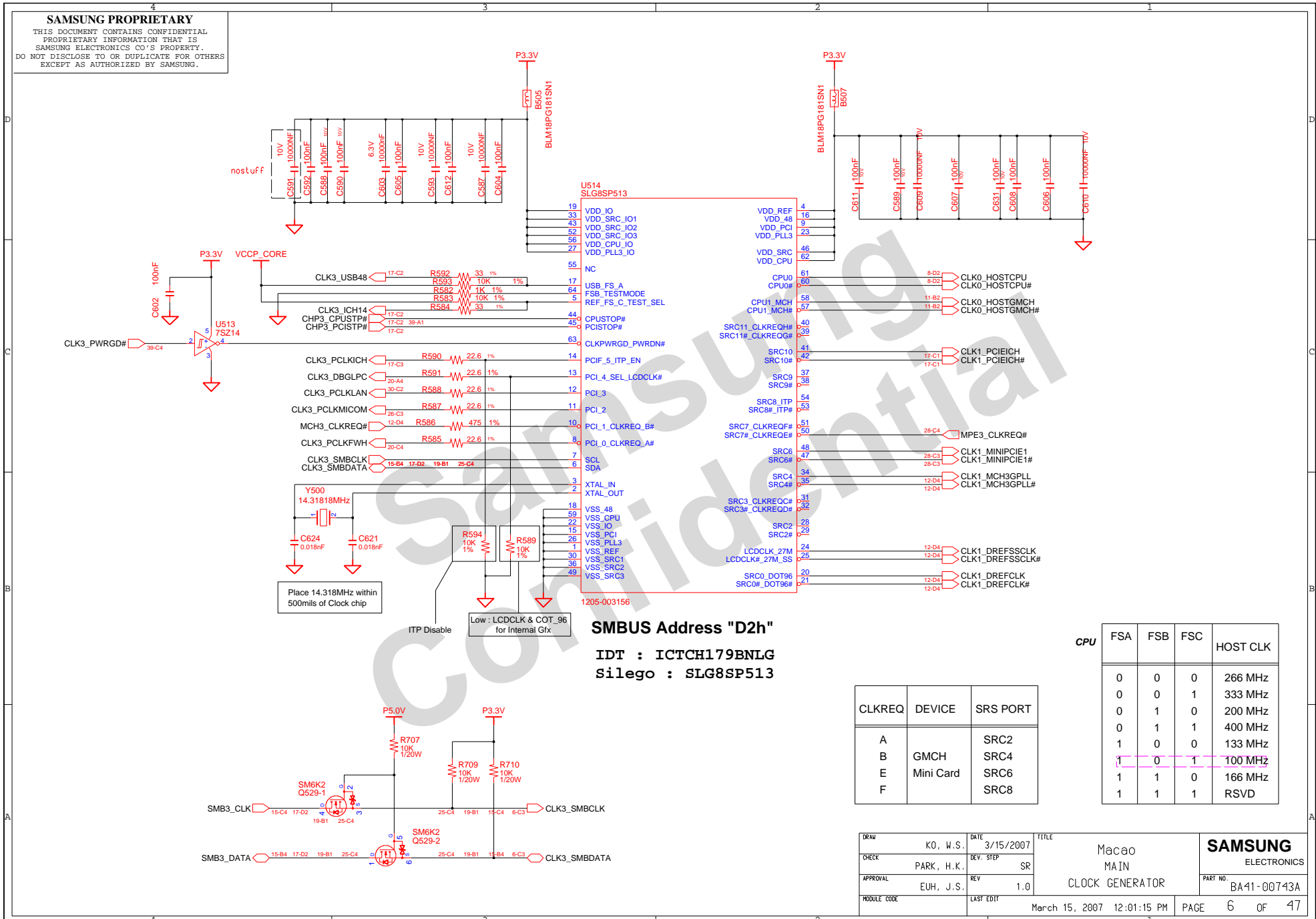
DOTHAN-ULV Base Stealey  
LOW FREQUENCY MODE

DOTHAN-ULV Base Stealey  
DEEPER SLEEP MODE  
Refer to page??

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Place 14.318MHz within 500mils of Clock chip

ITP Disable

Low : LCDCLK & COT\_96 for Internal Gix

**SMBUS Address "D2h"**

IDT : ICTCH179BNLG

Silego : SLG8SP513

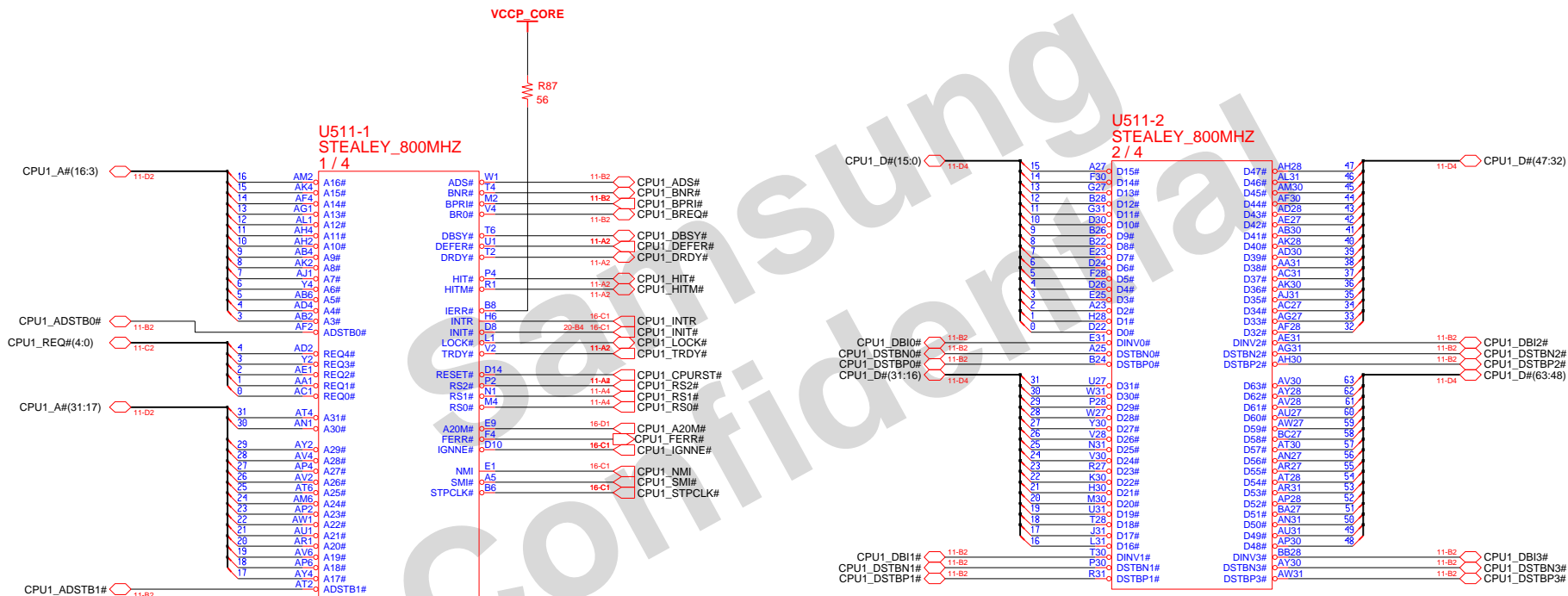
CLKREQ	DEVICE	SRS PORT
A	GMCH	SRC2
B	Mini Card	SRC4
E		SRC6
F		SRC8

CPU	FSA	FSB	FSC	HOST CLK
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD

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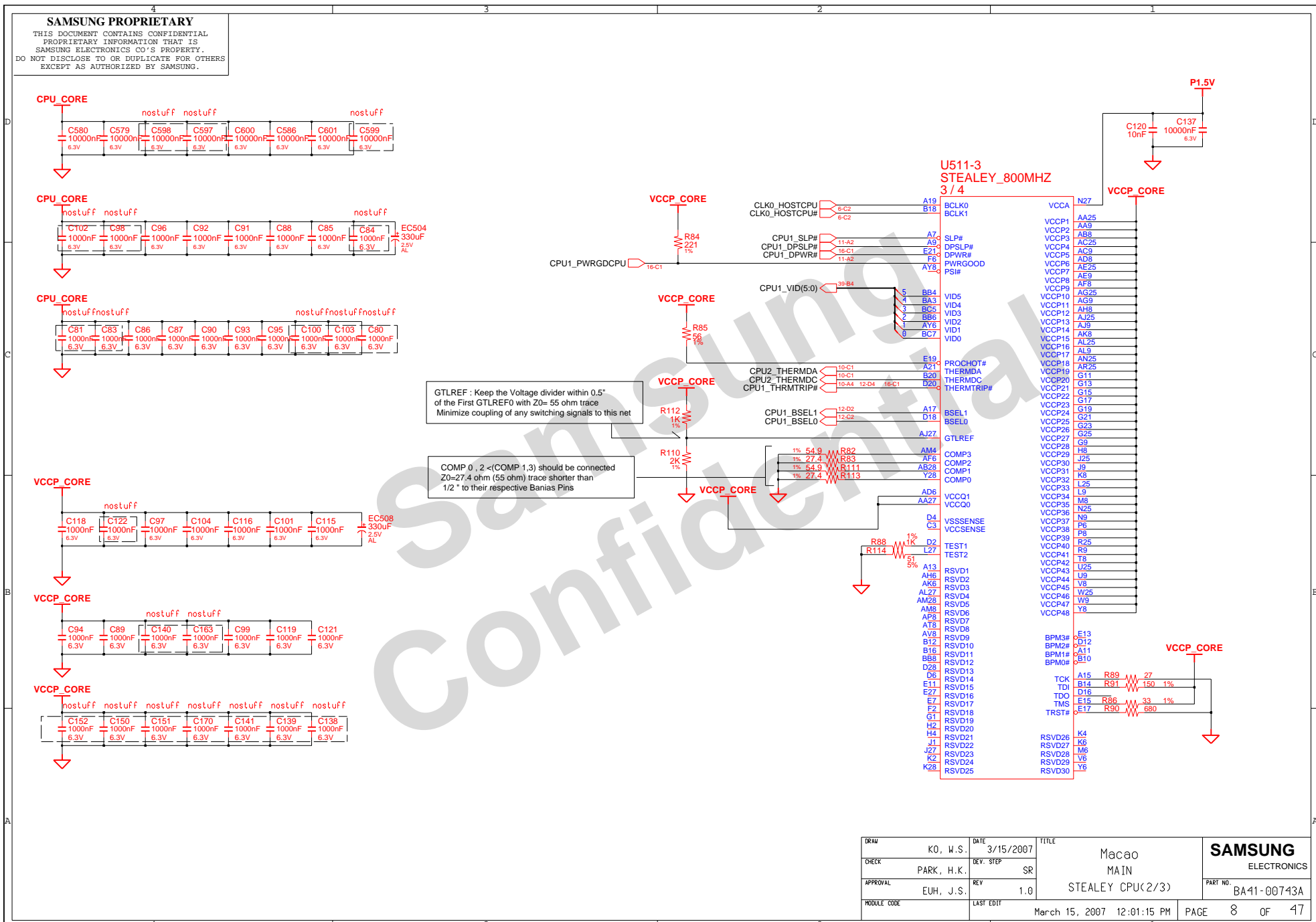
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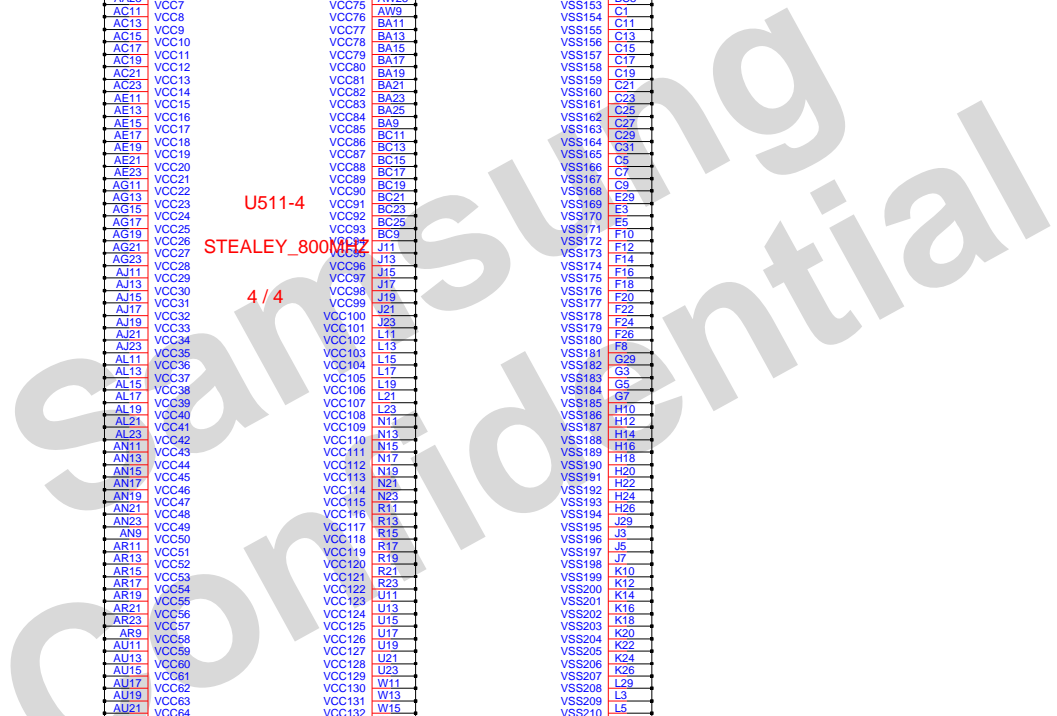


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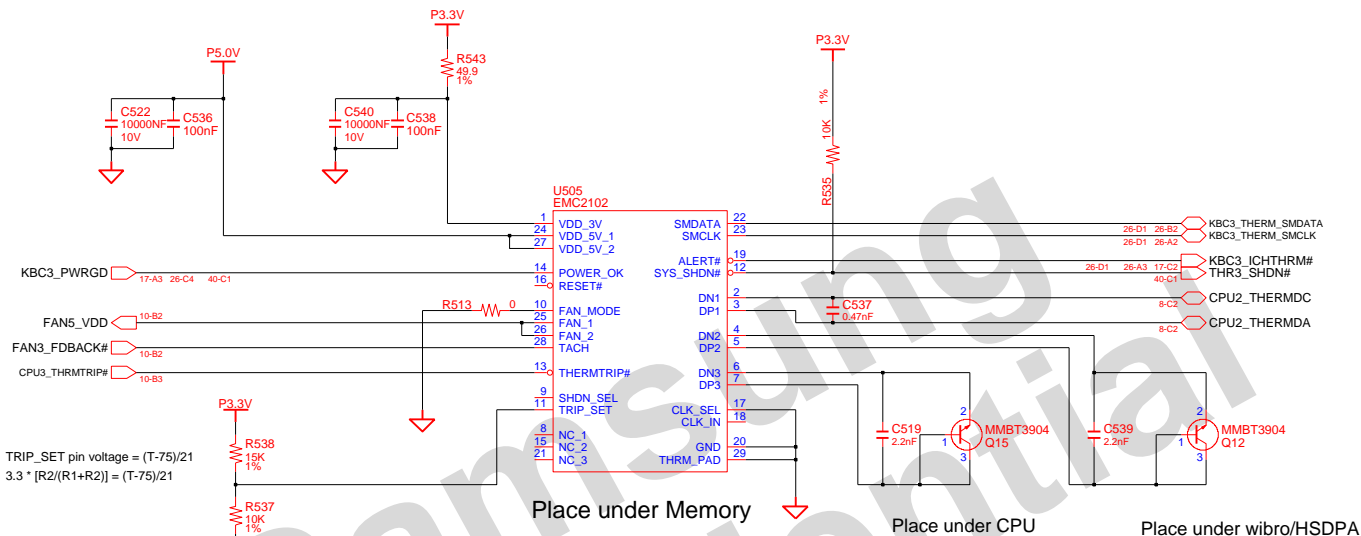
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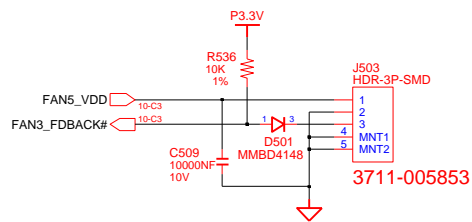
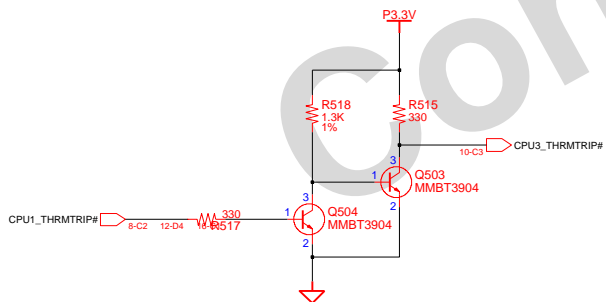
TRIP\_SET pin voltage =  $(T-75)/21$   
 $3.3 * [R2/(R1+R2)] = (T-75)/21$

Place under Memory

Place under CPU

Place under wibro/HSDPA

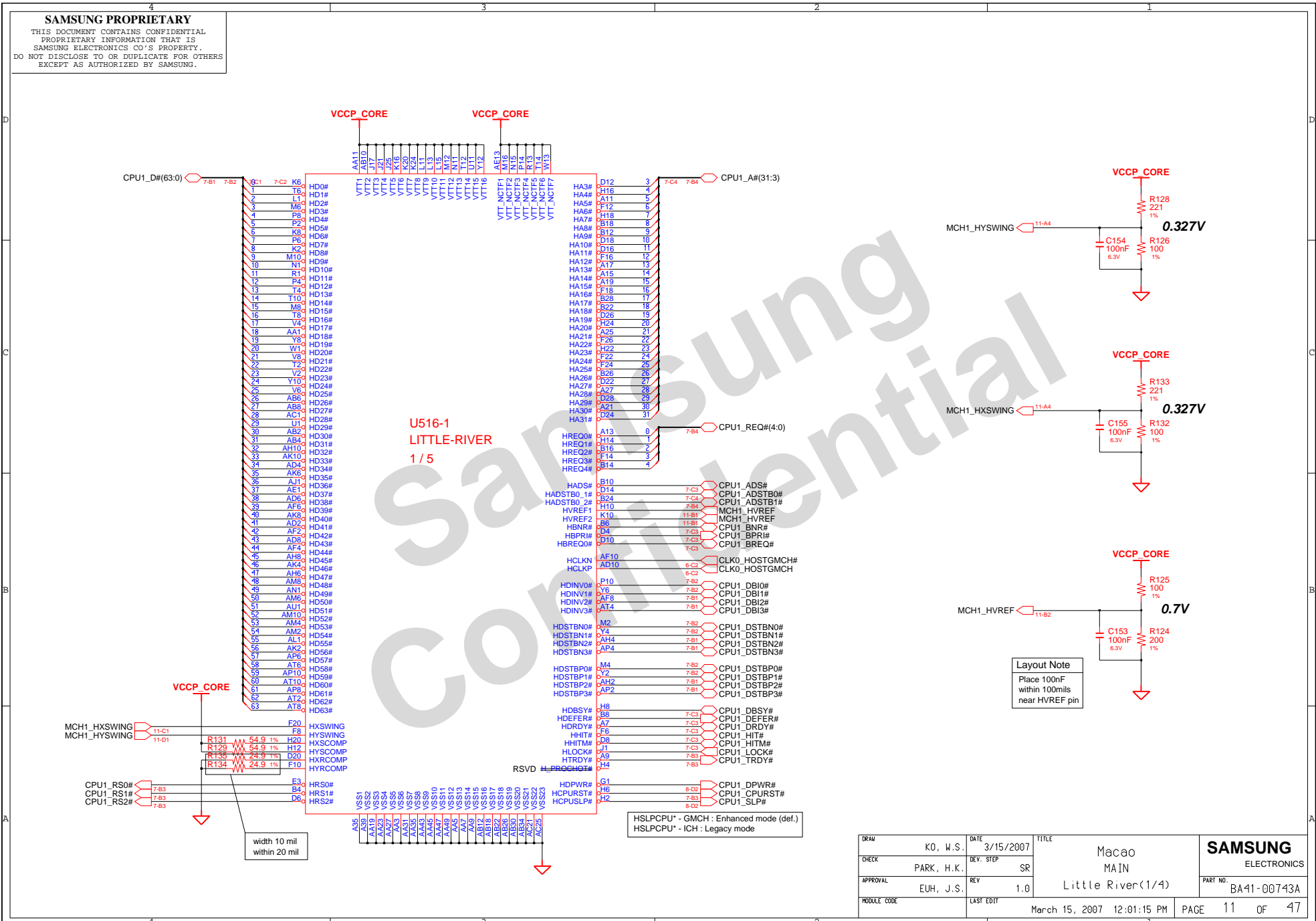
**CPU Thermal Sensor**  
 SMBUS Addr"7Ah"(x111 1010)



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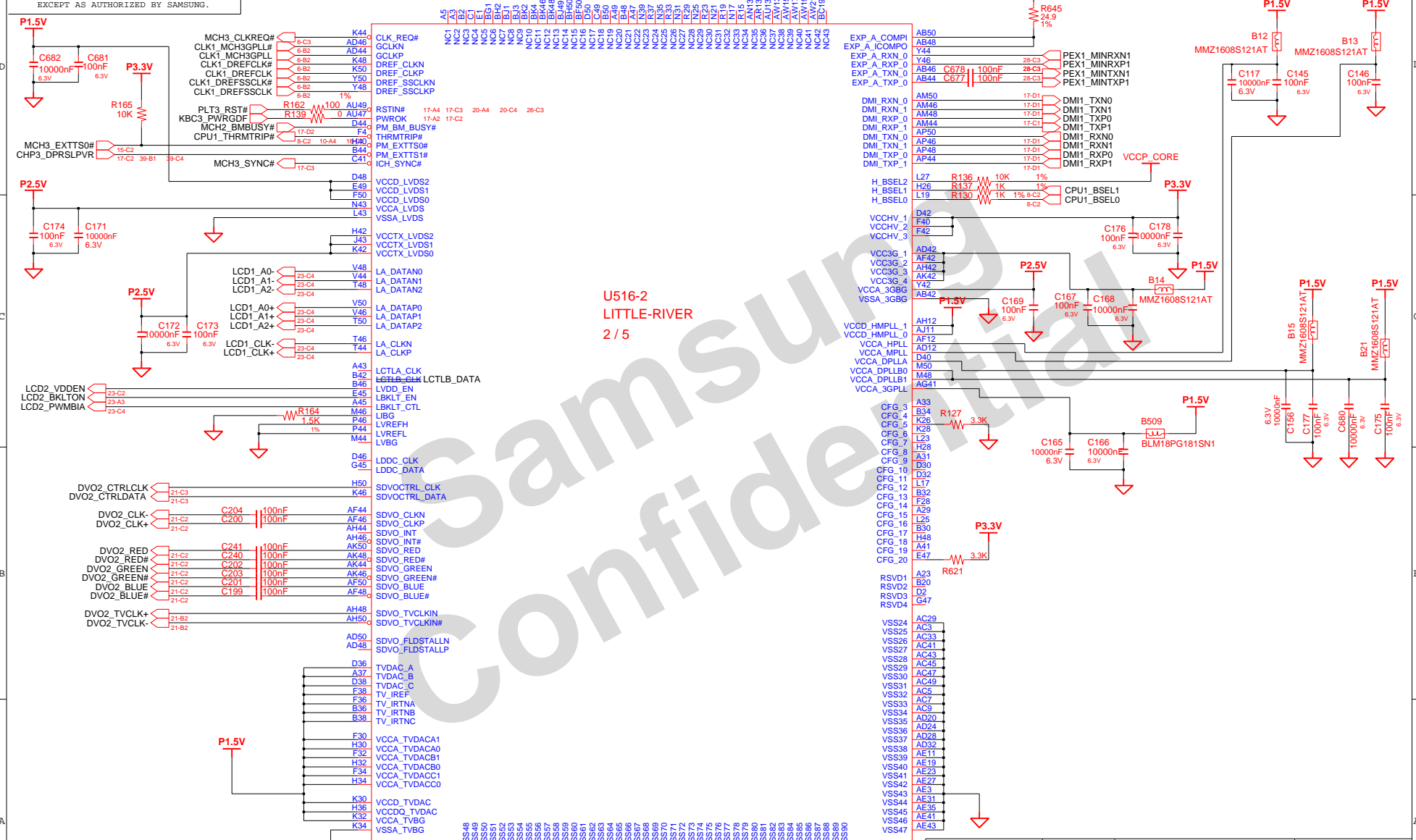


**Layout Note**  
Place 100nF within 100mils near HVREF pin

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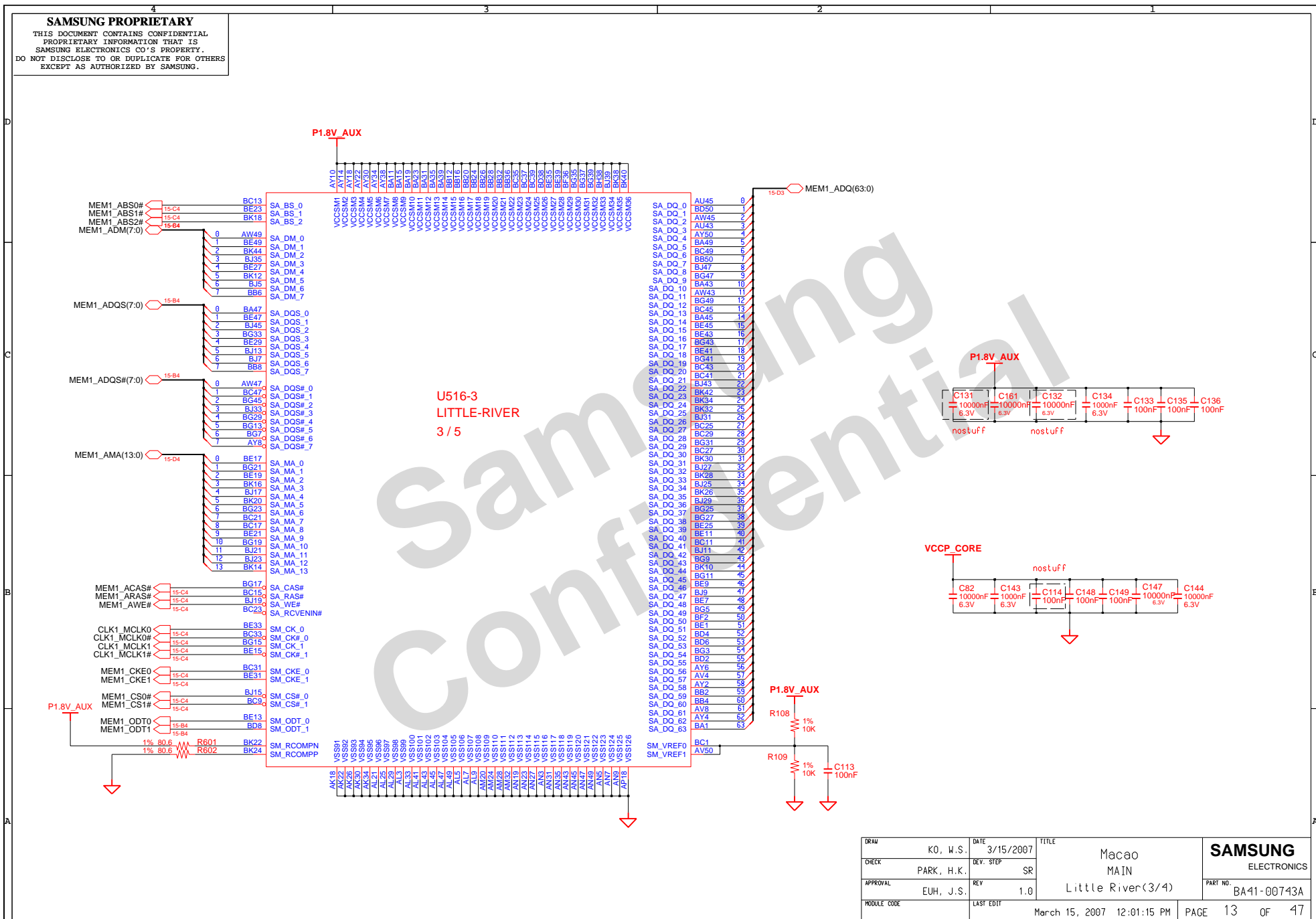


U516-2  
LITTLE-RIVER  
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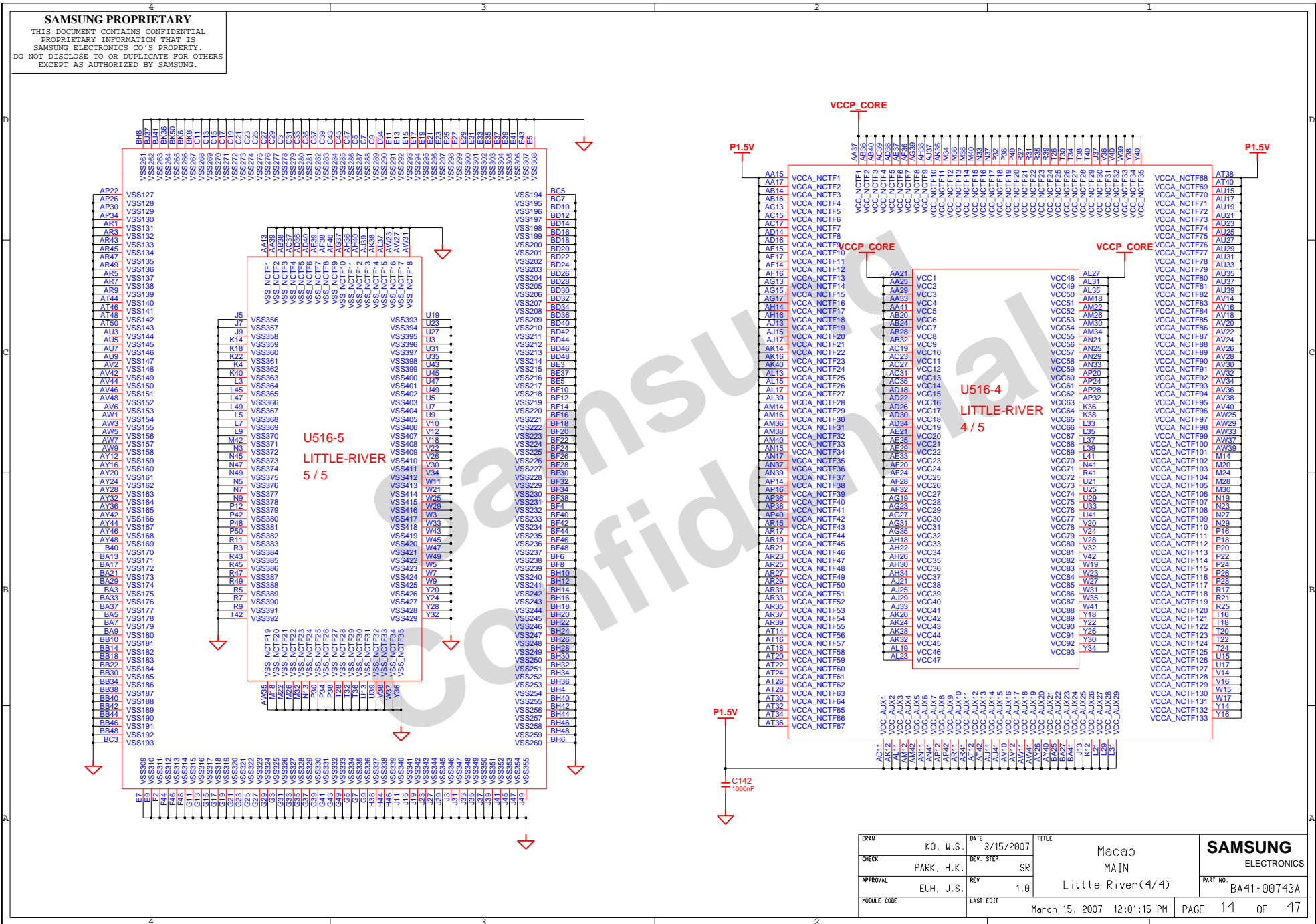
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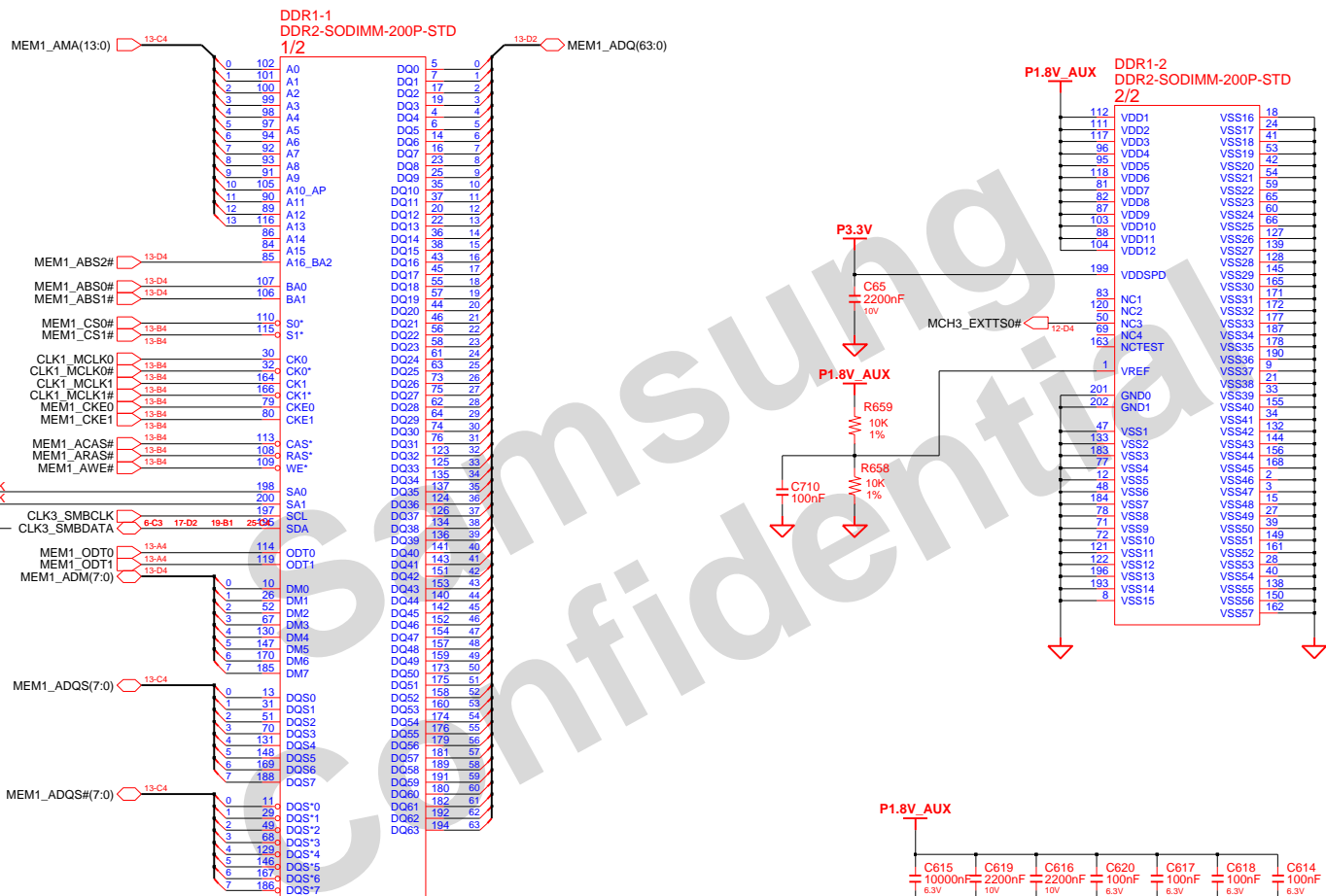
U516-5  
LITTLE-RIVER  
5 / 5

U516-4  
LITTLE-RIVER  
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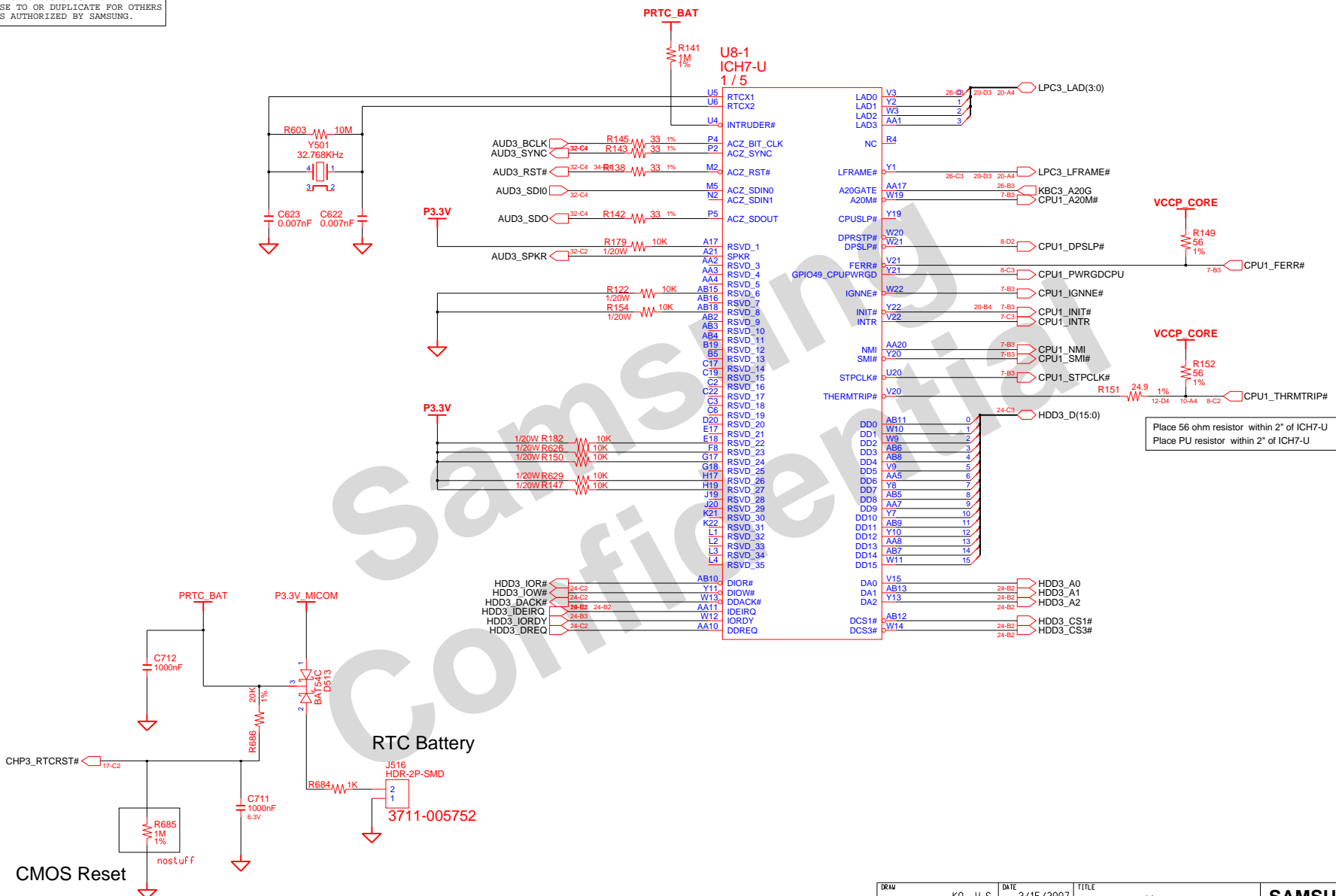
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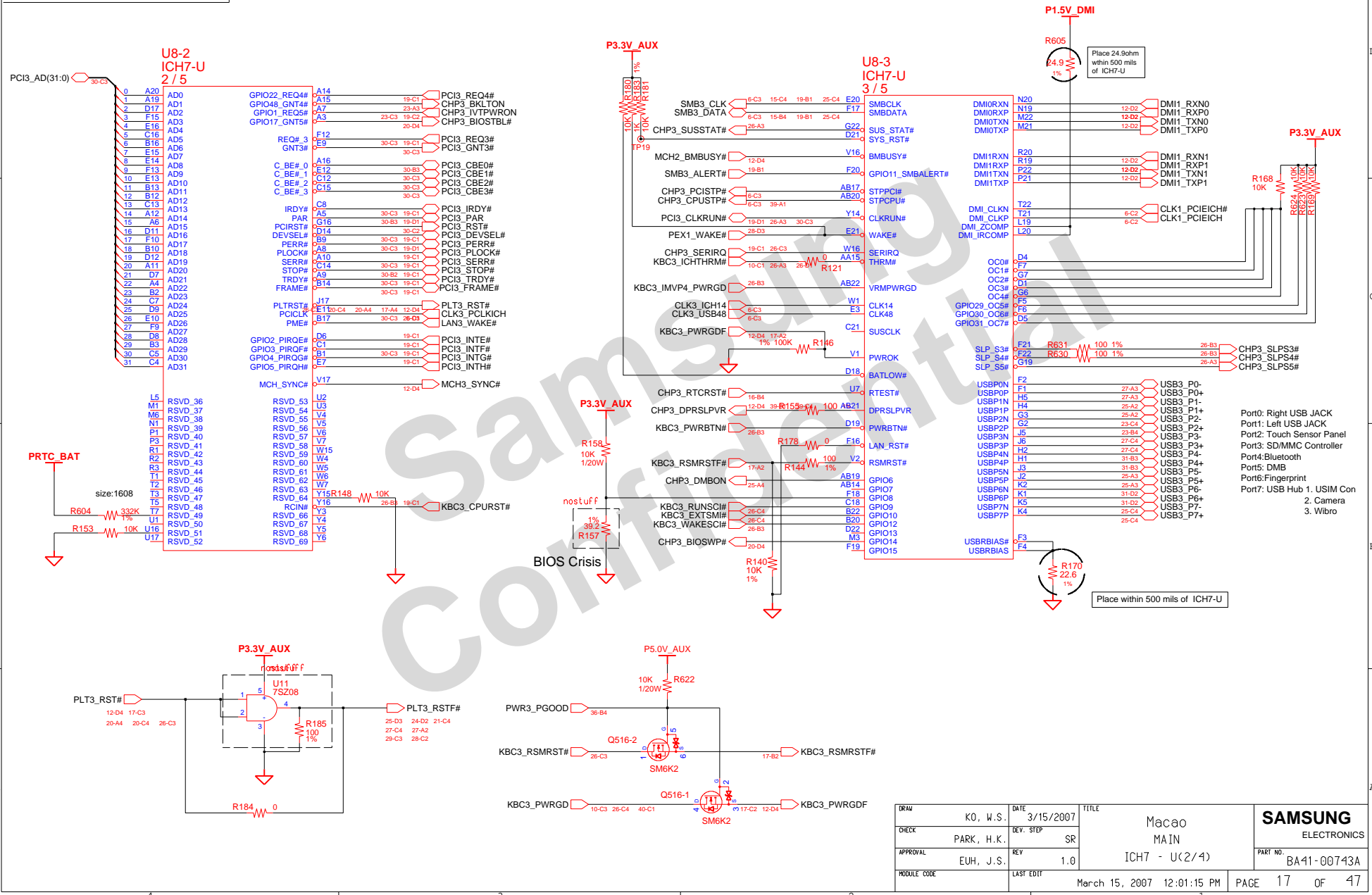
Place 56 ohm resistor within 2" of ICH7-U  
Place PU resistor within 2" of ICH7-U

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CHECK	PARK, H.K.	DEV. STEP	SR	MAIN		
APPROVAL	EUH, J.S.	REV	1.0	ICH7-U(1/4)		PART NO. BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	16	OF 47



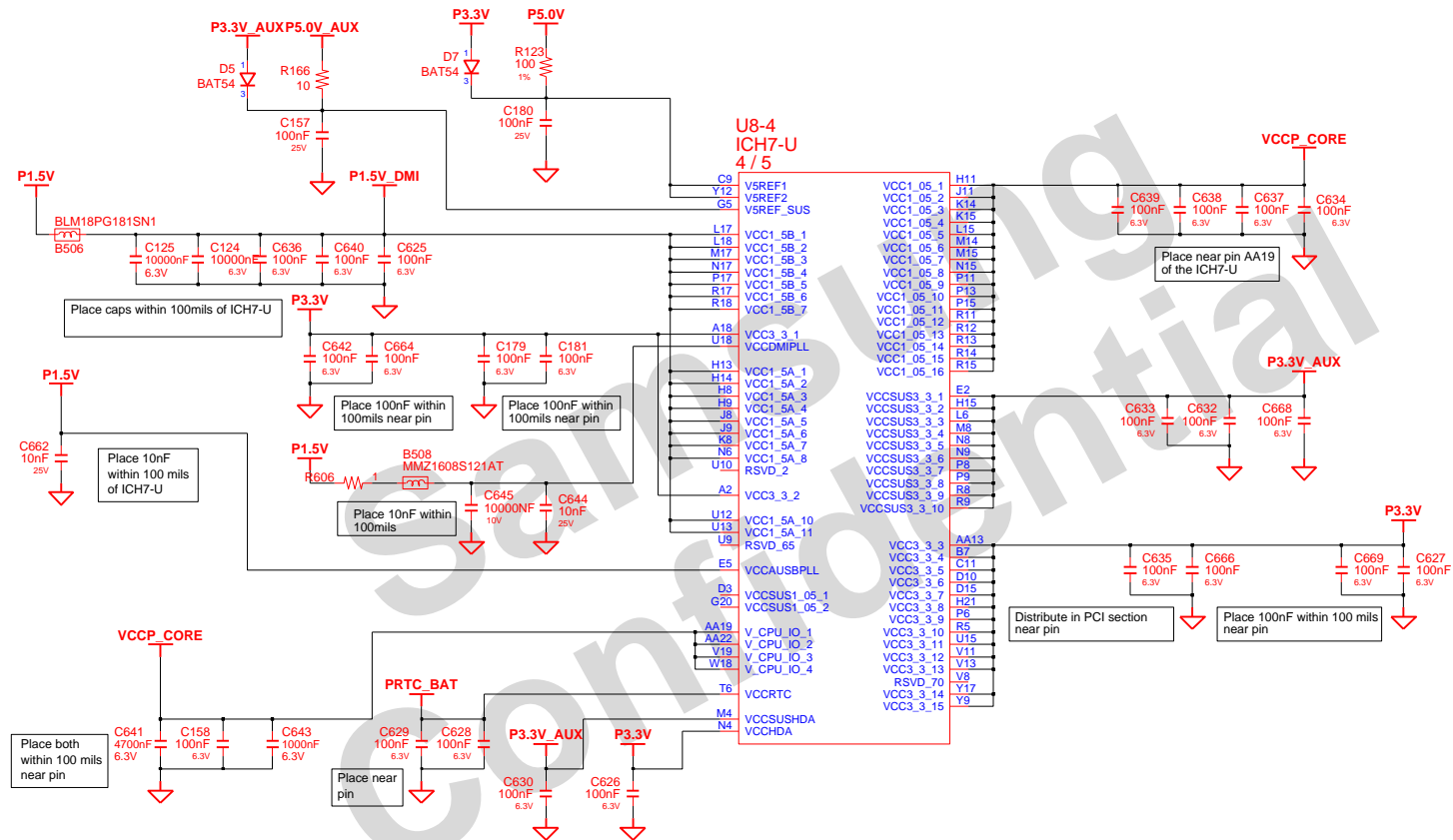
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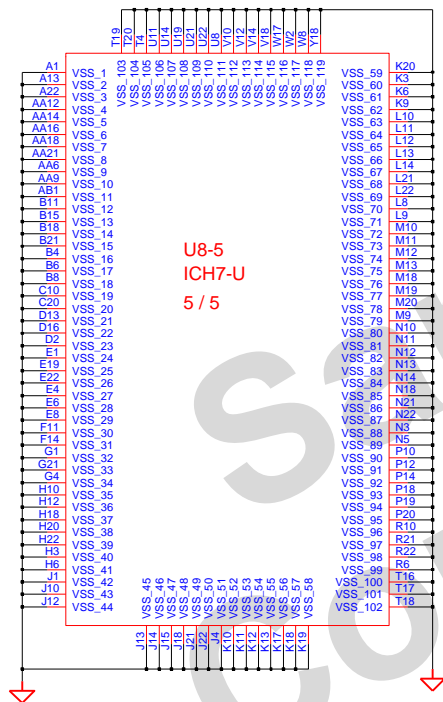
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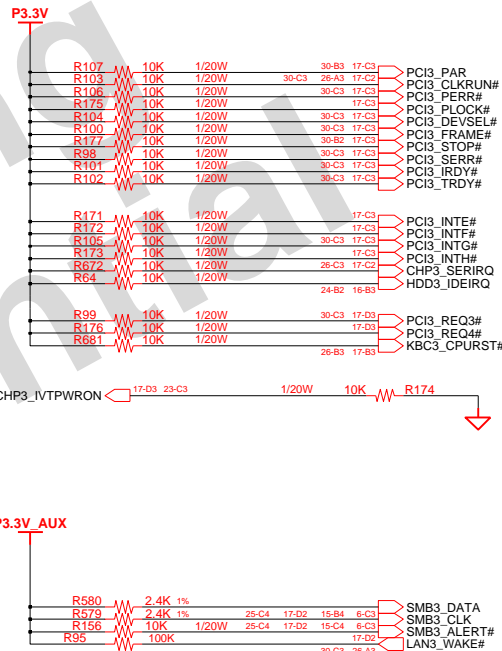
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CHECK	PARK, H.K.	DEV. STEP	SR		MAIN	
APPROVAL	EUH, J.S.	REV	1.0		ICH7 - U(3/4)	PART NO. BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	18	OF 47

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U8-5  
 ICH7-U  
 5/5

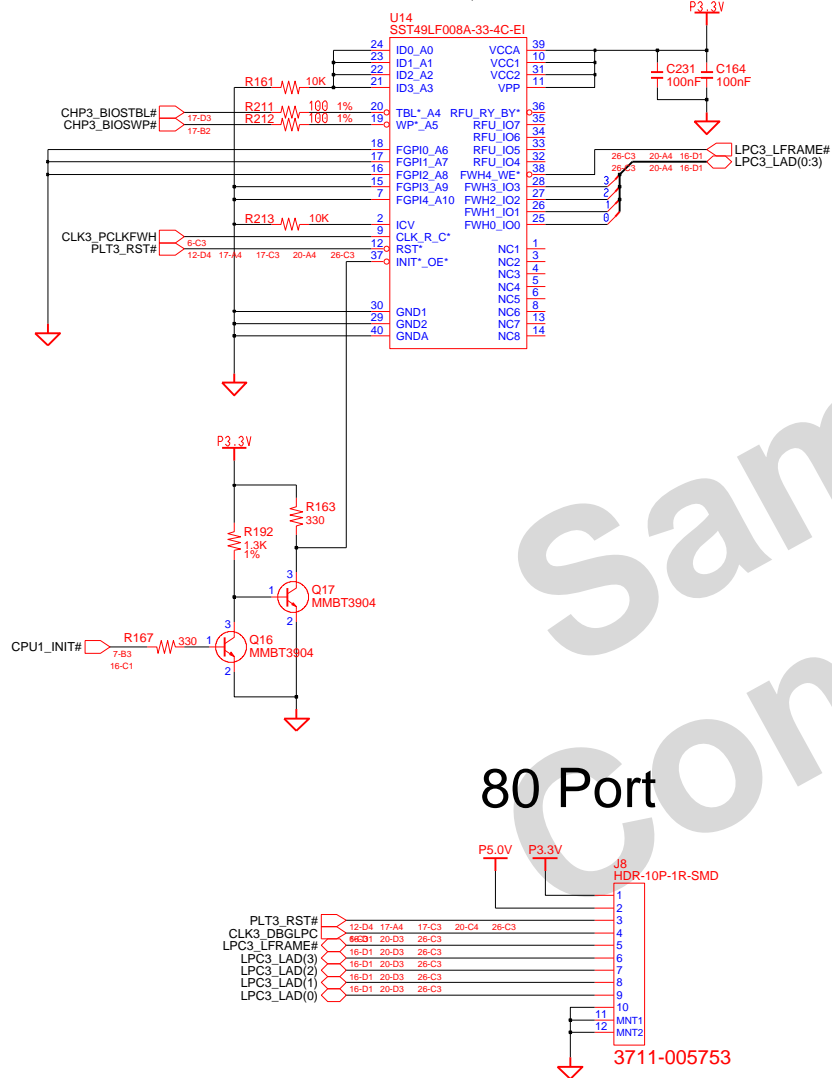


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CHECK	PARK, H.K.	DEV. STEP	SR	MAIN	BA41-00743A	
APPROVAL	EUH, J.S.	REV	1.0	ICH7 - U(4/4)	PART NO.	BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	19	OF 47

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VENDOR: SST, ATMEL



- 02 VERIFY REAL MODE
- 03 DISABLE NMI
- 04 GET CPU TYPE
- 06 INIT. SYSTEM H/W
- 08 INIT. CHIPSET REG.
- 09 SET IN POST FLAG
- 0A INIT CPU.REG
- 0B CPU CACHE ON
- 0C INIT.CACHE TO POST
- 0E INIT. I/O VALUE
- 0F ENABLE THE L-BUS IDE
- 10 INIT. POWER MANAGER
- 11 LOAD ALTERNATE REG.
- 13 PCI BUS MASTER RESET WITH INITIAL POST VALUE
- 14 INIT. KEYBOARD CONTROLLER
- 16 CHECK CHECKSUM
- 18 8254 TIMER INIT.
- 1A 8237 DMA CONTROLLER INIT.
- 1C RESET INTERRUPT CONTROLLER
- 20 TEST DRAM REFRESH
- 22 TEST 8742 KEYBOARD CONTROLLER
- 24 SET ES SEGMENT REG. TO 4GB
- 26 ENABLE A20
- 28 AUTO SIZING DRAM
- 32 COMPUTE THE CPU SPEED
- 34 TESET CMOS RAM
- 38 SHADOW SYSTEM BIOS ROM
- 3A AUTO SIZING CACHE
- 3C CONFIGURE ADVANCED CHIPSET REG.
- 3D LOAD ALTER REG. WITH CMOS VALUE
- 42 INIT. INTERRUPT VECTOR
- 44 INIT. BIOS INTERRUPT
- 46 CHECK ROM COPYRIGHT NOTICE
- 47 INIT. I20 SUPPORT IF INSTALLED
- 48 CHECK VIDEO CONFIGURE AGAINST CMOS
- 49 INIT. PCI BUS AND DEVICE
- 4A INIT. ALL VIDEO BIOS ROM
- 4C SHADOW VIDEO BIOS ROM
- 50 DISPLAY CPU TYPE AND SPEED
- 52 TEST KEYBOARD
- 54 SET KEYCLICK IF ENABLED
- 56 ENABLE KEYBOARD
- 58 TEST FOR UNEXPECTED INTERRUPTS
- 5A DISPLAY " PRESS ..... SETUP"
- 5C TEST RAM BETWEEN 512K AND 640K
- 60 TEST EXTENDED MEMORY
- 62 TEST EXTENDED MEMORY ADDRESS LINE
- 64 JUMP TO USER PATCH 1

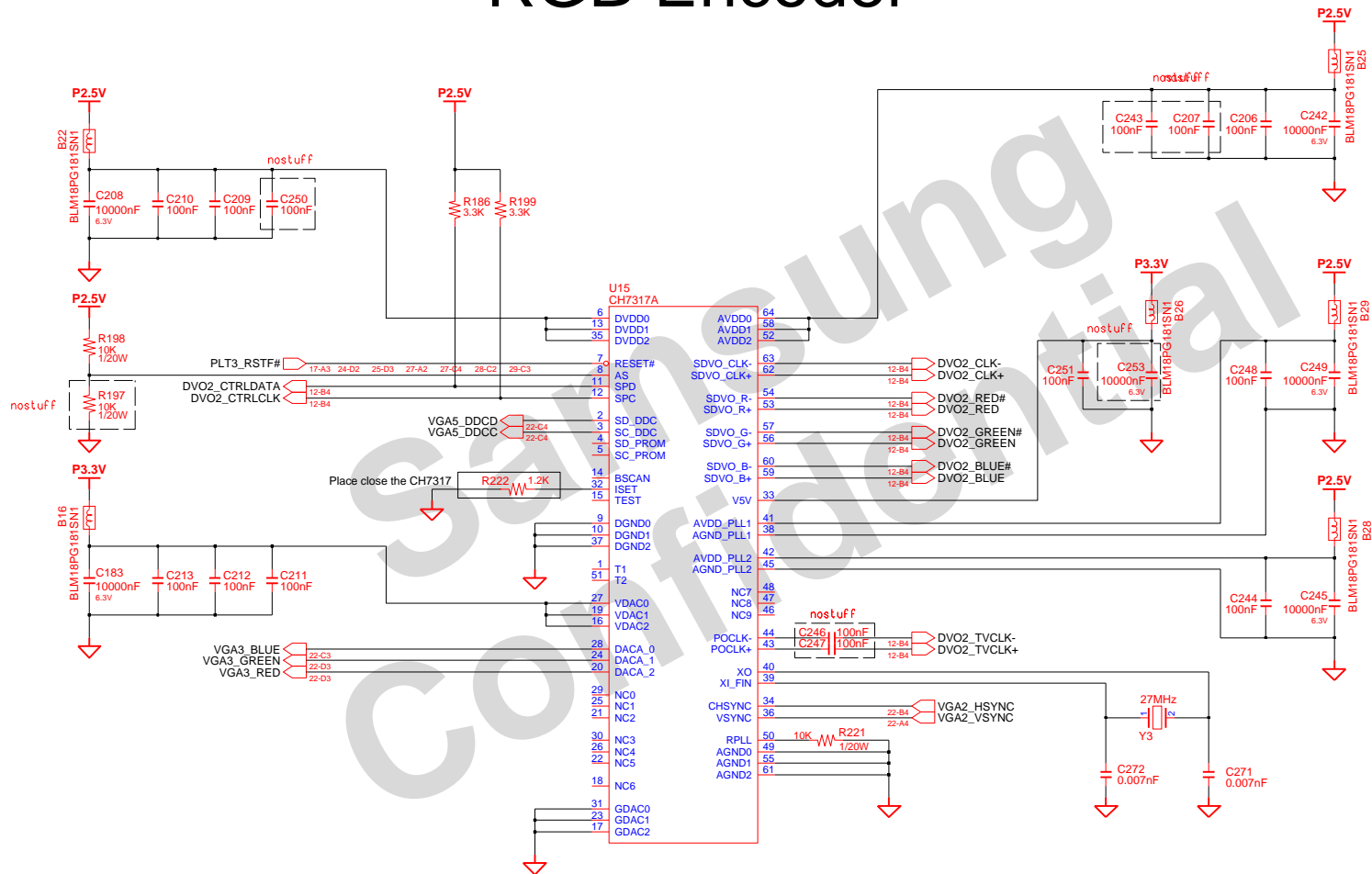
- 66 CONFIGURE ADVANCE CACHE REG.
- 6A DISPLAY EXTERNAL CACHE SIZE
- 6C DISPLAY SHADOW MESSAGE
- 6E DISPLAY NON-DISPOSABLE SEGMENT
- 70 DISPLAY ERROR MESSAGE
- 72 CHECK FOR CONFIGURATION ERROR
- 74 TEST REAL-TIME CLOCK
- 76 CHECK FOR KEYBOARD ERROR
- 7C SETUP HARDWARE INTERRUPT VECTOR
- 7E TEST COPROCESSER IF PRESENT
- 80 DISABLE ON-BOARD I/O PORT
- 82 DETECT AND INSTALL EXT.RS232C
- 84 DETECT AND INSTALL EXT.PARALLEL
- 86 RE-INIT. ON-BOARD I/O PORT
- 88 INIT. BIOS DATA ROM
- 8A INIT.EXTENDED BIOS DATA AREA
- 8C INIT. FDD CONTROLLER
- 9A SHADOW OPTION ROMS
- 9C SETUP POWER MANAGEMENT
- 9E ENABLE H/W INTERRUPT
- A0 SET TIME OF DAY
- A4 INIT. TYPOMATIC RATE
- A8 ERASE F2 PROMPT
- AA SCAN FOR F2 KEY STROKE
- AC ENTER SETUP
- AE CLEAR IN POST FLAG
- B0 CHECK FOR ERRORS
- B2 POST DONE-PREPARE TO BOOT O/S
- B4 ONE BEEP
- B6 CHECK PASSWORD (OPTION)
- B7 ACPI INIT
- BA DMI INIT
- BE CLEAR SCREEN
- C0 TRY BOOT WITH INT19
- D0 INTERRUPT HANDLER ERROR
- D2 UNKNOWN INTERRUPT ERROR
- D4 PENDING INTERRUPT ERROR
- D6 SHUTDOWN 5
- D8 SHUTDOWN ERROR
- DA EXTENDED BLOCK MOVE
- DC SHUTDOWN 10
- 89 ENABLE NMI
- 90 INIT. HDD CONTROLLER
- 91 INIT. LOCAL BUS HDD CONTROLLER
- 92 JUMP TO USER PATCH 2
- 94 DISABLE A20 ADDRESS LINE
- 96 CLEAR HUGE ES SEGMENT REG.
- 98 SEARCH FOR OPTION ROMS

DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	<b>SAMSUNG</b> ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR	MAIN		
APPROVAL	EUH, J.S.	REV	1.0	FWH & 80port	PART NO.	BA41-00743A
MODULE CODE		LAST EDIT		March 15, 2007 12:01:15 PM	PAGE	20 OF 47

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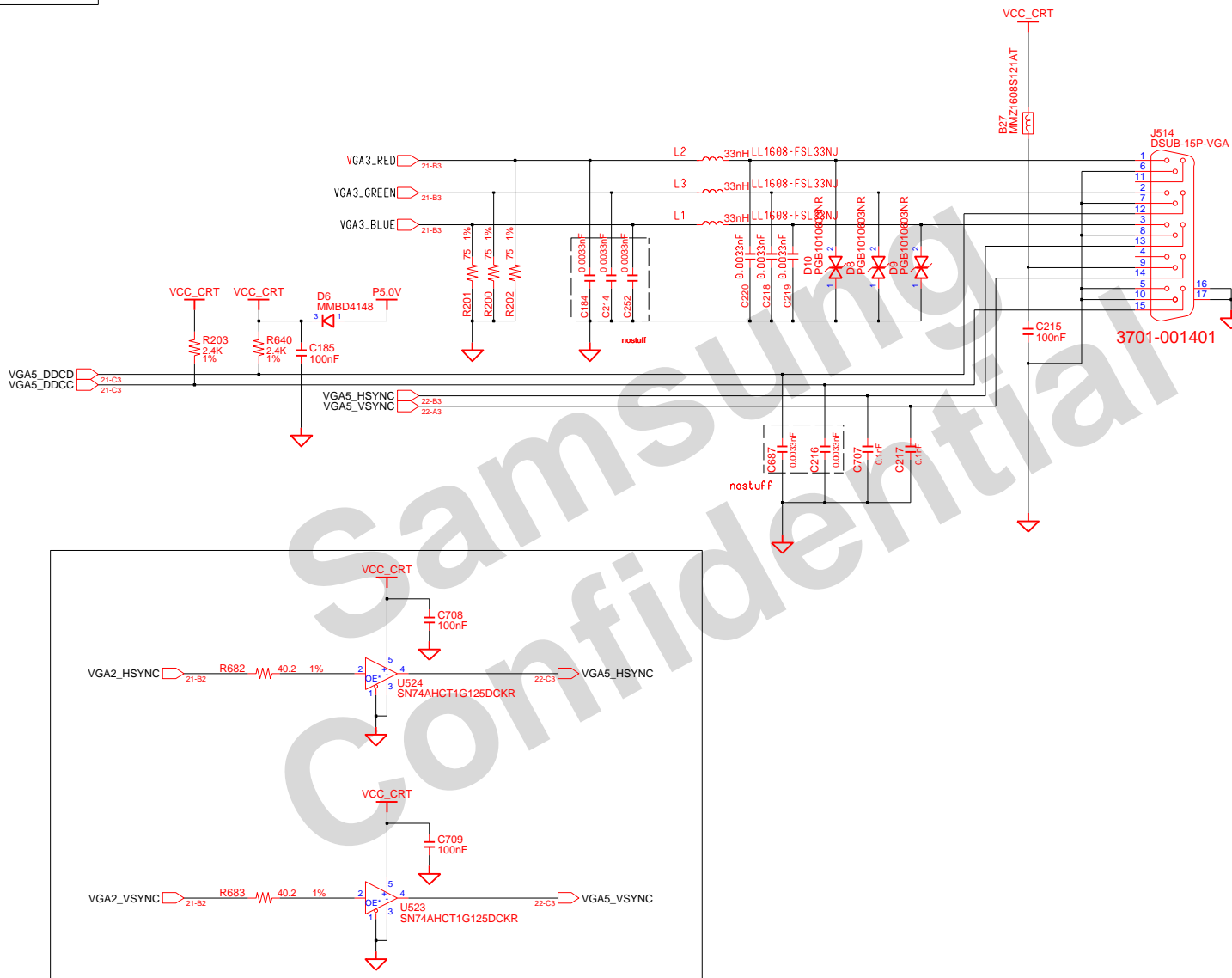
# RGB Encoder



DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR	MAIN		
APPROVAL	EUH, J.S.	REV	1.0	SDVO to RGB	PART NO.	BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	21	OF 47

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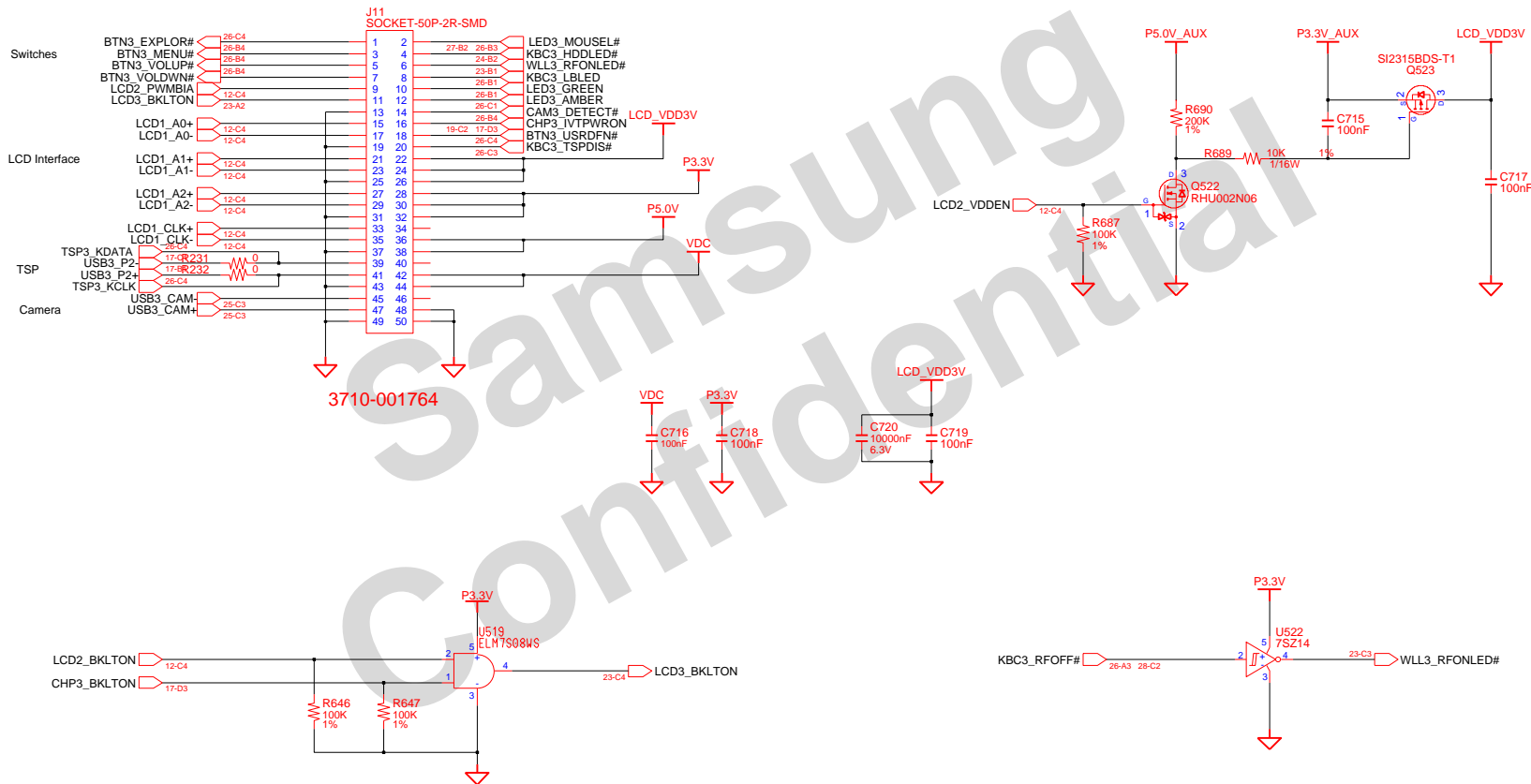


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CHECK	PARK, H.K.	DEV. STEP	SR	MAIN		
APPROVAL	EUH, J.S.	REV	1.0	VGA Conn(CRT)	PART NO.	BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	22	OF 47

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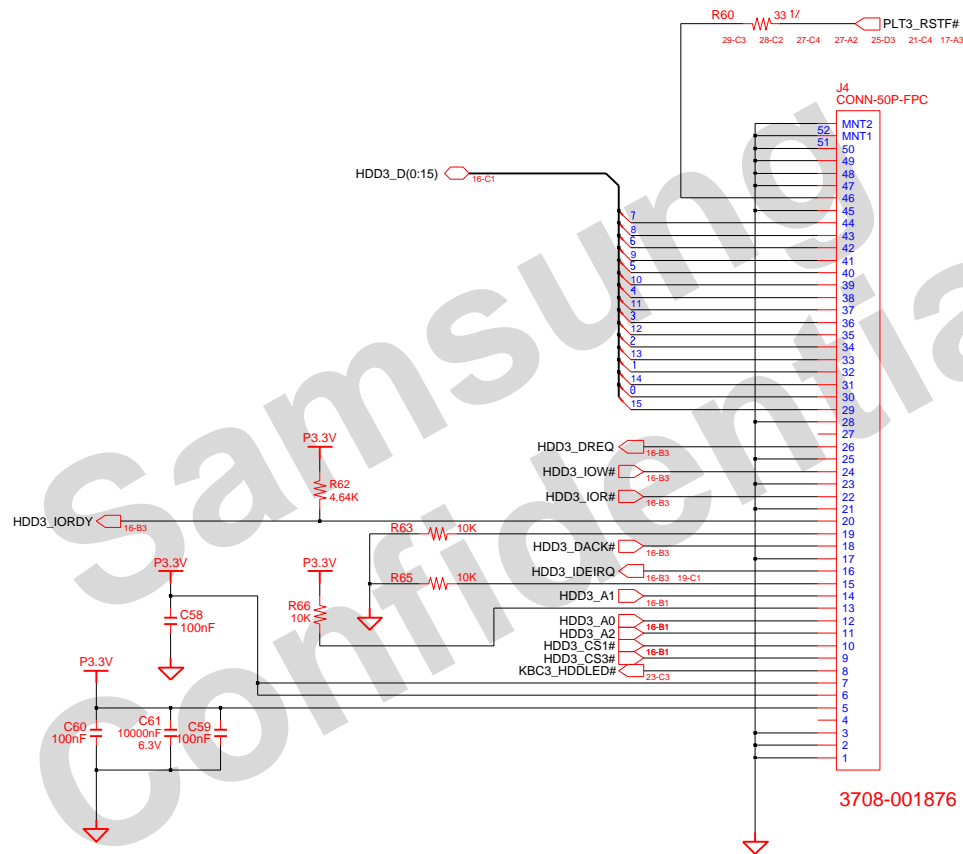
**TCON Sub B'd**



DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR	MAIN		
APPROVAL	EUH, J.S.	REV	1.0	TCON Sub Conn	PART NO.	BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	23	OF 47

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3708-001876

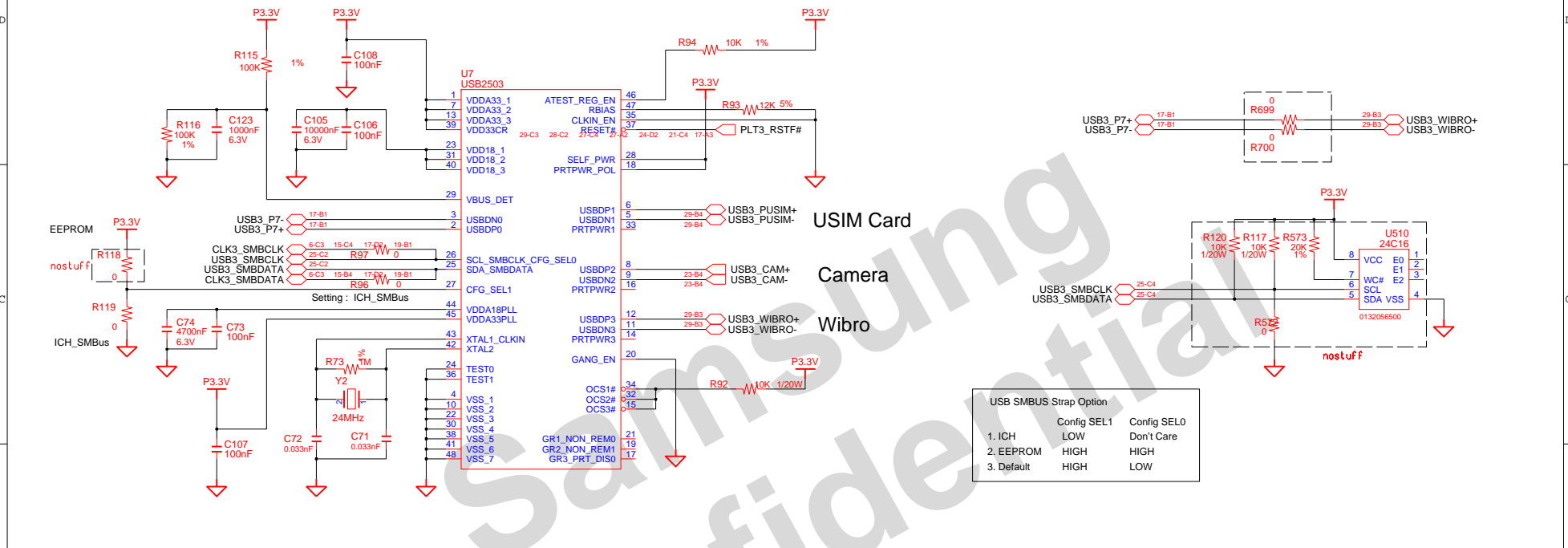
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APPROVAL	EUH, J.S.	REV	1.0	HDD CONNECTOR	PART NO.	BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	24	OF 47



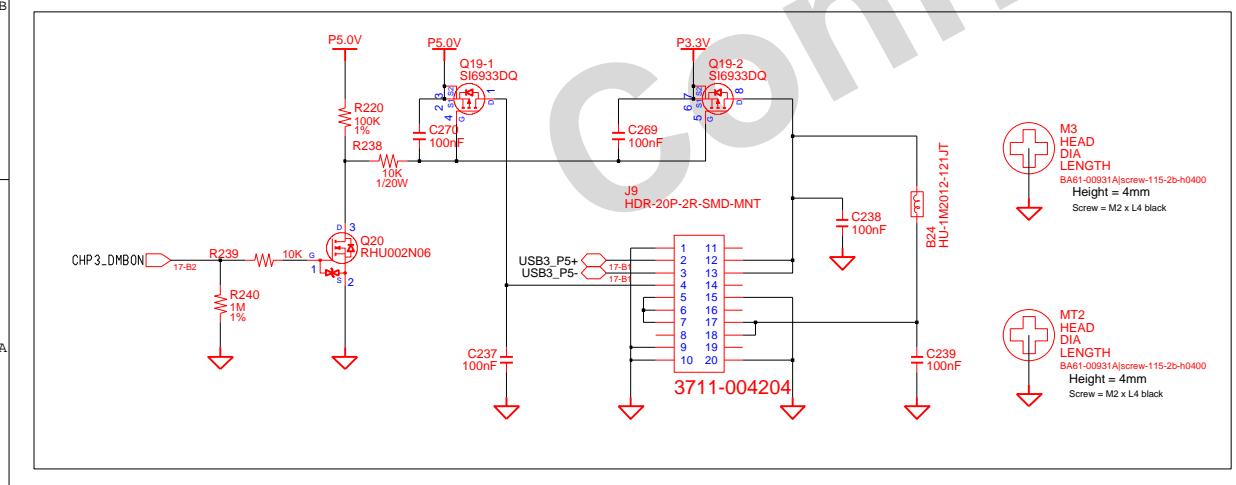
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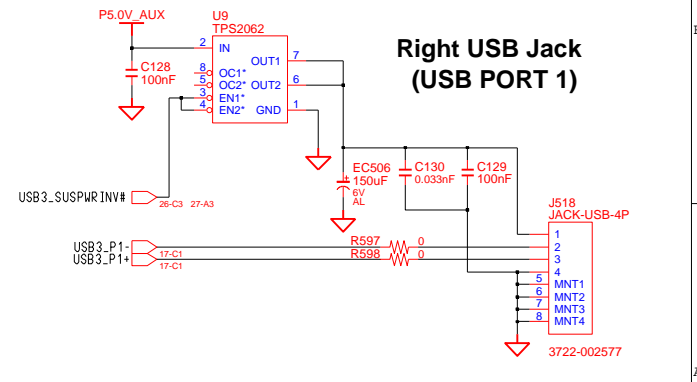
**USB Hub 4 ports + EEPROM**



**DMB Connector & Pem(4mm Height)**



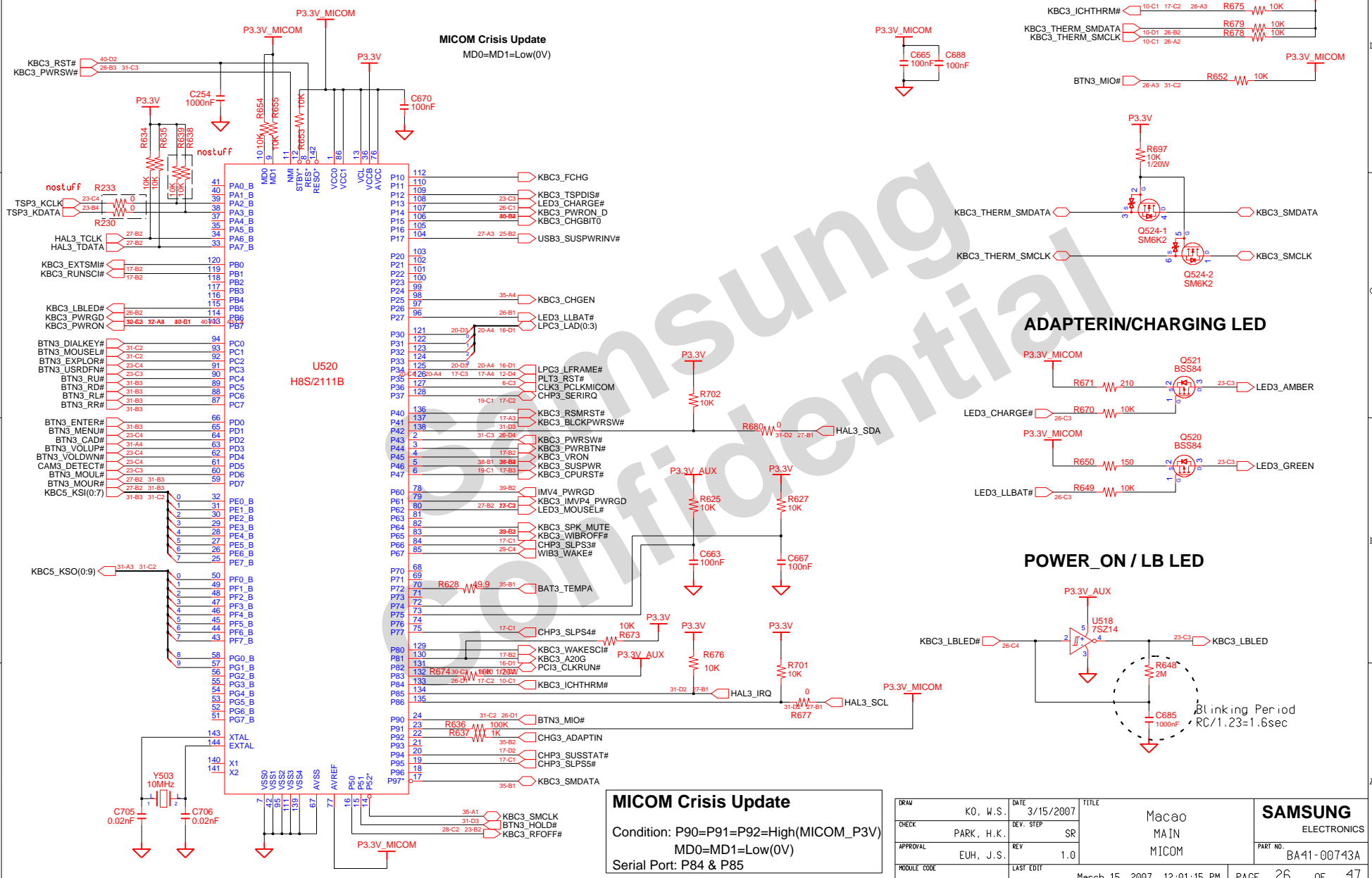
**Right USB Jack (USB PORT 1)**



DRAW	K0, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR	MAIN	PART NO.	
APPROVAL	EUH, J.S.	REV	1.0	USB & DMB	BA41-00743A	PAGE 25 OF 47
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM			

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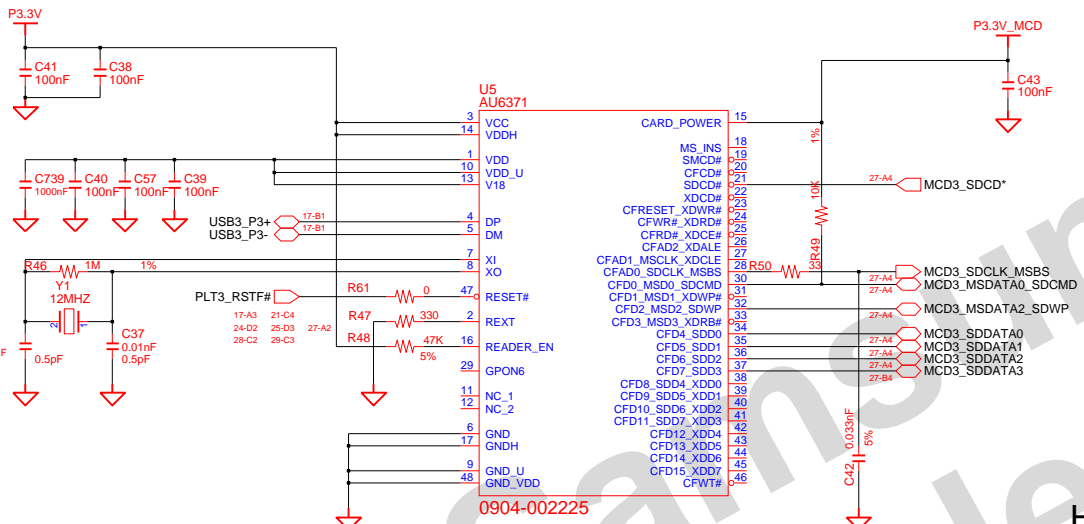
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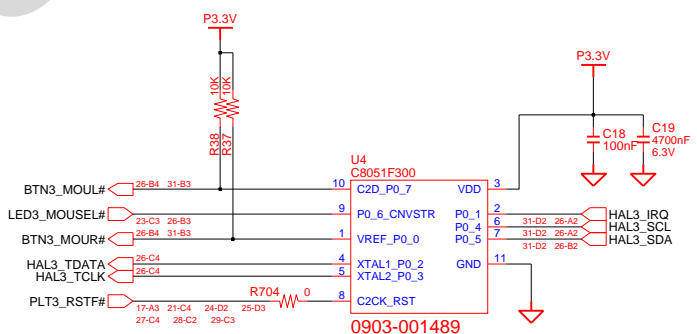
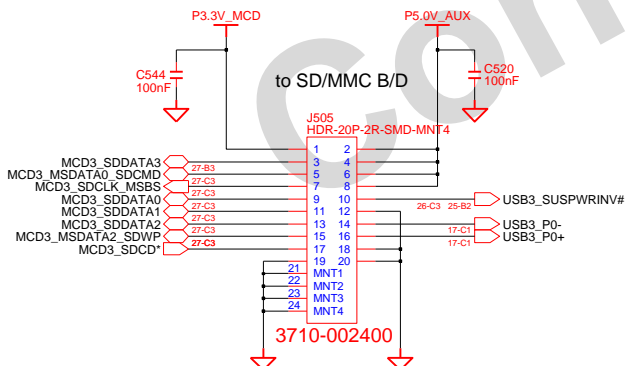
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APPROVAL	EUH, J.S.	REV	1.0	MICOM	BA41-00743A	
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	26	OF 47

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**Hall Mouse IC (I2C to PS2 Conversion IC)**

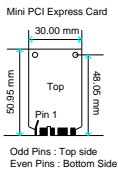
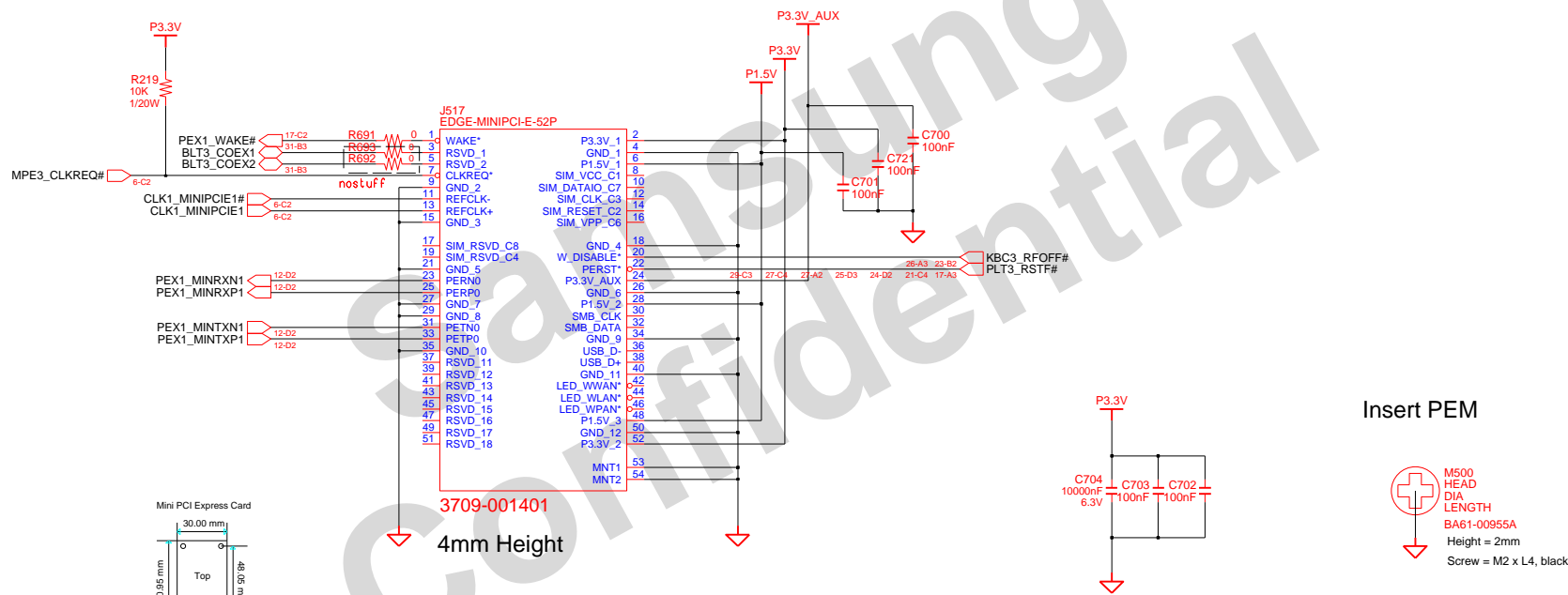


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CHECK	PARK, H.K.	DEV. STEP	SR	MAIN		
APPROVAL	EUH, J.S.	REV	1.0	SD/MMC Controller		PART NO. BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM		PAGE	27 OF 47

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# WirelessLAN ( PCI-E 1x )



**Mini PCI Express**

PCI Express Mini Card ElectroMechanical Spec. 1.0

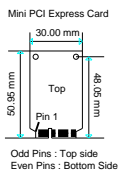
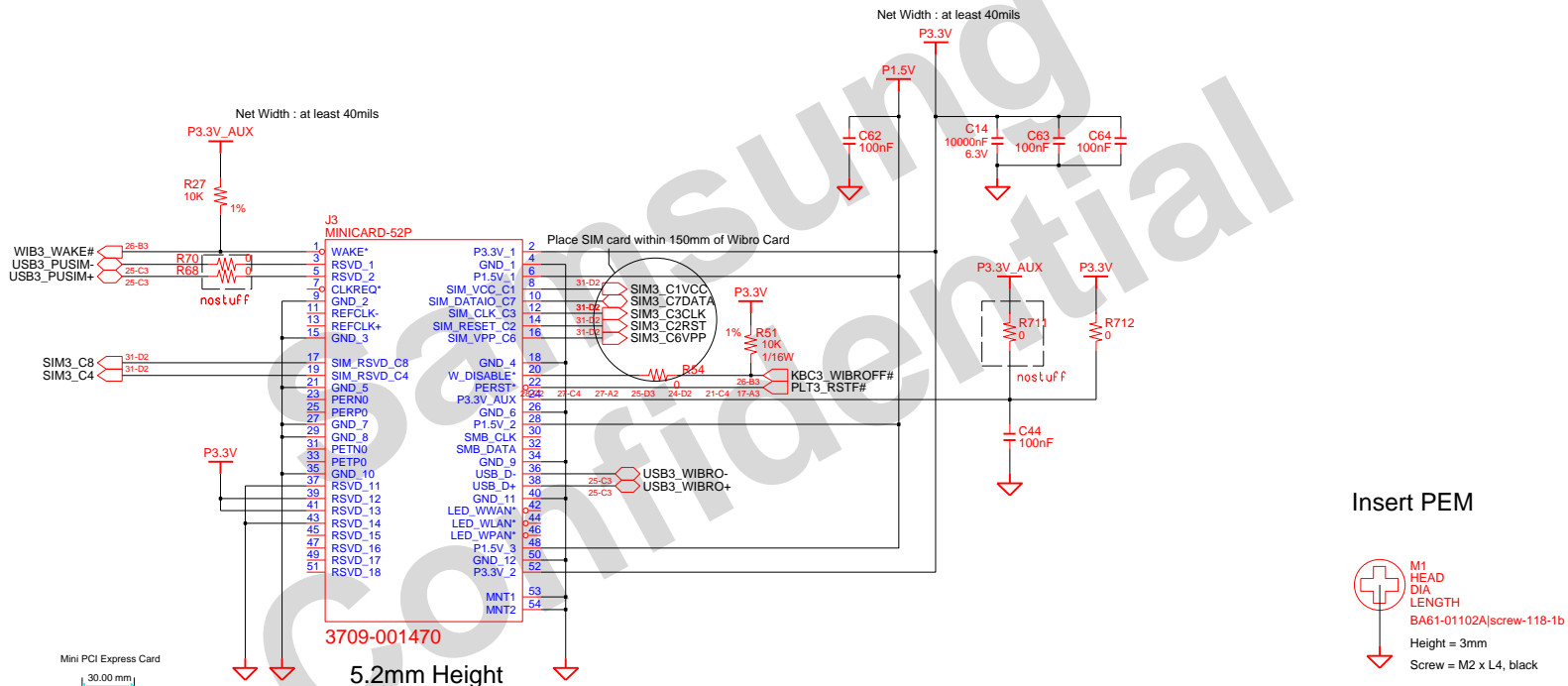
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APPROVAL	EUH, J.S.	REV	1.0	WirelessLAN	PART NO.	BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	28	OF 47

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# Wibro / HSDPA ( USB 4 )

## Wibro Socket



**Mini Card (Socket Only)**

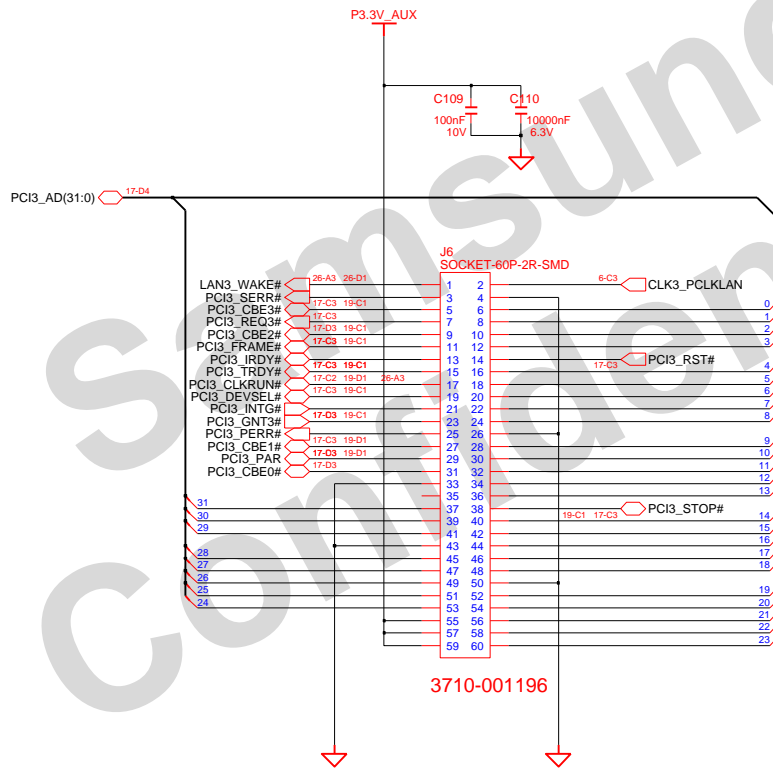
PCI Express Mini Card ElectroMechanical Spec. 1.0

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APPROVAL	EUH, J.S.	REV	1.0	Wibro/HSDPA	PART NO.	BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	29	OF 47

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# Wired LAN : 60p Conn

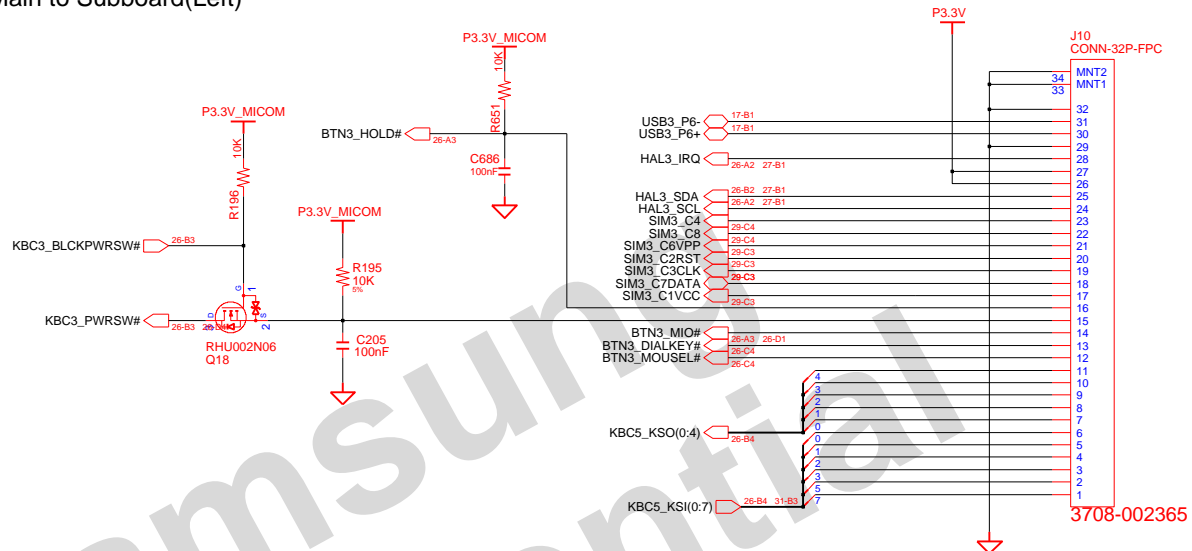


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MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	30	OF 47

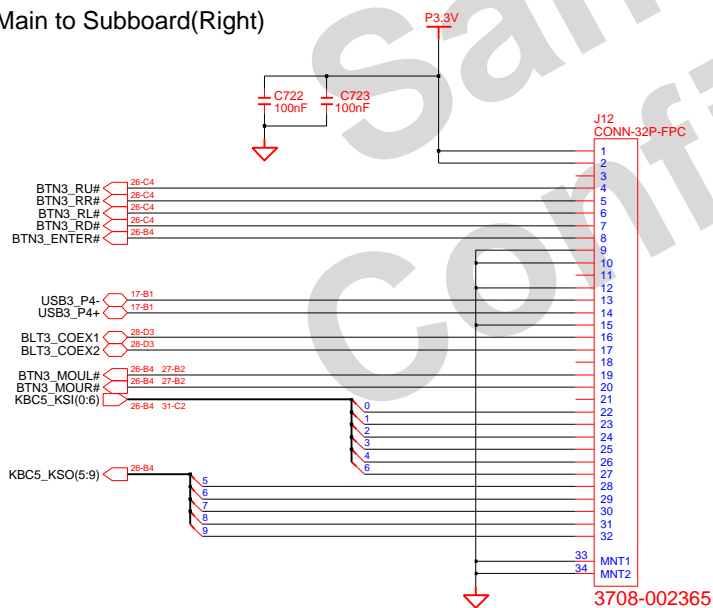
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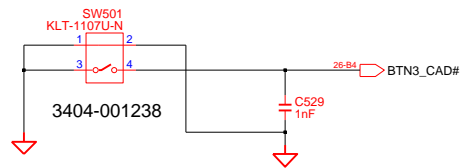
**Main to Subboard(Left)**



**Main to Subboard(Right)**



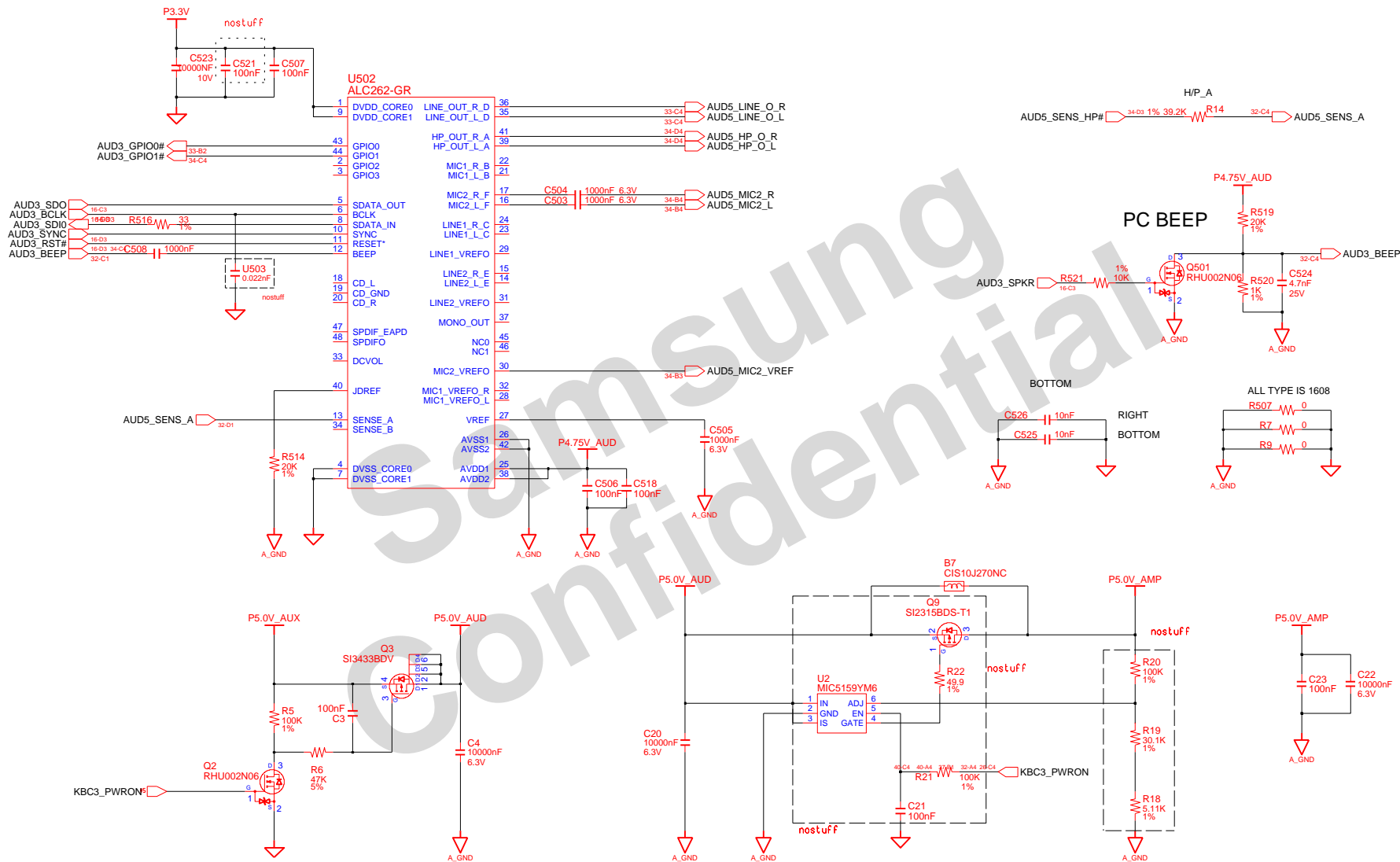
**Ctrl\_Alt\_Del Button**



DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR	MAIN		
APPROVAL	EUH, J.S.	REV	1.0	SUB B'D Conn. & S/W	PART NO.	BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	31	OF 47

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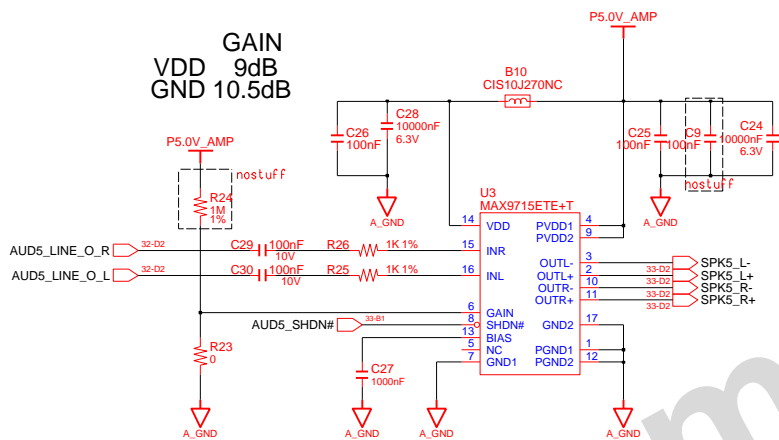


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CHECK	PARK, H.K.	DEV. STEP	SR			
APPROVAL	EUH, J.S.	REV	1.0		Audio Codec	PART NO. BA41-00743A
MODULE CODE		LAST EDIT		March 15, 2007 12:01:15 PM	PAGE	32 OF 47

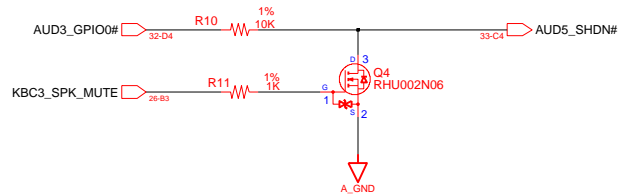
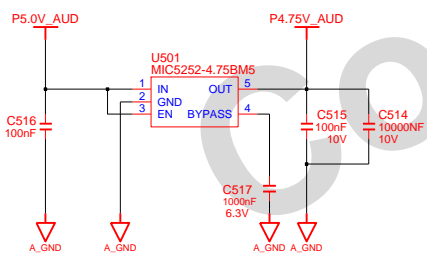
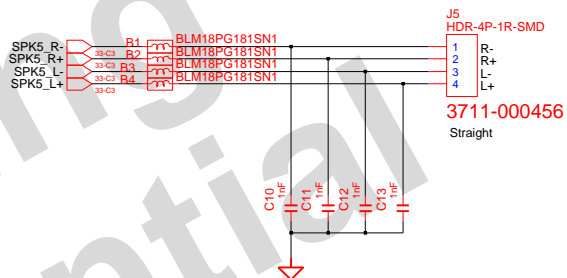


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**INTERNAL STEREO SPEAKERS**

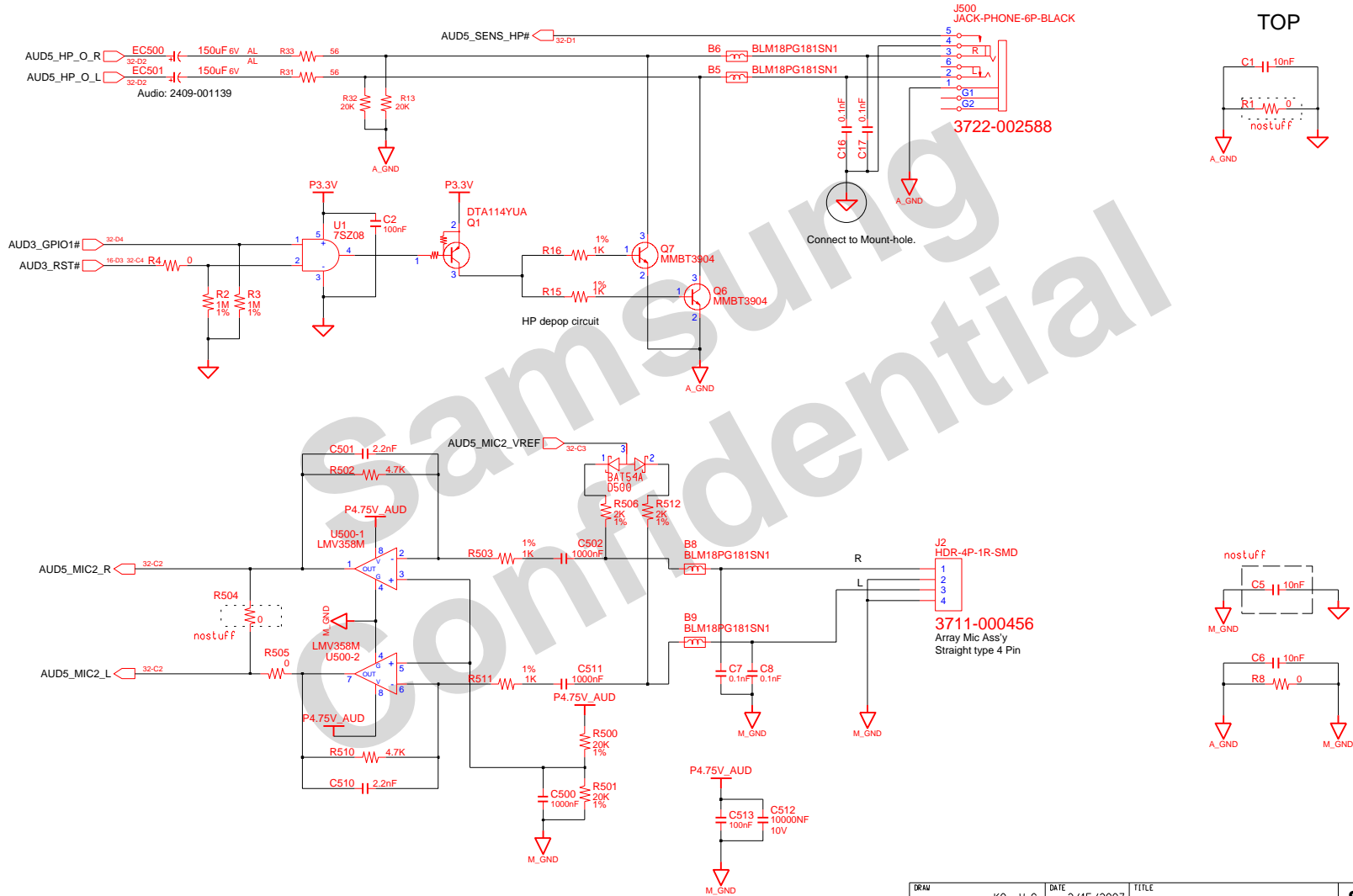


DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao MAIN AMP & Spkr Conn	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00743A
CHECK	PARK, H.K.	DEV. STEP	SR			
APPROVAL	EUH, J.S.	REV	1.0			
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	33 OF 47	

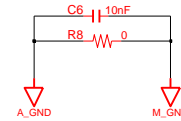
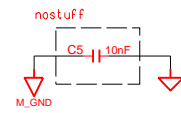
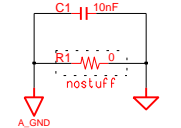
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**HEADPHONE**



**TOP**

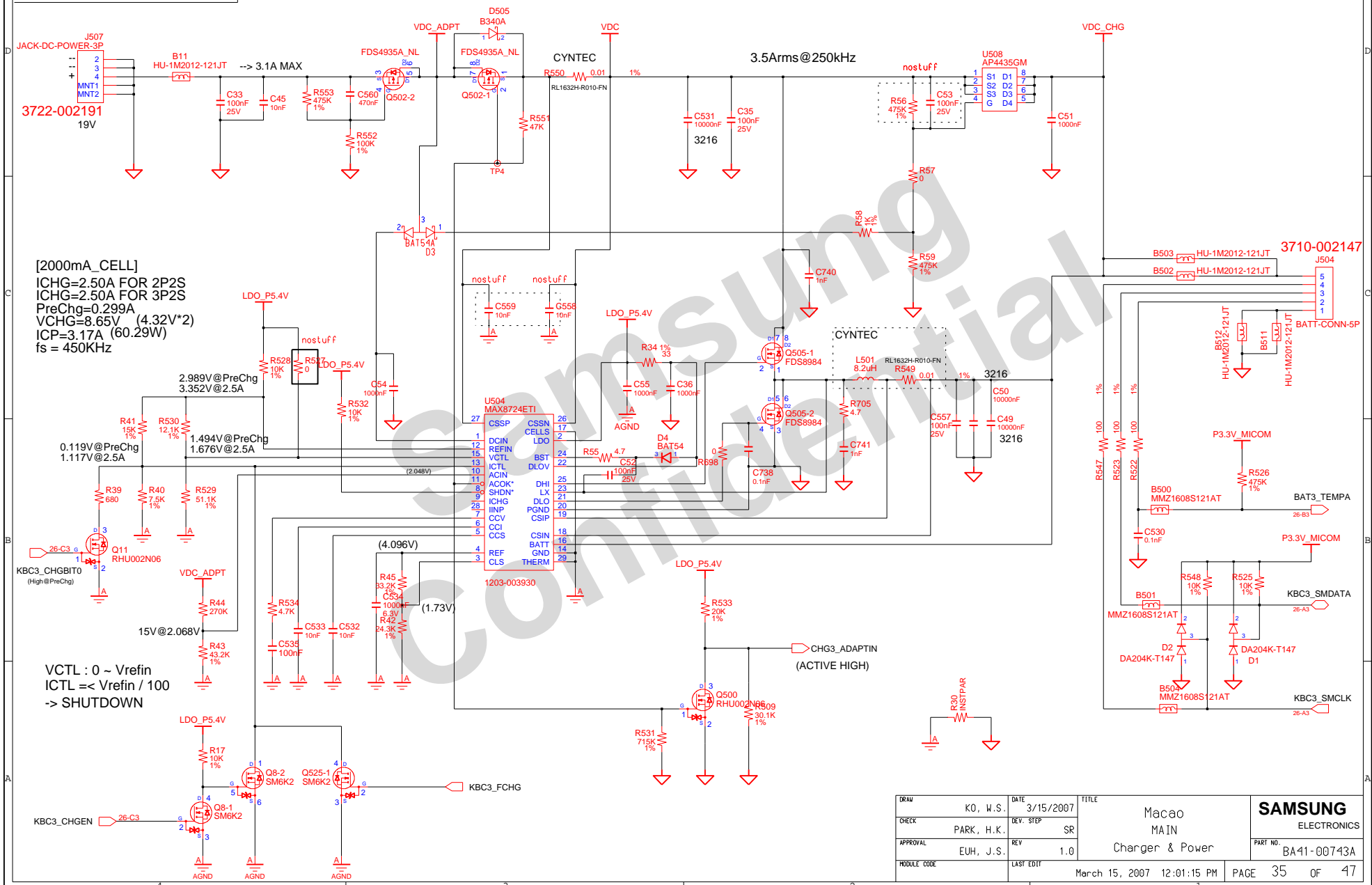


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CHECK	PARK, H.K.	DEV. STEP	SR	MAIN	PART NO.	
APPROVAL	EUH, J.S.	REV	1.0	Phone Jack & MIC	BA41-00743A	
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	34	OF 47

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# CHARGER & POWER MANAGEMENT



[2000mA\_CELL]  
 ICHG=2.50A FOR 2P2S  
 ICHG=2.50A FOR 3P2S  
 PreChg=0.299A  
 VCHG=8.65V (4.32V\*2)  
 ICP=3.17A (60.29W)  
 fs = 450KHz

2.989V@PreChg  
 3.352V@2.5A  
 1.494V@PreChg  
 1.676V@2.5A

VCTL : 0 ~ Vrefin  
 ICTL =< Vrefin / 100  
 -> SHUTDOWN

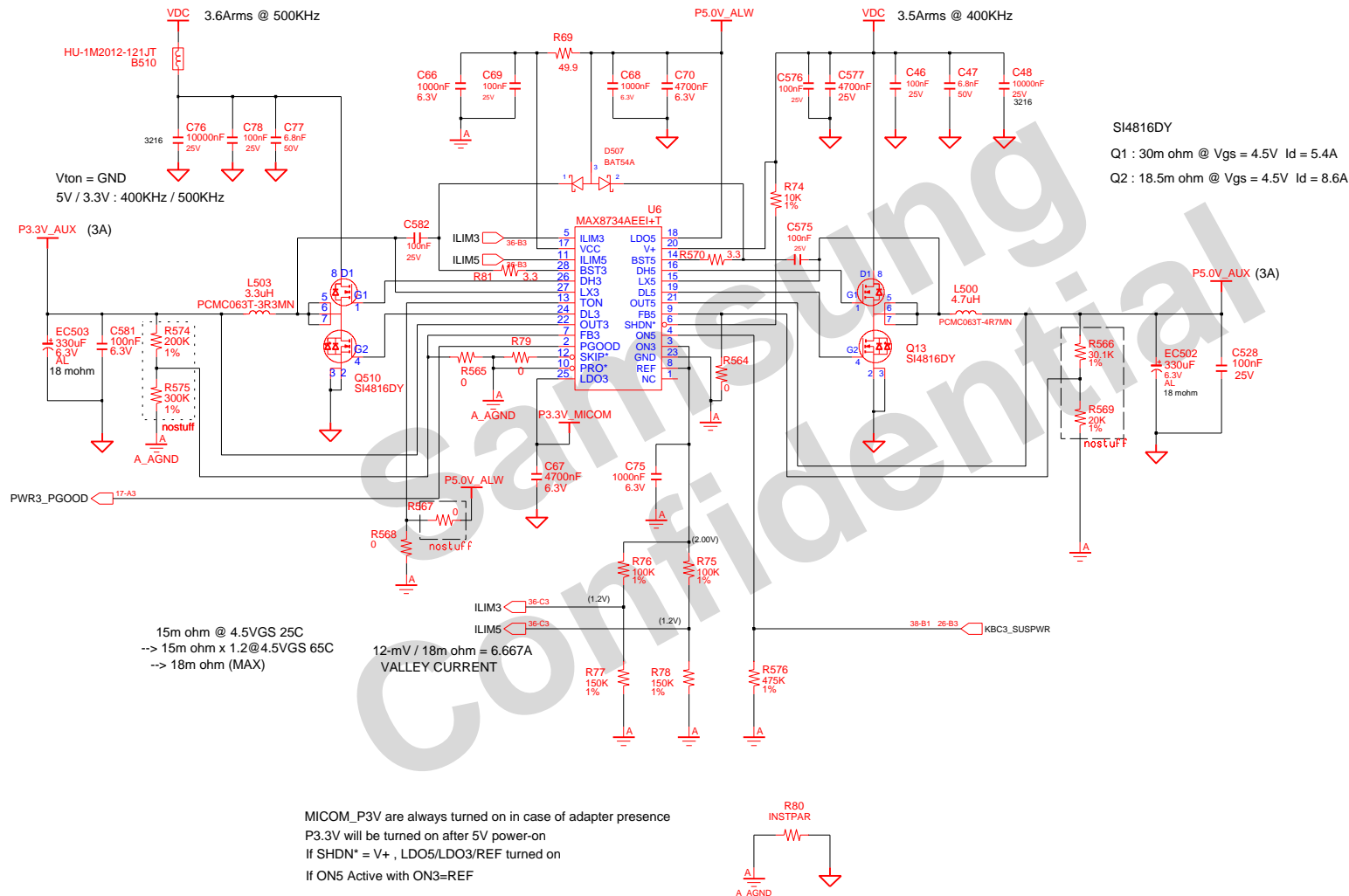
KBC3\_CHGEN

DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR	MAIN	PART NO.	
APPROVAL	EUH, J.S.	REV	1.0	Charger & Power	BA41-00743A	
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	35	OF 47

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# P3.3V\_AUX & P5V\_AUX & P3.3V\_MICOM



SI4816DY  
 Q1 : 30m ohm @ Vgs = 4.5V Id = 5.4A  
 Q2 : 18.5m ohm @ Vgs = 4.5V Id = 8.6A

Vton = GND  
 5V / 3.3V : 400KHz / 500KHz

15m ohm @ 4.5VGS 25C  
 --> 15m ohm x 1.2@4.5VGS 65C  
 --> 18m ohm (MAX)

12-mV / 18m ohm = 6.667A  
 VALLEY CURRENT

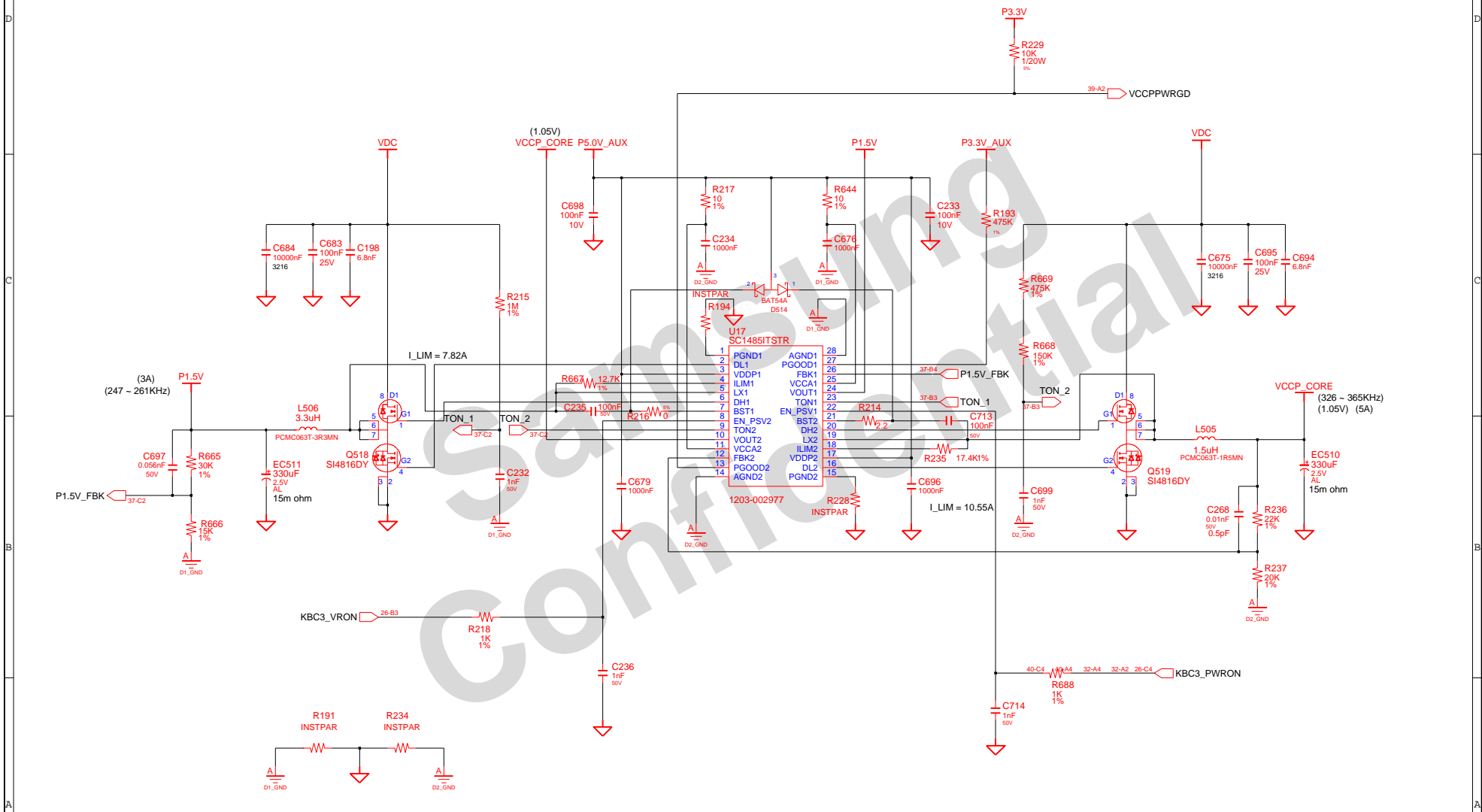
MICOM\_P3V are always turned on in case of adapter presence  
 P3.3V will be turned on after 5V power-on  
 If SHDN\* = V+ , LDO5/LDO3/REF turned on  
 If ON5 Active with ON3=REF

DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR	MAIN		
APPROVAL	EUH, J.S.	REV	P3	P3V_AUX & P5V_AUX & MICOM_P3V	DRY NO. BA41-00743A	
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	36	OF 47

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# P1.5V & VCCP\_CORE

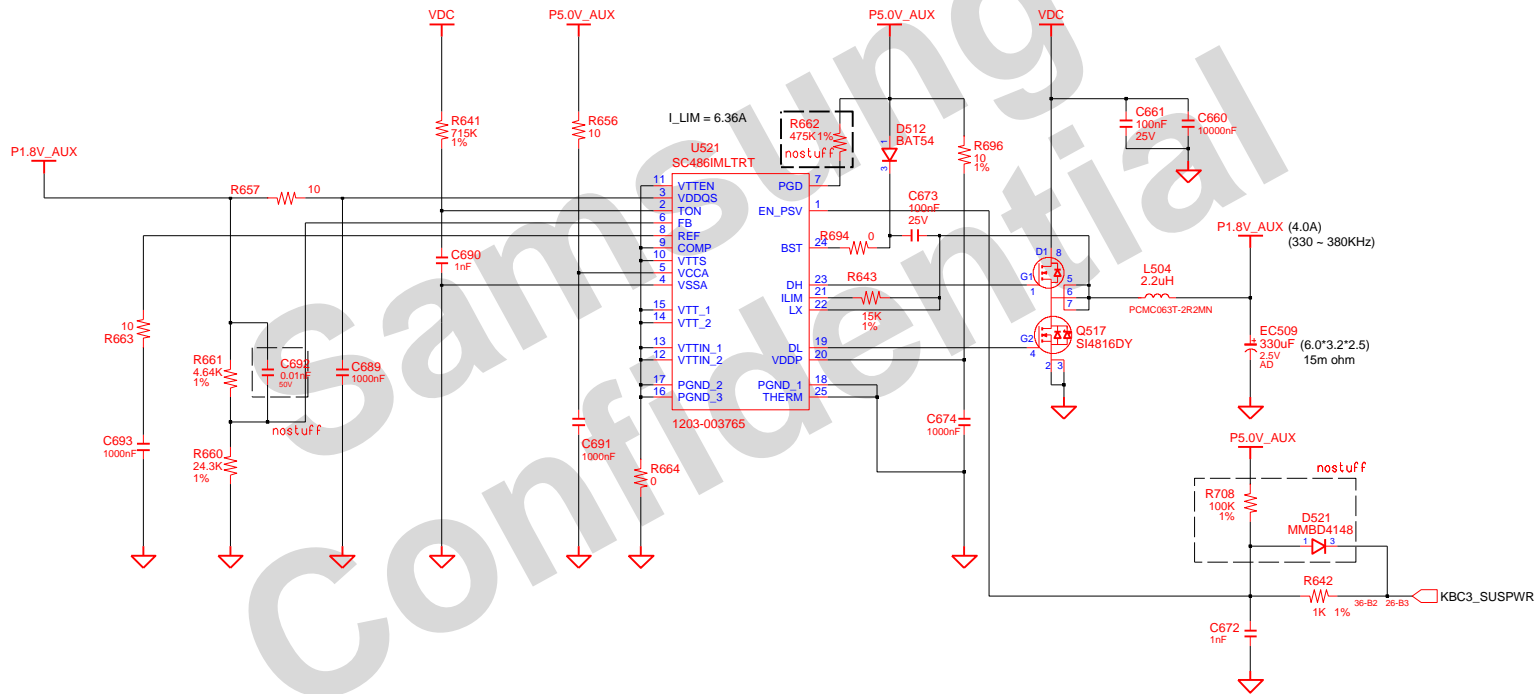


DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR	MAIN		
APPROVAL	EUH, J.S.	REV	1.0	P1.5V & VCCP	PART NO.	BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	37	OF 47

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# DDR2 POWER

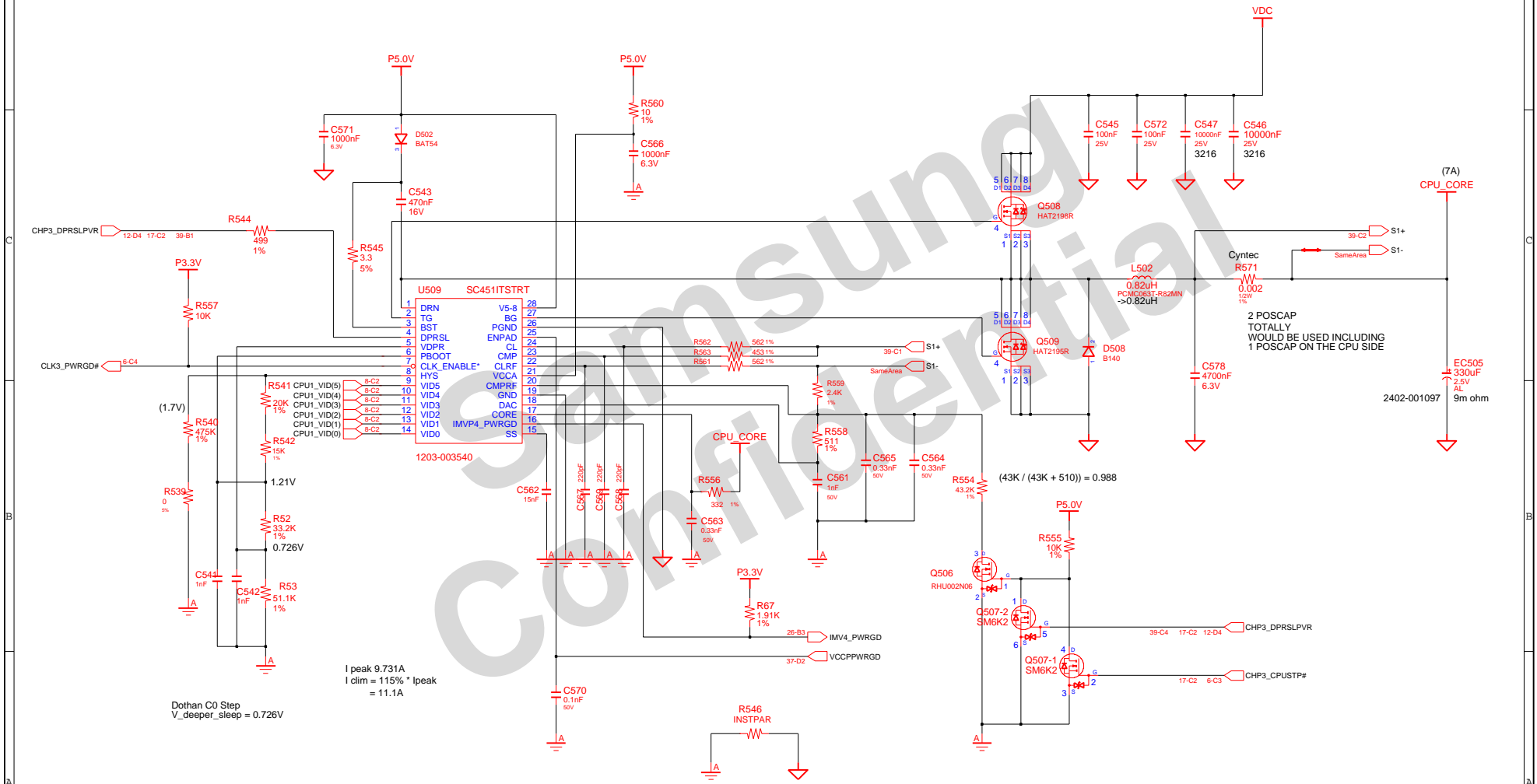


DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR	MAIN		
APPROVAL	EUH, J.S.	REV	1.0	DDR2 Power	PART NO.	BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	38	OF 47

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# CPU VRM

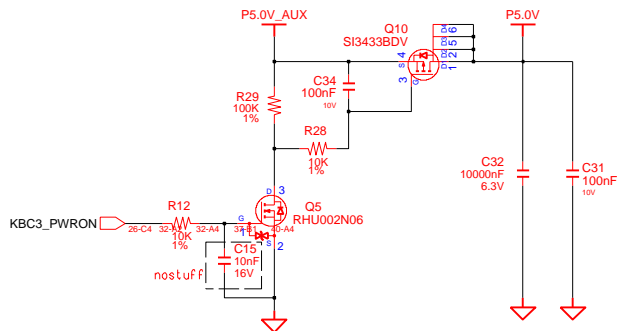


DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao MAIN CPU VRM	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00743A
CHECK	PARK, H.K.	DEV. STEP	SR			
APPROVAL	EUH, J.S.	REV	1.0			
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	39	OF 47

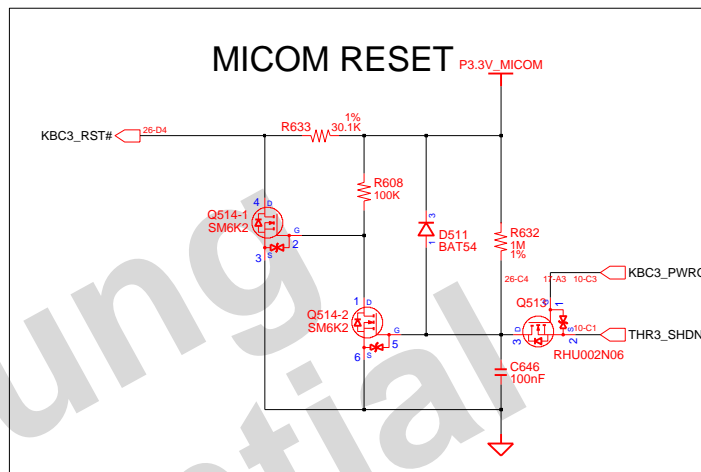
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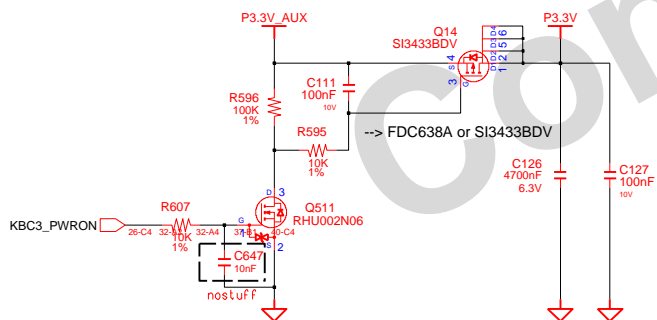
**Load Switch Control(P5.0V)**



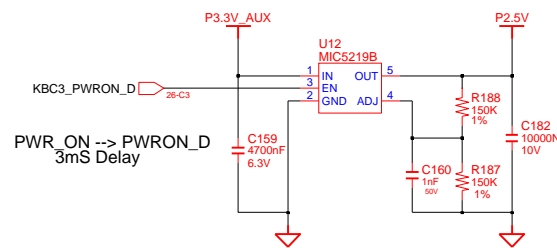
**MICOM RESET**



**Load Switch Control(P3.3V)**



**LDO Power (P2.5V)**



DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao MAIN Switched Power	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00743A
CHECK	PARK, H.K.	DEV. STEP	SR			
APPROVAL	EUH, J.S.	REV	1.0			
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	40 OF 47	



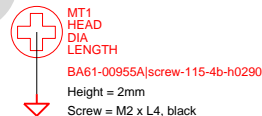
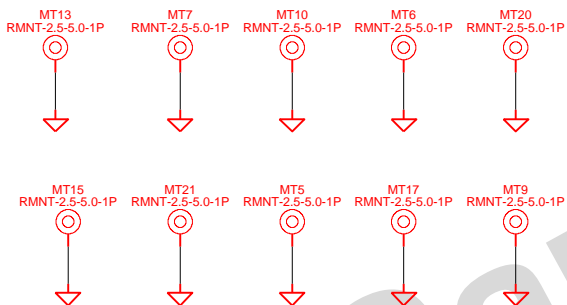
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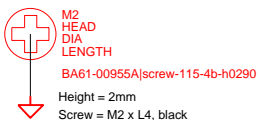
PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV1  
1 O  
2 O 3

**Main Board Mount Hole**



**Mount Hole for LAN sub board**



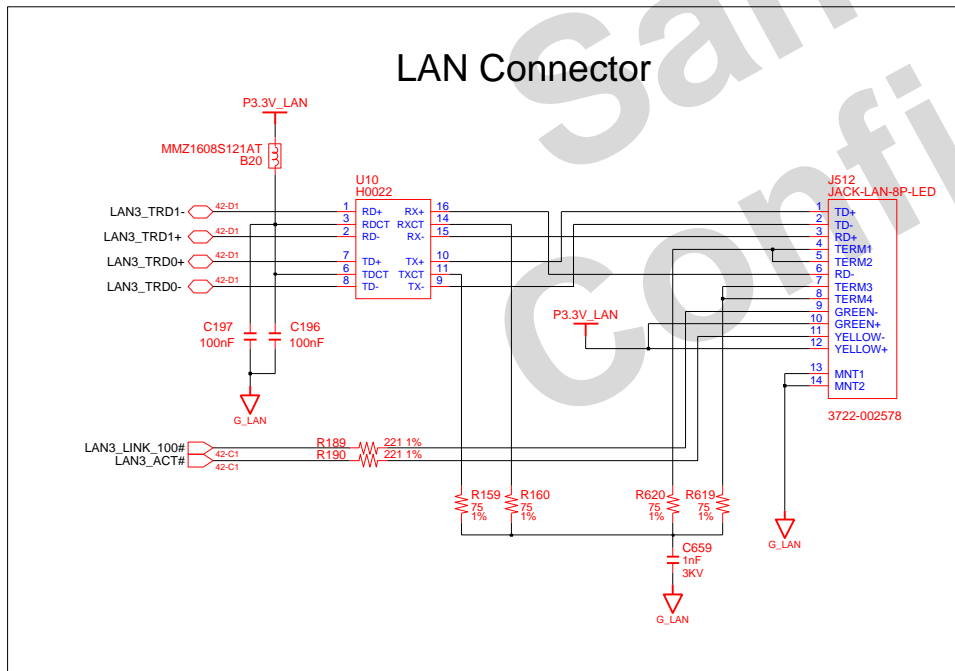
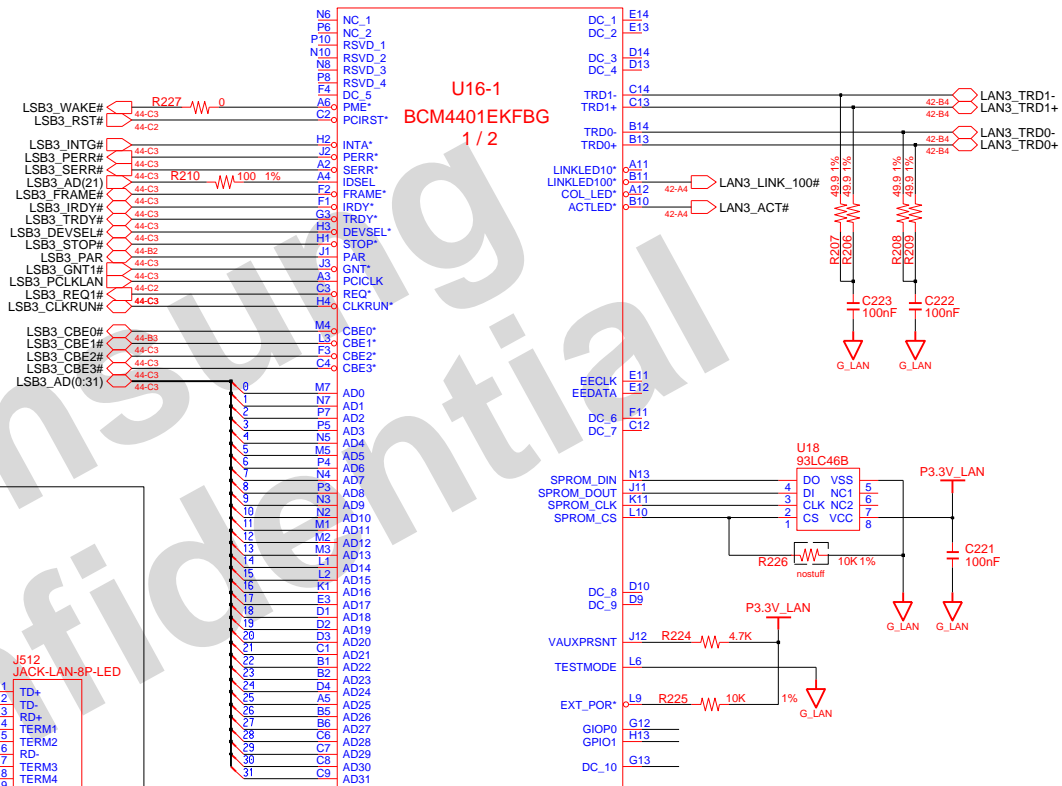
DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	<b>SAMSUNG</b> ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR	MAIN		
APPROVAL	EUH, J.S.	REV	1.0	Mount Hole		PART NO. BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	41	OF 47

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**LAN Controller (Only 10/100M)**

**LAN Board**  
(Page 42 ~ 44)

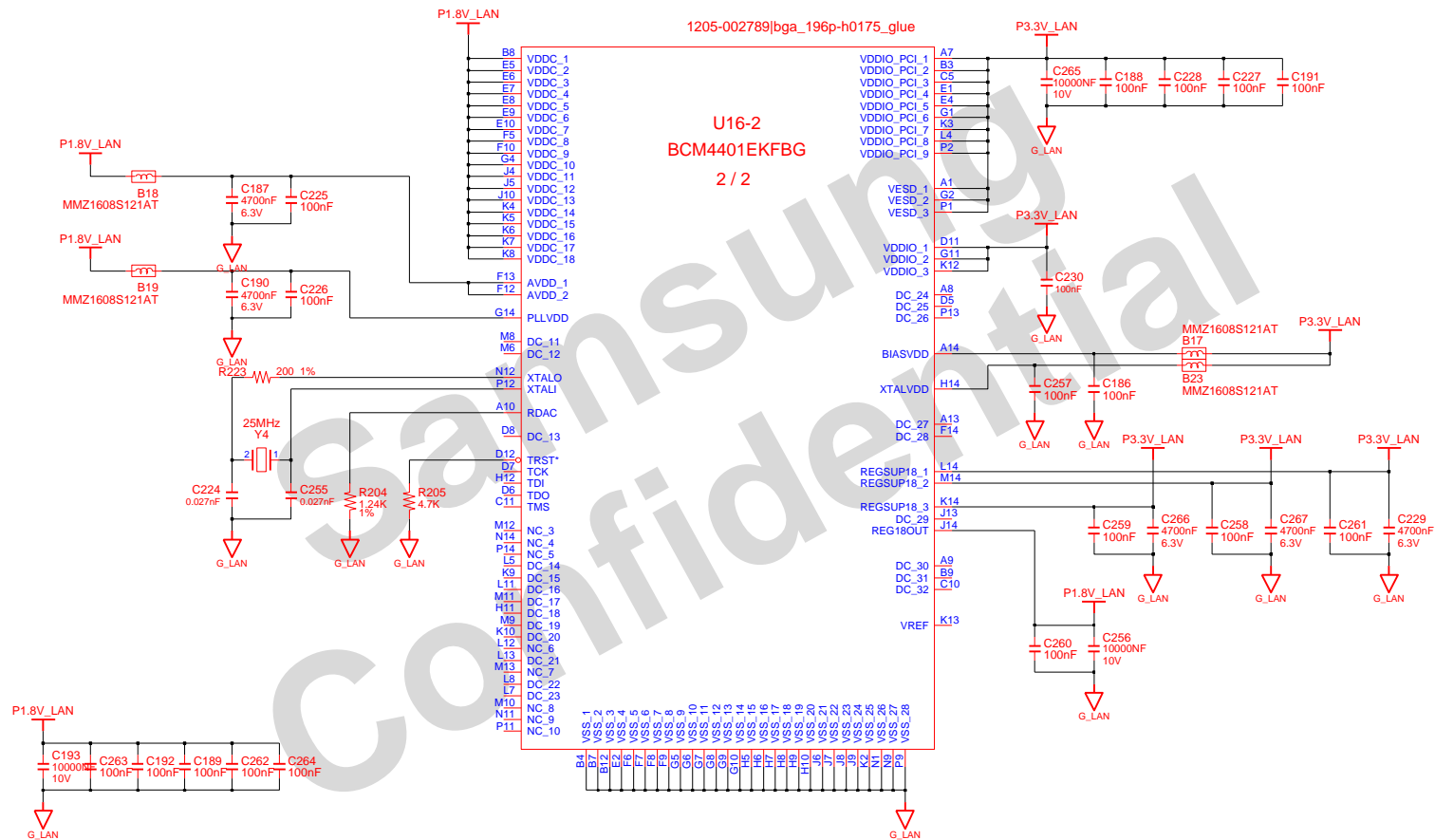


DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR		LAN B'd	
APPROVAL	EUH, J.S.	REV	1.0		LAN(1/3)	
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	42	OF 47

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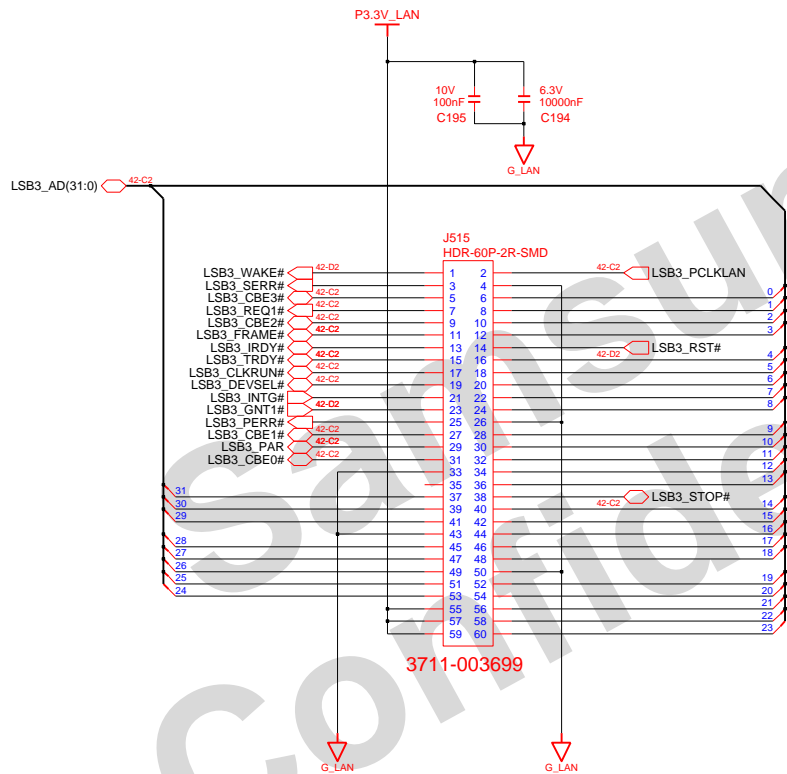
# LAN Controller (Only 10/100M)



DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao LAN B'd LAN(2/3)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00743A
CHECK	PARK, H.K.	DEV. STEP	SR			
APPROVAL	EUH, J.S.	REV	1.0			
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	43 OF 47	

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Bottom MT for LAN sub board  
 Screw = 6001-001570, M2xL4 black

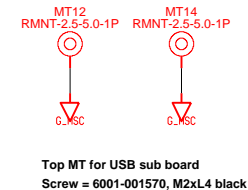
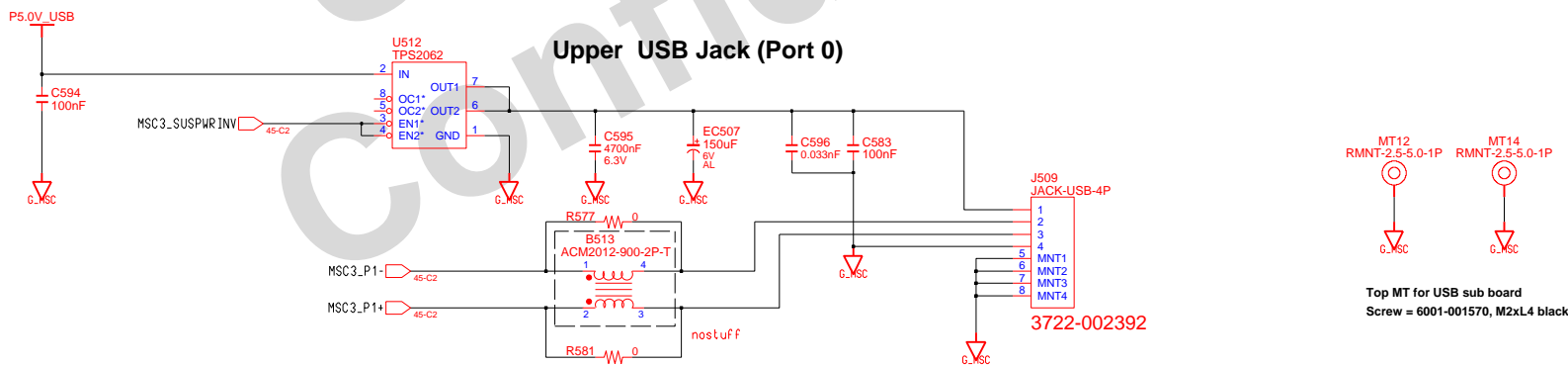
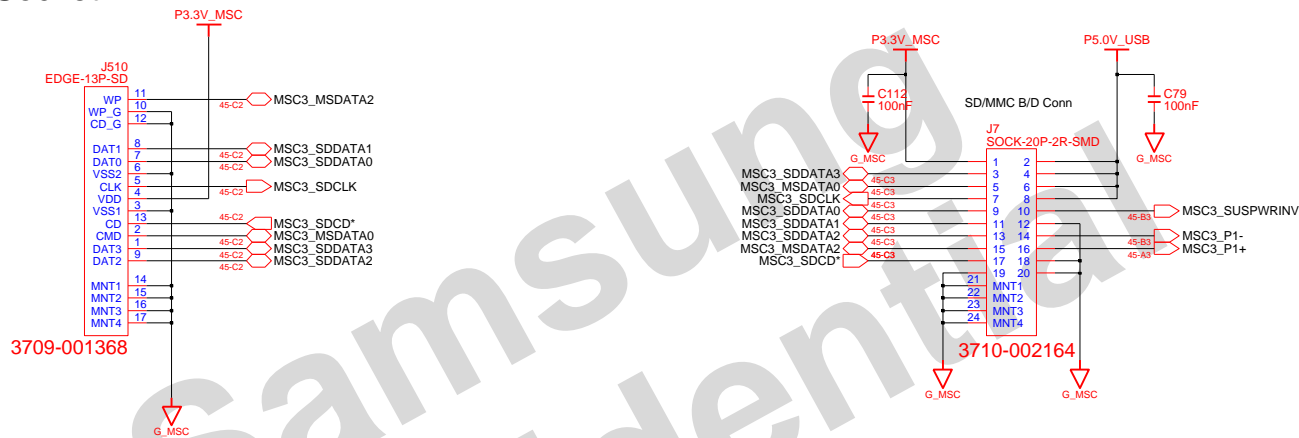
DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR	LAN B'd	LAN(3/3)	
APPROVAL	EUH, J.S.	REV	1.0			PART NO. BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	44	OF 47

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# SD/MMC Socket Board

## SD/MMC Socket



DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	<b>SAMSUNG</b> ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR	SD/MMC Socket B'd		
APPROVAL	EUH, J.S.	REV	1.0	SD/MMC Socket	PART NO.	BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	45	OF 47

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# Sub Board Left

## Sub Left Board to Main board

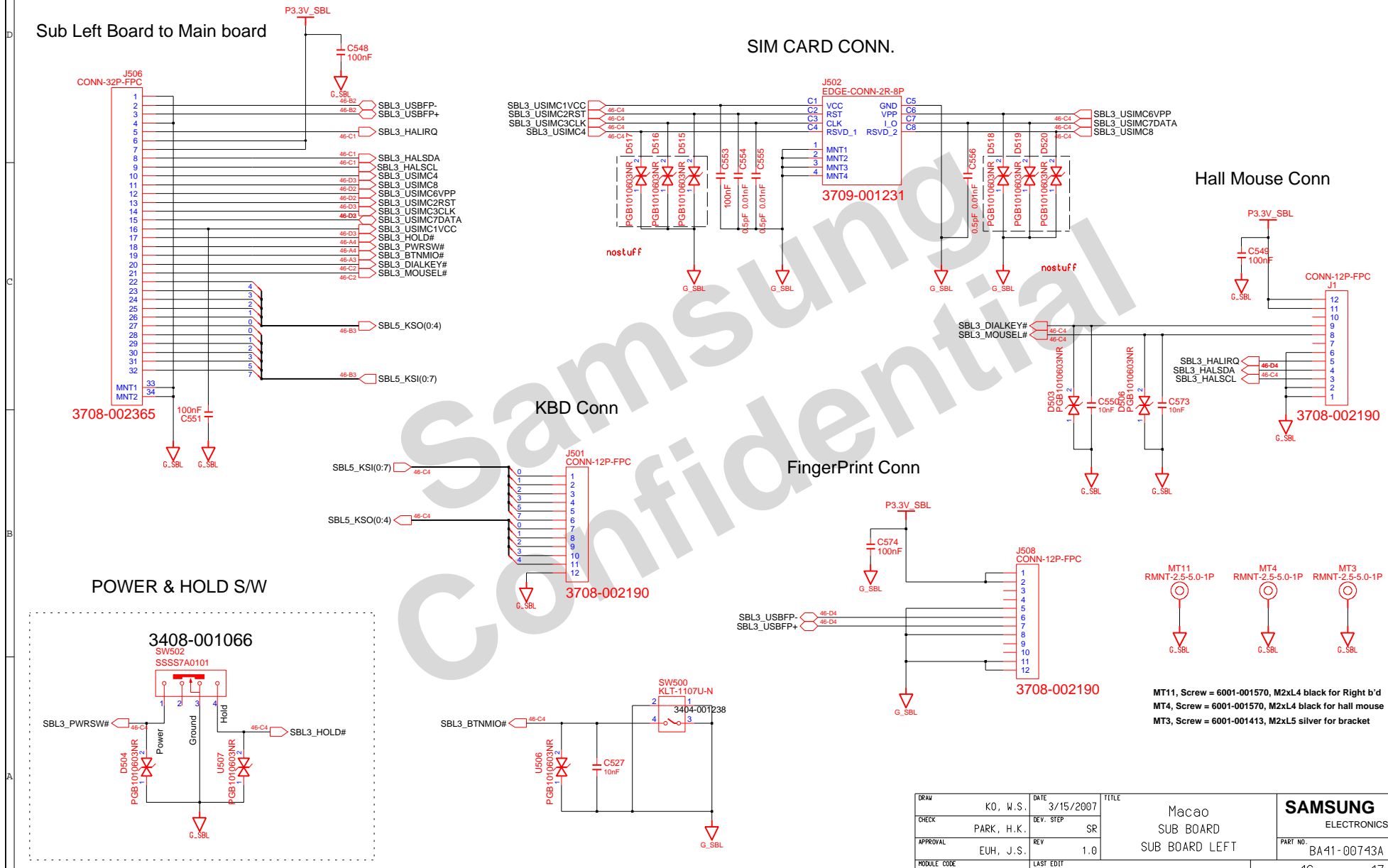
## SIM CARD CONN.

## Hall Mouse Conn

## KBD Conn

## Fingerprint Conn

## POWER & HOLD S/W



MT11, Screw = 6001-001570, M2xL4 black for Right b'd  
 MT4, Screw = 6001-001570, M2xL4 black for hall mouse  
 MT3, Screw = 6001-001413, M2xL5 silver for bracket

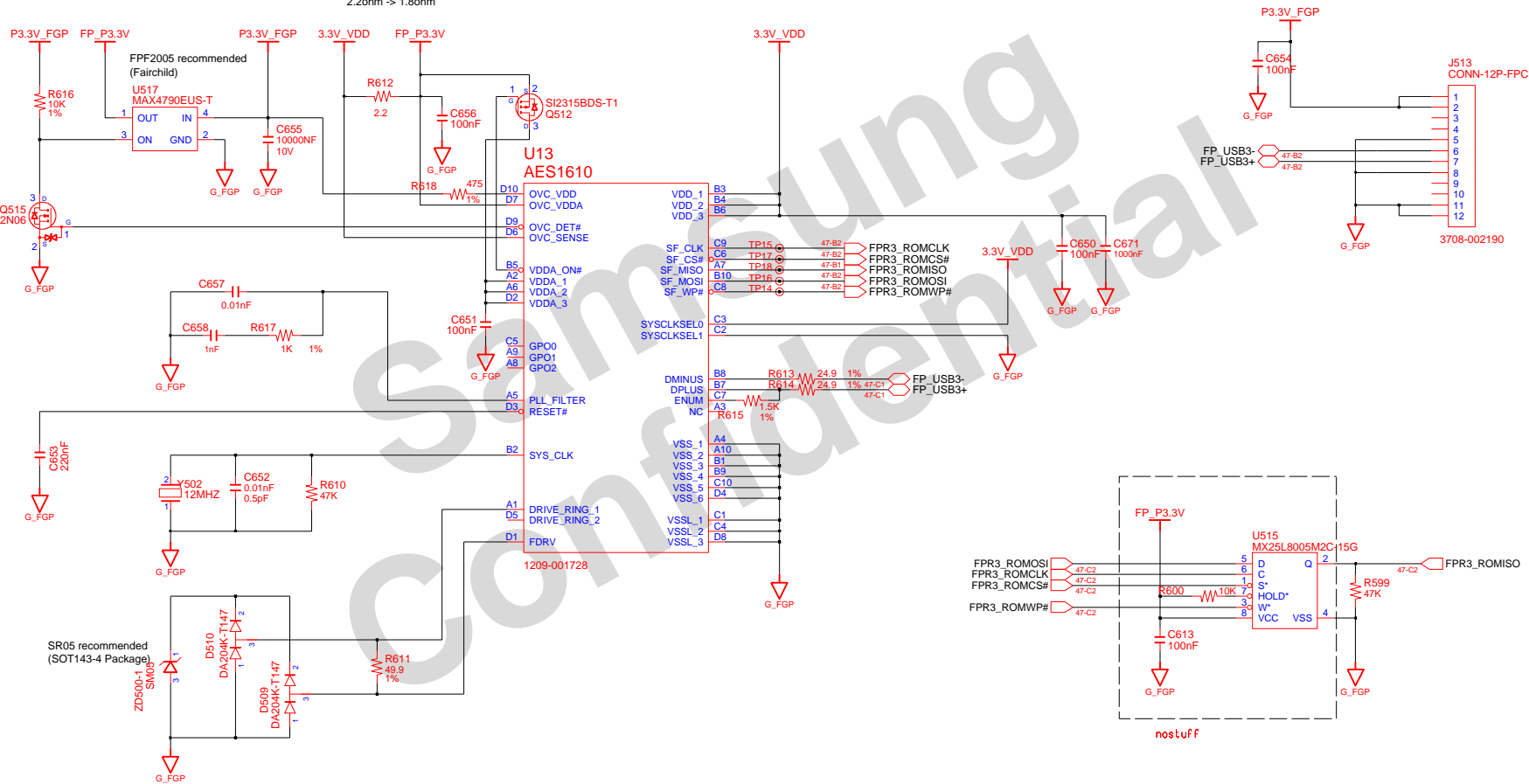
DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao SUB BOARD SUB BOARD LEFT	<b>SAMSUNG</b> ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR	REV	1.0	
APPROVAL	EUH, J.S.	LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	46	OF 47
MODULE CODE						BA41-00743A

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# Finger Print Sub Board

Recommend value  
2.2ohm -> 1.8ohm



DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao SUB BOARD FINGERPRINT	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00743A
CHECK	PARK, H.K.	DEV. STEP	SR			
APPROVAL	EUH, J.S.	REV	1.0			
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	47 OF 47	