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FIRENZE II

CPU : Intel Yonah (533/667MHz)

Chip Set : RC410MD & SB450

Remarks : Mobility Platform

Model Name : FIRENZE II

PBA Name : MAIN

PCB Code : GCE : BA41-00659A
 TPT : BA41-00671A

Dev. Step : PRR

Revision : X03

T.R. Date : 2006.03.30

DRAW	CHECK	APPROVAL
TERMI	HJ KIM	SJ PARK

■ Owner : SEC Mobile R & D Signature : X

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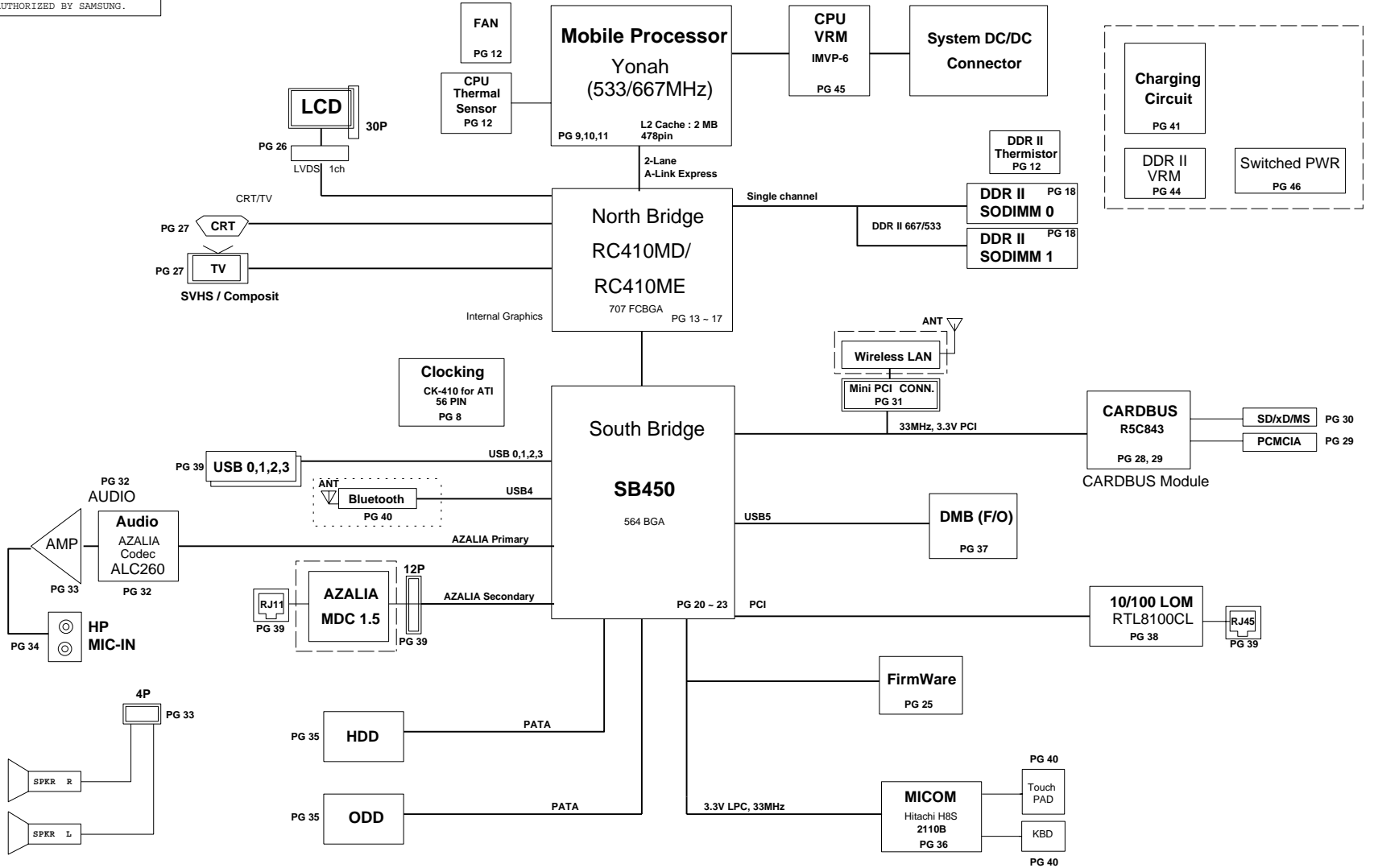
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DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR	COVER	PART NO.	
APPROVAL	SJ PARK	REV	1.0		BA41-00659A	
MODULE CODE		LAST EDIT				

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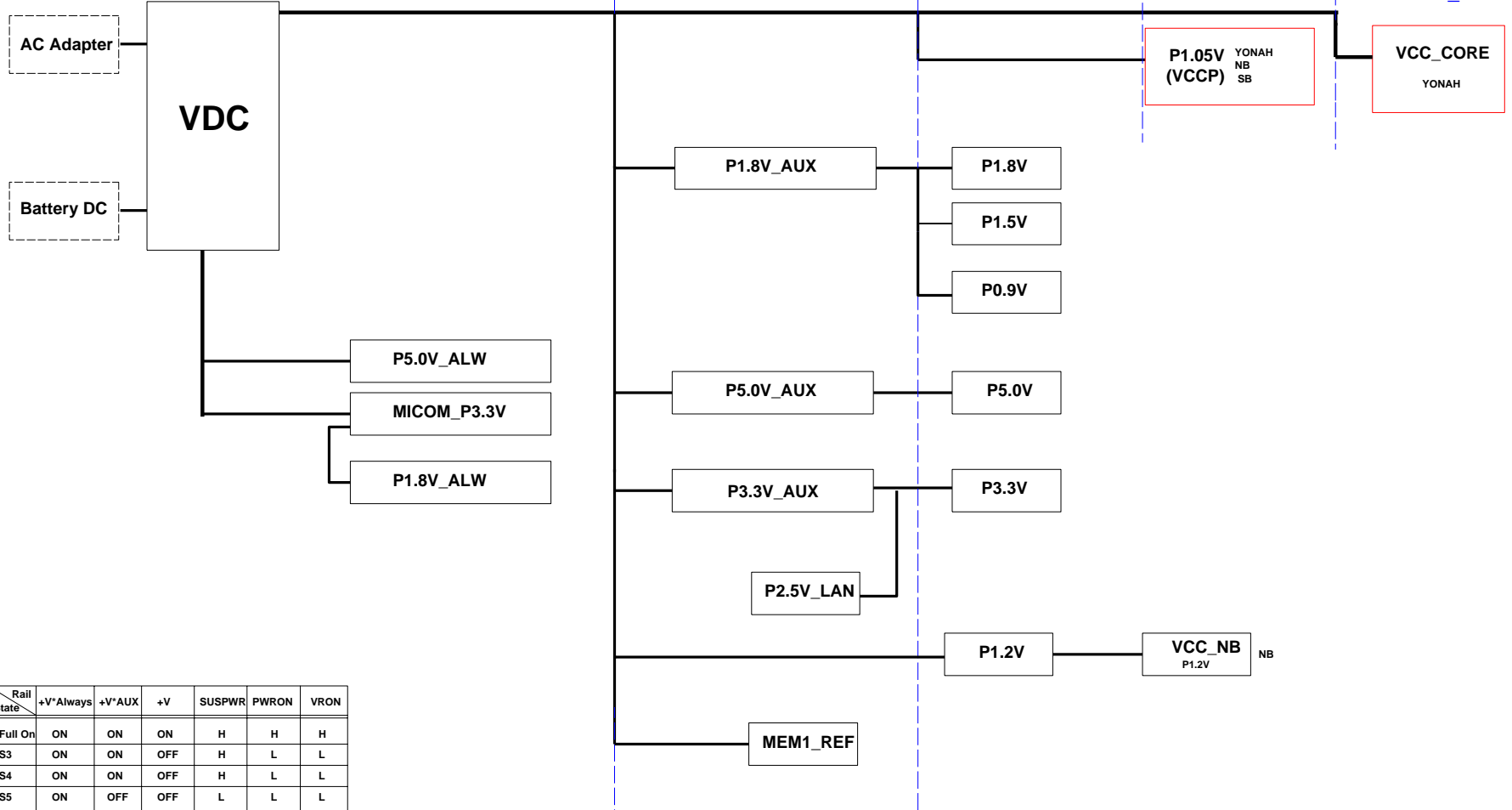
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CHECK	HJ KIM	DEV. STEP	SR	MAIN	OPERATION BLOCK DIAGRAM	
APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00659A
MODULE CODE		LAST EDIT				

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Power Diagram

KBC3_LANPWRON KBC3_SUSPWR KBC3_PWRON KBC3_VRON VCCP3_PWRGD

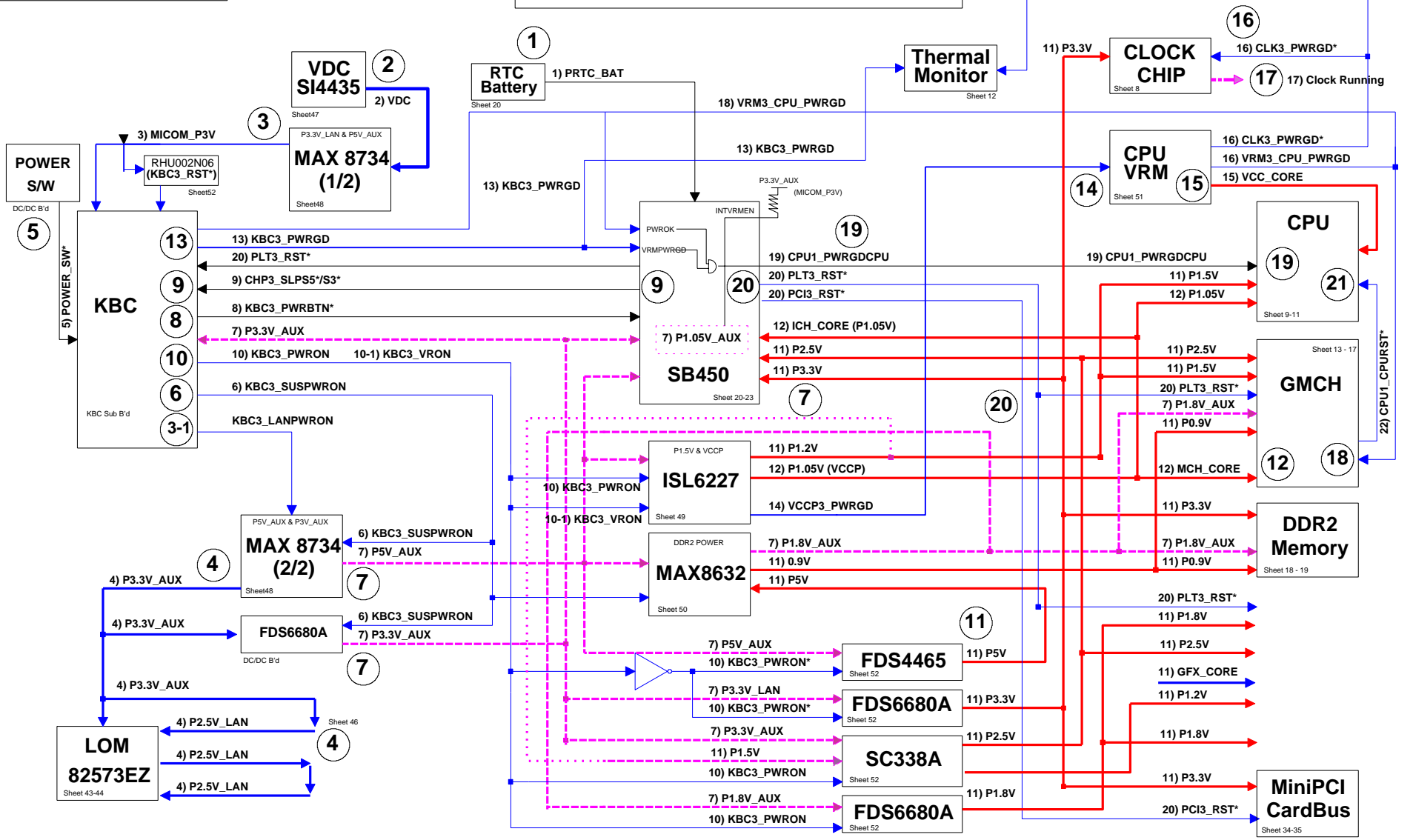


Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT				

POWER SEQUENCE Rev. 0.8



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II
CHECK	HJ KIM	DEV. STEP	SR	SAMSUNG ELECTRONICS	
APPROVAL	SJ PARK	REV	1.0	POWER SEQUENCE	PART NO. BA41-00659A
MODULE CODE		LAST EDIT		Apr 5, 2006 8:18:08 PM	PAGE 4 OF 52

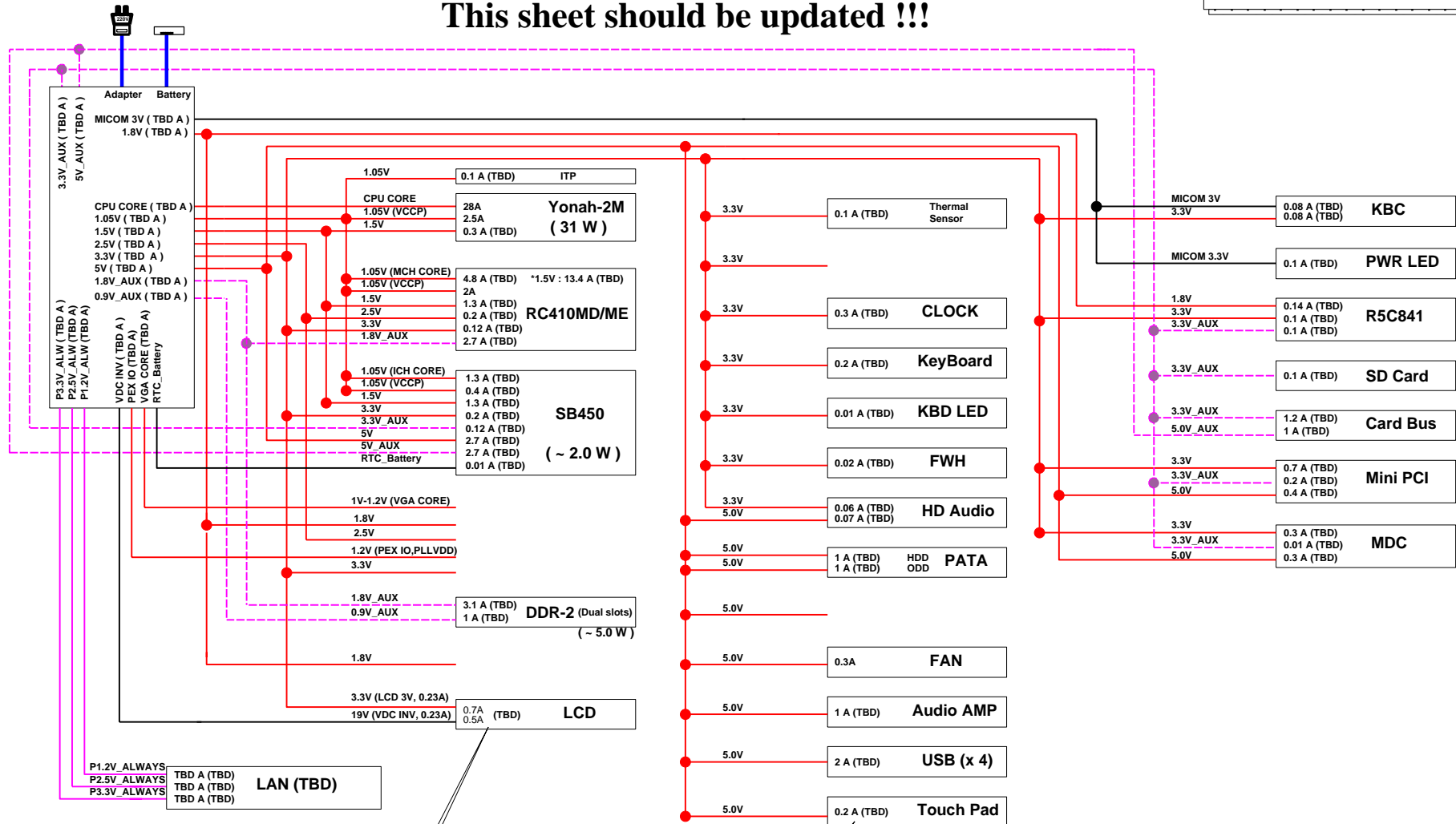
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POWER RAILS ANALYSIS Rev. 0.8

—————	S0 - S5
.....	S0 - S3
—————	OFF IN S3 - S5

This sheet should be updated !!!

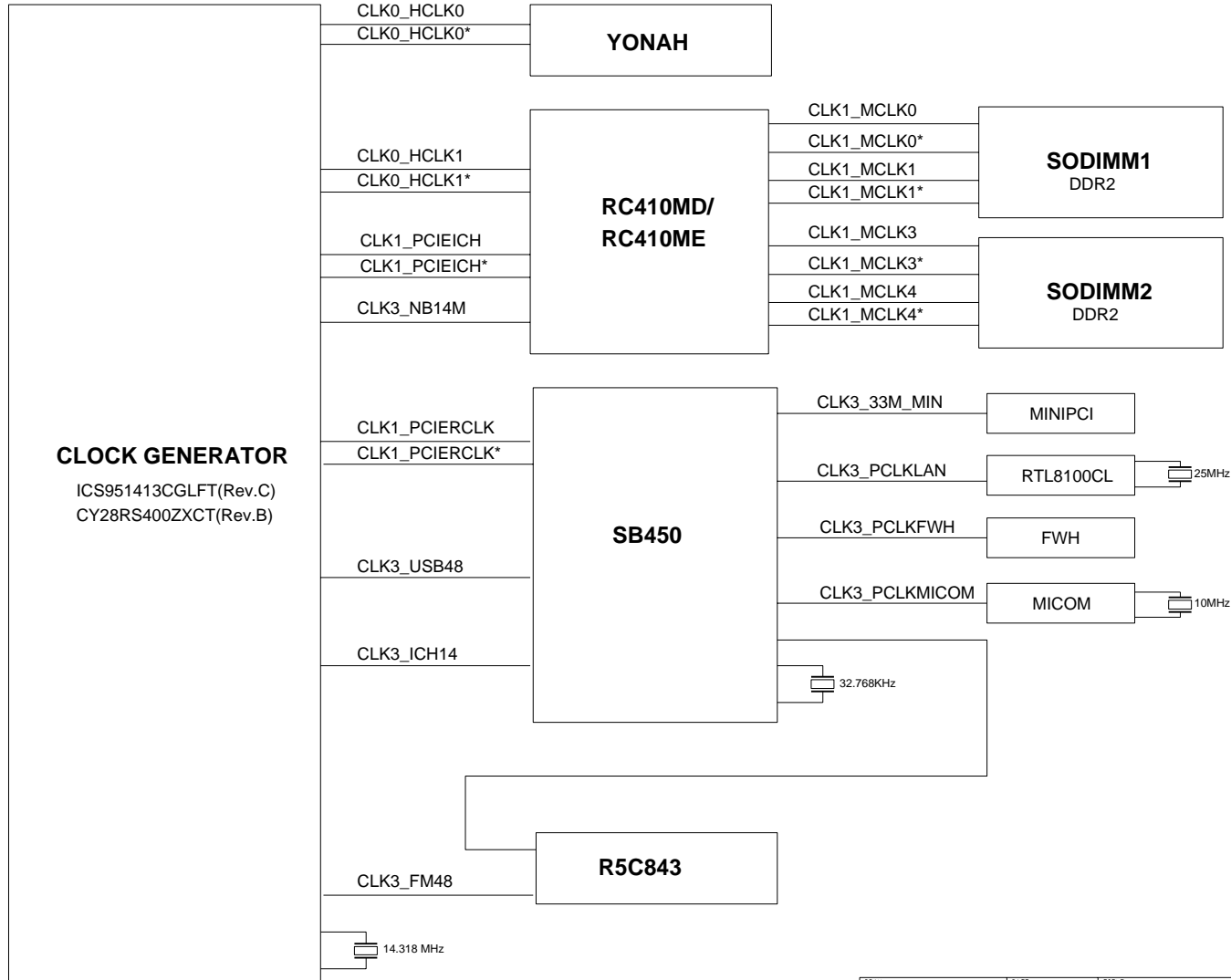


Value by Datasheet/Application notes (Value by measurement)

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II POWER BLOCK	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT				
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DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II CLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00659A
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	E, F, G
LAN	AD21	1	C
MINIPCI	AD23	2	A, B
USB	AD30(internal)	-	-
Hub to PCI	AD31(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	--
Internal MAC	AD31(internal)	-	-
AC Link	-	-	-

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB450	Real Time Clock
Crystal	10MHz	MICOM	HGS-2110B
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	25MHz	LAN	LOM

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308-1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P3.3V_DTV	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_ALWS	3.3V power rail (Always On)
P2.5V_ALWS	2.5V power rail (Always On)
P1.2V_ALWS	1.2V power rail (Always On)

CPU Core Voltage Table

VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0 0	1.708 V	1 0 0 0 0 0	1.196 V
0 0 0 0 0 1	1.692 V	1 0 0 0 0 1	1.180 V
0 0 0 0 1 0	1.676 V	1 0 0 0 1 0	1.164 V
0 0 0 0 1 1	1.660 V	1 0 0 0 1 1	1.148 V
0 0 0 1 0 0	1.644 V	1 0 0 1 0 0	1.132 V
0 0 0 1 0 1	1.628 V	1 0 0 1 0 1	1.116 V
0 0 0 1 1 0	1.612 V	1 0 0 1 1 0	1.100 V
0 0 0 1 1 1	1.596 V	1 0 0 1 1 1	1.084 V
0 0 1 0 0 0	1.580 V	1 0 1 0 0 0	1.068 V
0 0 1 0 0 1	1.564 V	1 0 1 0 0 1	1.052 V
0 0 1 0 1 0	1.548 V	1 0 1 0 1 0	1.036 V
0 0 1 0 1 1	1.532 V	1 0 1 0 1 1	1.020 V
0 0 1 1 0 0	1.516 V	1 0 1 1 0 0	1.004 V
0 0 1 1 0 1	1.500 V	1 0 1 1 0 1	0.988 V
0 0 1 1 1 0	1.484 V	1 0 1 1 1 0	0.972 V
0 0 1 1 1 1	1.468 V	1 0 1 1 1 1	0.956 V
0 1 0 0 0 0	1.452 V	1 1 0 0 0 0	0.940 V
0 1 0 0 0 1	1.436 V	1 1 0 0 0 1	0.924 V
0 1 0 0 1 0	1.420 V	1 1 0 0 1 0	0.908 V
0 1 0 0 1 1	1.404 V	1 1 0 0 1 1	0.892 V
0 1 0 1 0 0	1.388 V	1 1 0 1 0 0	0.876 V
0 1 0 1 0 1	1.372 V	1 1 0 1 0 1	0.860 V
0 1 0 1 1 0	1.356 V	1 1 0 1 1 0	0.844 V
0 1 0 1 1 1	1.340 V	1 1 0 1 1 1	0.828 V
0 1 1 0 0 0	1.324 V	1 1 1 0 0 0	0.812 V
0 1 1 0 0 1	1.308 V	1 1 1 0 0 1	0.796 V
0 1 1 0 1 0	1.292 V	1 1 1 0 1 0	0.780 V
0 1 1 0 1 1	1.276 V	1 1 1 0 1 1	0.764 V
0 1 1 1 0 0	1.260 V	1 1 1 1 0 0	0.748 V
0 1 1 1 0 1	1.244 V	1 1 1 1 0 1	0.732 V
0 1 1 1 1 0	1.228 V	1 1 1 1 1 0	0.716 V
0 1 1 1 1 1	1.212 V	1 1 1 1 1 1	0.700 V

Lowest Freq.

HFM Voltage
770:1.26V->1.372V
730,740,750,760:1.26->1.356V

IC / SMB Address

Devices	Address	Hex	Bus
SB450	Master	-	SMBUS Master
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-410 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0, 1	SYSTEM PORT A
2, 3	SYSTEM PORT B
4	BLUETOOTH
5	DMB

System Power States

CHP3_SLP1S* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
 In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.
 CHP3_SLP3S* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
 CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
 CHP3_SLP5S* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

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CHECK	HJ KIM	DEV. STEP	SR	MAIN	BOARD INFORMATION	ELECTRONICS
APPROVAL	SU PARK	REV	1.0			PART NO. BA41-00659A
MODULE CODE		LAST EDIT		Apr 15, 2006 8:18:08 PM	PAGE	7 OF 52

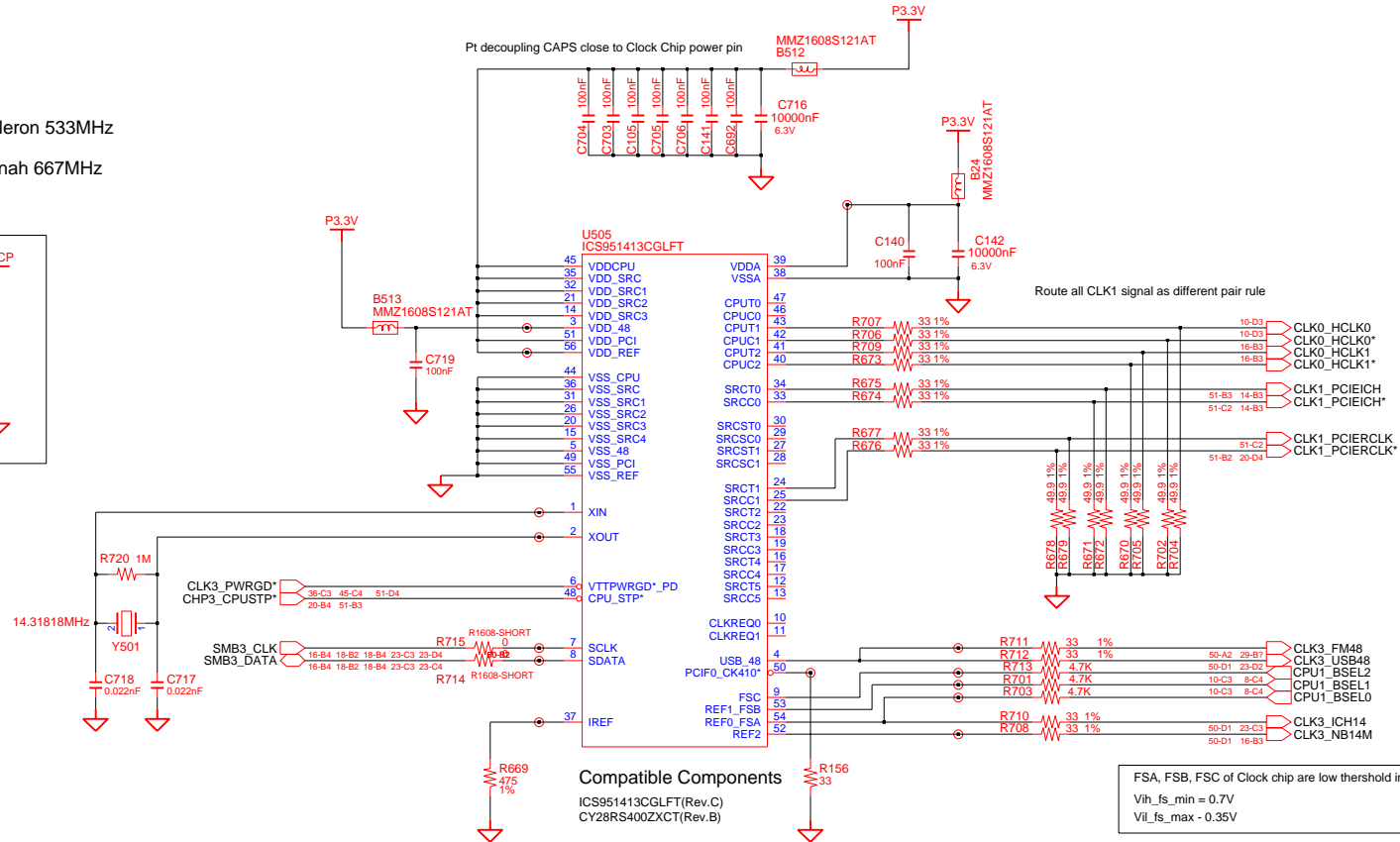
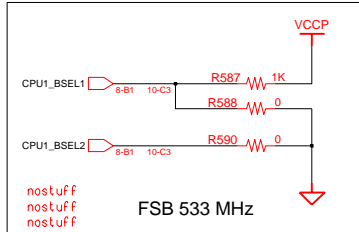
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FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

Celeron 533MHz

Yonah 667MHz



Compatible Components
 ICS951413CGLFT(Rev.C)
 CY28RS400ZXCT(Rev.B)

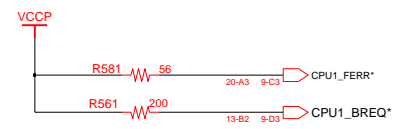
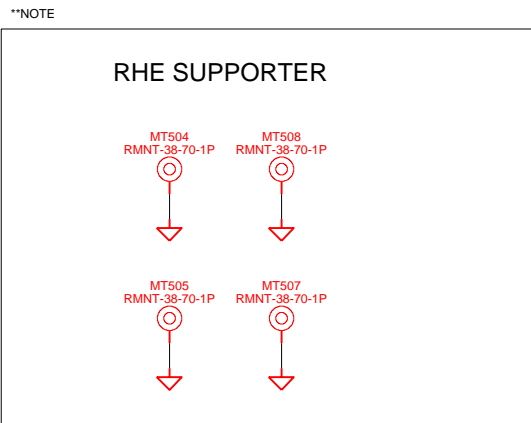
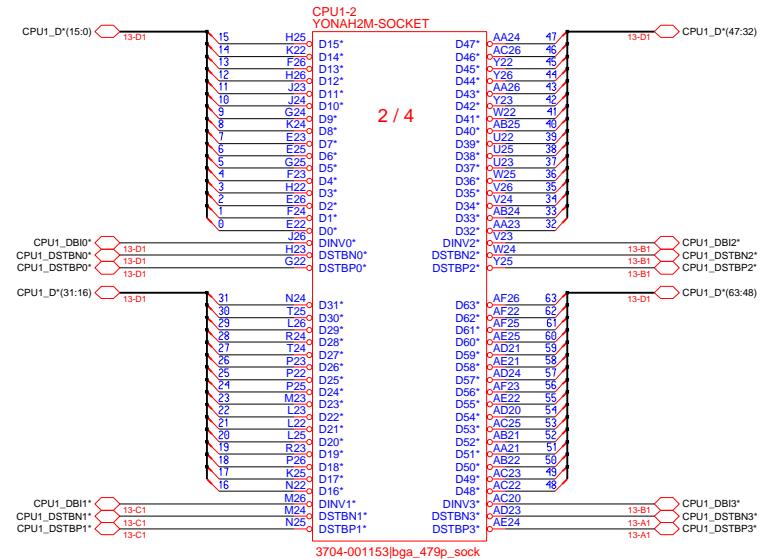
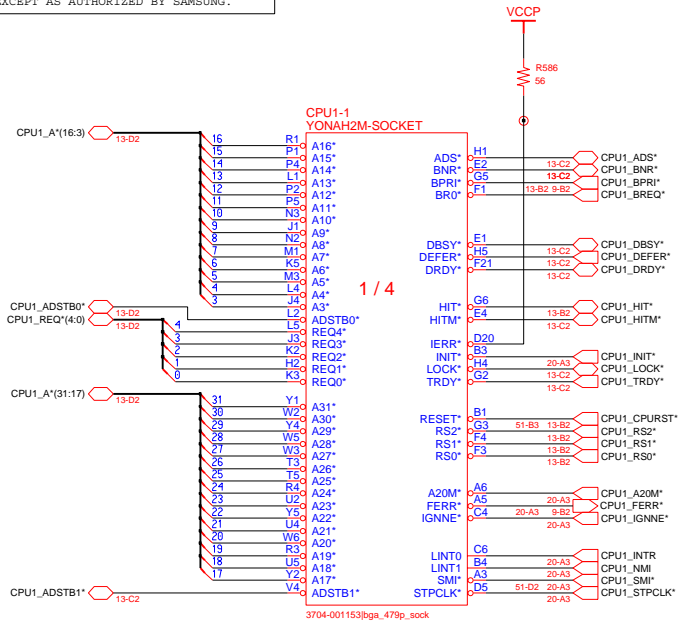
FSA, FSB, FSC of Clock chip are low threshold inputs
 Vih_fs_min = 0.7V
 Vil_fs_max = 0.35V

Place all the series termination resistor as close as Clock Chip as possible

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR	CLOCK GENERATOR		
APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00659A
MODULE CODE	LAST EDIT		Apr 15, 2006 8:18:08 PM		PAGE	8 OF 52

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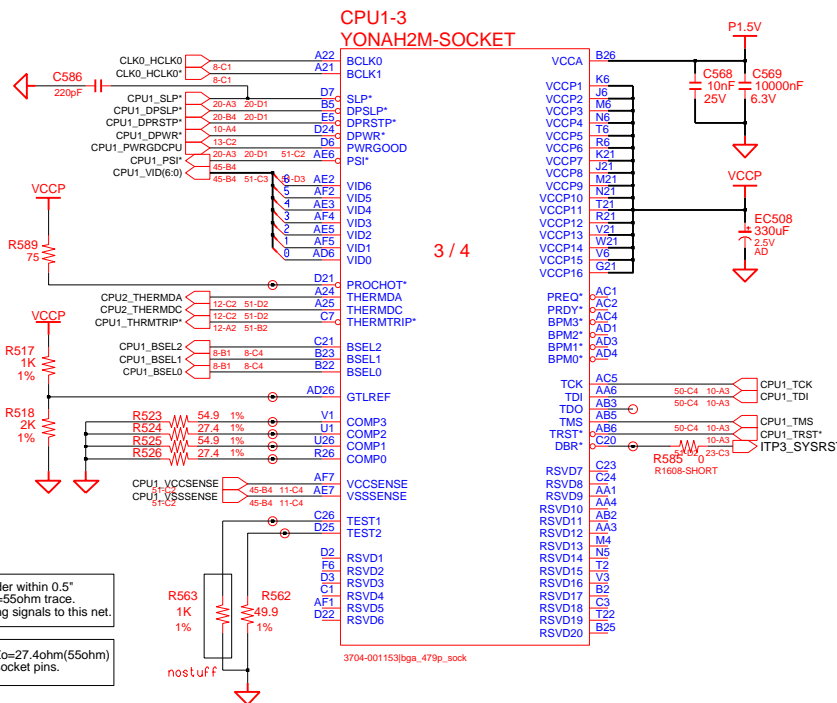
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CHECK	HJ KIM	DEV. STEP	SR	REV	YONAH CPU (1/3)	
APPROVAL	SJ PARK	REV	1.0	LAST EDIT		
MODULE CODE						

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GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0.2/COMP1.3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

3704-001153bga_479p_sock

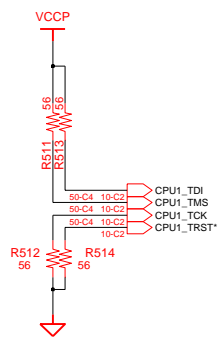
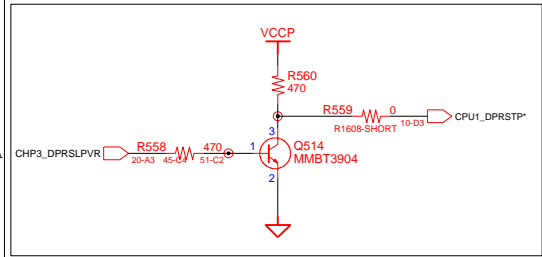
CPU Core Voltage Table MVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 0	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 0 1	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 0	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 0 1 1	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 0	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 0 1	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 0	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 0 0	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 1	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 0 1 1 1 1	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

***11111111** : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

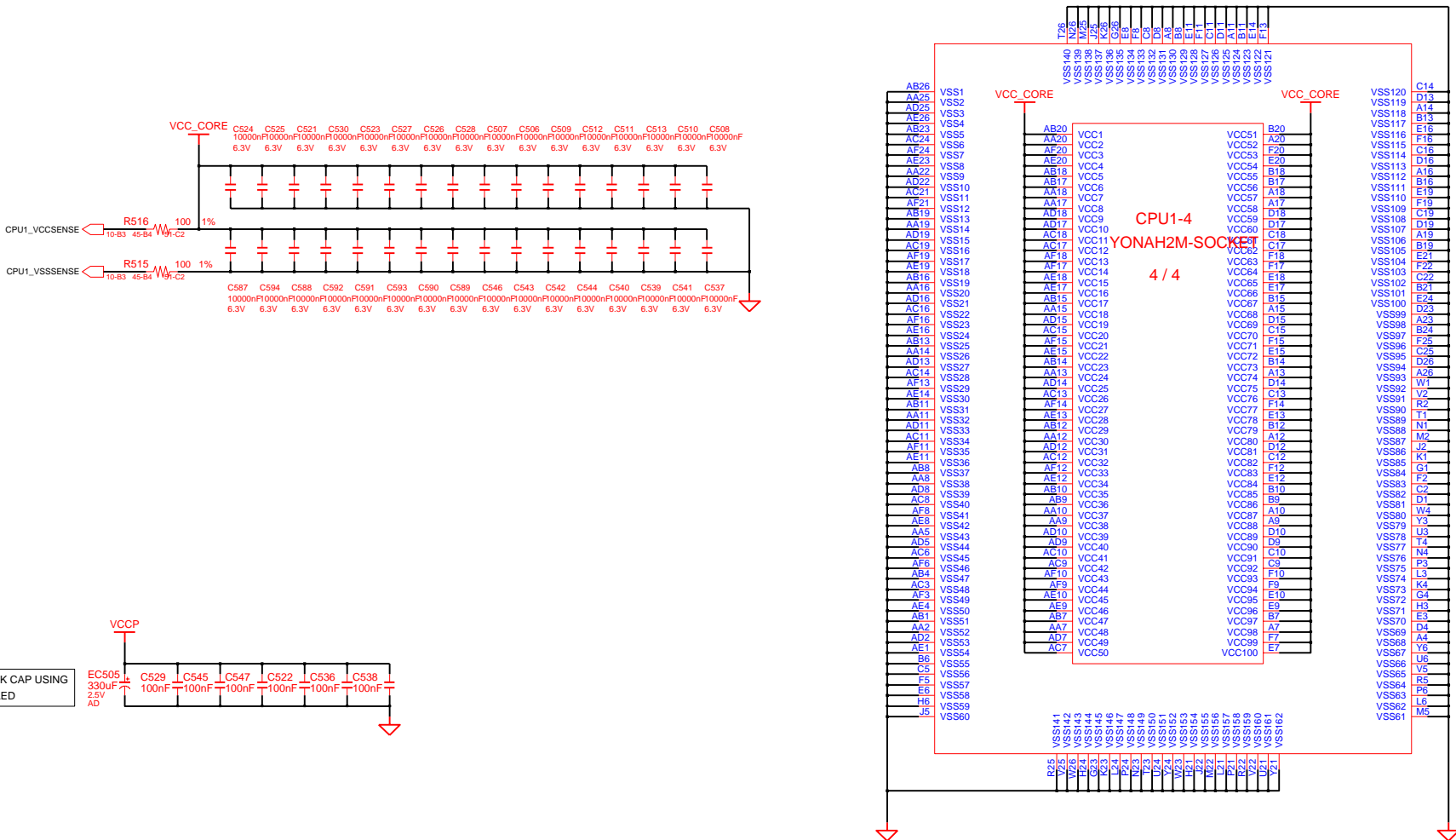
Check CPU Power Page (P46)& SB450(P20)



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR	APPROVAL	YONAH CPU(2/3)	
APPROVAL	SJ PARK	REV	1.0	MODULE CODE	LAST EDIT	PART NO. BA41-00659A
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DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0	YONAH CPU(3/3)		
MODULE CODE		LAST EDIT				

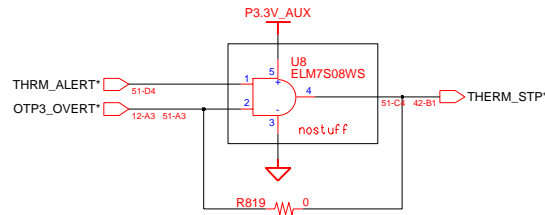
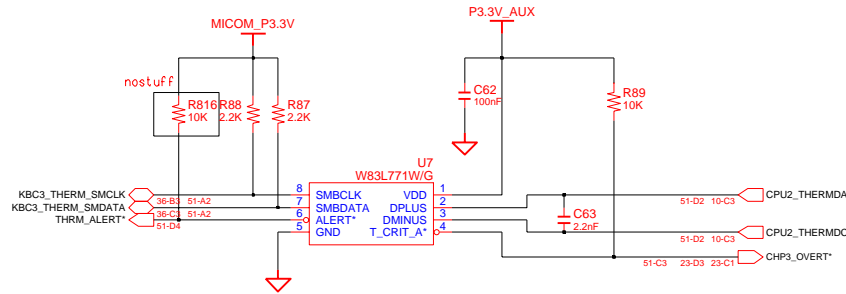
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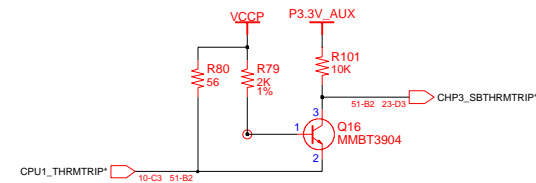
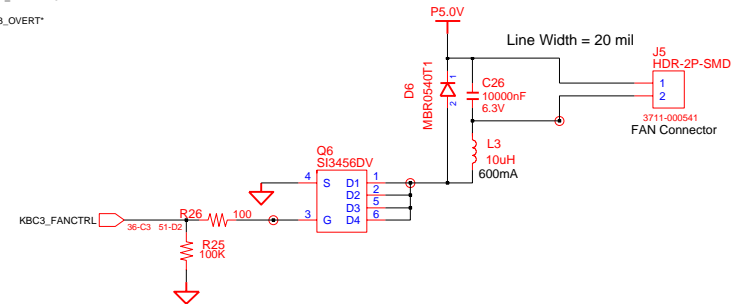
Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

CPU Thermal Sensor



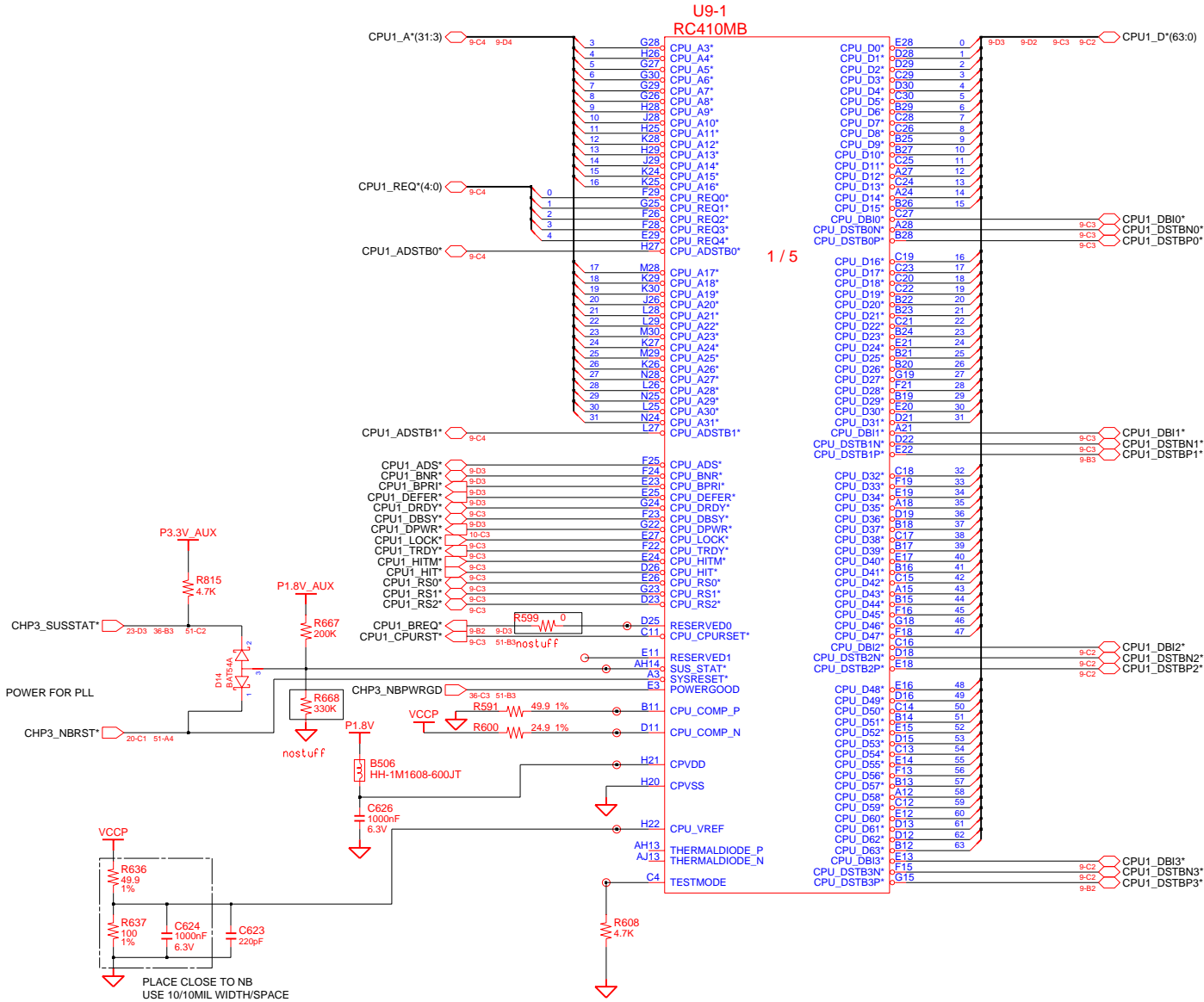
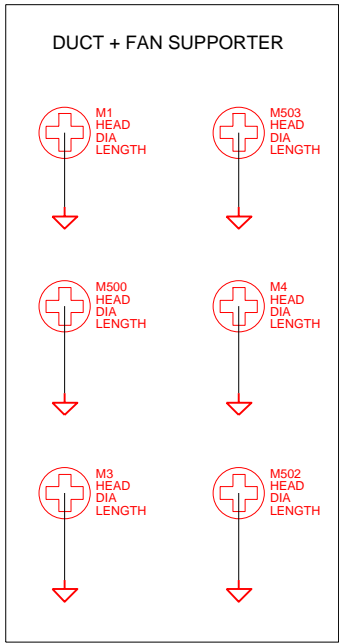
FAN Control Logic



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR	MAIN		
APPROVAL	SJ PARK	REV	1.0	THERMAL SENSOR/FAN CONTRL	PART NO.	BA41-00659A
MODULE CODE		LAST EDIT		Apr 15, 2006 8:18:08 PM	PAGE	12 OF 52

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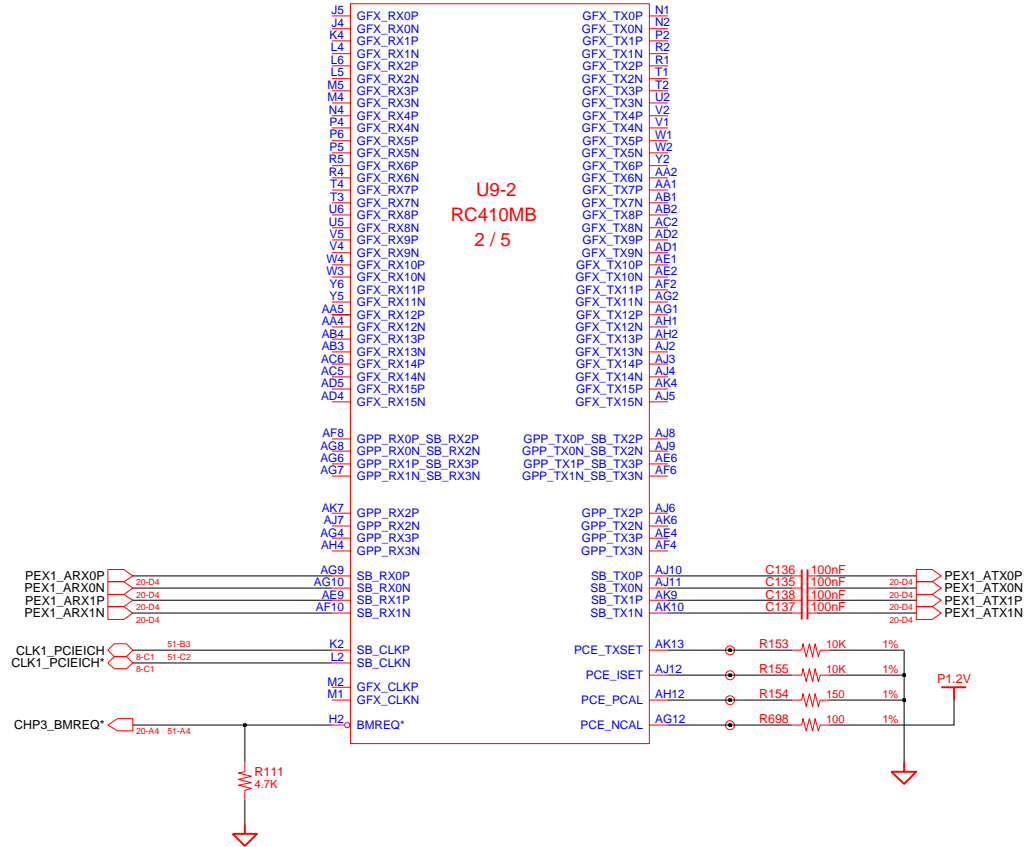
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DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN RC410MD(1/5)	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT				
				Apr 15, 2006 8:18:08 PM	PAGE	13 OF 52

SAMSUNG PROPRIETARY

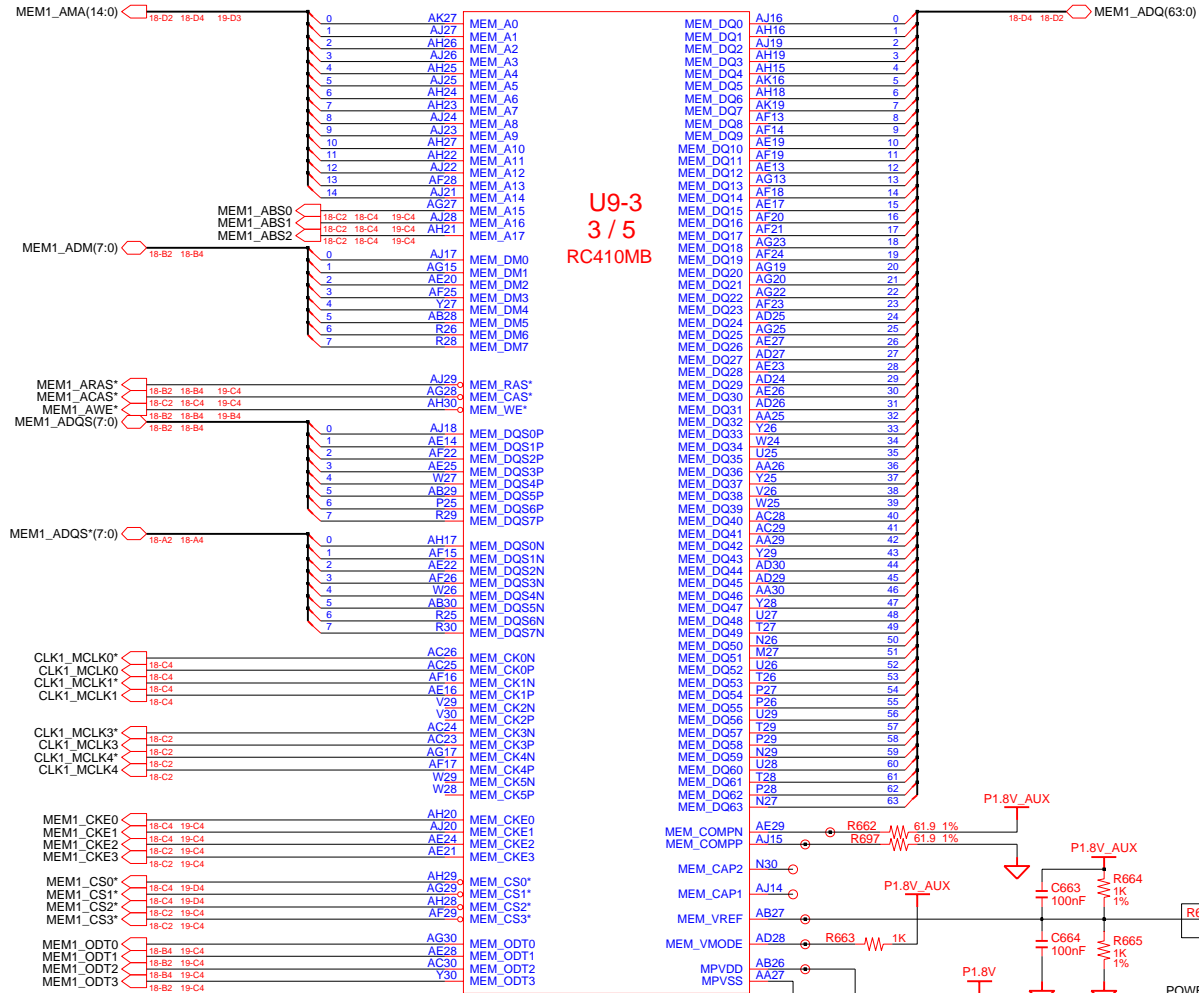
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DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN RC410MD(2/5)	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT				

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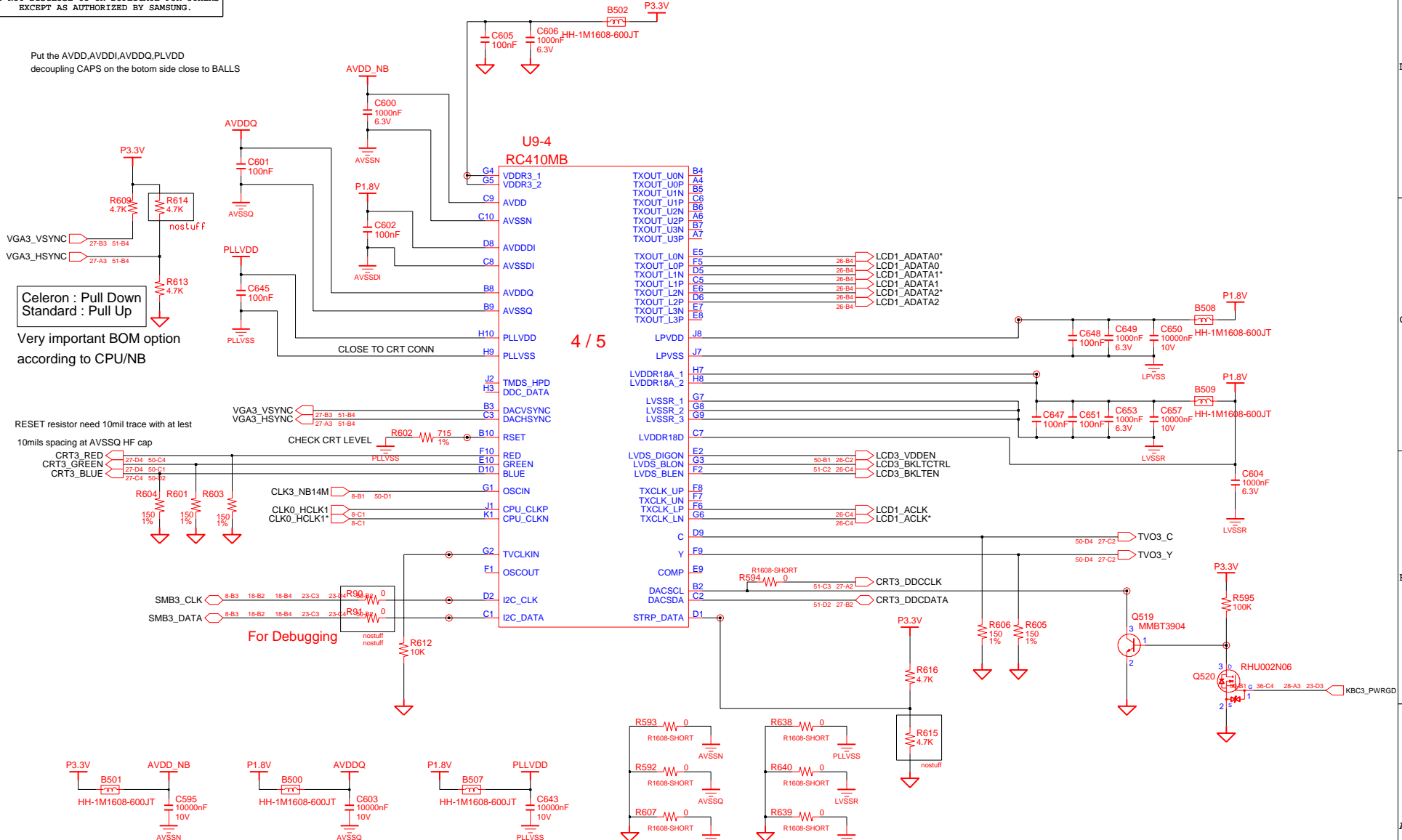
U9-3
3/5
RC410MB

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN RC410MD(3/5)	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT				

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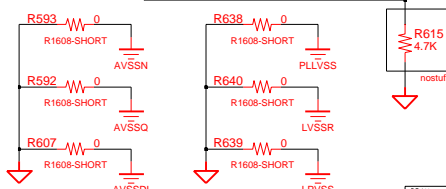
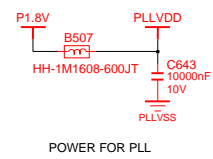
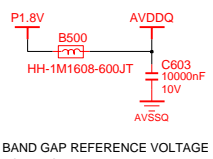
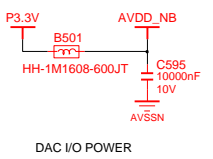
Put the AVDD,AVDDI,AVDDQ,PLVDD decoupling CAPS on the botom side close to BALLS



**Celeron : Pull Down
Standard : Pull Up**
Very important BOM option
according to CPU/NB

RESET resistor need 10mil trace with at lest
10mils spacing at AVSSQ HF cap

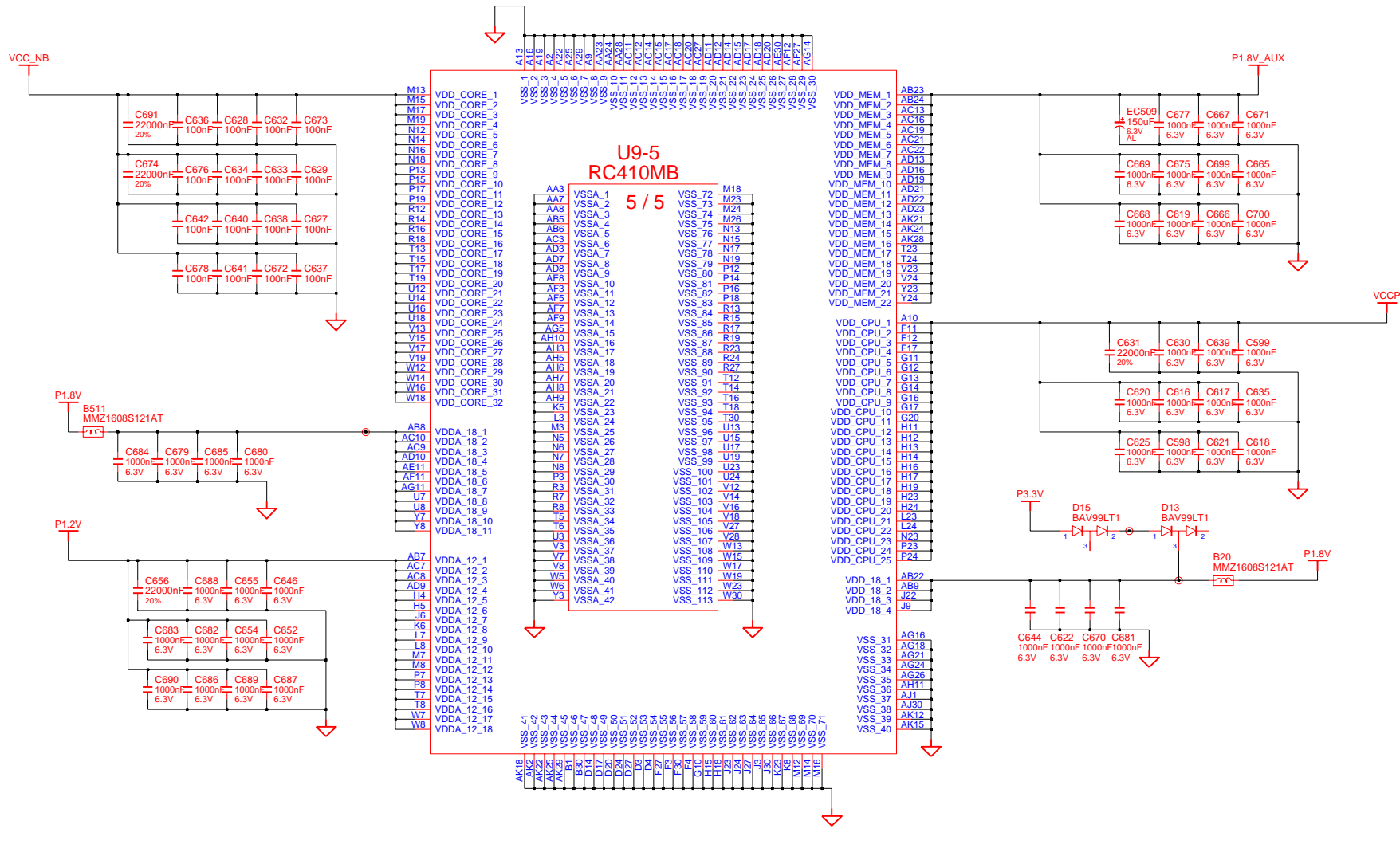
For Debugging



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN RC410MD(4/5)	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT				
				Apr 15, 2006 8:18:08 PM	PAGE 16	OF 52

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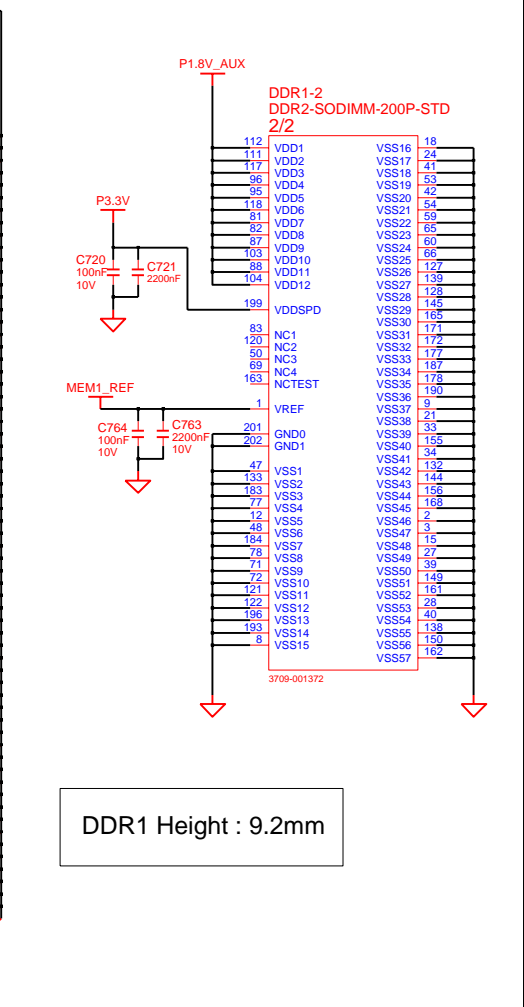
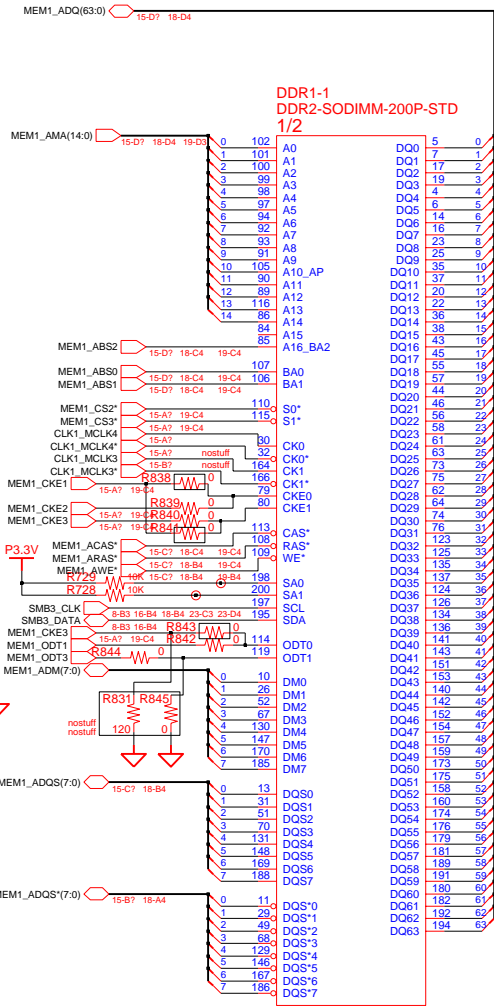
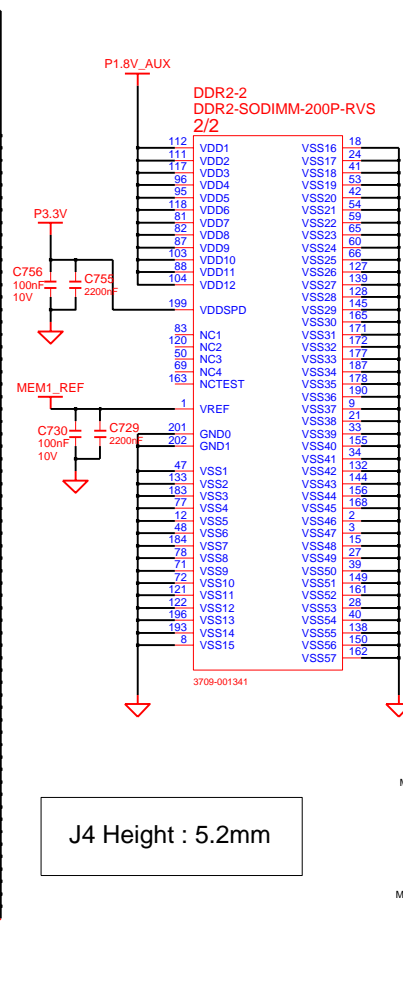
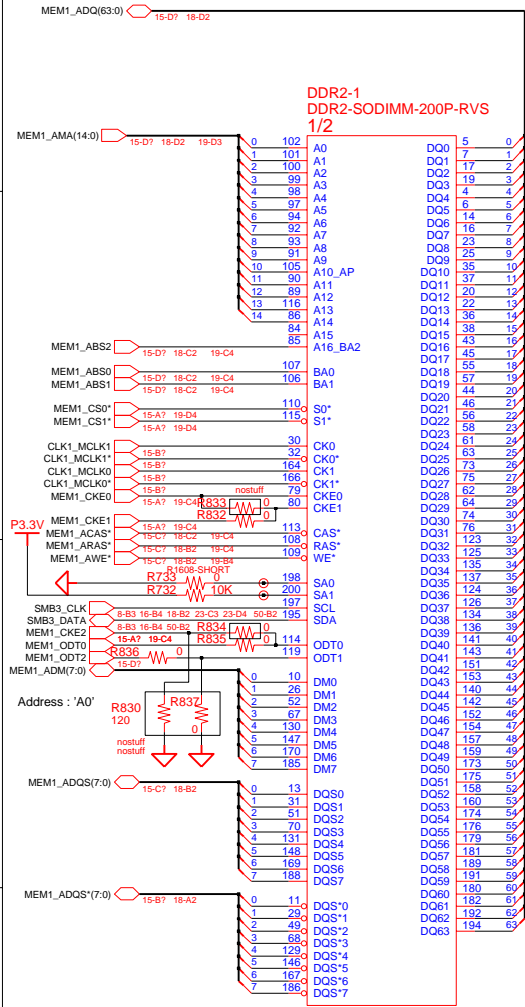
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DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN RC410MD(5/5)	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT				

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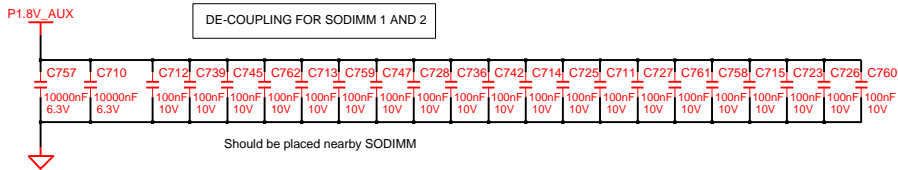
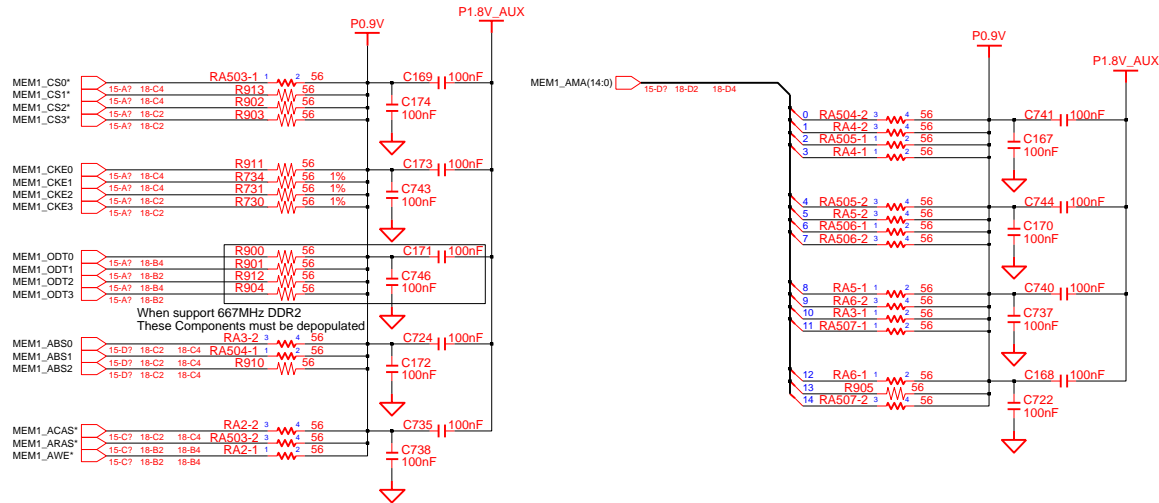
J4 Height : 5.2mm

DDR1 Height : 9.2mm

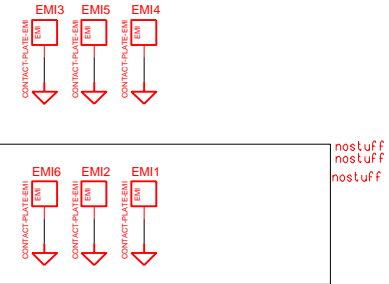
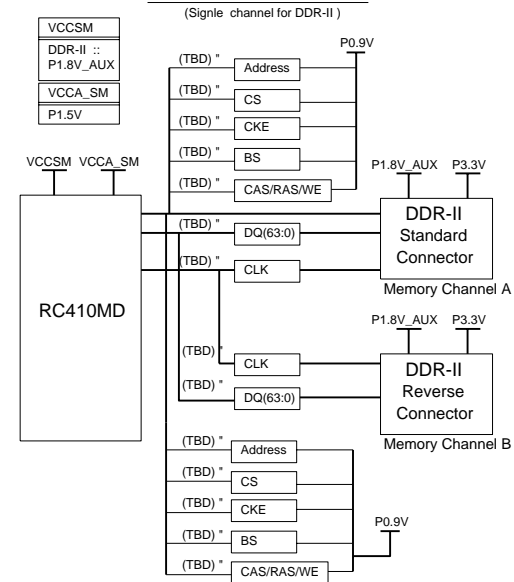
DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR	DDR2 - SODIMM		
APPROVAL	SJ PARK	REV	1.0	PART NO.		BA41-00659A
MODULE CODE		LAST EDIT		Apr 15, 2006 8:18:08 PM		PAGE 18 OF 52

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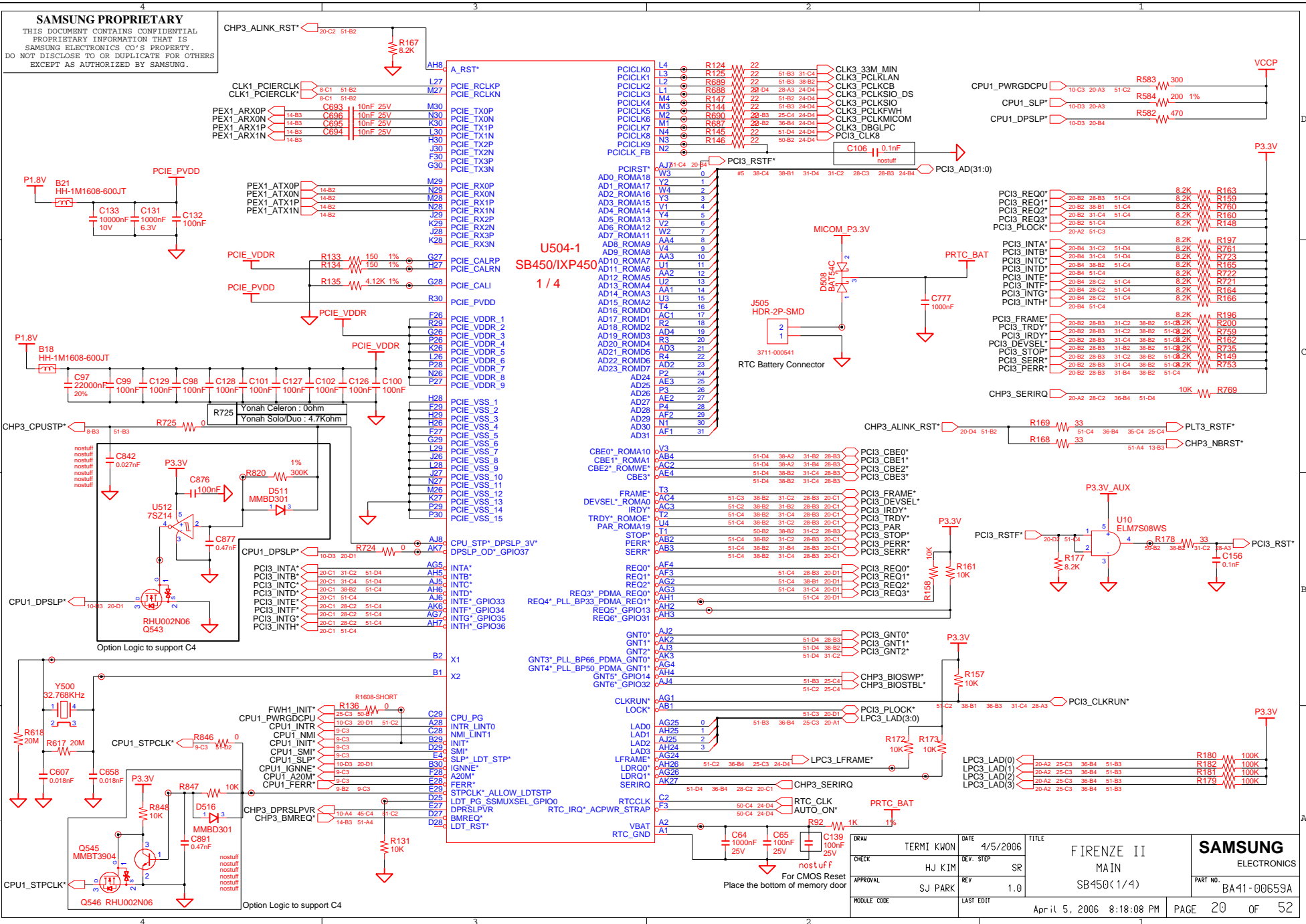
Memory Topology



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR	DDR2 - TERMINATION		
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT				
				Apr 15, 2006 8:18:08 PM	PAGE	19 OF 52

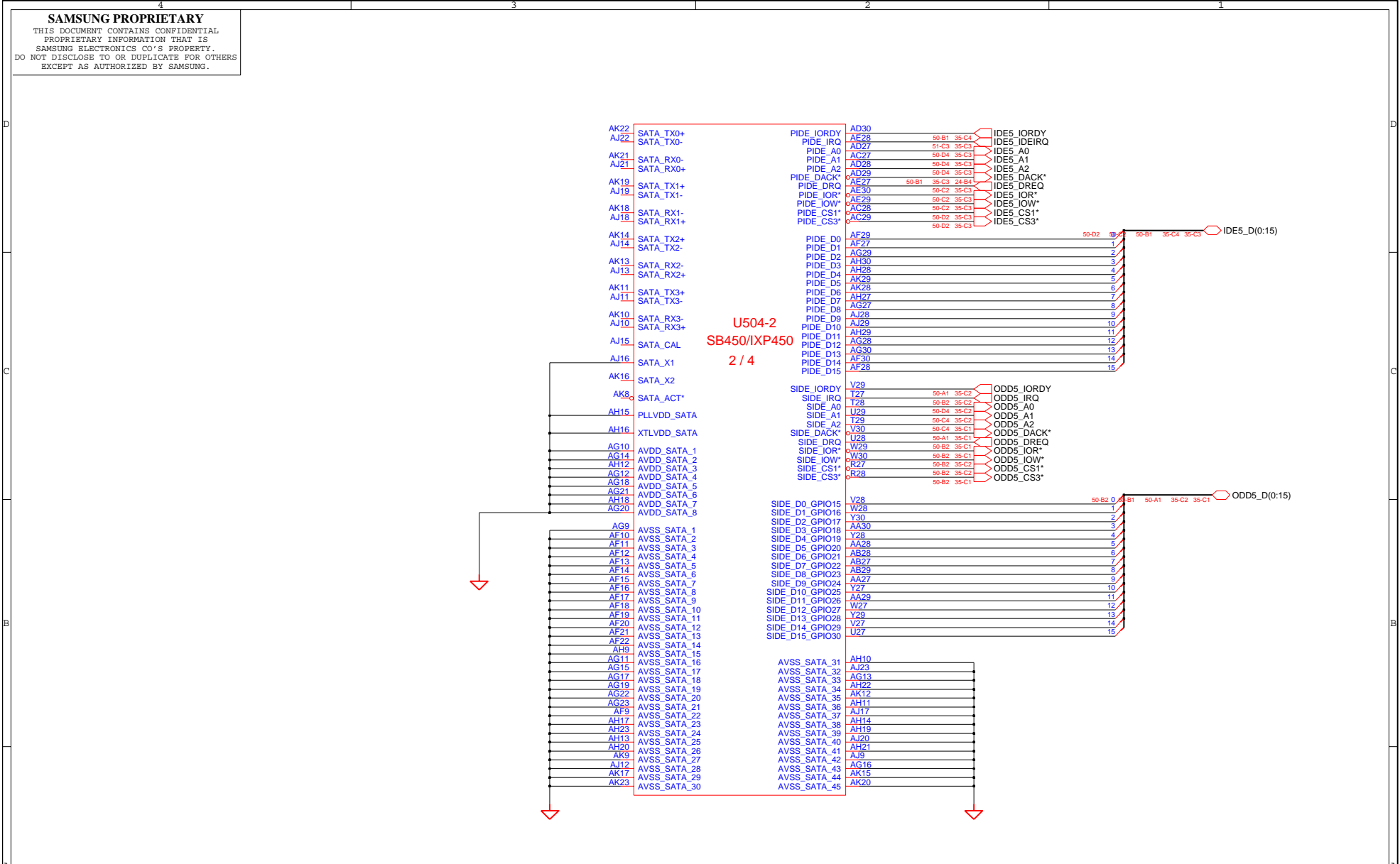
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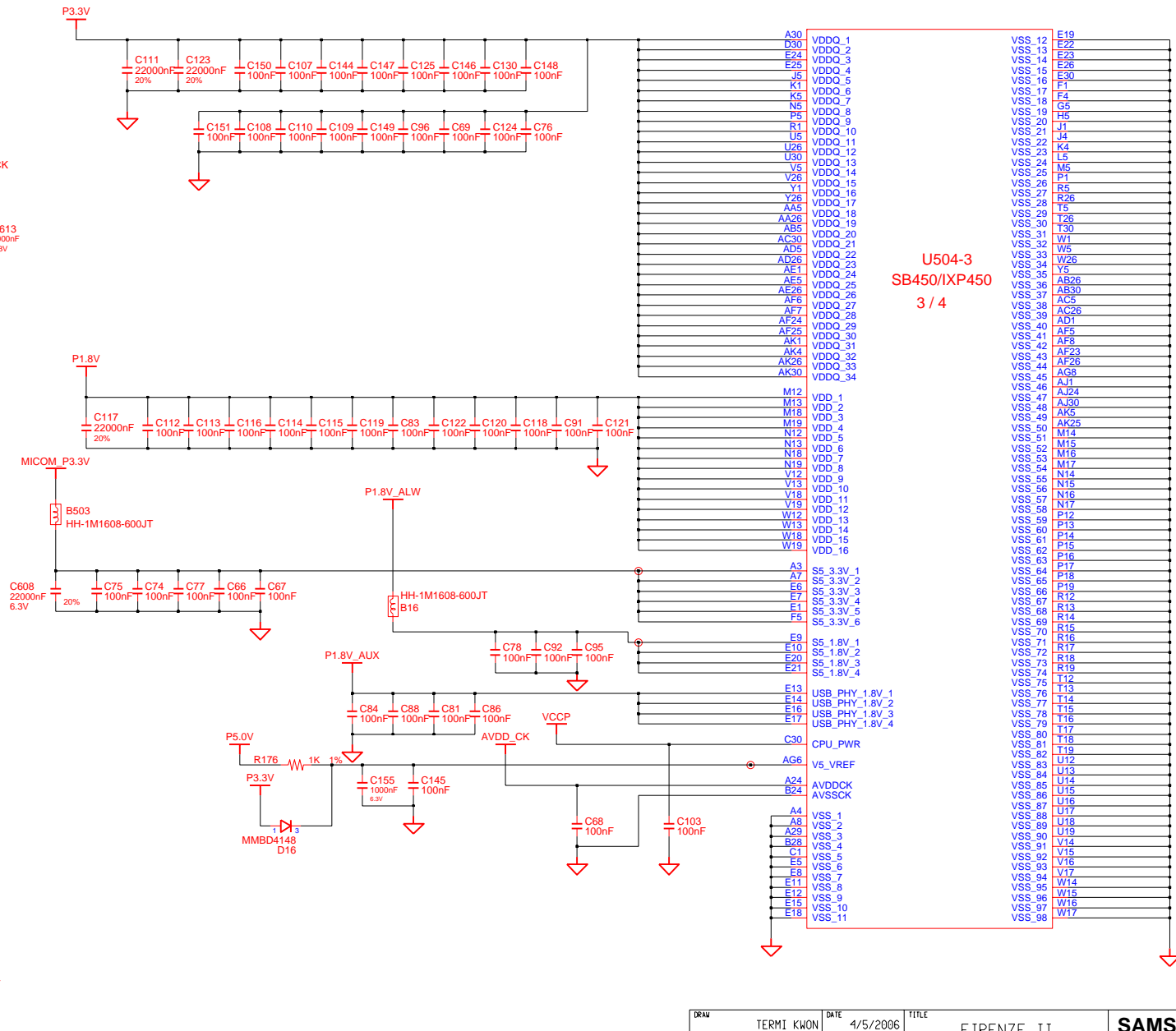


U504-2
SB450/IXP450
2 / 4

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II POWER SB450(2/4)	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT				
				Apr 11 5, 2006 8:18:08 PM	PAGE	21 OF 52

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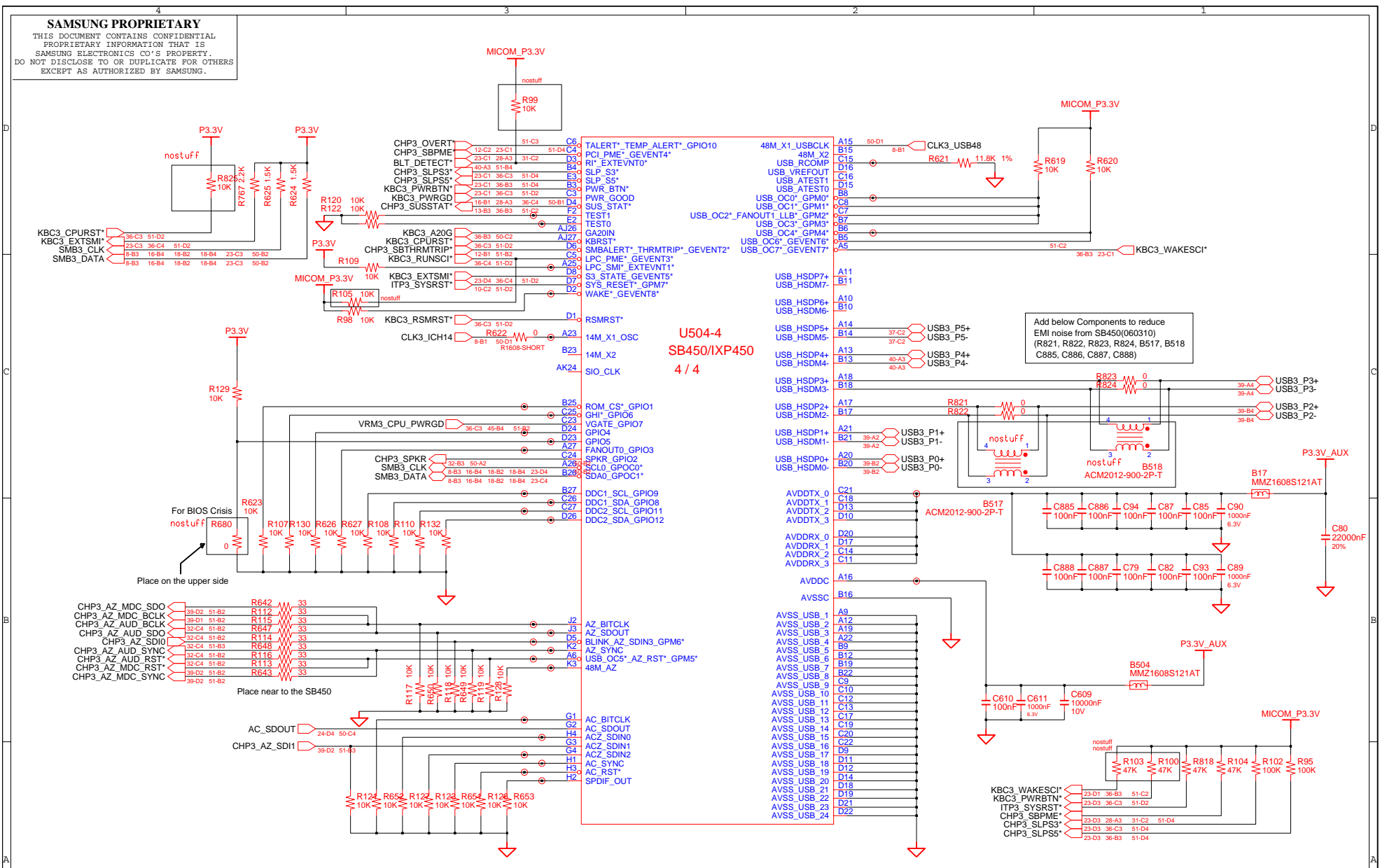


U504-3
SB450/IXP450
3 / 4

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR	MAIN		
APPROVAL	SJ PARK	REV	1.0	SB450(3/4)	PART NO.	BA41-00659A
MODULE CODE		LAST EDIT				

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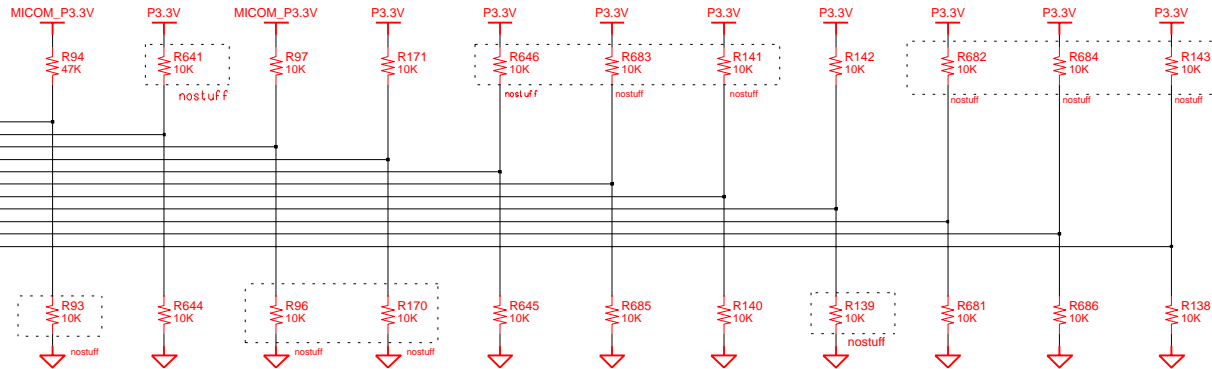
DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN SB450(4/4)	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT				

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REQUIRED SYSTE STRAPS

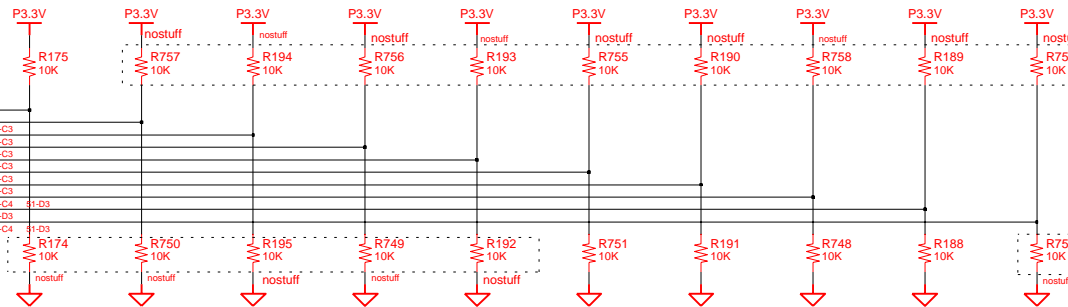
- AUTO_ON* 20-A2 50-C4
- AC_SDOUT 23-B4 50-C4
- RTC_CLK 20-A2 50-C4
- LPC3_LFRAME* 20-A2 25-C3 36-B4 51-C2
- CLK3_PCLKCB 20-D2 28-A3 51-D4
- CLK3_PCLKSIO_DS 20-D2 51-B2
- CLK3_PCLKSIO 20-D2 51-B3
- CLK3_PCLKFWH 20-D2 25-C4 51-B3
- CLK3_PCLKMICOM 20-D2 36-B4 51-B2
- CLK3_DBG LPC 20-D2 51-D4
- PCI3_CLK8 20-D2 50-B2



	AUTO_ON	AC_SDOUT	RTC_CLK	LPC3_FRAME	PCI3_CLK2	PCI3_CLK3	PCI3_CLK4	PCI3_CLK5	PCI3_CLK6	PCI3_CLK7, PCI3_CLK8
STRAP HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	Enable thermtrip* on power up	48MHZ XTAL MODE	USB PHY PWRDOWN DISABLE	USE USB PLL	PCI-E lane auto detect	CPU I/F = KB	ROM TYPE H,H = PCI ROM H,L = LPCROM I LPC ADDRESS MAPPED
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXRERNAL RTC	Disable thermtrip* on power up	48MHZ OSC MODE	USB PHY PWRDOWN ENABLE	BYPASS USB PLL	Force PCI-E to lane2	CPU I/F = P4	BELOW 1 M LPC ADDRESS MAPPED TO TOP-4G L,H = LPC ROM II L,L = FWH ROM

DEBUS STRAPS

- IDE5_DACK* 21-D2 35-C3 50-B1
- PCI3_AD(31) 20-D2 28-C3 31-D4 38-C4 51-C3
- PCI3_AD(30) 20-D2 28-C3 31-D4 38-C4 51-C3
- PCI3_AD(29) 20-D2 28-C3 31-D4 38-C4 51-C3
- PCI3_AD(28) 20-D2 28-C3 31-D4 38-C4 51-C3
- PCI3_AD(27) 20-D2 28-C3 31-D4 38-C4 51-C3
- PCI3_AD(26) 20-D2 28-C3 31-D4 38-C4 51-C3
- PCI3_AD(25) 20-D2 28-C3 31-D4 38-C4 51-C3
- PCI3_AD(24) 20-D2 28-C3 31-D4 38-C4 51-C3
- PCI3_AD(23) 20-D2 28-C3 31-C2 31-D4 38-C4 51-C3

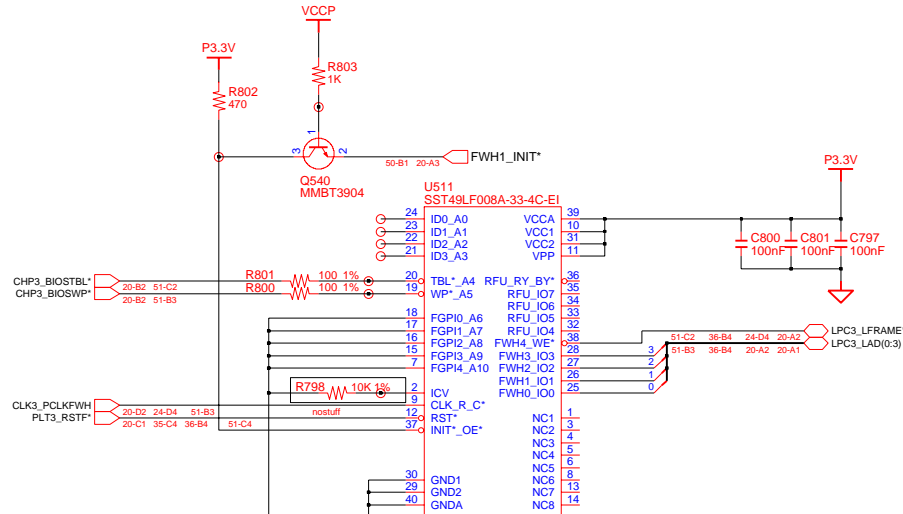


	IDE5_DACK*	PCI3_AD(31)	PCI3_AD(30)	PCI3_AD(29)	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	BYPASS EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR	STRAPS		
APPROVAL	SJ PARK	REV	1.0	April 5, 2006 8:18:08 PM		
MODULE CODE		LAST EDIT		PAGE	24 OF 52	

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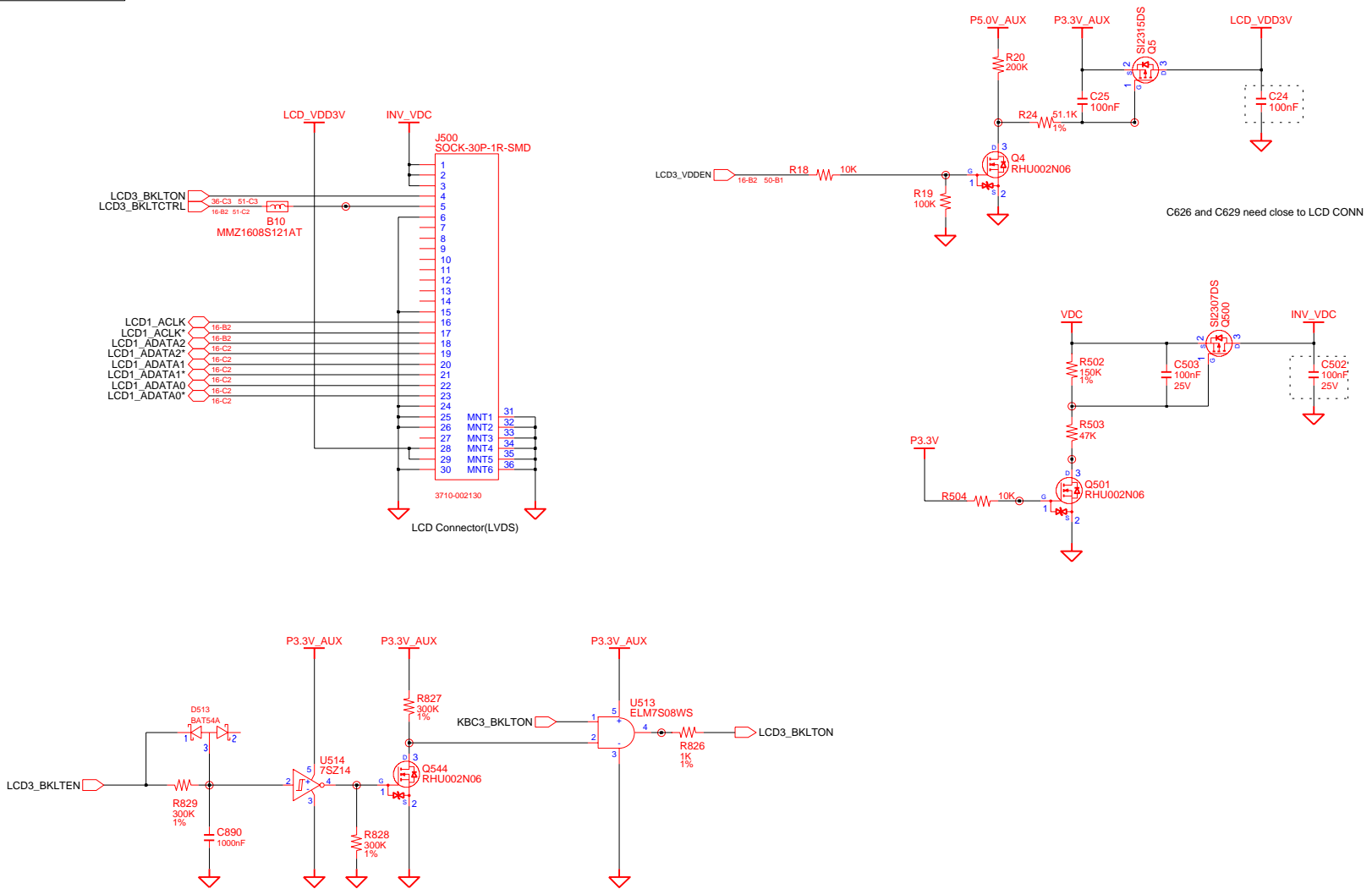


- | | |
|---|------------------------------------|
| 02 VERIFY REAL MODE | 66 CONFIGURE ADVANCE CACHE REG. |
| 03 DISABLE NMI | 6A DISPLAY EXTERNAL CACHE SIZE |
| 04 GET CPU TYPE | 6C DISPLAY SHADOW MESSAGE |
| 06 INIT. SYSTEM H/W | 6E DISPLAY NON-DISPOSABLE SEGMENT |
| 08 INIT. CHIPSET REG. | 70 DISPLAY ERROR MESSAGE |
| 09 SET IN POST FLAG | 72 CHECK FOR CONFIGURATION ERROR |
| 0A INIT CPU.REG | 74 TEST REAL-TIME CLOCK |
| 0B CPU CACHE ON | 76 CHECK FOR KEYBOARD ERROR |
| 0C INIT.CACHE TO POST | 7C SETUP HARDWARE INTERRUPT VECTOR |
| 0E INIT. I/O VALUE | 7E TEST COPROCESSOR IF PRESENT |
| 0F ENABLE THE L-BUS IDE | 80 DISABLE ON-BOARD I/O PORT |
| 10 INIT. POWER MANAGER | 82 DETECT AND INSTALL EXT.RS232C |
| 11 LOAD ALTERNATE REG. | 84 DETECT AND INSTALL EXT.PARALLEL |
| 13 PCI BUS MASTER RESET WITH INITIAL POST VALUE | 86 RE-INIT. ON-BOARD I/O PORT |
| 14 INIT. KEYBOARD CONTROLLER | 88 INIT. BIOS DATA ROM |
| 16 CHECK CHECKSUM | 8A INIT.EXTENDED BIOS DATA AREA |
| 18 8254 TIMER INIT. | 8C INIT. FDD CONTROLLER |
| 1A 8237 DMA CONTROLLER INIT. | 9A SHADOW OPTION ROMS |
| 1C RESET INTERRUPT CONTROLLER | 9C SETUP POWER MANAGEMENT |
| 20 TEST DRAM REFRESH | 9E ENABLE H/W INTERRUPT |
| 22 TEST 8742 KEYBOARD CONTROLLER | A0 SET TIME OF DAY |
| 24 SET ES SEGMENT REG. TO 4GB | A4 INIT. TYPEMATIC RATE |
| 26 ENABLE A20 | A8 ERASE F2 PROMPT |
| 28 AUTO SIZING DRAM | AA SCAN FOR F2 KEY STROKE |
| 32 COMPUTE THE CPU SPEED | AC ENTER SETUP |
| 34 TESET CMOS RAM | AE CLEAR IN POST FLAG |
| 38 SHADOW SYSTEM BIOS ROM | B0 CHECK FOR ERRORS |
| 3A AUTO SIZING CACHE | B2 POST DONE-PREPARE TO BOOT O/S |
| 3C CONFIGURE ADVANCED CHIPSET REG. | B4 ONE BEEP |
| 3D LOAD ALTER REG. WITH CMOS VALUE | B6 CHECK PASSWORD (OPTION) |
| 42 INIT. INTERRUPT VECTOR | B7 ACPI INIT |
| 44 INIT. BIOS INTERRUPT | BA DMI INIT |
| 46 CHECK ROM COPYRIGHT NOTICE | BE CLEAR SCREEN |
| 47 INIT. I20 SUPPORT IF INSTALLED | C0 TRY BOOT WITH INT19 |
| 48 CHECK VIDEO CONFIGURE AGAINST CMOS | D0 INTERRUPT HANDLER ERROR |
| 49 INIT. PCI BUS AND DEVICE | D2 UNKNOWN INTERRUPT ERROR |
| 4A INIT. ALL VIDEO BIOS ROM | D4 PENDING INTERRUPT ERROR |
| 4C SHADOW VIDEO BIOS ROM | D6 SHUTDOWN 5 |
| 50 DISPLAY CPU TYPE AND SPEED | D8 SHUTDOWN ERROR |
| 52 TEST KEYBOARD | DA EXTENDED BLOCK MOVE |
| 54 SET KEYCLICK IF ENABLED | DC SHUTDOWN 10 |
| 56 ENABLE KEYBOARD | 89 ENABLE NMI |
| 58 TEST FOR UNEXPECTED INTERRUPTS | 90 INIT. HDD CONTROLLER |
| 5A DISPLAY * PRESS SETUP* | 91 INIT. LOCAL BUS HDD CONTROLLER |
| 5C TEST RAM BETWEEN 512K AND 640K | 92 JUMP TO USER PATCH 2 |
| 60 TEST EXTENDED MEMORY | 94 DISABLE A20 ADDRESS LINE |
| 62 TEST EXTENDED MEMORY ADDRESS LINE | 96 CLEAR HUGE ES SEGMENT REG. |
| 64 JUMP TO USER PATCH 1 | 98 SEARCH FOR OPTION ROMS |

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR	MAIN		
APPROVAL	SJ PARK	REV	1.0	FIRMWARE HUB		PART NO. BA41-00659A
MODULE CODE		LAST EDIT				

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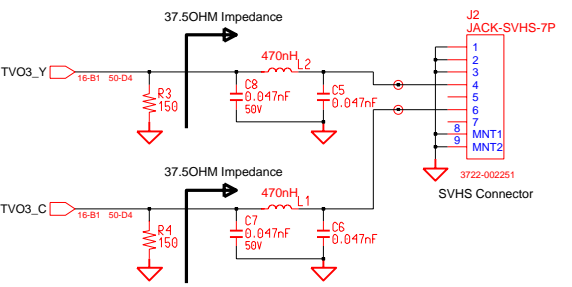
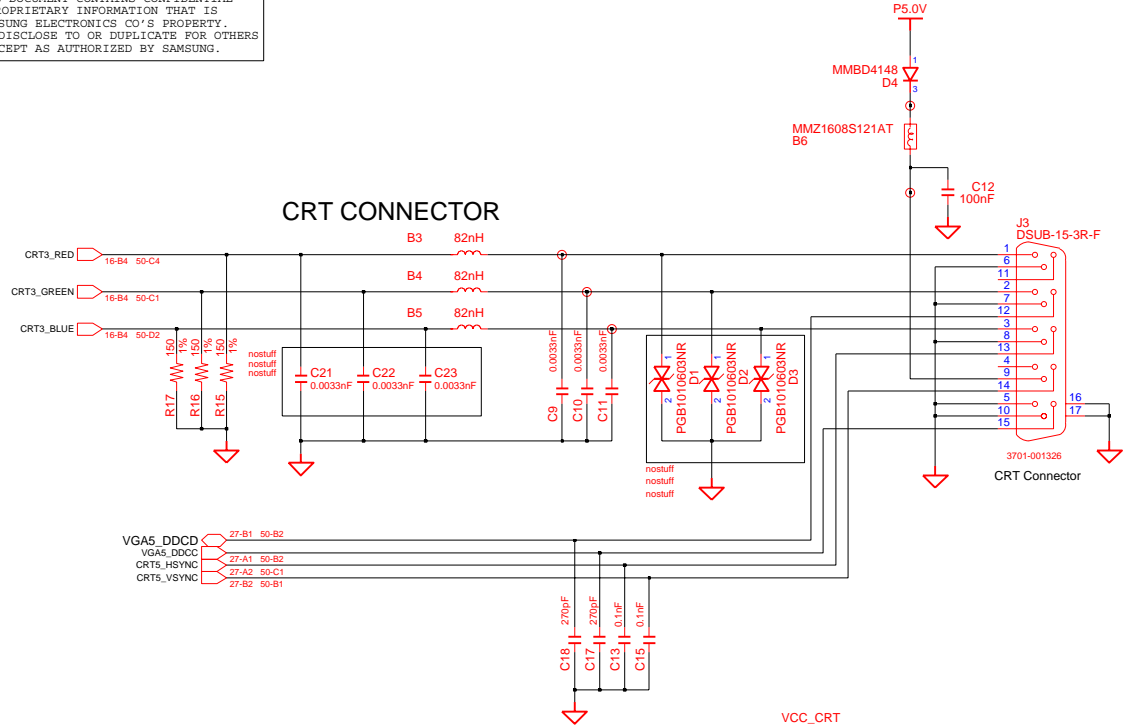
C626 and C629 need close to LCD CONN

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II LCD Connector & SPREAD SPECTRUM	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR	PART NO.		
APPROVAL	SJ PARK	REV	1.0	BA41-00659A		
MODULE CODE		LAST EDIT				

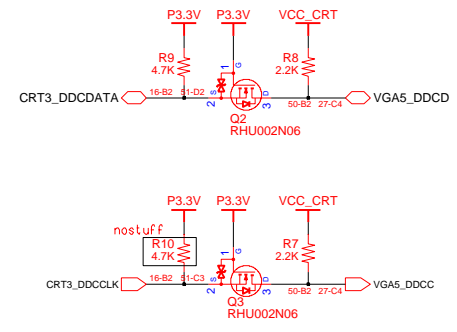
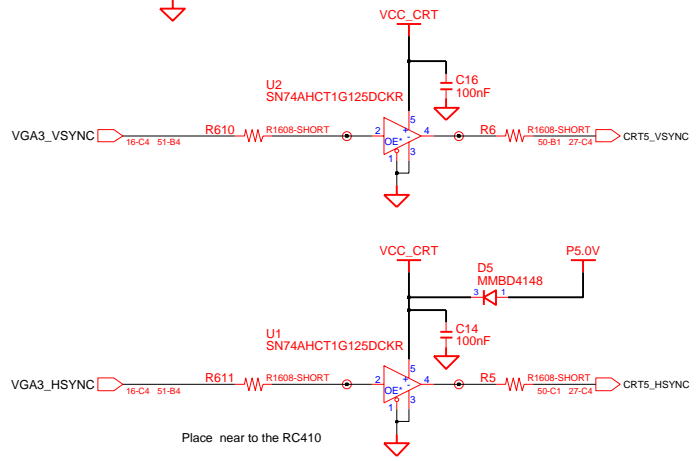
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CRT CONNECTOR



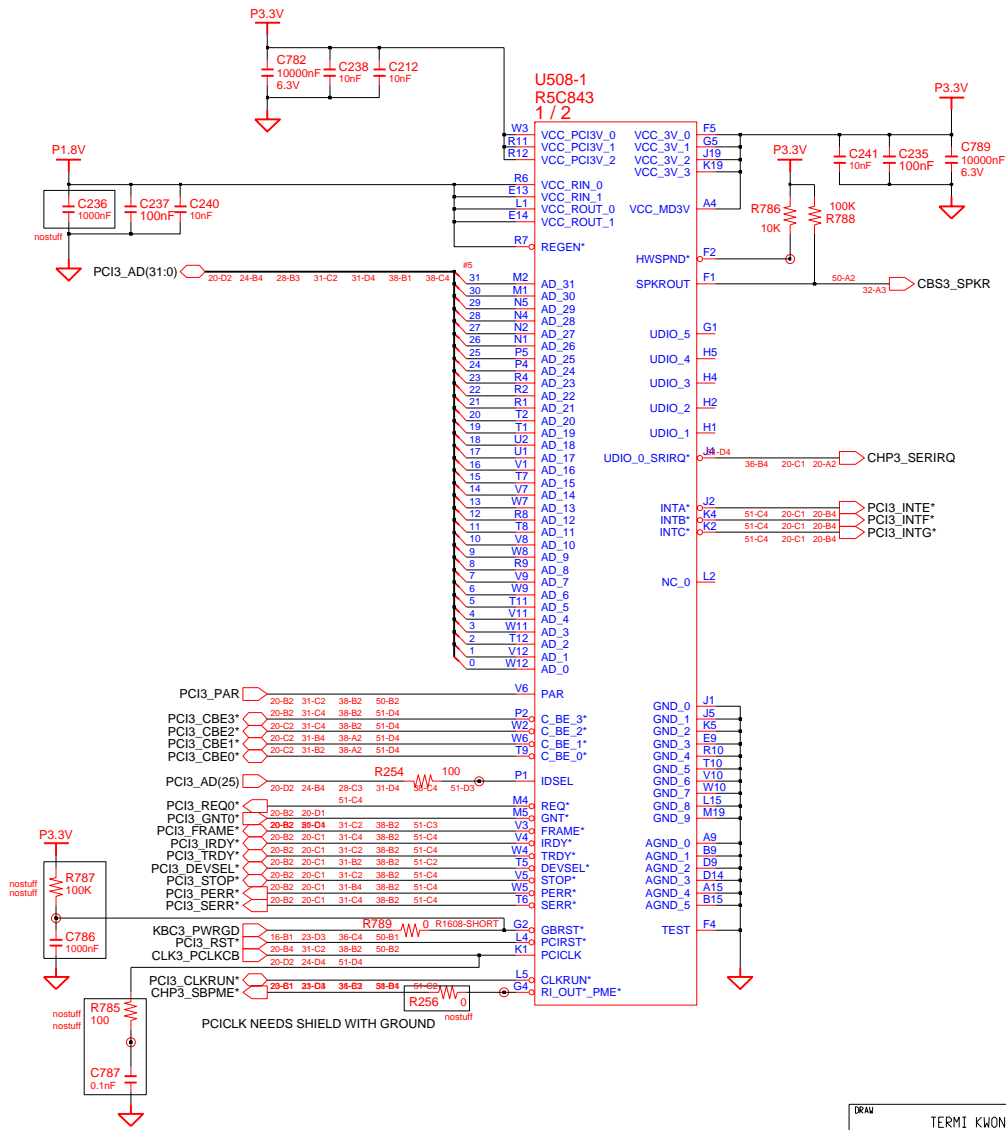
TV-OUT(S-VHS, COMPOSIT)



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0		CRT AND TV-OUT	PART NO. BA41-00659A
MODULE CODE		LAST EDIT				

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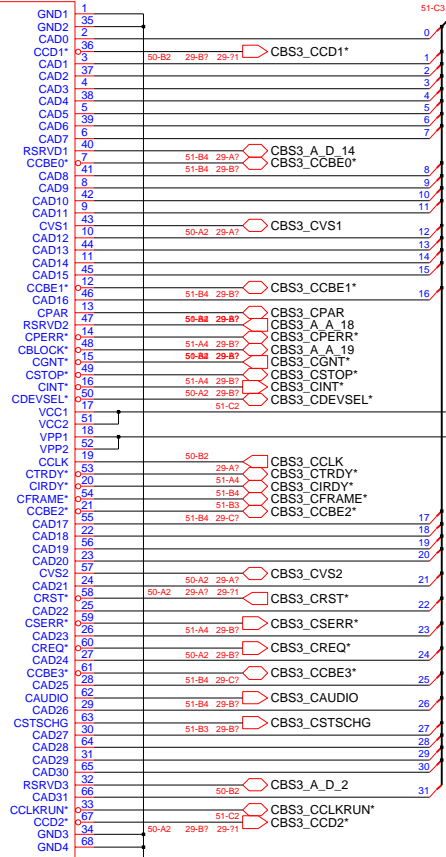


DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0		CARDBUS(1/2)	PART NO. BA41-00659A
MODULE CODE		LAST EDIT		Apr 15, 2006 8:18:08 PM	PAGE	28 OF 52

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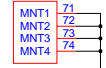
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**J507
PCMCIA-68P-A**



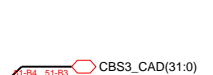
3711-004646

**J506
PCMCIA-68P-MNT**

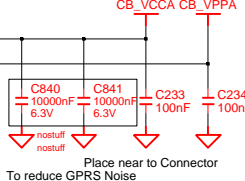


3709-001425

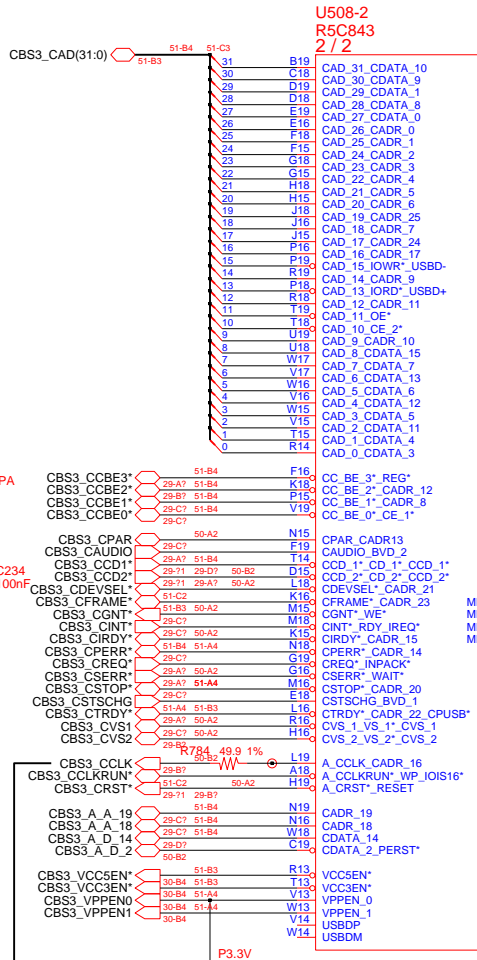
PCMCIA FRAME
PBA Material



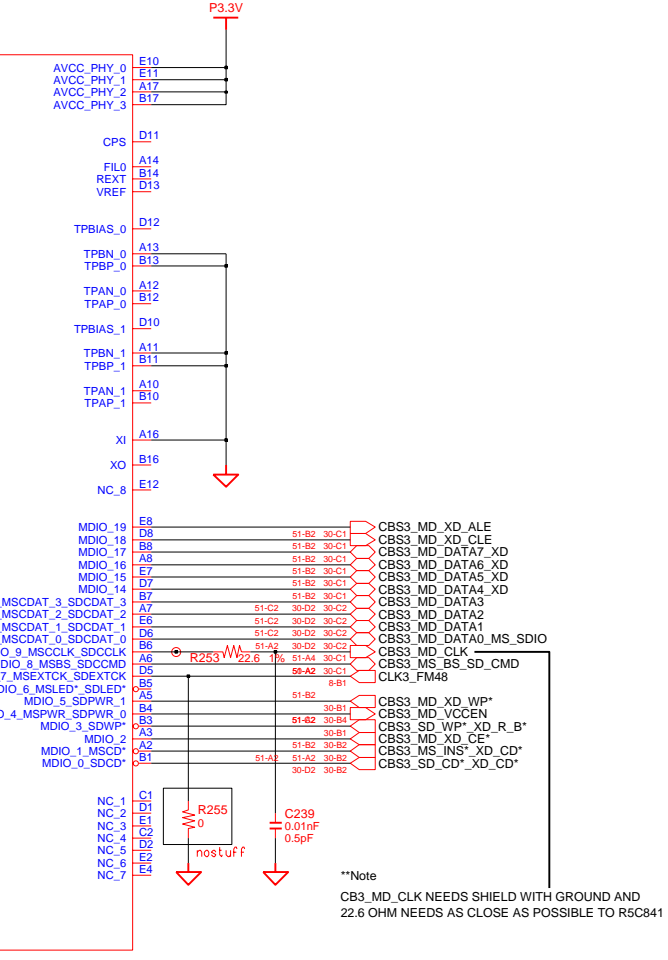
At least 40mil path width
CB_VCCA CB_VPPA



Place near to Connector
To reduce GPRS Noise



**Note
CB3_CLK NEEDS SHIELD WITH GROUND AND 47 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C841



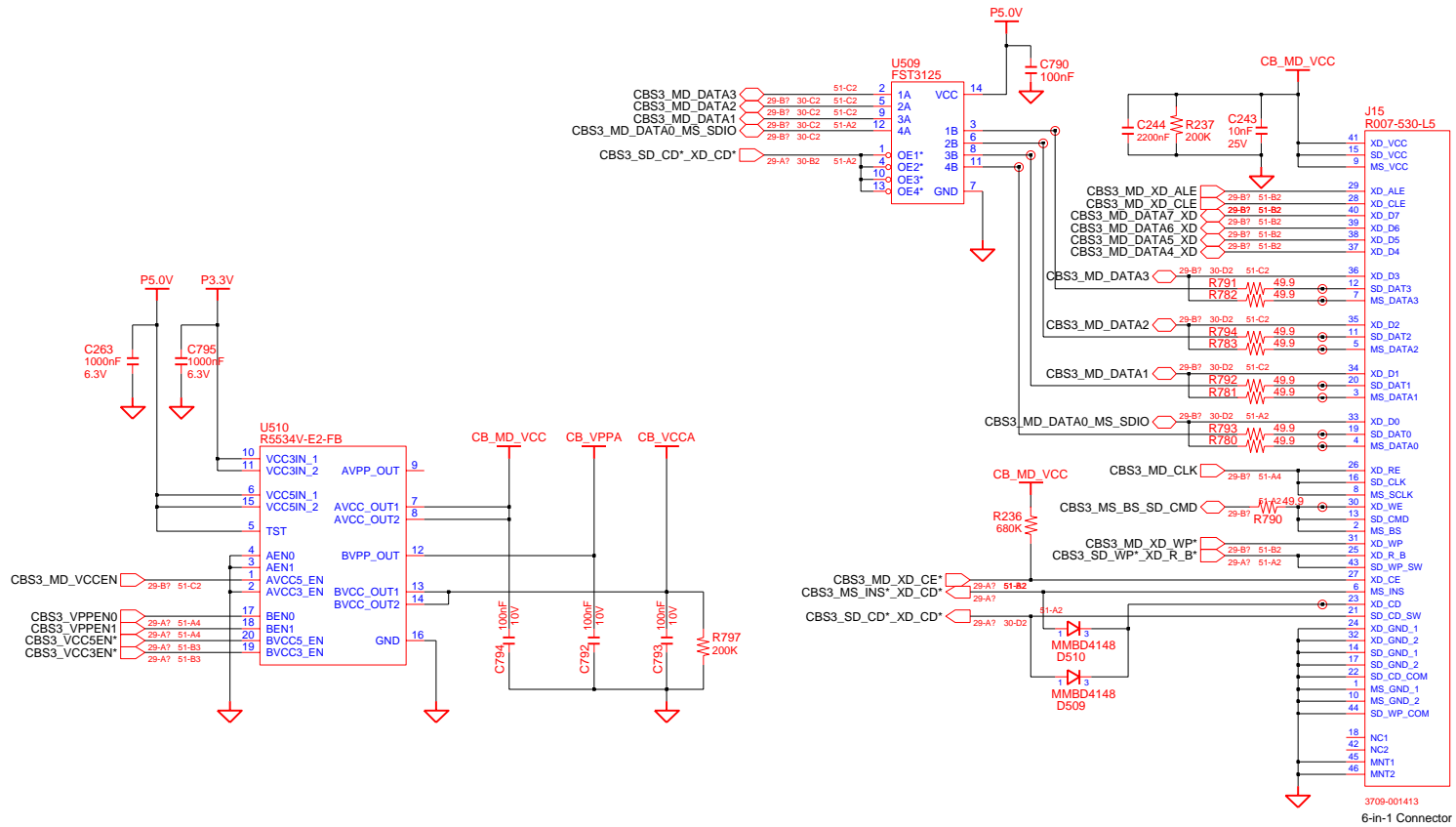
**Note
CB3_MD_CLK NEEDS SHIELD WITH GROUND AND 22.6 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C841



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KTM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT				

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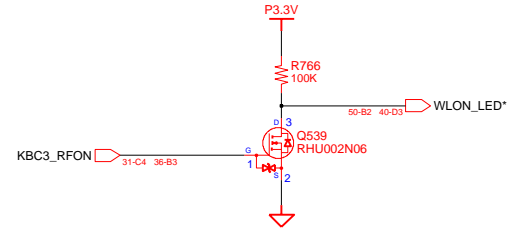
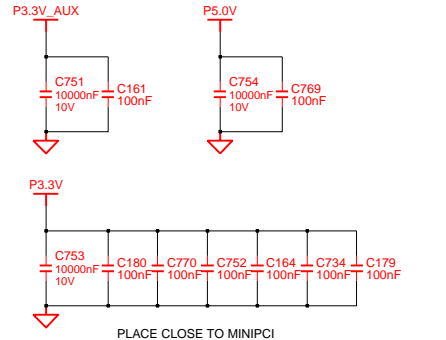
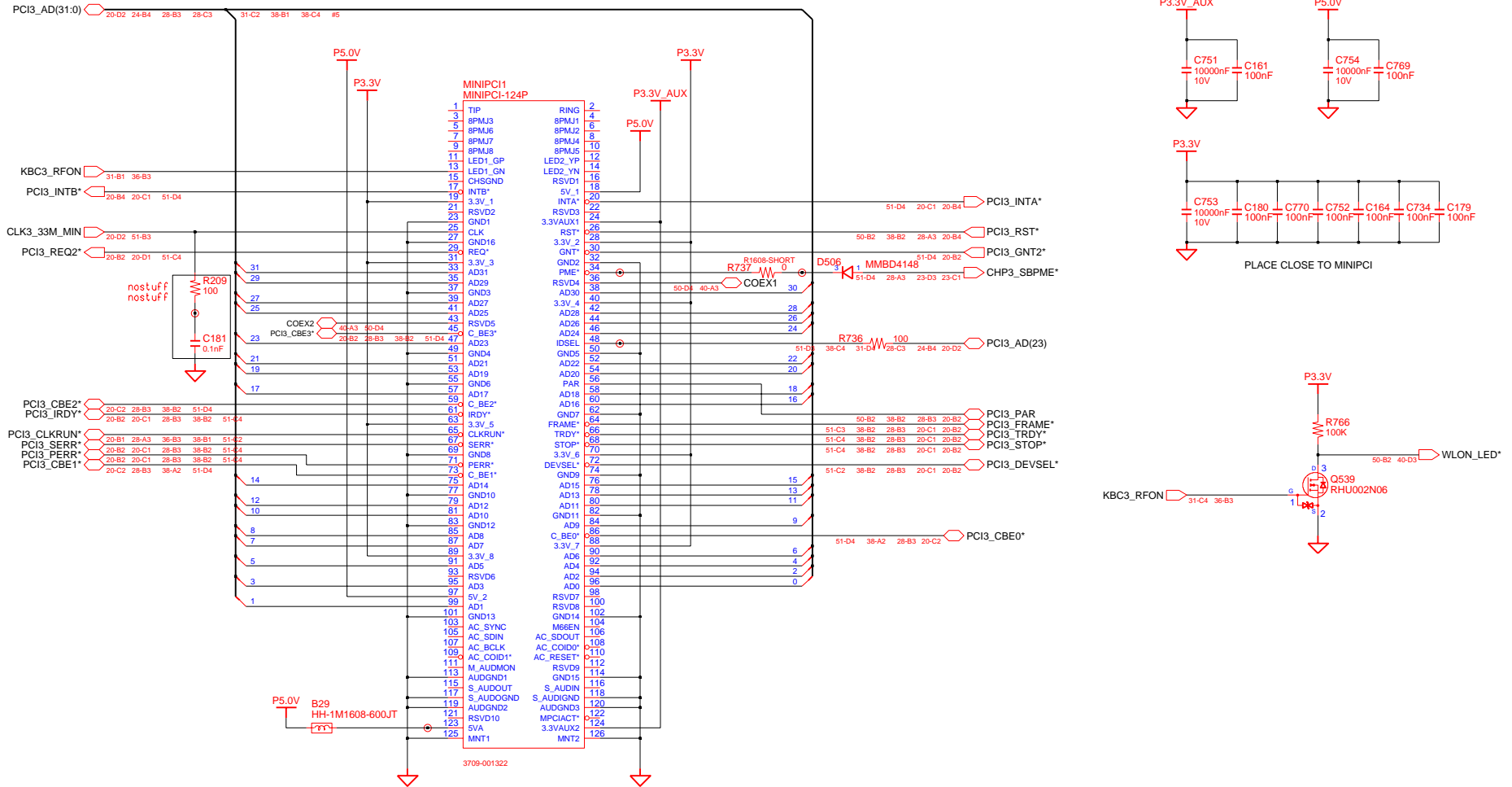


DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR		5 in 1 Socket	
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT				

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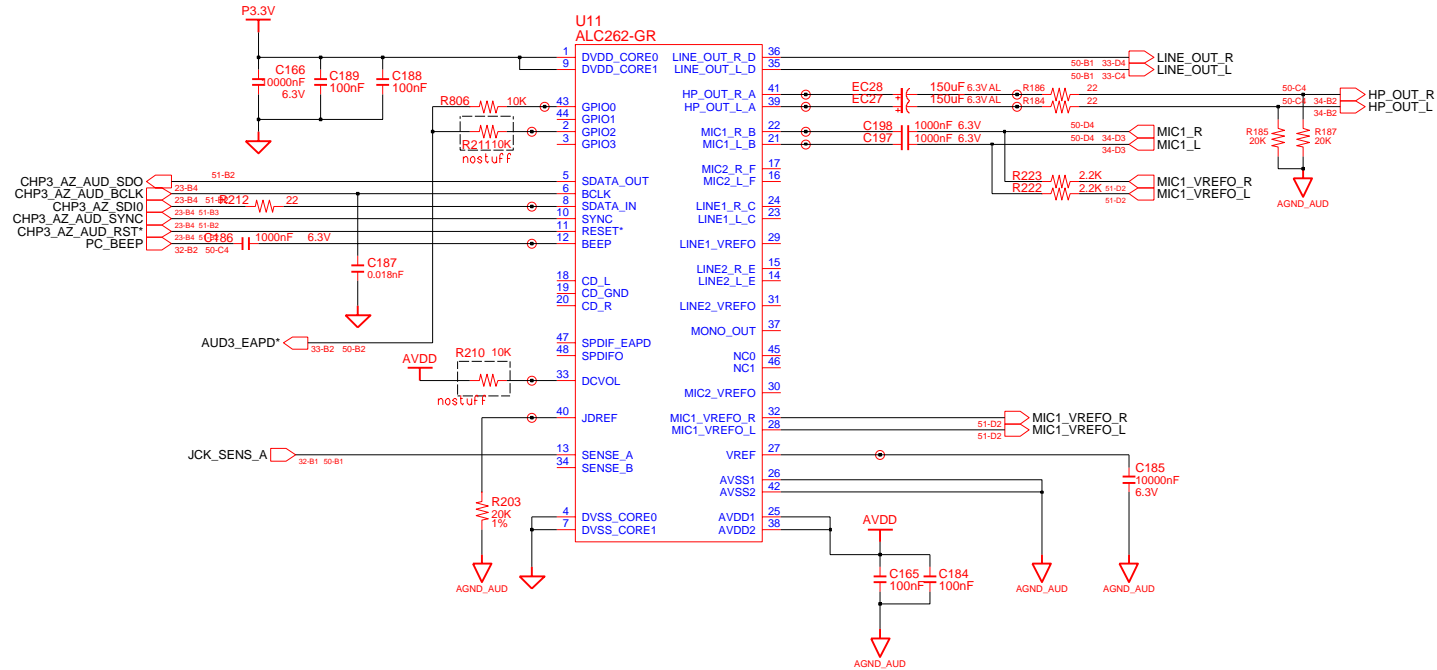
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DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN MINI PCI	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undef ined	LAST EDIT				
				April 5, 2006 8:18:08 PM	PAGE	31 OF 52

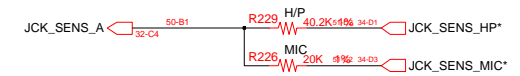
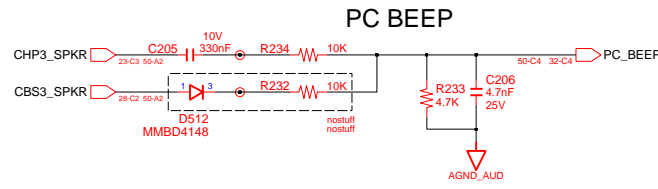
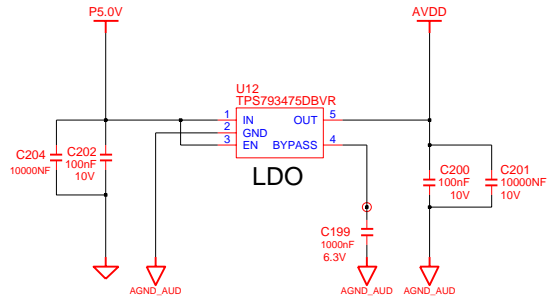
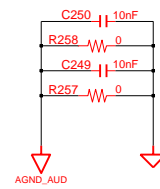
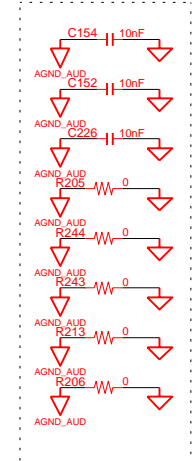
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- 1.AGND_AUD IS AUDIO GROUND
2. GND IS DIGITAL GROUND
- 3.AGND_MIC IS MIC GROUND
- 4.AGND_CHS IS CHASS GROUND

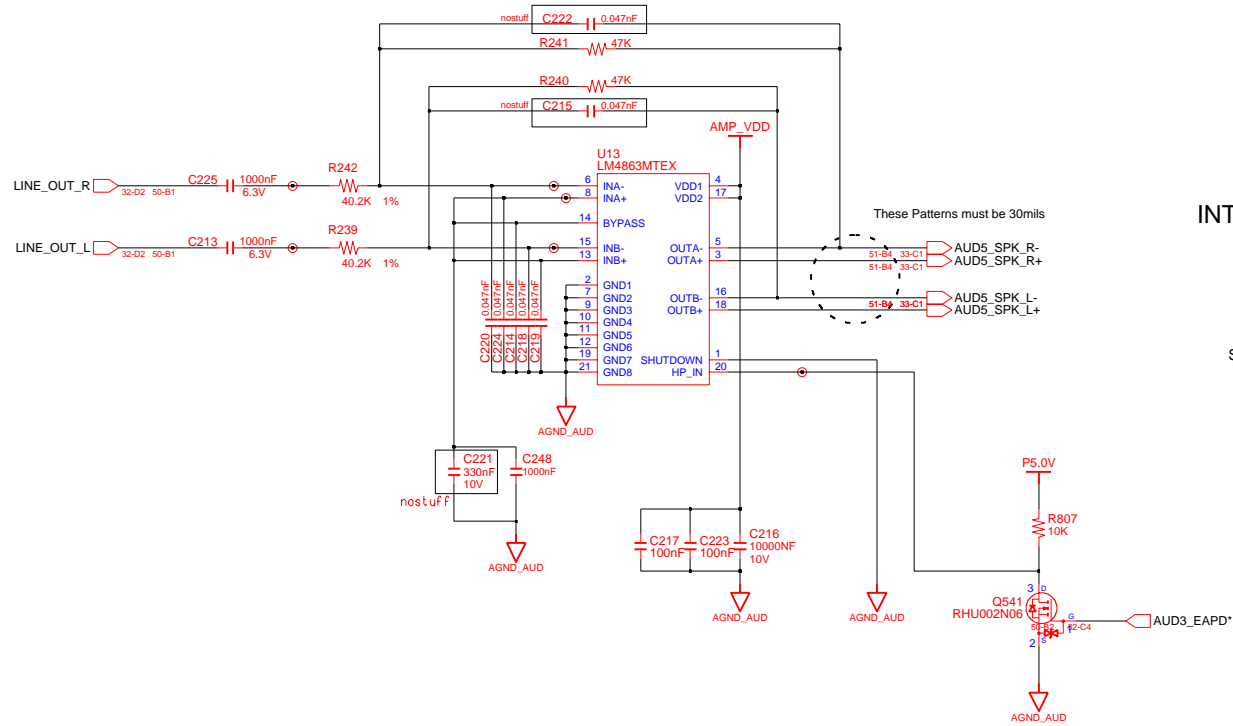
ALL TYPE IS 1608



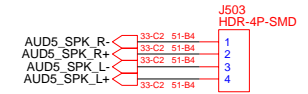
DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN AUDIO CODEC	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undef ined	LAST EDIT				
				Apr il 5, 2006 8:18:08 PM	PAGE	32 OF 52

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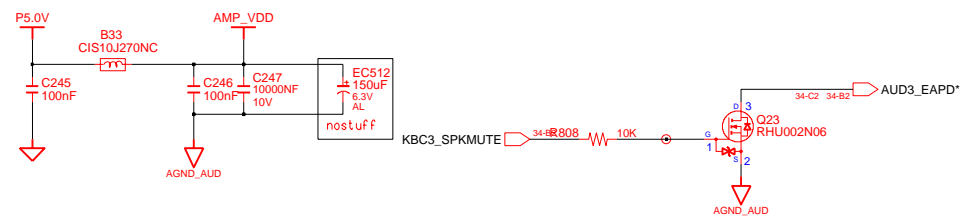


INTERNAL STEREO SPEAKERS



Should be written sign "L", "R" on the PCB

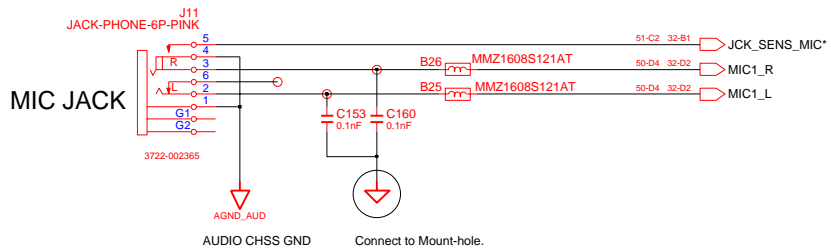
AMP_VDD



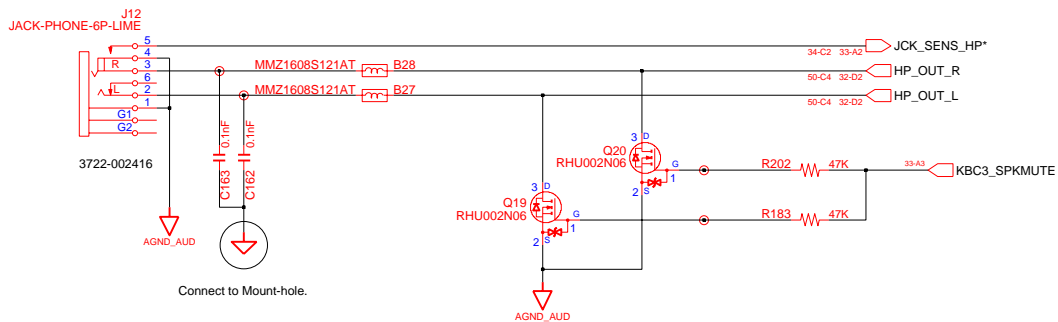
DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN LIMITER & AMP	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT				
				Apr 15, 2006 8:18:08 PM	PAGE 33 OF 52	

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HEADPHONE

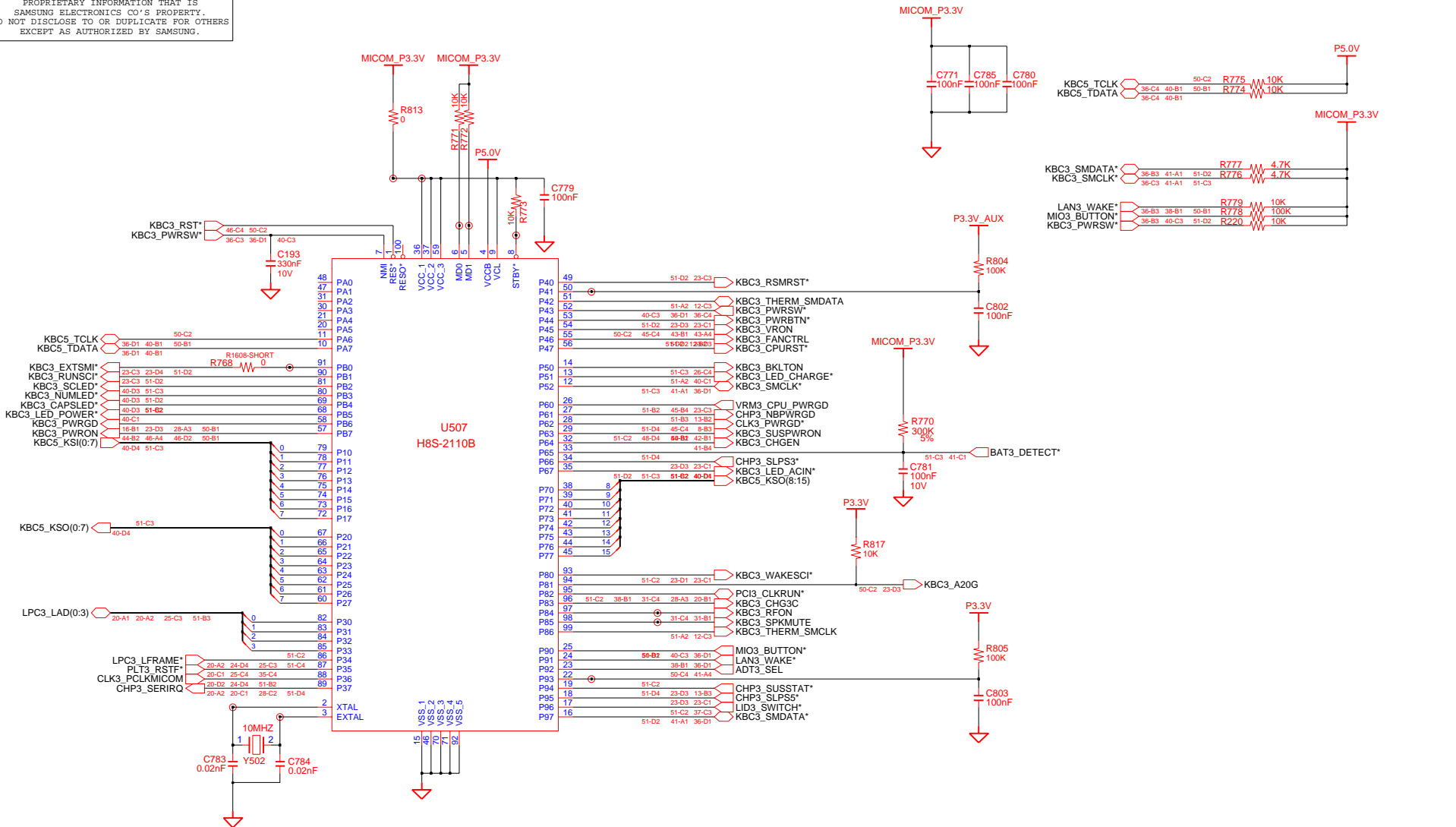


The traces led to Audio Jacks have the width over 10mil

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN UPPER & AUDIO CONN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00659A
MODULE CODE	undefined	LAST EDIT		April 5, 2006 8:18:08 PM	PAGE	34 OF 52

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MICOM Crisis Update
 Condition: P90=P91=P92=High(MICOM_P3V)
 MD0=MD1=Low(0V)
 Serial Port: P84 & P85

The removed signal compared from 144pin

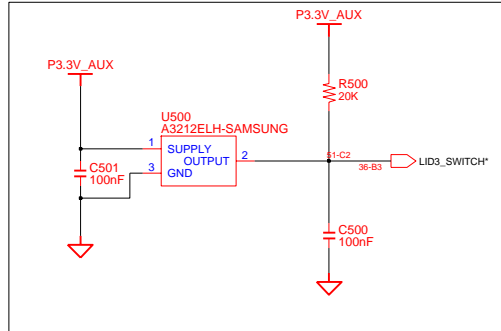
- KBC5_CAL_THRM*
- THRM_ALERT*
- LCD3_BKLTEN
- FAN3_FDBACK*
- THERM_STP*

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II POWER MICOM	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undef ined	LAST EDIT		April 5, 2006 8:18:08 PM	PAGE	36 OF 52

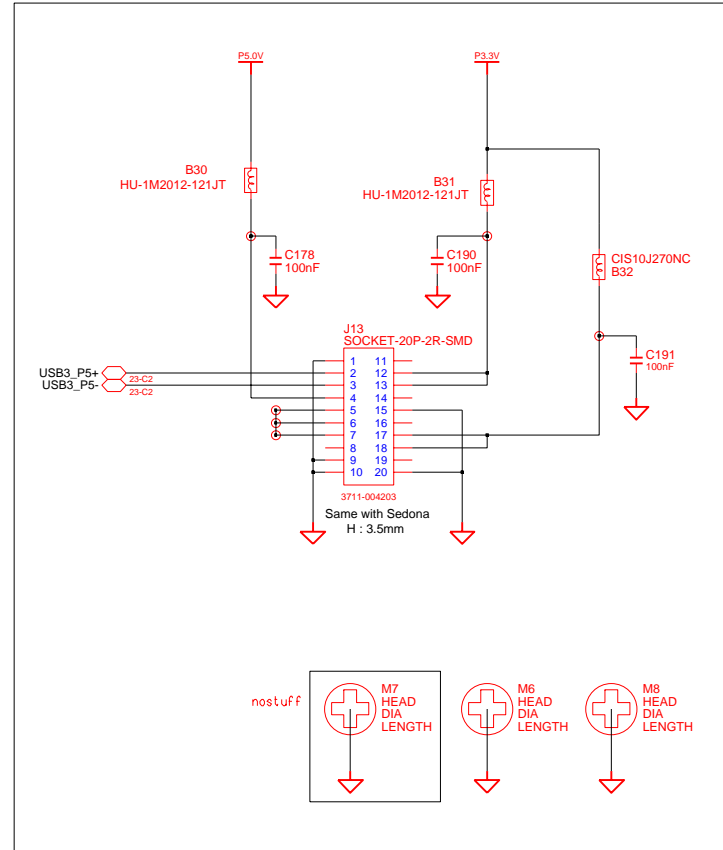
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LID SWITCH



**DMB
Factory Option**

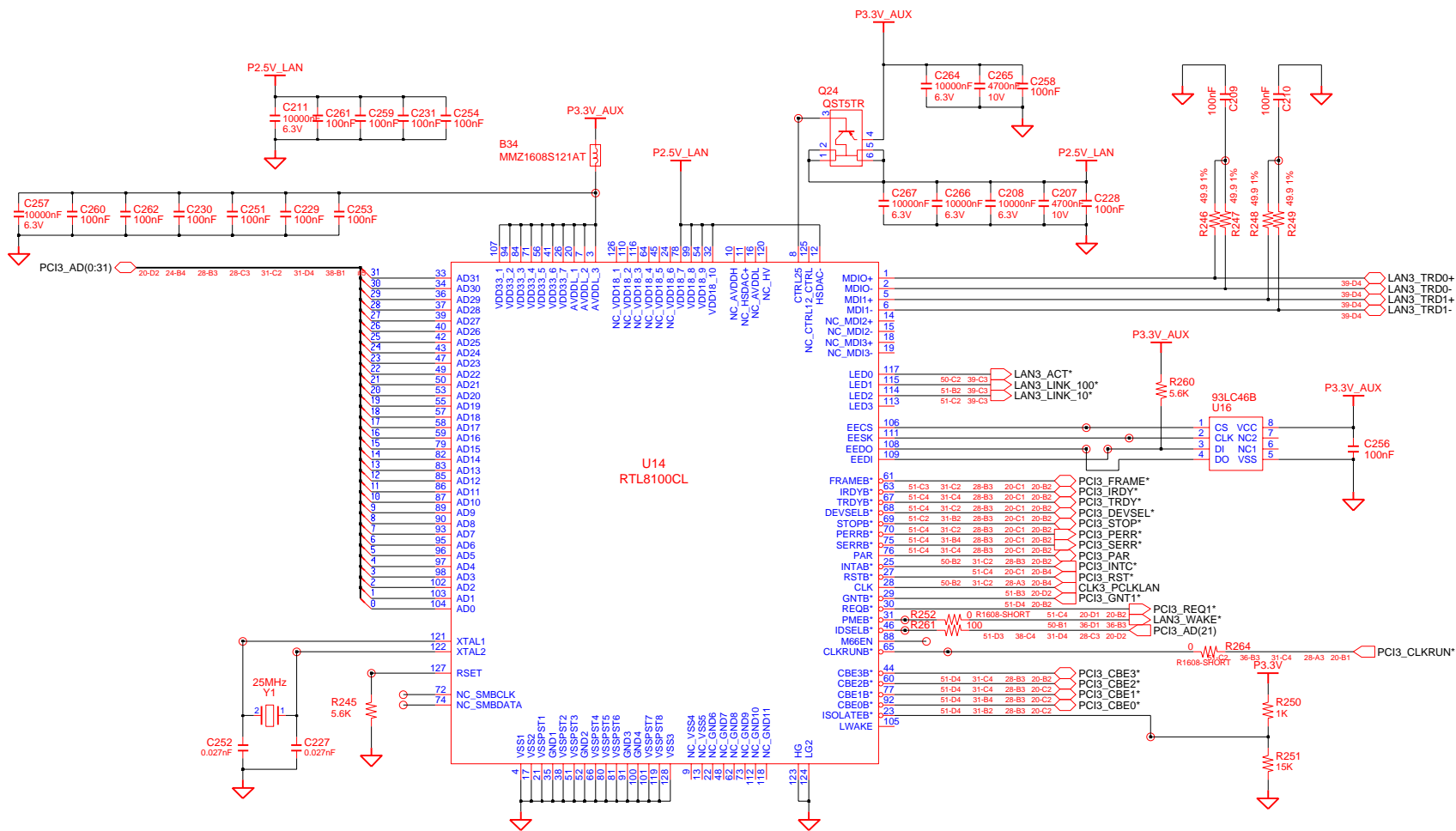


DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR		MAIN	
APPROVAL	SJ PARK	REV	1.0		LPC	PART NO. BA41-00659A
MODULE CODE	undef ined	LAST EDIT		April 5, 2006 8:18:08 PM	PAGE	37 OF 52

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LAN Controller (Only 10/100M)

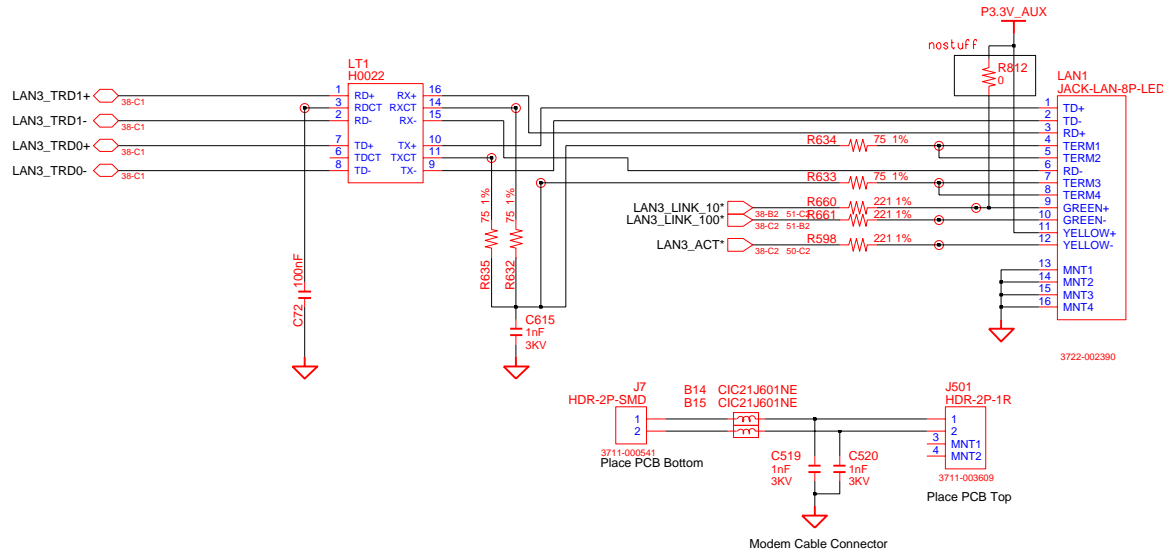


DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR	MAIN	LAN	
APPROVAL	SJ PARK	REV	1.0	PART NO.		BA41-00659A
MODULE CODE	undef ined	LAST EDIT	April 5, 2006 8:18:08 PM	PAGE	38	OF 52

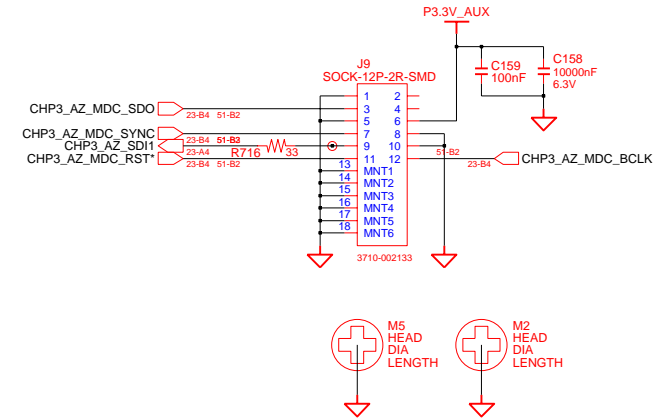
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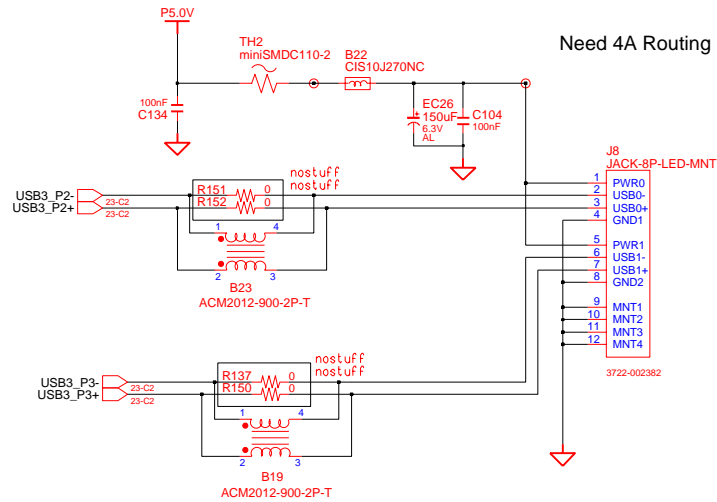
LAN Connector



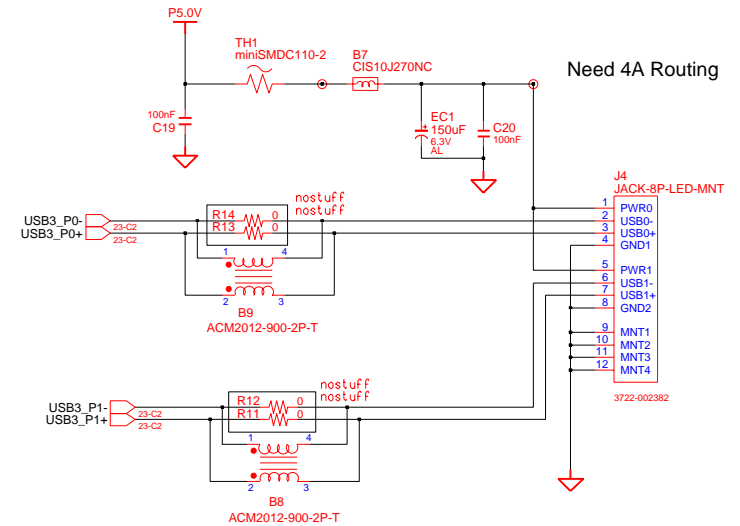
MDC Connector



Need 4A Routing



Need 4A Routing



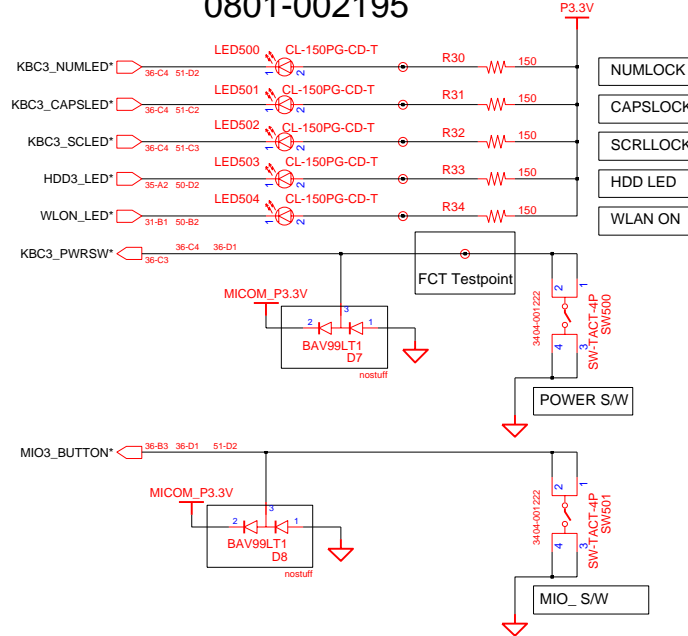
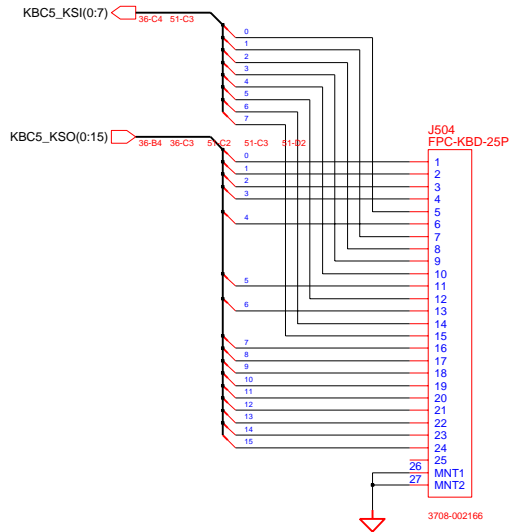
DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR	MAIN		
APPROVAL	SJ PARK	REV	1.0	LAN & USB0 & MODEM Conn.	PART NO.	BA41-00659A
MODULE CODE	undef ined	LAST EDIT		Apr il 5, 2006 8:18:08 PM	PAGE	39 OF 52

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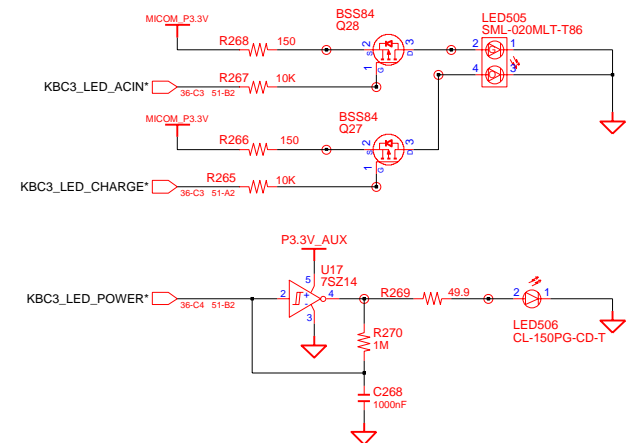
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LED 0801-002195

KEYBOARD Same connector with Sedona

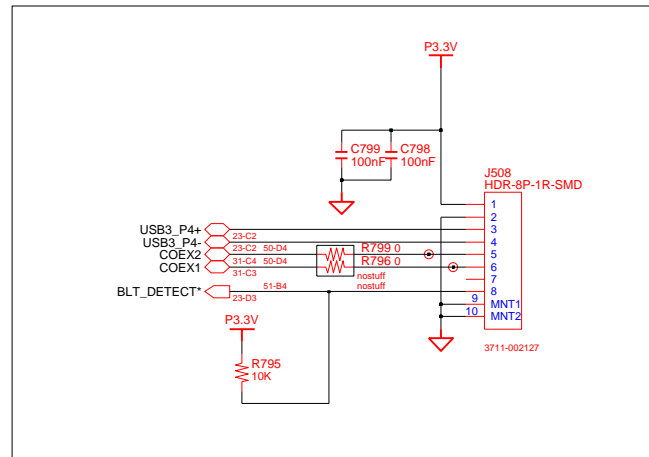
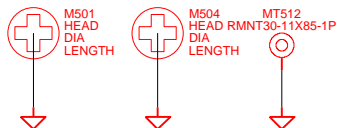


ADAPTER/CHARGING LED

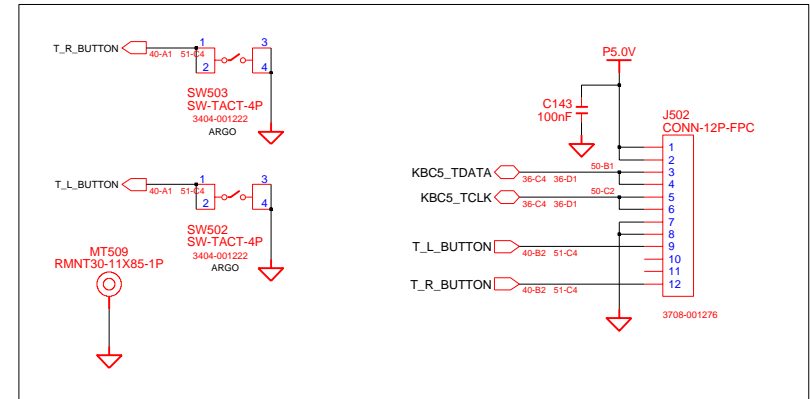


Bluetooth Interface

Factory Option



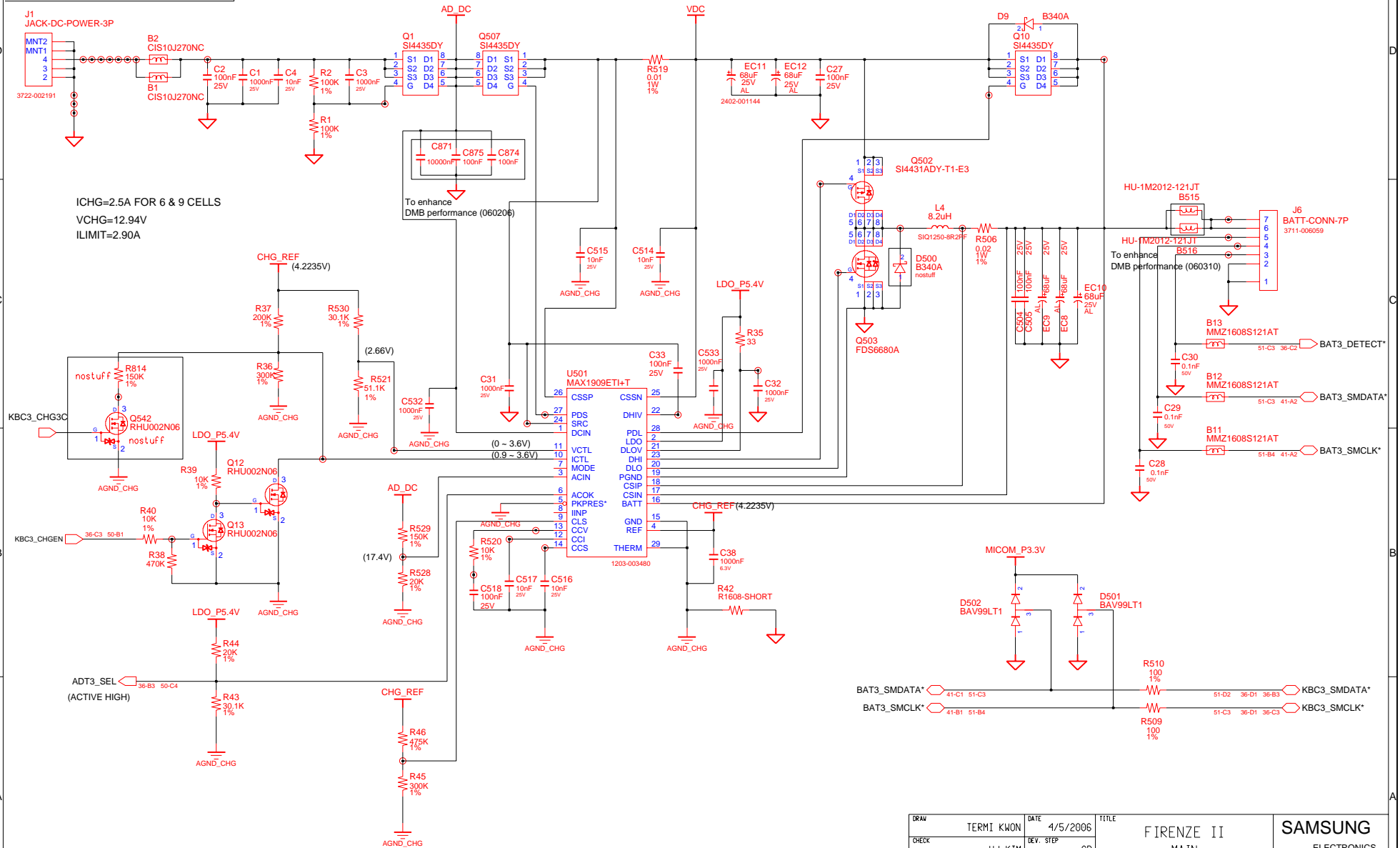
TOUCHPAD



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR		MAIN	
APPROVAL	SJ PARK	REV	1.0		B'D TO B'D CONNECTOR	PART NO. BA41-00659A
MODULE CODE	undef ined	LAST EDIT				PAGE 40 OF 52

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CHARGER & POWER MANAGEMENT

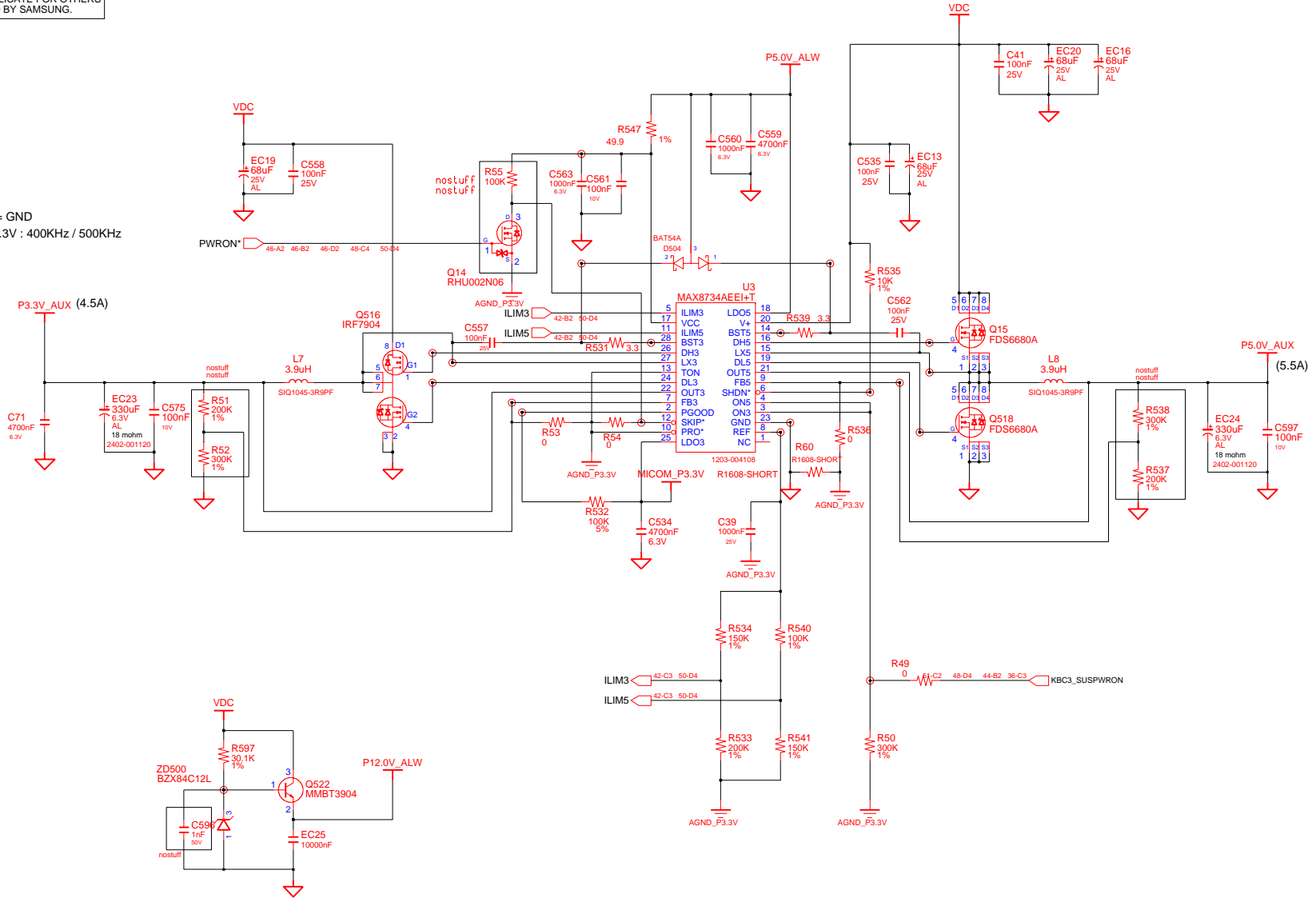


DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN CHARGER	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR	REV	1.0	
APPROVAL	SJ PARK	REV	1.0	LAST EDIT		
MODULE CODE	undef ined	DATE	April 5, 2006 8:18:08 PM	PAGE	41 OF 52	

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P3.3V_AUX & P5.0V_AUX

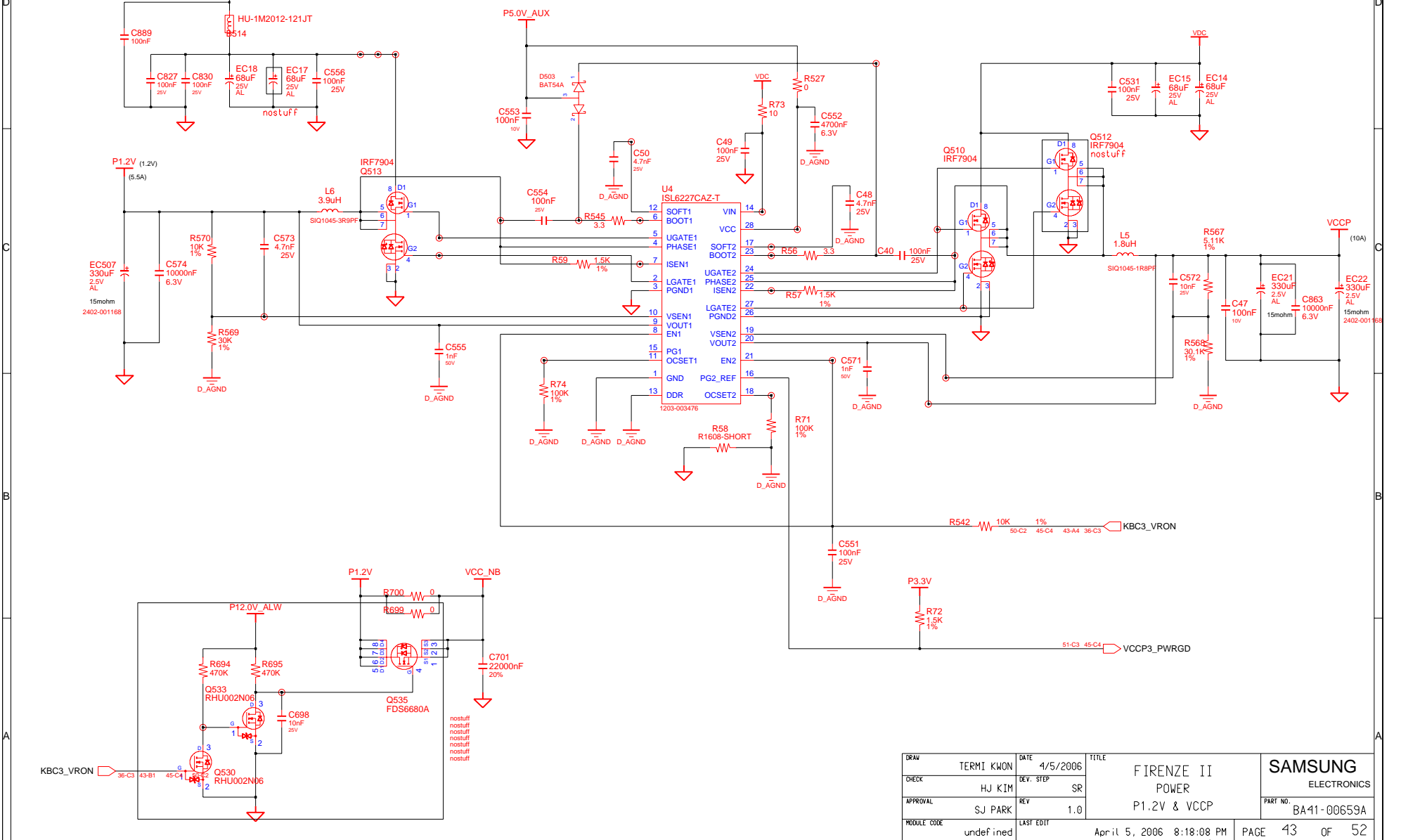
V_{ton} = GND
 5V / 3.3V : 400KHz / 500KHz



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II POWER	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR	P3.3V ALWAYS & P5V-AUX		
APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00659A
MODULE CODE	undef ined	LAST EDIT	Apr il 5, 2006 8:18:08 PM	PAGE	42	OF 52

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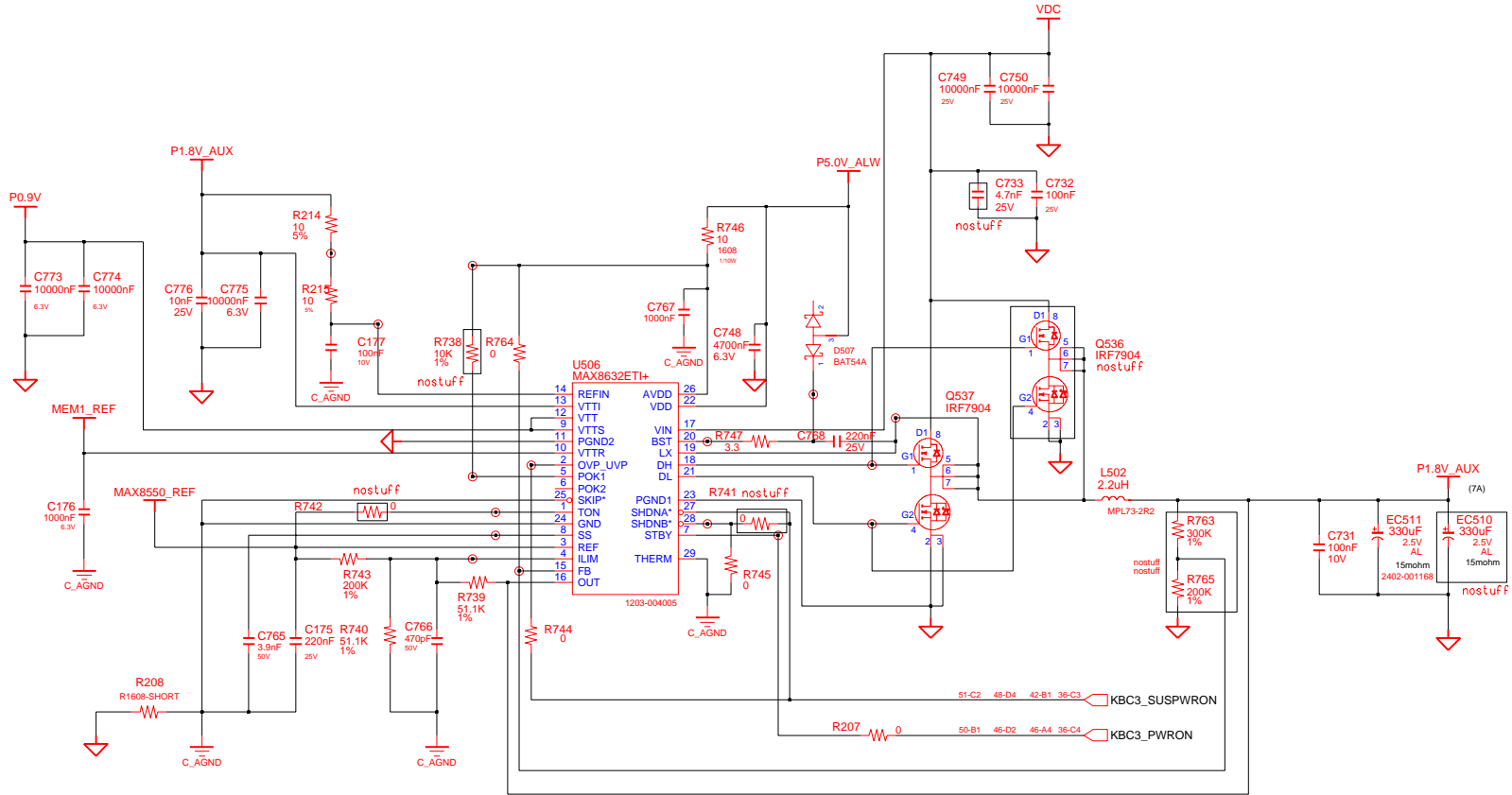
P1.2V(VCC_NB) & VCCP (1.05V)



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II POWER	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR	P1.2V & VCCP		
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undef ined	LAST EDIT		April 5, 2006 8:18:08 PM	PAGE	43 OF 52

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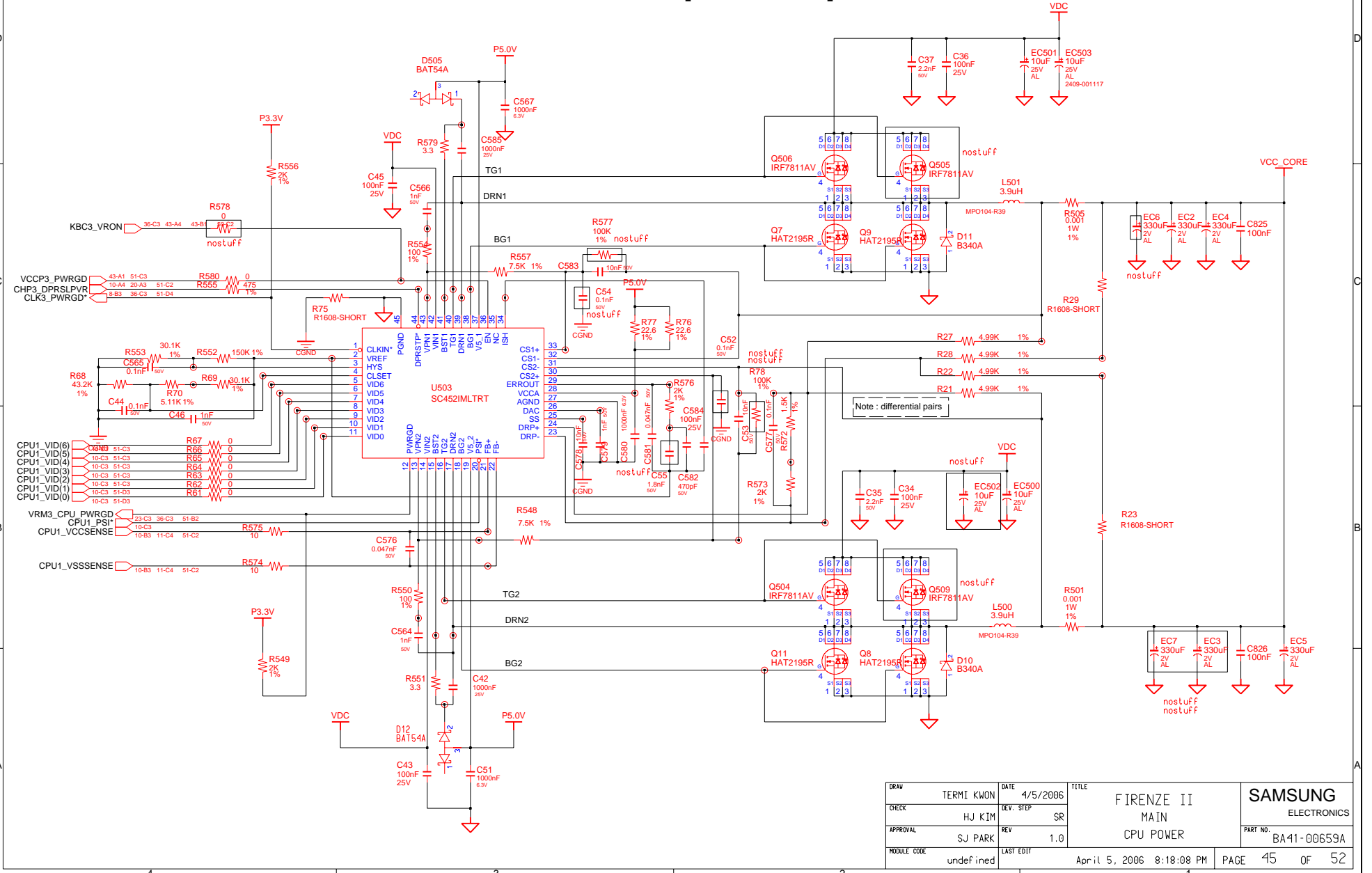
DDR2 Power



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN DDR POWER	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00659A
MODULE CODE	undef ined	LAST EDIT		April 5, 2006 8:18:08 PM	PAGE	44 OF 52

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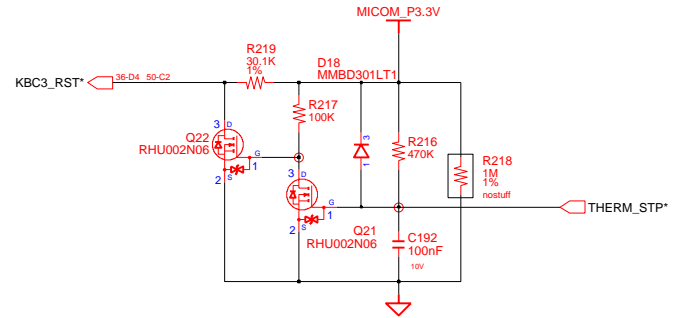
CPU VRM [SEMTECH]



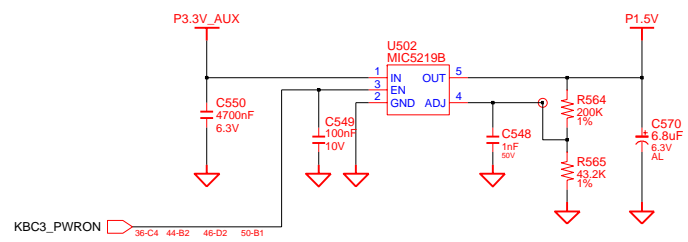
DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN CPU POWER	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undef ined	LAST EDIT				
				April 5, 2006 8:18:08 PM	PAGE	45 OF 52

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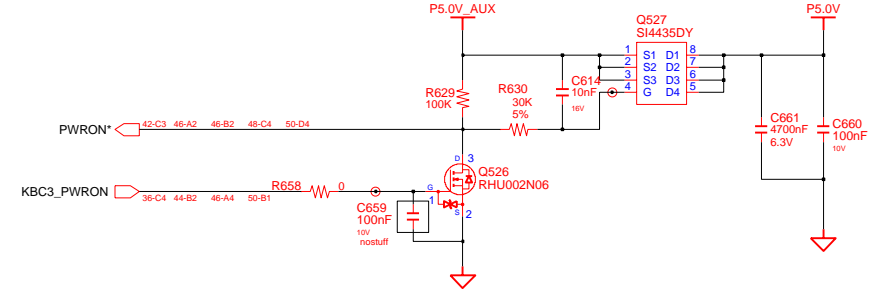
MICOM RESET



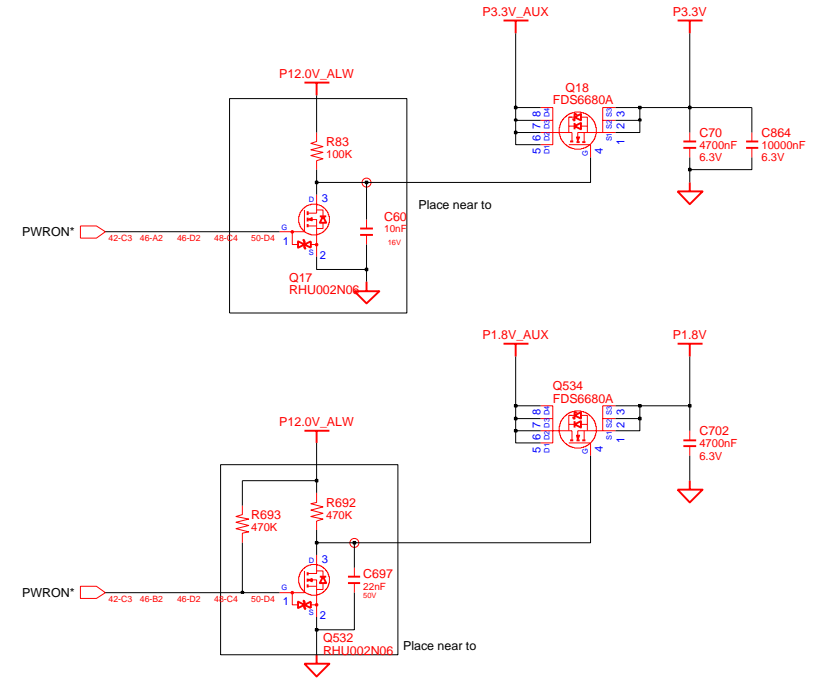
P1.5V POWER



Switched Power On (P5V)

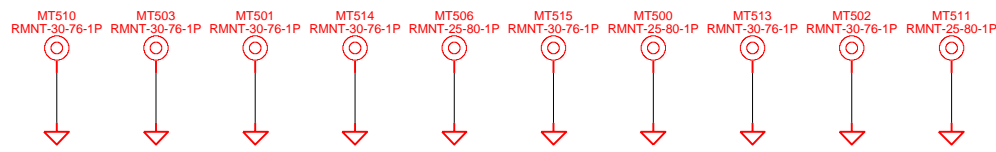
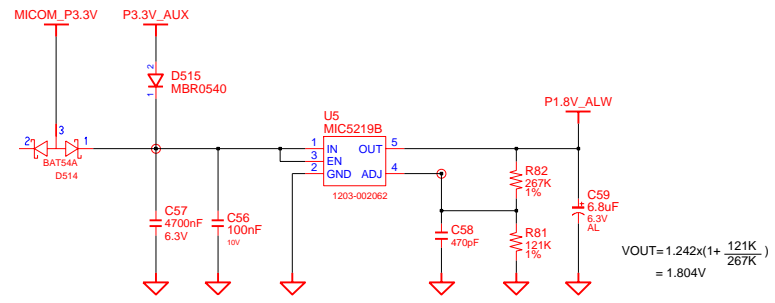


Switched Power On (P3.3V & 1.8V)



DRW#	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR	MICOM & SWITCHED POWER		
APPROVAL	SJ PARK	REV	1.0	PART NO.		BA41-00659A
MODULE CODE	undefined	LAST EDIT		Apr 15, 2006 8:18:08 PM		PAGE 46 OF 52

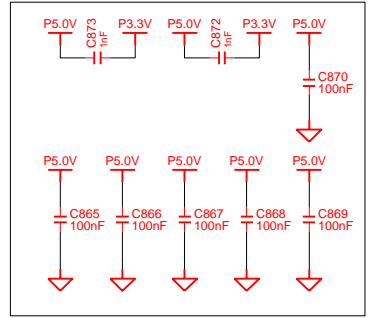
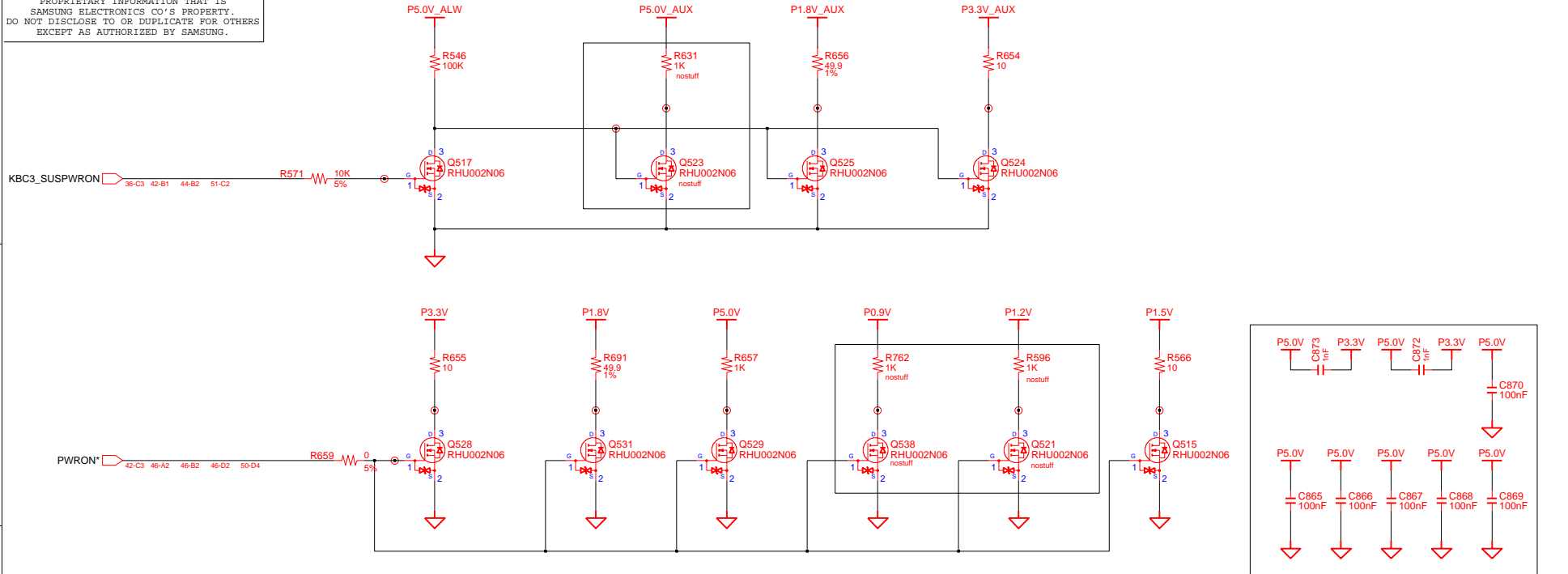
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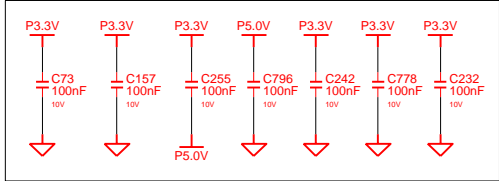
DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR	P1.2V & P2.5V AUX POWER	PART NO. BA41-00659A	
APPROVAL	SJ PARK	REV	1.0			LAST EDIT
MODULE CODE	undefined					

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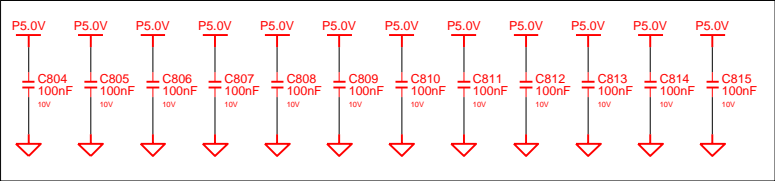
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To enhance DMB performance(060206)

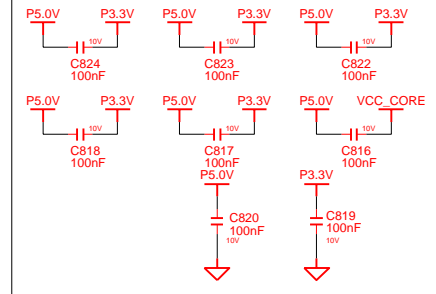


STITCHING CAP

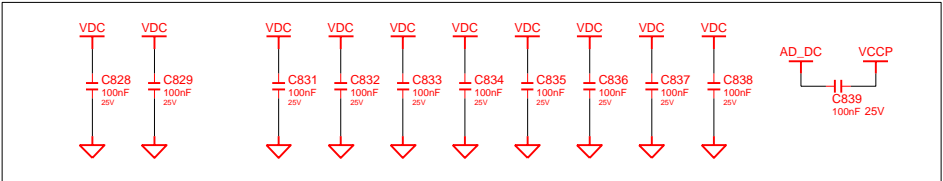


Decap for P5.0V Plane

To reduce BB noise(120 ~ 230MHz) from Power Line (2006/01/24 relate on EMI)



Stitching Cap for Power partition To reduce BB noise(120 ~ 230MHz) from Power Partition points (2006/01/24 relate on EMI)



Decap for VDC

To reduce BB noise(120 ~ 230MHz) from Power Line (2006/01/24 relate on EMI)

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAINBD	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR		POWER ADAPT	
APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00659A
MODULE CODE	undef ined	LAST EDIT		Apr il 5, 2006 8:18:08 PM	PAGE	48 OF 52

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PCB REVISION CONTROL (ICT)

NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV500
1 ○
2 ○ ○3

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0		TP	PART NO. BA41-00659A
MODULE CODE		LAST EDIT		April 5, 2006 8:18:08 PM	PAGE 49 OF 52	

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○COEX1
 ○COEX2
 ○ILIM3
 ○ILIM6
 ○MIC1_L
 ○MIC1_R
 ○PWRON*
 ○TVO3_C
 ○TVO3_Y
 ○IDES_A0
 ○IDES_A1
 ○IDES_A2
 ○ODDS_A0
 ○ODDS_A1
 ○ODDS_A2
 ○PC_BEEF
 ○RTC_CLK
 ○AC_SDOOUT
 ○ADT3_SEL
 ○AUTO_ON*

 ○CPU1_ICK
 ○CPU1_ID1
 ○CPU1_TMS
 ○CRT3_RED

 ○HP_OUT_L
 ○HP_OUT_R

○ODDS_IRO
 ○PCT3_PAR
 ○SMB3_CLK

○CRS3_CCLK
 ○CRS3_CPAR
 ○CRS3_CVS1
 ○CRS3_CVS2
 ○CRS3_SPK6
 ○CHP3_SPKR
 ○CLK3_FM48

○ORT3_BLUE
 ○HDD3_ED*
 ○IDES_CS1*
 ○IDES_CS3*
 ○IDES_D(0)
 ○IDES_D(1)
 ○IDES_D(2)
 ○IDES_D(3)
 ○IDES_D(4)
 ○IDES_D(5)
 ○IDES_D(6)
 ○IDES_D(7)
 ○IDES_D(8)
 ○IDES_D(9)
 ○IDES_DREQ
 ○IDES_IOR*
 ○IDES_IOW*
 ○KBC3_A29G
 ○KBC3_RST*
 ○KBC3_VRON
 ○KBC5_TCLK
 ○LAN3_ACT*

○ODDS_CS1*
 ○ODDS_CS3*
 ○ODDS_D(8)
 ○ODDS_D(1)
 ○ODDS_D(2)
 ○ODDS_D(3)
 ○ODDS_D(4)
 ○ODDS_D(5)
 ○ODDS_D(6)
 ○ODDS_D(7)
 ○ODDS_D(8)
 ○ODDS_D(9)
 ○ODDS_DREQ
 ○ODDS_IOR*
 ○ODDS_IOW*
 ○ODDS_RST*
 ○PCT3_CLK8
 ○PCT3_RST*
 ○SMB3_DATA
 ○VGAS_DDCD
 ○VGAS_DDCD
 ○WLAN_LED*
 ○AUD3_EAPD*
 ○CRS3_I_D2*
 ○CRS3_CCD1*
 ○CRS3_CCD2*
 ○CRS3_CGNT*
 ○CRS3_CINT*
 ○CRS3_SPK4*
 ○CRS3_CRST*

○CLK3_I0H14
 ○CLK3_N0H14M
 ○CLK3_USB48

○CRT3_GREEN
 ○CRT5_HSYNC
 ○CRT5_VSYNC
 ○FWH1_INIT*
 ○IDES_D(10)
 ○IDES_D(11)
 ○IDES_D(12)
 ○IDES_D(13)
 ○IDES_D(14)
 ○IDES_D(15)
 ○IDES_DACK*
 ○IDES_DASP*
 ○IDES_IORDY
 ○JCK_SENS_A
 ○KBC3_CHGEN
 ○KBC3_PWRGD
 ○KBC3_PWRON
 ○KBC5_TDATA

○LAN3_WAKE*
 ○LCD3_VDDEN
 ○LINE_OUT_L
 ○LINE_OUT_R

○ODDS_D(10)
 ○ODDS_D(11)
 ○ODDS_D(12)
 ○ODDS_D(13)
 ○ODDS_D(14)
 ○ODDS_D(15)
 ○ODDS_DACK*
 ○ODDS_IORDY
 ○PCT3_AD(0)
 ○PCT3_AD(1)
 ○PCT3_AD(2)
 ○PCT3_AD(3)

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR		TP	
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT		April 5, 2006 8:18:08 PM	PAGE	50 OF 52

