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# Compal Confidential

## HTW00 LA-2871 Schematics Document

Intel Dothan with 915PM(GM)/910GML + DDRII + ICH6M  
(+VGA/B ATi M24C/M26P)

2005-08-22

REV: 1.0

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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
1394	D0	AD20	2	A, B, C, D
LAN	D1	AD17	3	F
CARD BUS	D4	AD20	2	A, B, C, D
5IN1	D4	AD20	2	A, B, C, D
Mini-PCI	D2	AD18	1	G, H

## KB910 I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
SM1 24C16	A0H	1 0 1 0 0 0 0 X b
SM1 SMART BATTERY	16H	0 0 0 1 0 1 1 X b
SM2 ADM0132 CPU THERMAL MONITOR	98H	1 0 0 1 1 0 0 X b
SM2 GMT G781-1 VGA THERMAL MONITOR	9AH	1 0 0 1 1 0 1 X b

## ICH6M SM Bus address

Device	Address
Clock Generator ( ICS 954226)	1101 001Xb
DDR11 DIMM0	1001 000Xb
DDR11 DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

## BTO Option Table

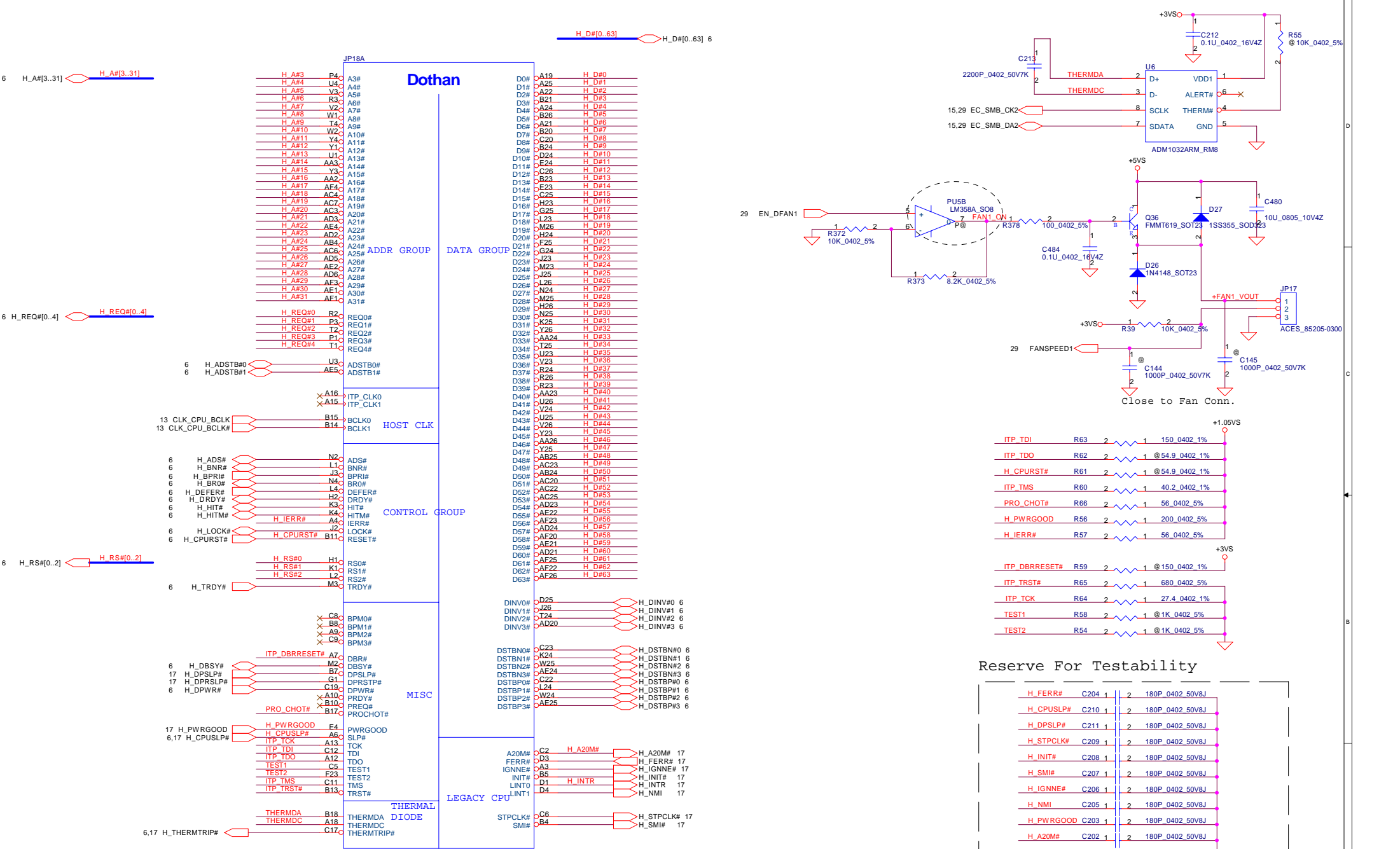
BTO Item	BOM Structure
VGA	GM@ PM@
Card Reader	5IN1@
Giga LAN	8100C@ 8110S@
New Card	NEWCARD@
IEEE1394	1394@
TV Tuner	TUNER@
INT MIC.	MIC@
KILL SW	WLAN@
CIR	CIR@
HWEQ	EQ@ NOEQ@

(TBD)

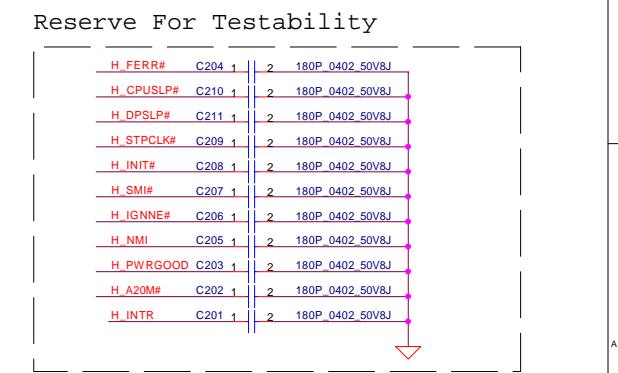
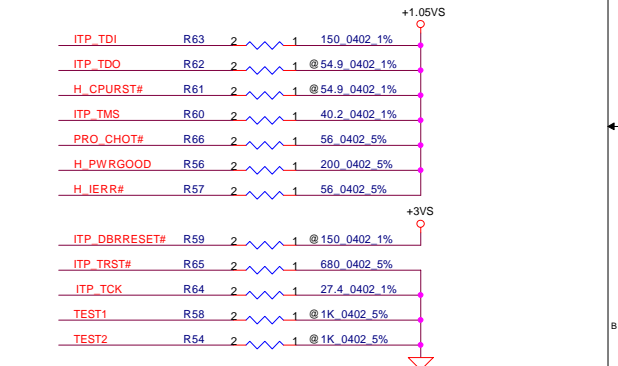
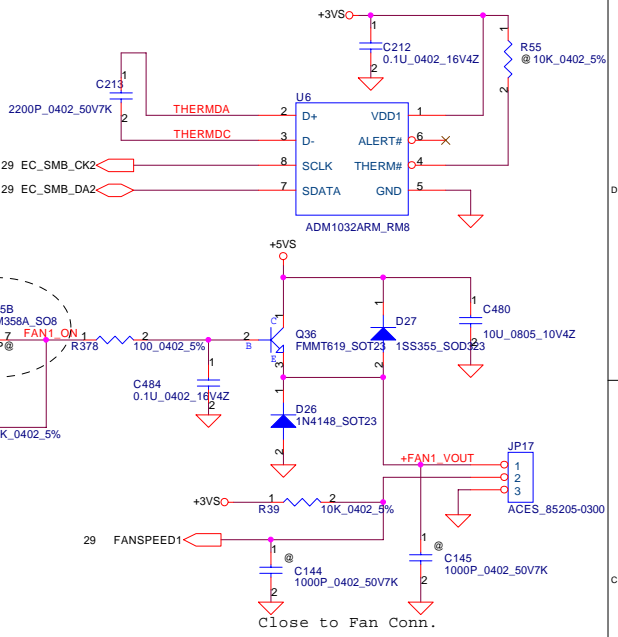
## SKU ID Table

SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	

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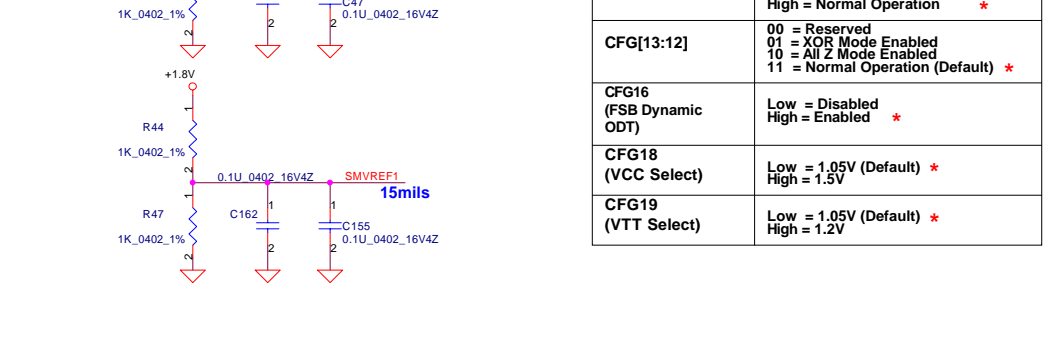
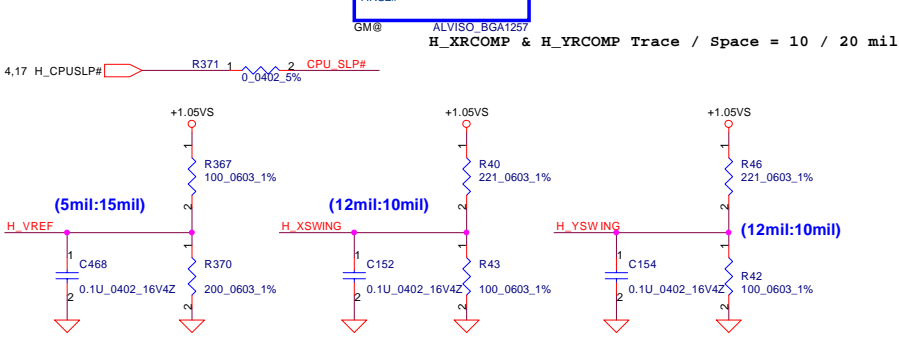
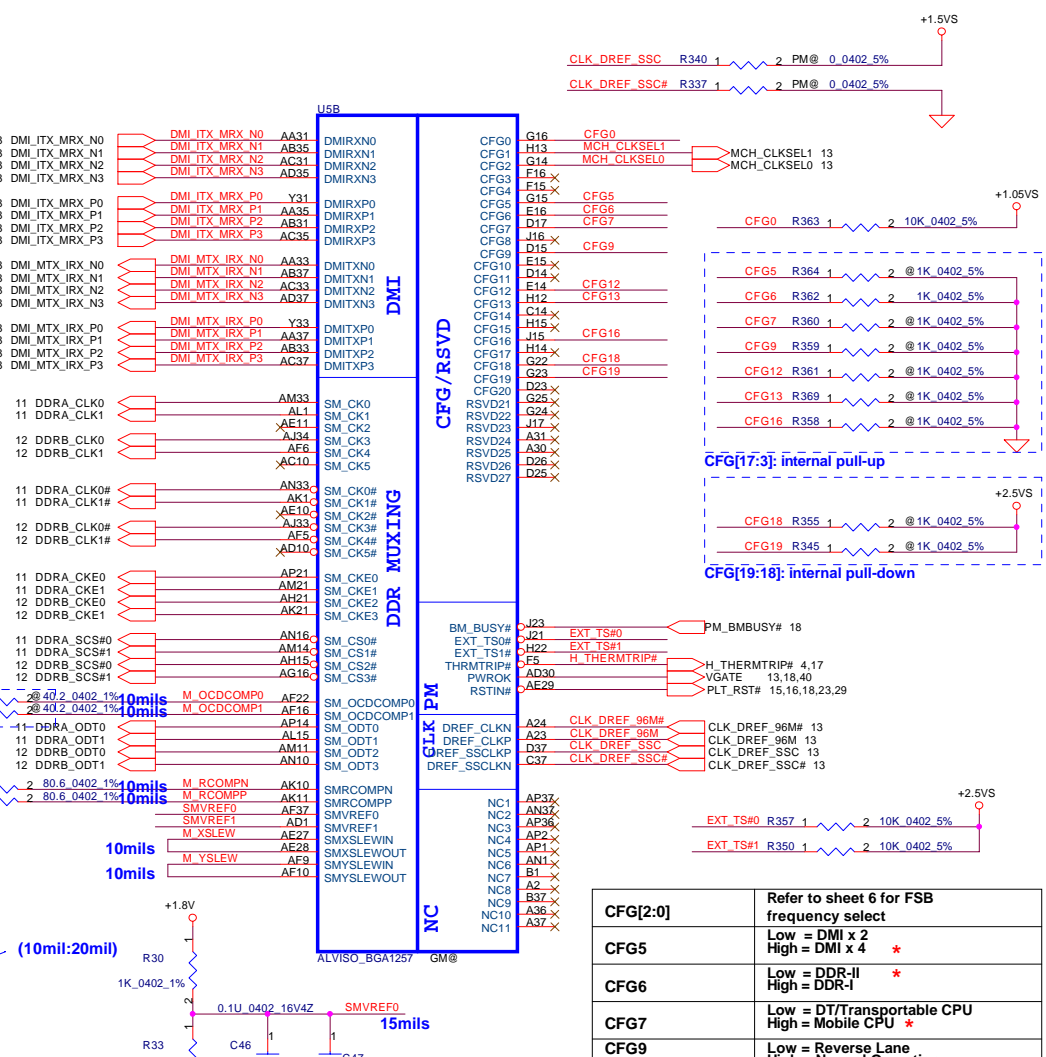
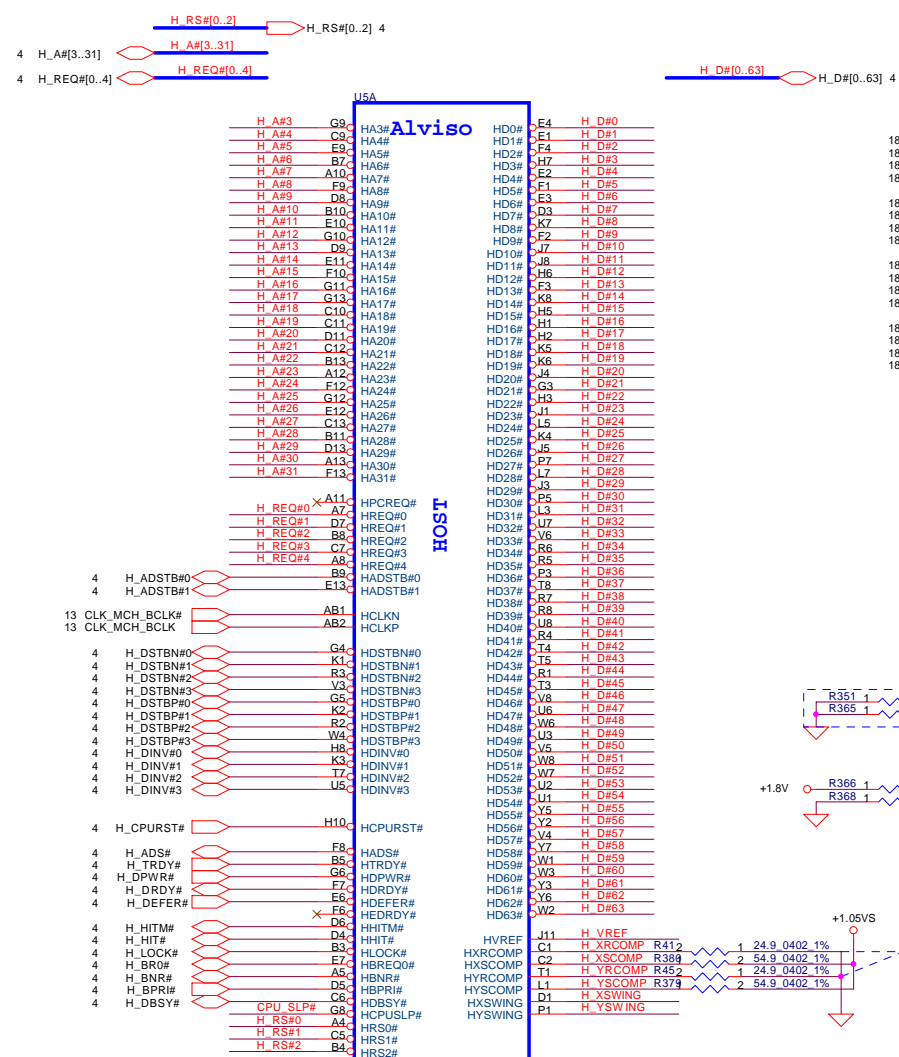


THERMDA & THERMDC Trace / Space = 10 / 10 mil

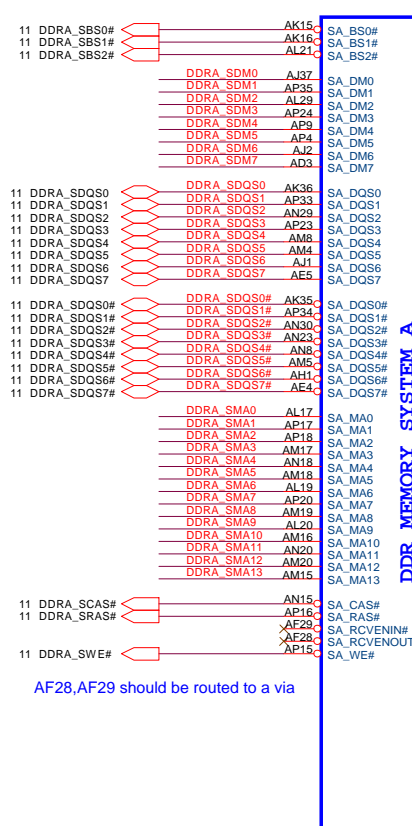
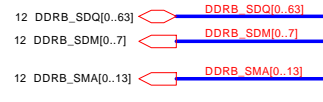
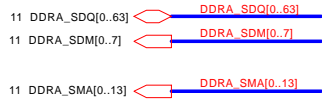


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CFG[2:0]	Refer to sheet 6 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II High = DDR-I *
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V



DDR MEMORY SYSTEM A



DDR MEMORY SYSTEM B

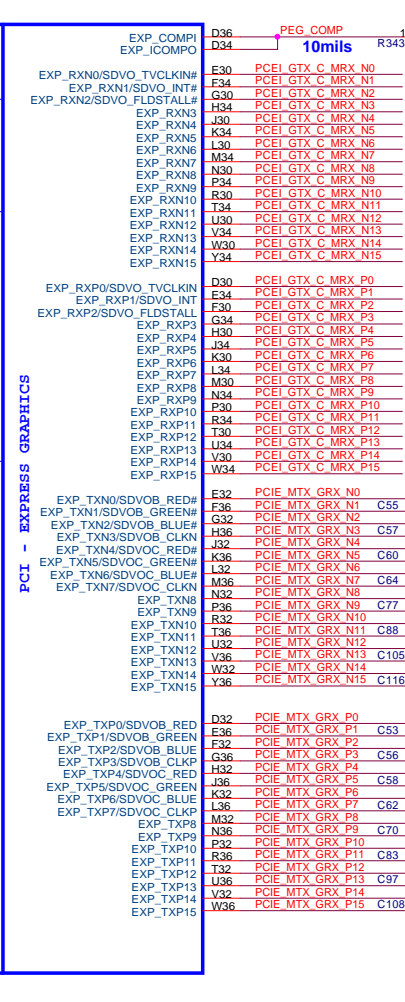
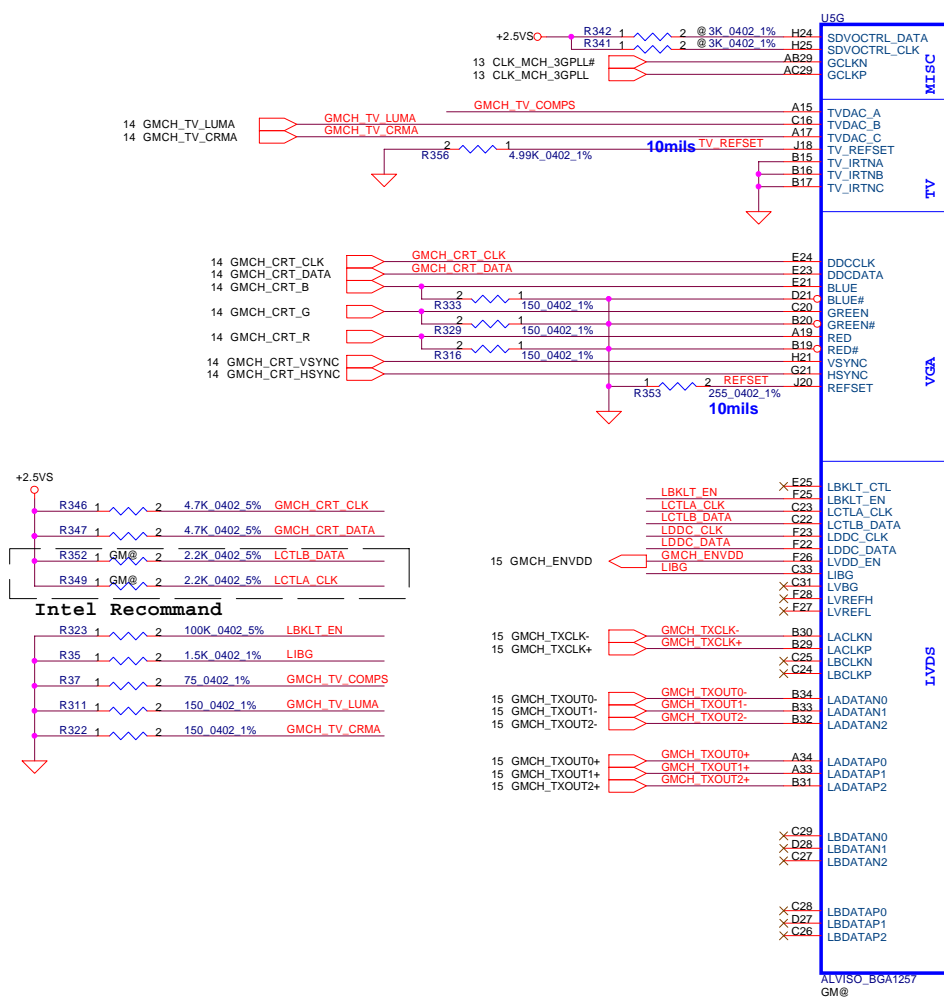
AF28,AF29 should be routed to a via

AF14,AF15 should be routed to a via

GM@ ALVISO\_BGA1257

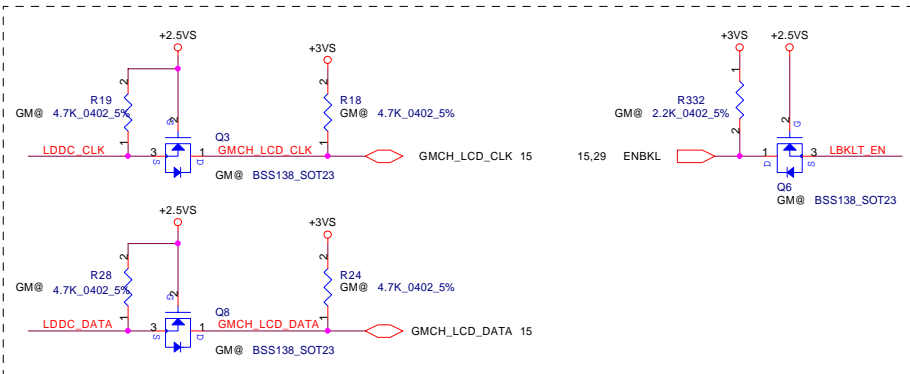
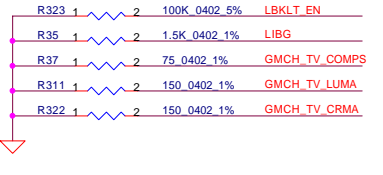
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				Alviso DDR(2/5)	
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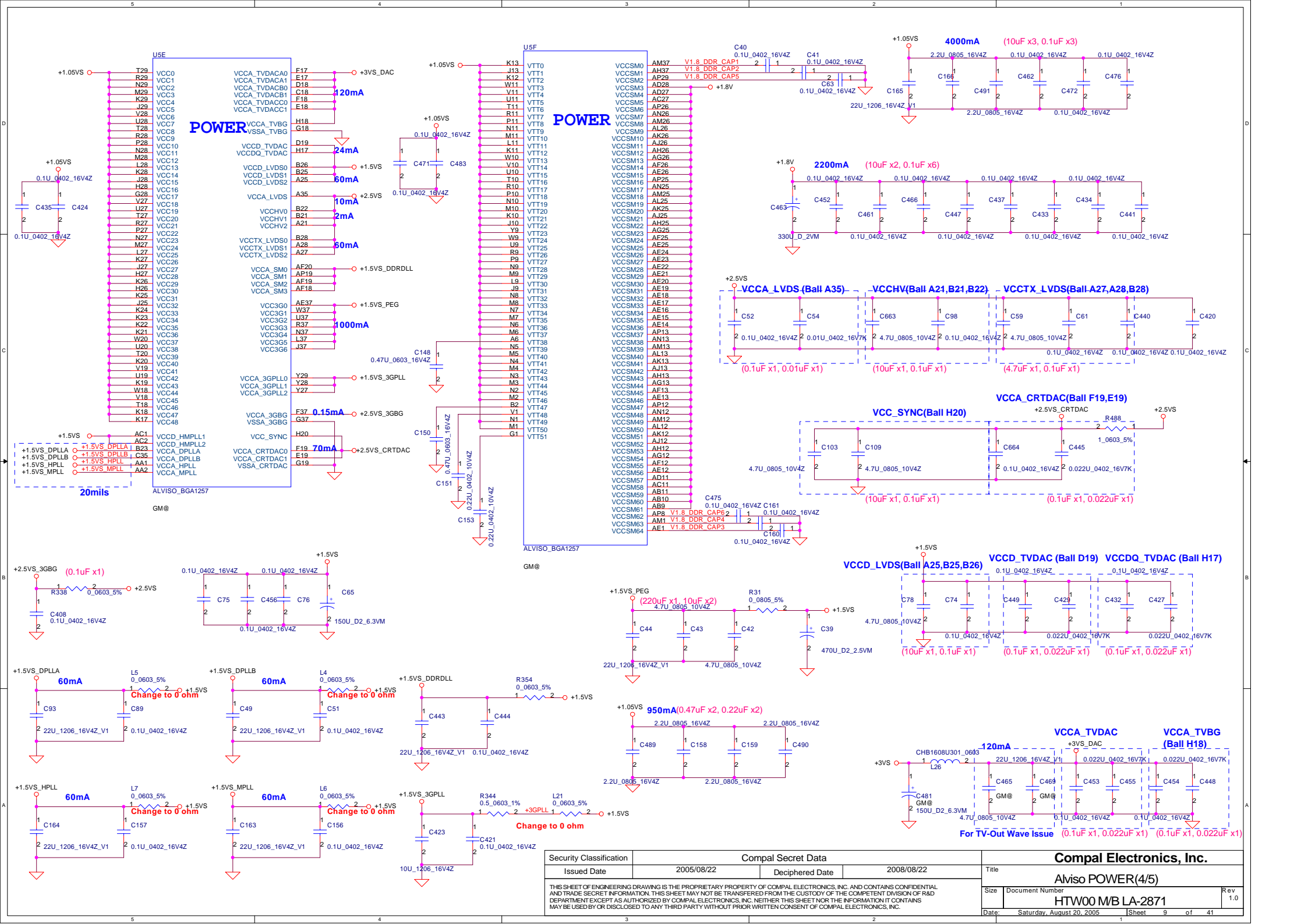
Pin	Signal	Value	Notes
E32	PCIE MTX GRX N0	C411 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N0
F36	PCIE MTX GRX N1	C55 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N1
G32	PCIE MTX GRX N2	C415 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N2
H36	PCIE MTX GRX N3	C57 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N3
J32	PCIE MTX GRX N4	C419 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N4
K36	PCIE MTX GRX N5	C60 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N5
L32	PCIE MTX GRX N6	C425 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N6
M36	PCIE MTX GRX N7	C64 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N7
N32	PCIE MTX GRX N8	C431 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N8
P36	PCIE MTX GRX N9	C77 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N9
R32	PCIE MTX GRX N10	C438 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N10
T36	PCIE MTX GRX N11	C88 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N11
U32	PCIE MTX GRX N12	C442 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N12
V36	PCIE MTX GRX N13	C105 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N13
W32	PCIE MTX GRX N14	C457 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N14
X36	PCIE MTX GRX N15	C116 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX N15
D32	PCIE MTX GRX P0	C410 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P0
E36	PCIE MTX GRX P1	C53 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P1
F32	PCIE MTX GRX P2	C414 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P2
G36	PCIE MTX GRX P3	C56 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P3
H32	PCIE MTX GRX P4	C418 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P4
J36	PCIE MTX GRX P5	C58 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P5
K32	PCIE MTX GRX P6	C422 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P6
L36	PCIE MTX GRX P7	C62 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P7
M32	PCIE MTX GRX P8	C428 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P8
N36	PCIE MTX GRX P9	C70 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P9
P32	PCIE MTX GRX P10	C436 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P10
R36	PCIE MTX GRX P11	C83 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P11
T32	PCIE MTX GRX P12	C439 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P12
U36	PCIE MTX GRX P13	C97 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P13
V32	PCIE MTX GRX P14	C450 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P14
W36	PCIE MTX GRX P15	C108 1	2 PM@ 0.1U 0402 16V4Z PCIE MTX C GRX P15

**Intel Recommend**



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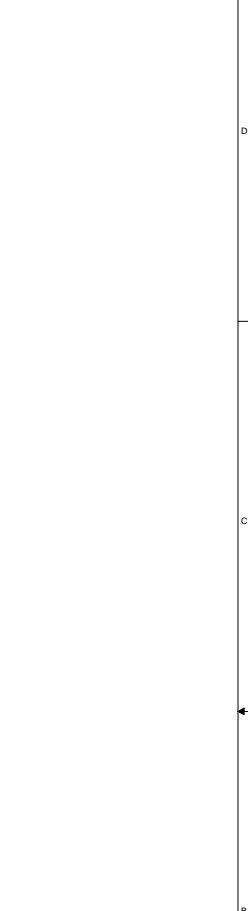
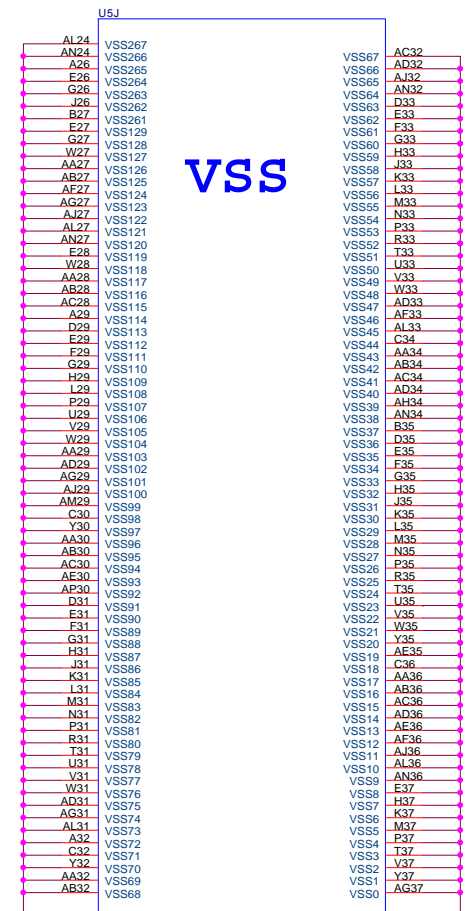
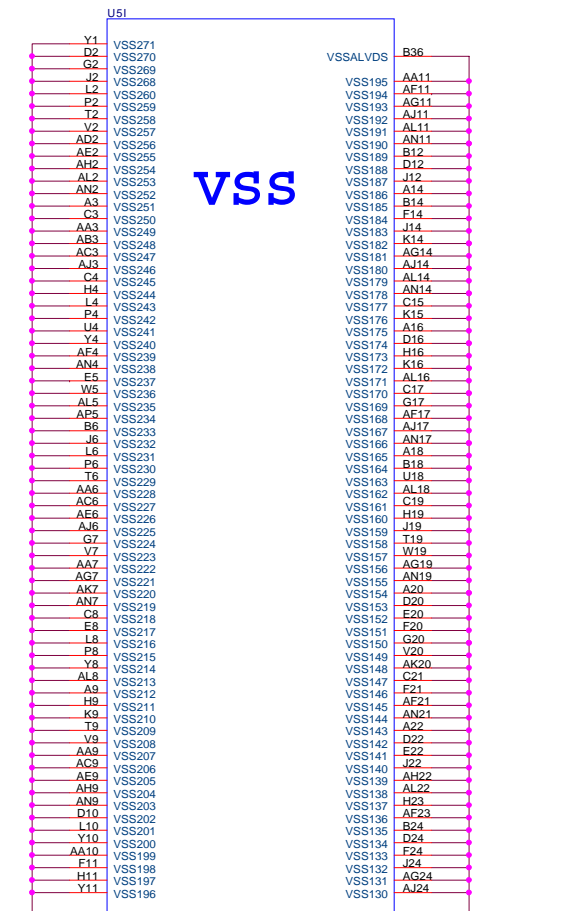
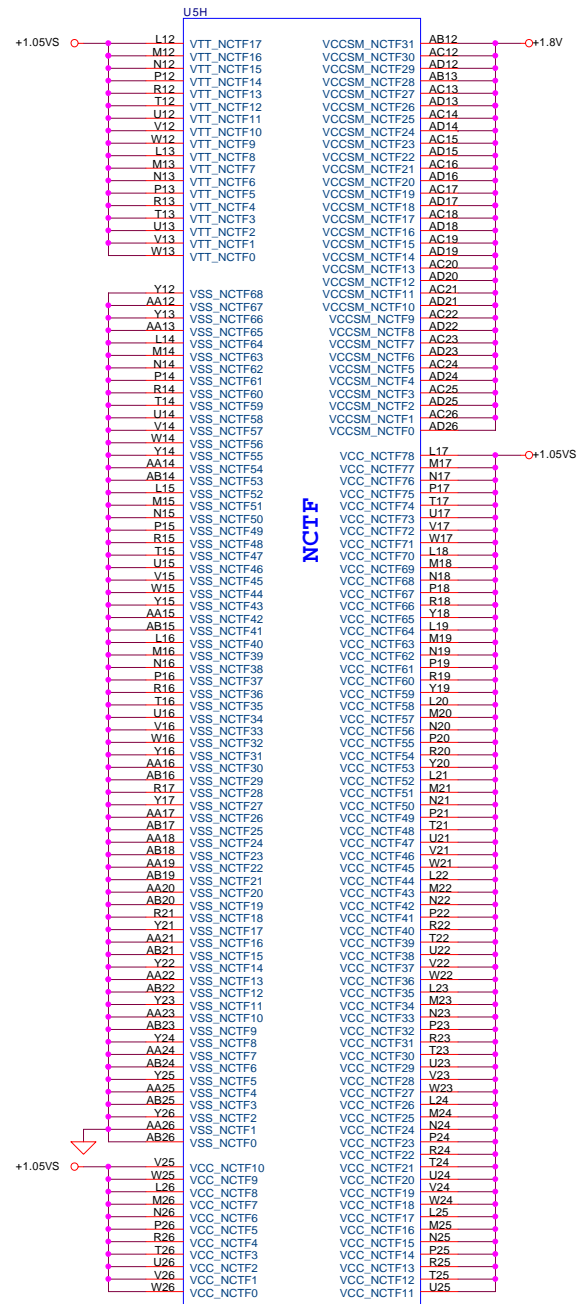
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**POWER**

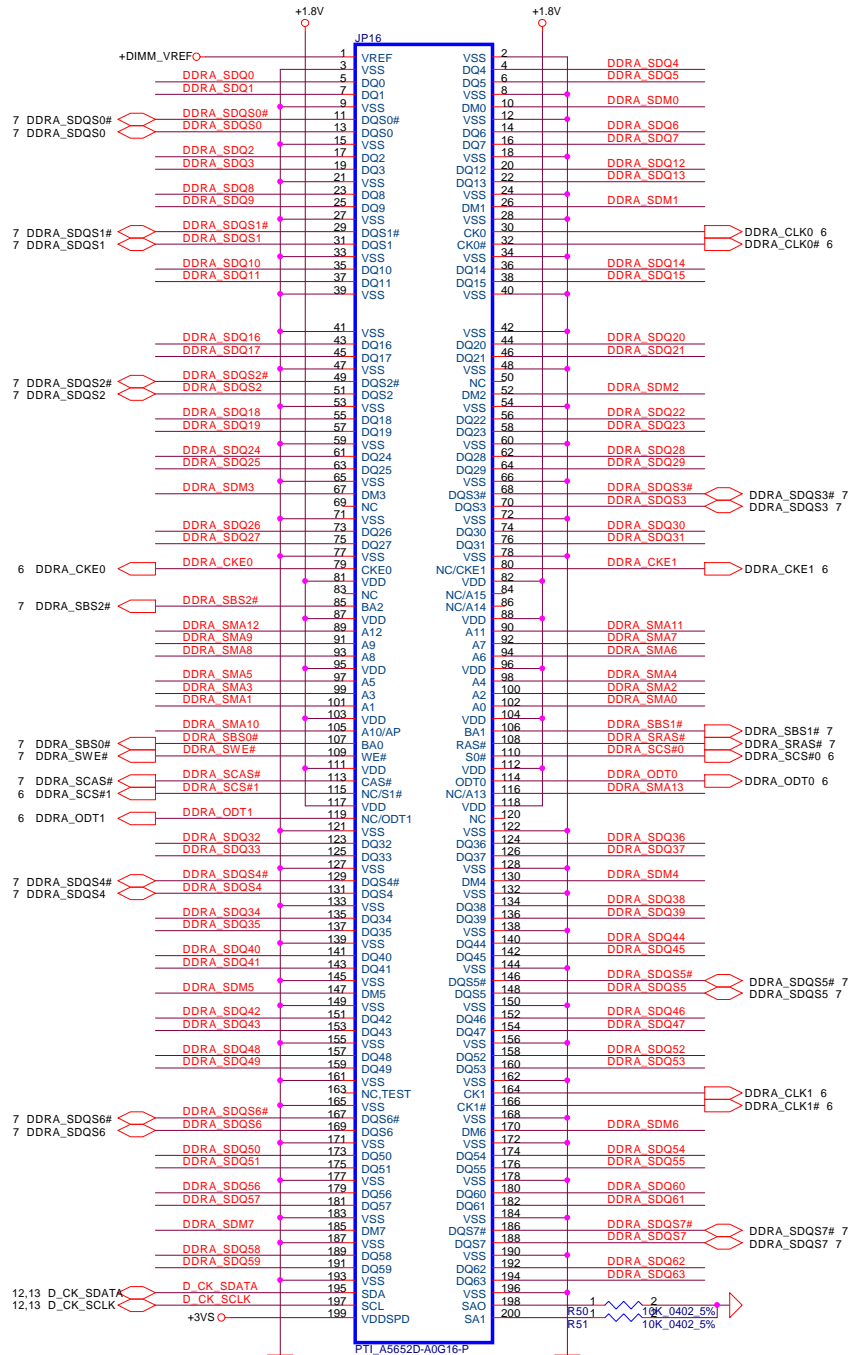
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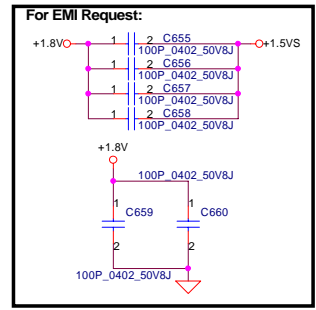
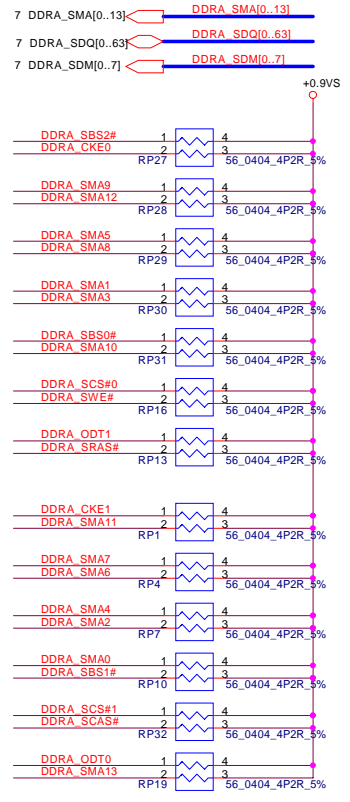
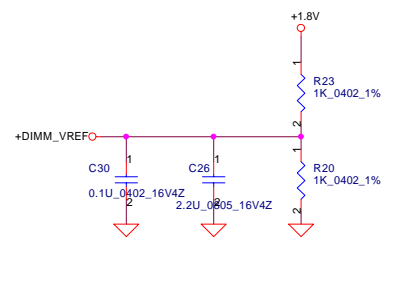
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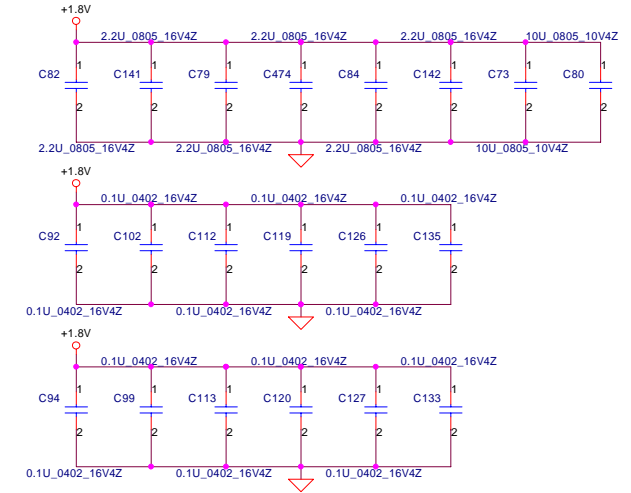
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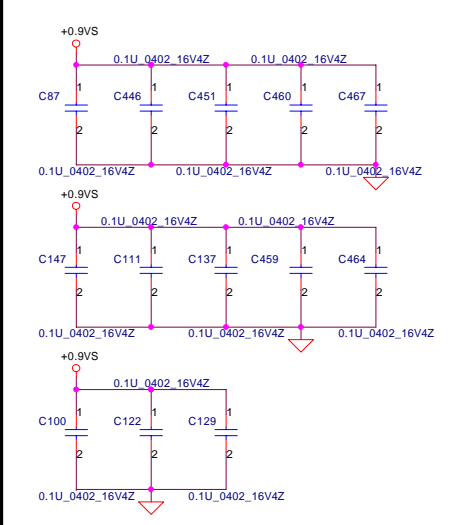
**DIMM0 STD H:5.2mm (BOT)**



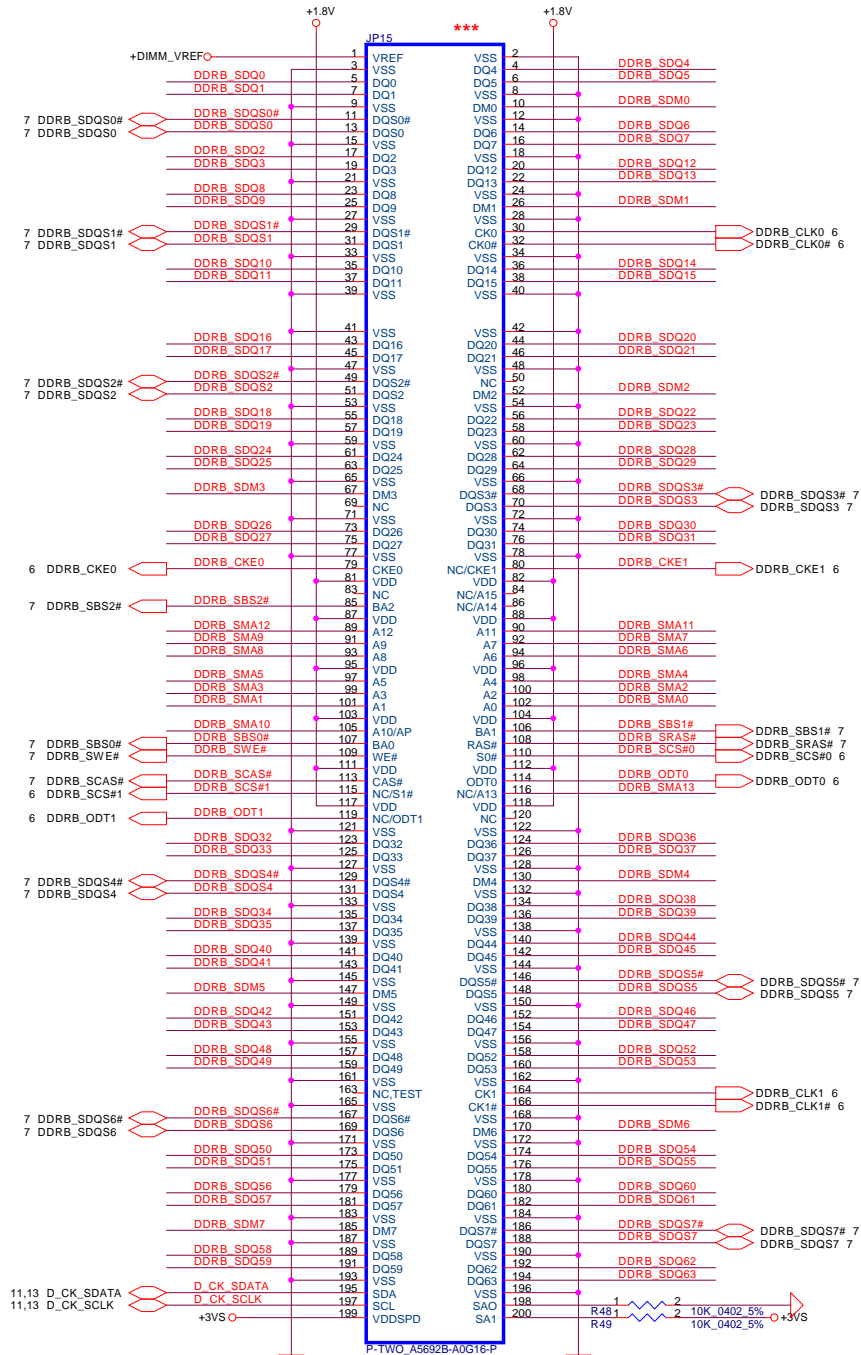
**Layout note :** Place one 0.1u cap close to every DDR-SODIMM pin one 2.2u cap close to every 2 0.1u cap



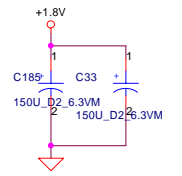
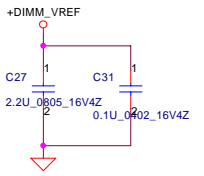
**Layout note :** Place one cap close to every 2 pull up resistors termination to +0.9VS



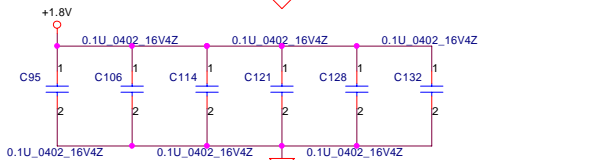
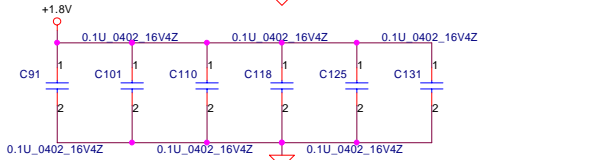
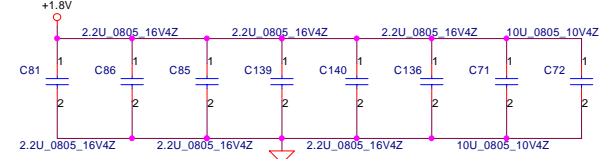
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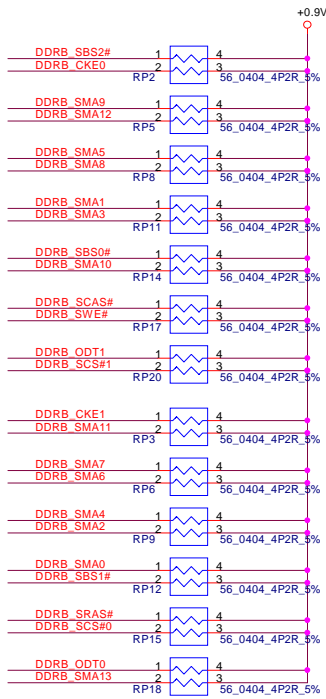
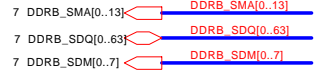
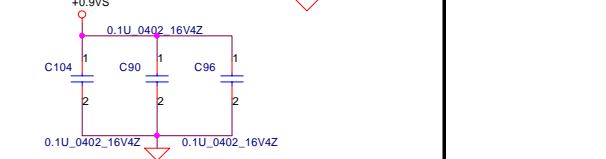
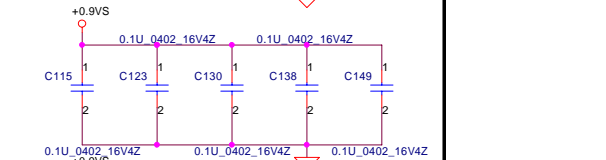
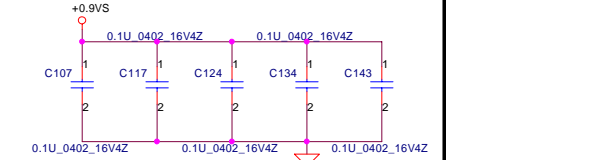
**DIMM1 STD H:9.2mm (BOT)**



**Layout note :** Place one 0.1u cap close to every DDR-SODIMM pin  
one 2.2u cap close to every 2.0u cap



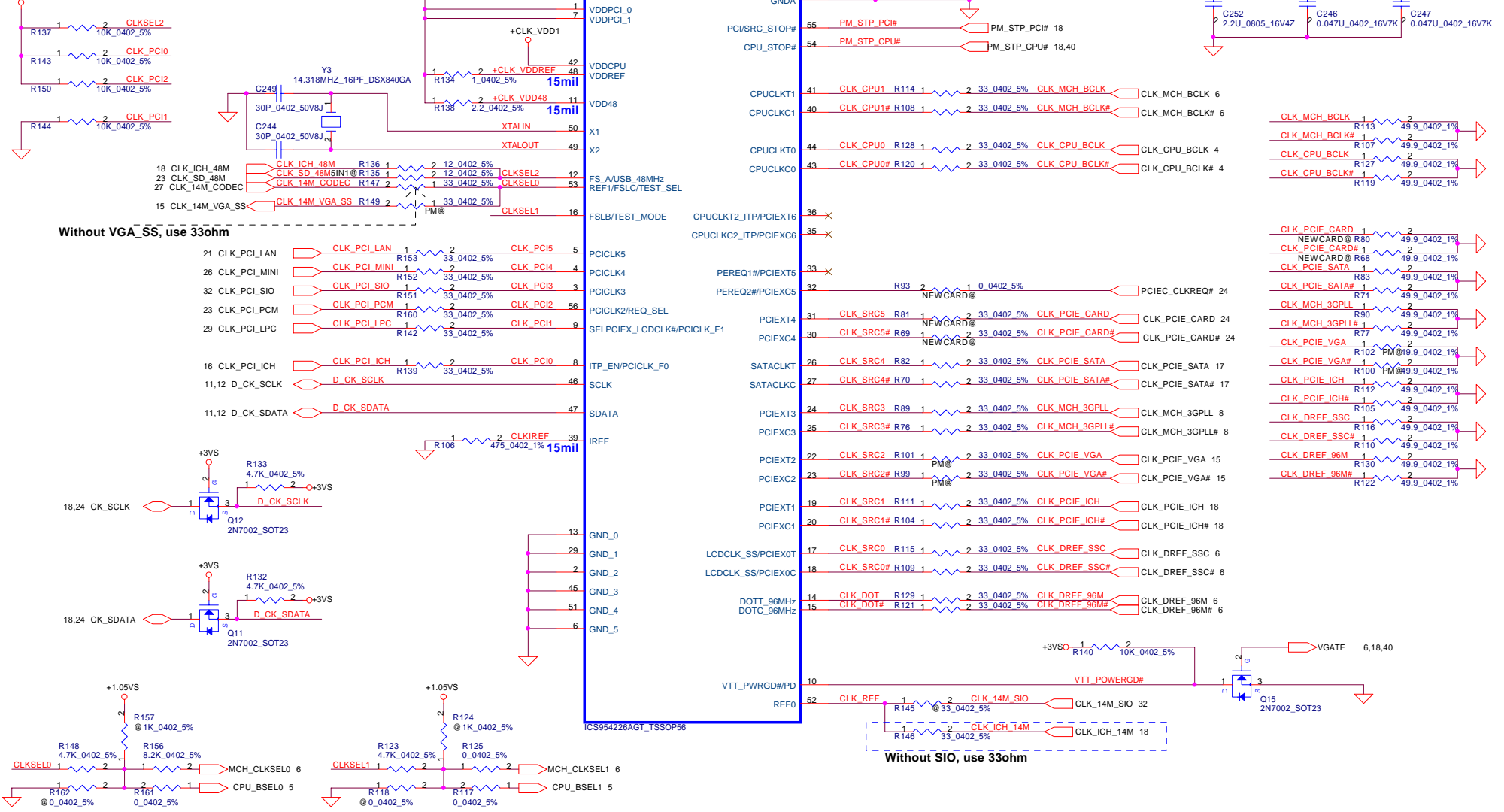
**Layout note :**  
Place one cap close to every 2 pull up resistors termination to +0.9VS



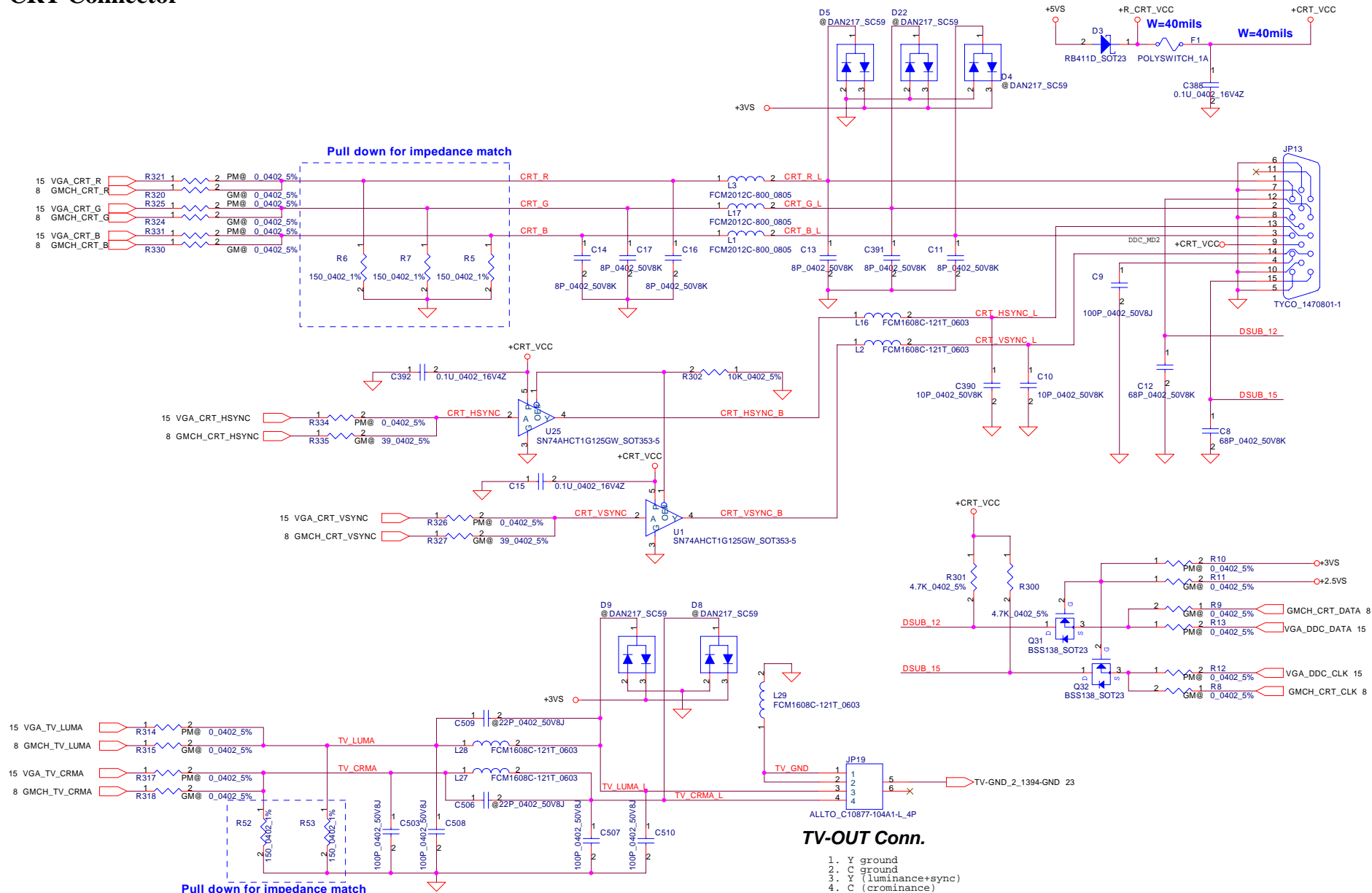
# Clock Generator

FSC	FSB	FSA	CPU MHz	SRC MHz	PCI MHz
1	0	1	100	100	33.3
0	0	1	133	100	33.3
0	1	1	166	100	33.3
0	1	0	200	100	33.3

Table : ICS 954226AG

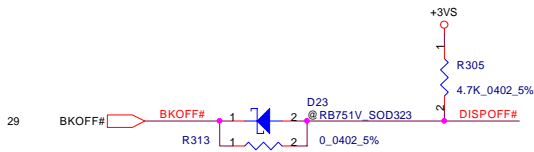
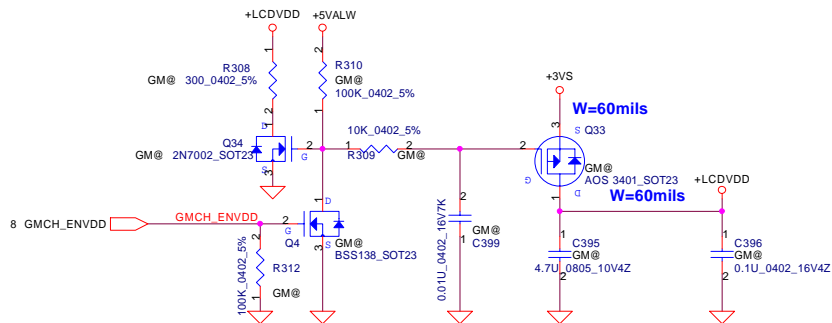


# CRT Connector

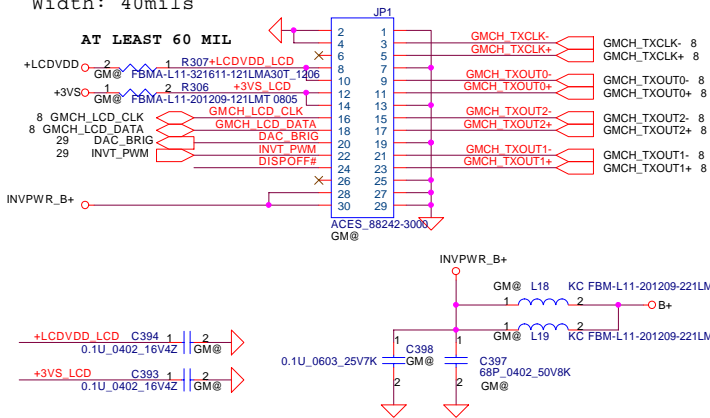


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Issued Date	2005/08/22	Deciphered Date	2008/08/22	CRT & TVout Connector
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				Document Number
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				Rev
				1.0
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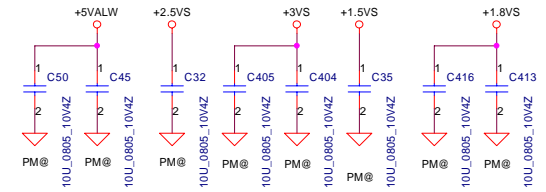
# LCD POWER CIRCUIT



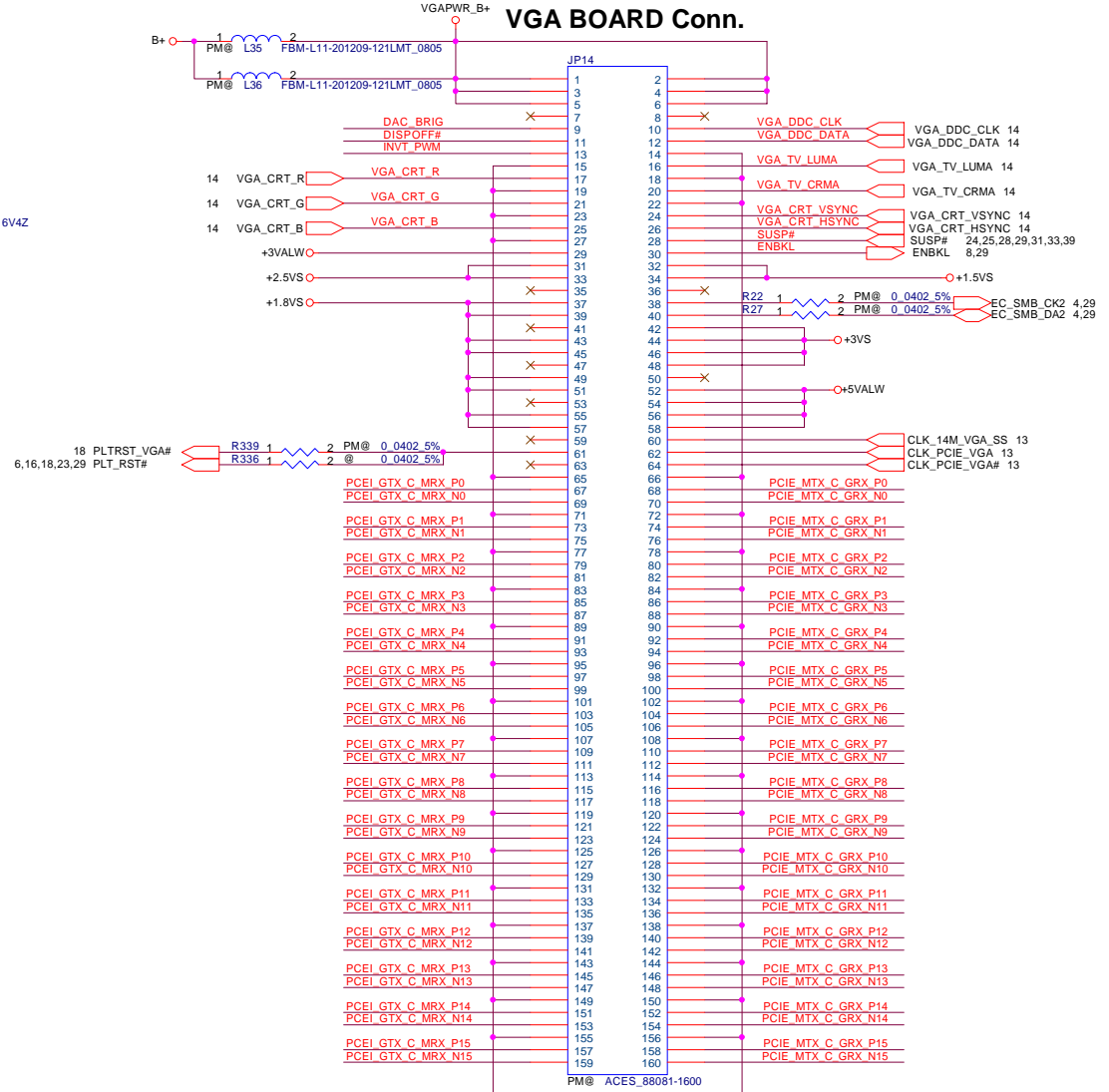
Width: 40mils



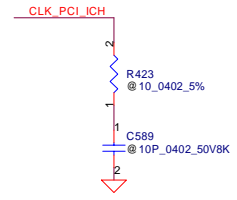
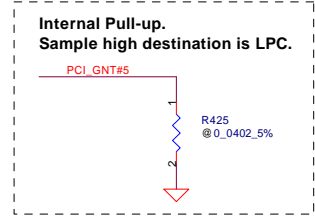
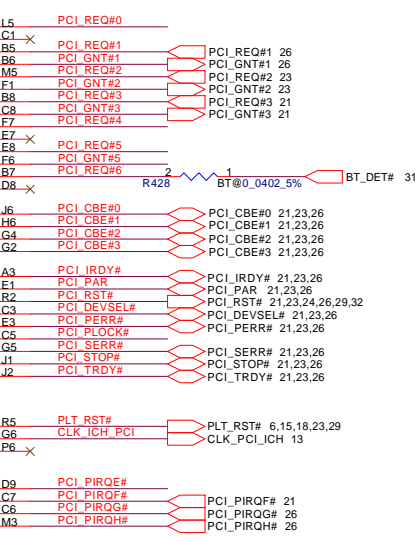
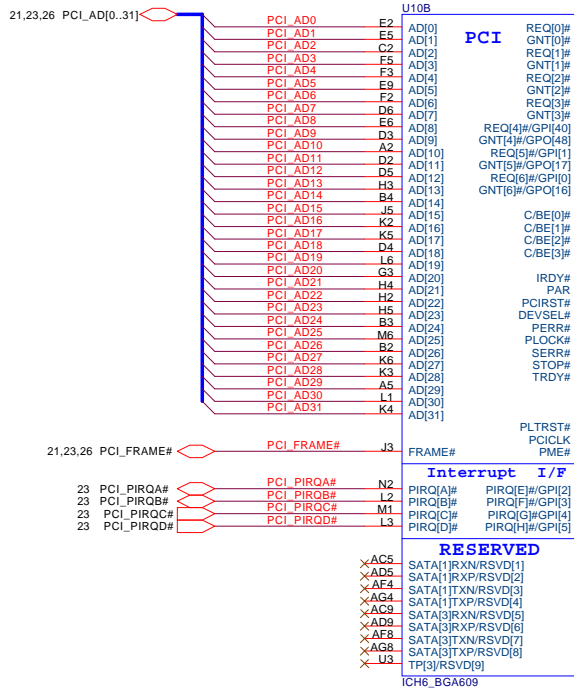
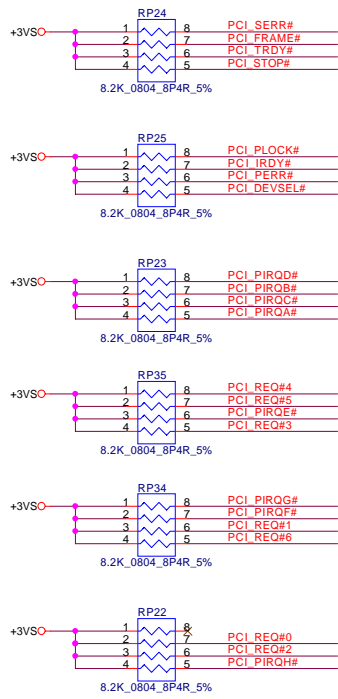
- 8 PCEI\_GTX\_C\_MRX\_N[0..15] <=> PCEI GTX C\_MRX N[0..15]
- 8 PCEI\_GTX\_C\_MRX\_P[0..15] <=> PCEI GTX C\_MRX P[0..15]
- 8 PCIE\_MTX\_C\_GRX\_N[0..15] <=> PCIE MTX C\_GRX N[0..15]
- 8 PCIE\_MTX\_C\_GRX\_P[0..15] <=> PCIE MTX C\_GRX P[0..15]



# VGA BOARD Conn.



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				Document Number
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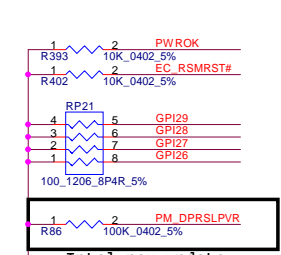
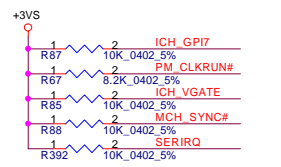
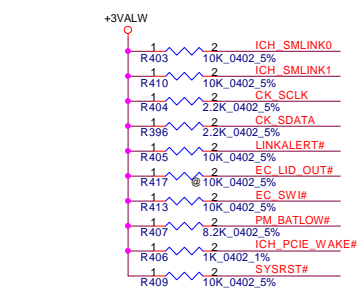


**ICH6-M**  
**(R3: SA828010890)**  
**(R1: SA8280108B0)**

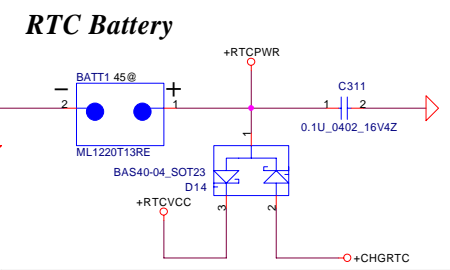
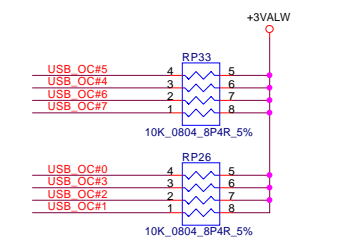
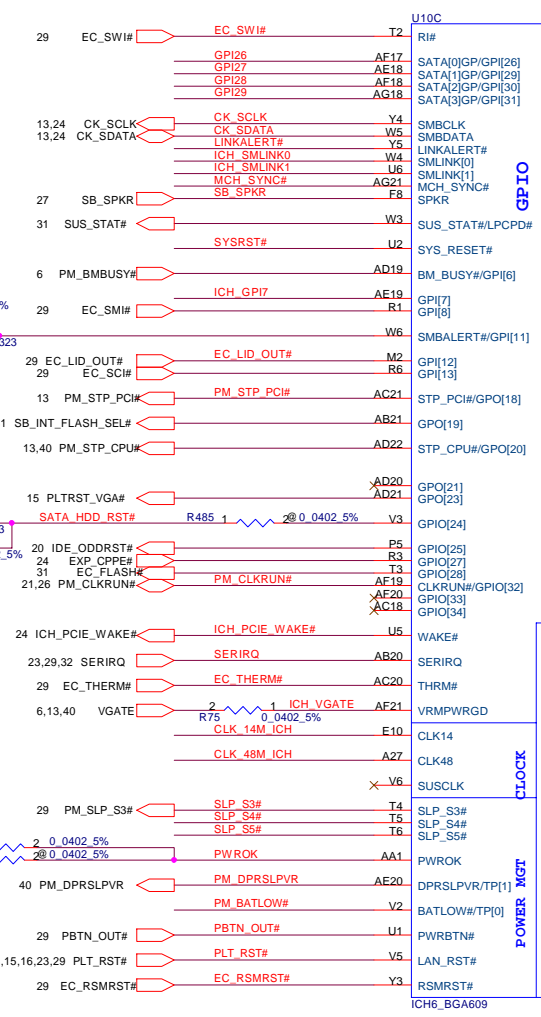
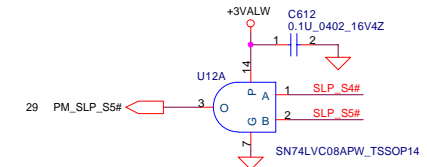
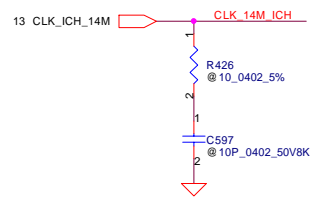
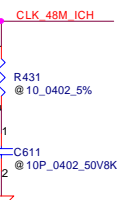
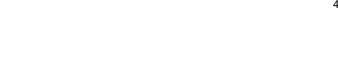
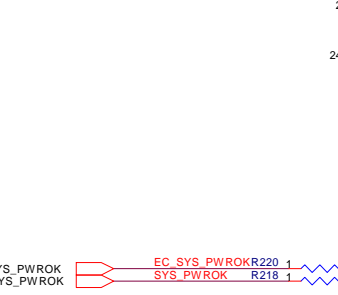
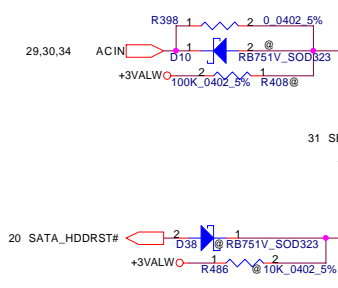
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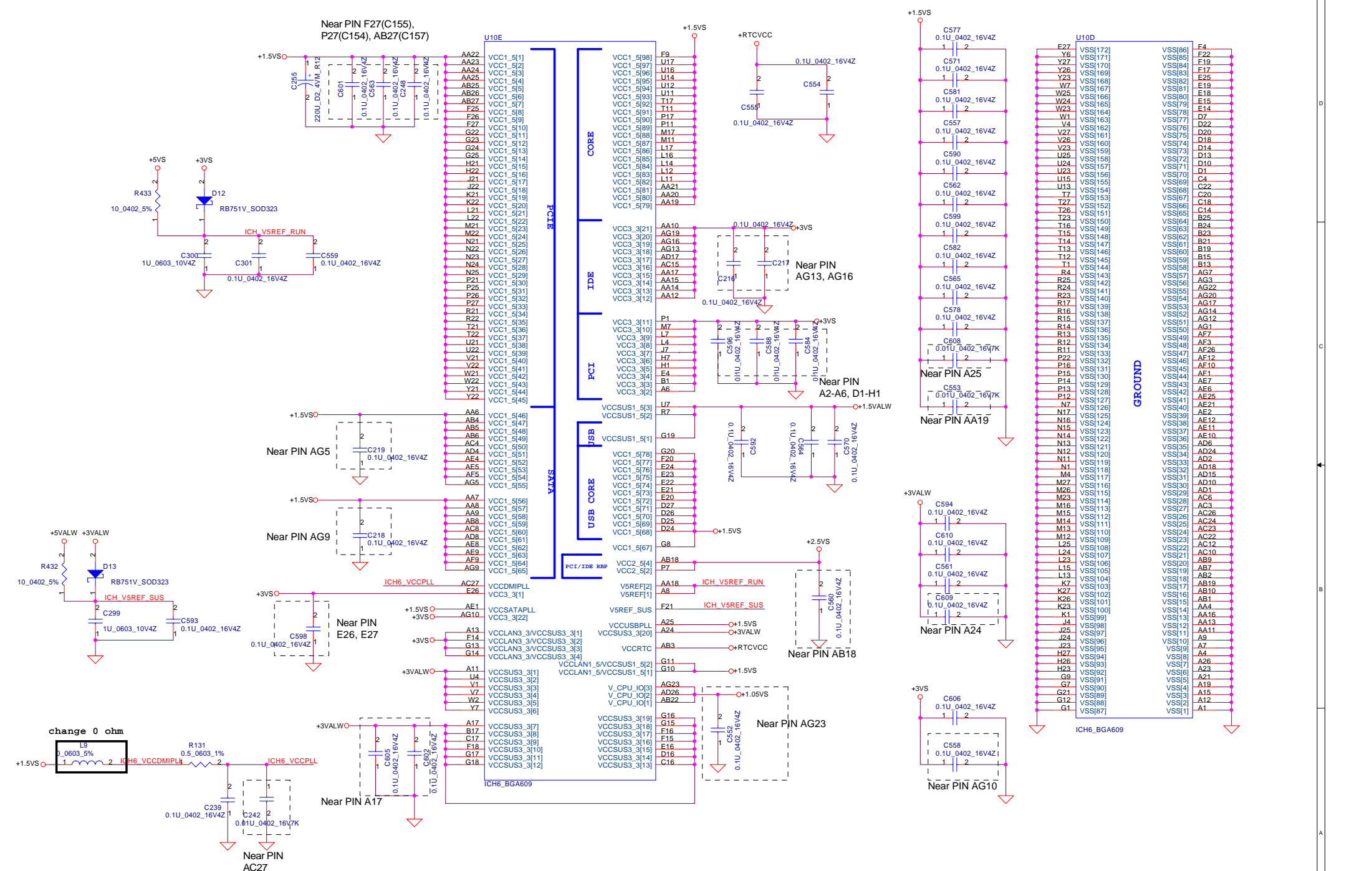


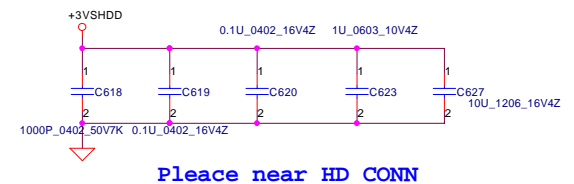
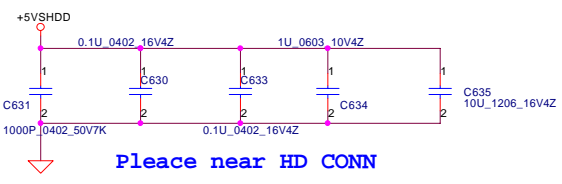


Intel new update

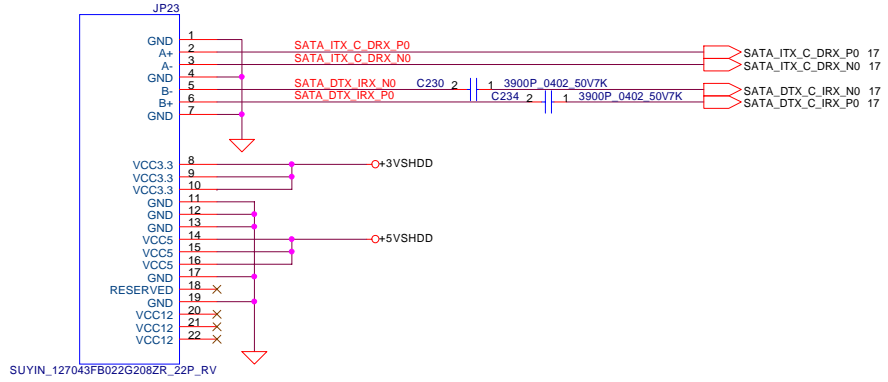


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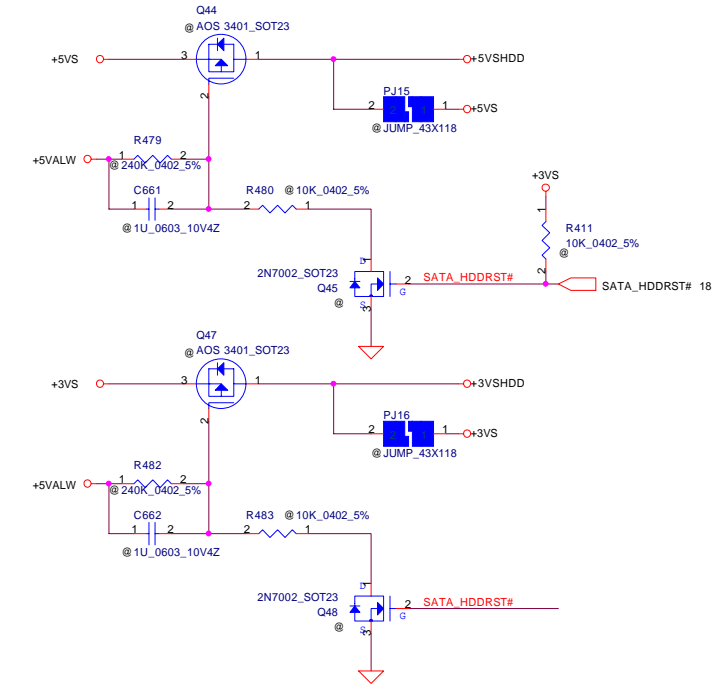




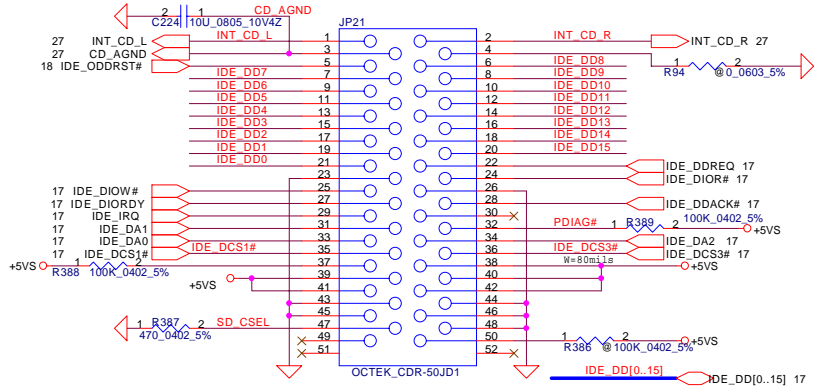
**S-ATA HDD Conn.**



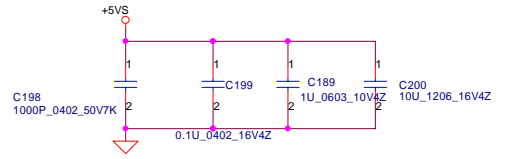
**Reserve for SATA HDD RESET**



**CDROM CONN**

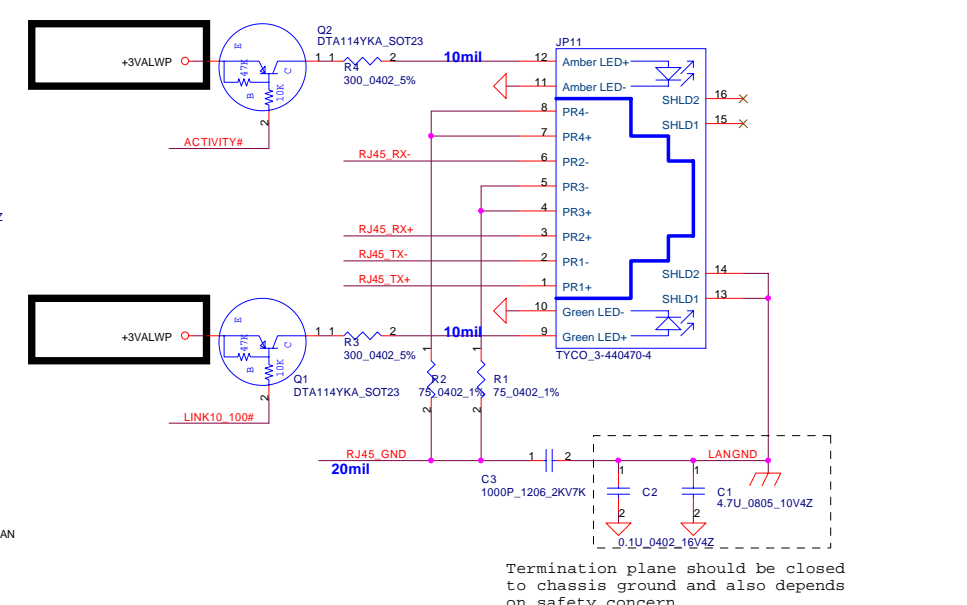
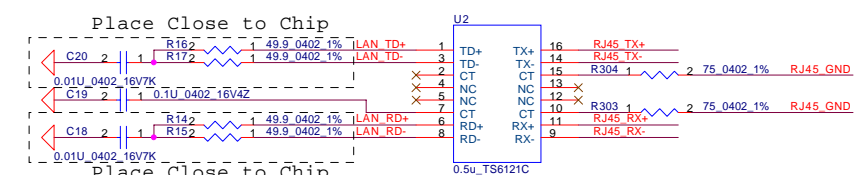
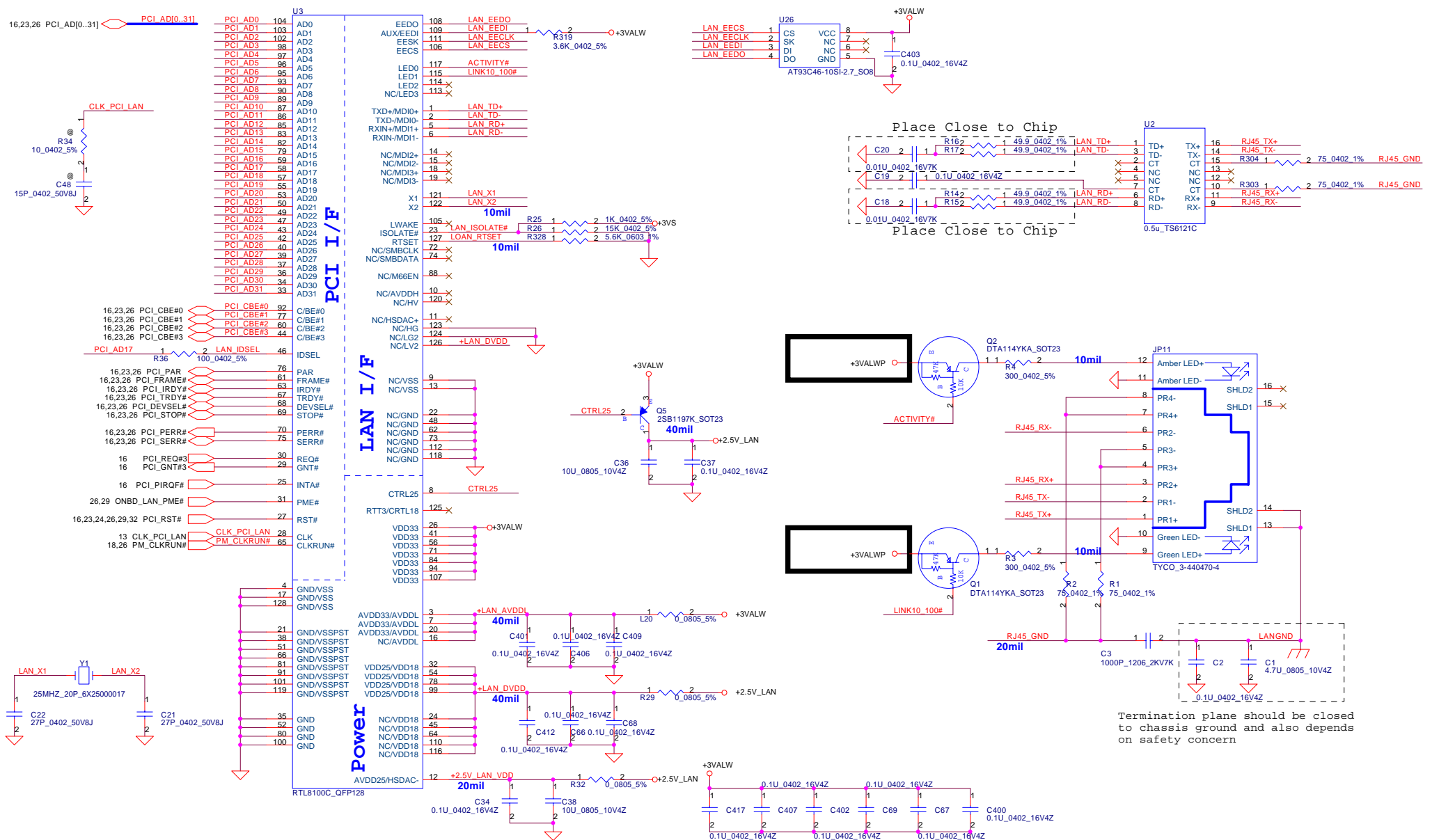


**Place caps. near CDROM CONN.**



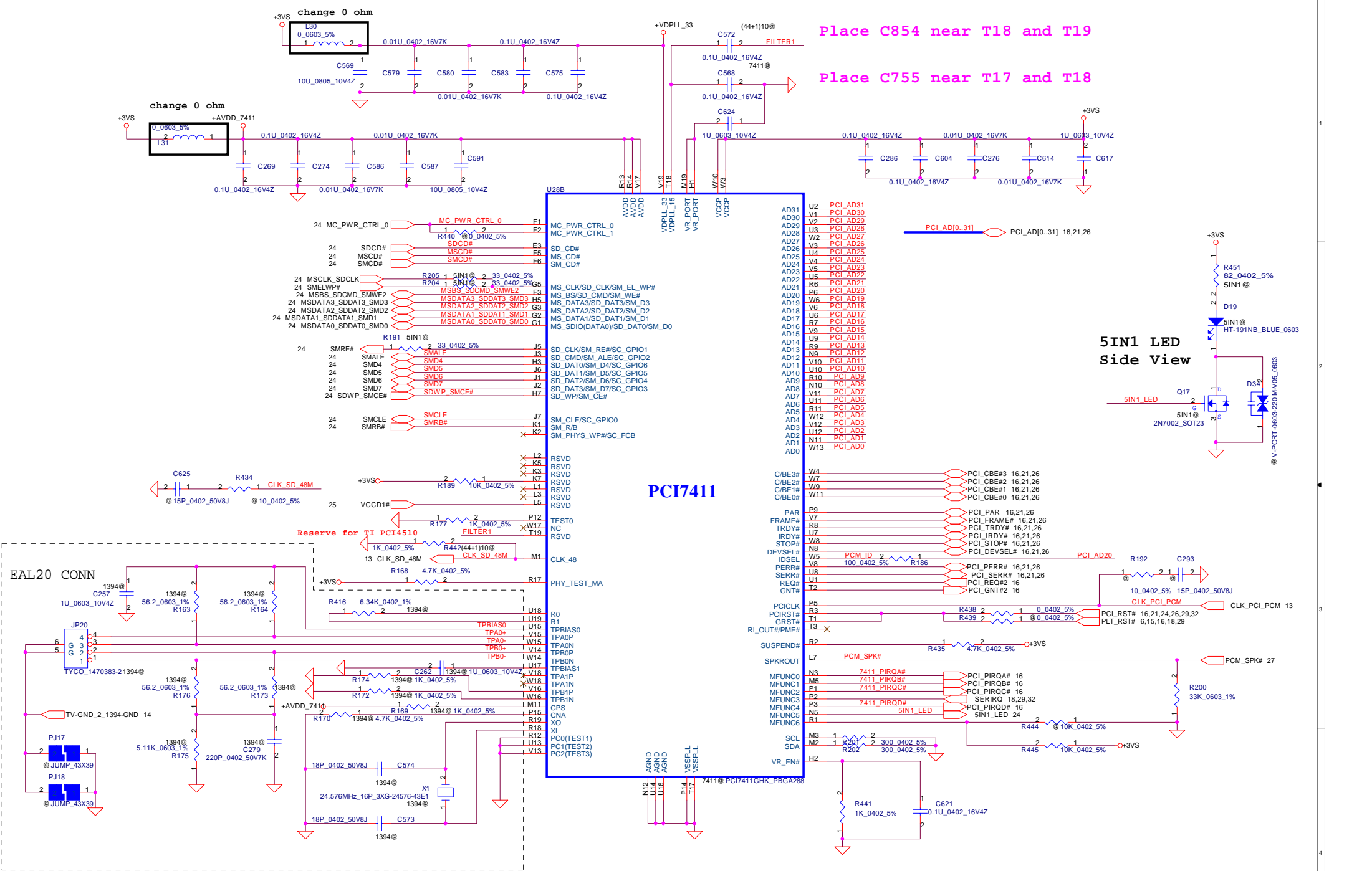
Security Classification	Compal Secret Data		Title	
Issued Date	2005/08/22	Deciphered Date	2008/08/22	SATAPATA-HDD, PATA ODD Connector
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# LAN RTL8100C(L)



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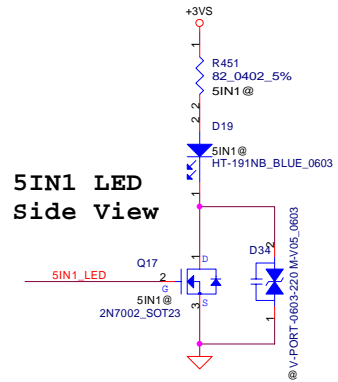




Place C854 near T18 and T19

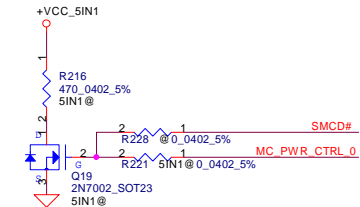
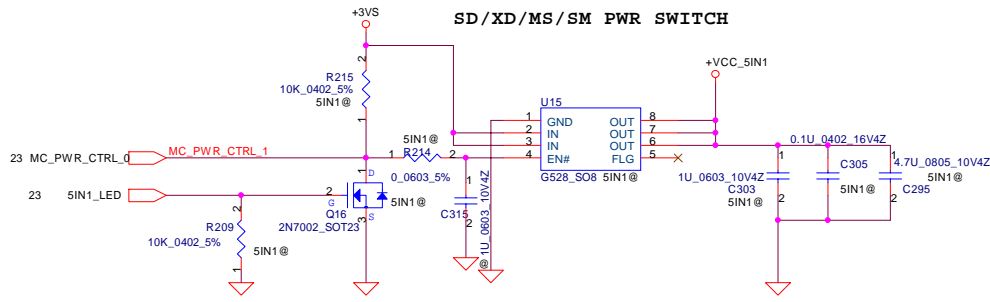
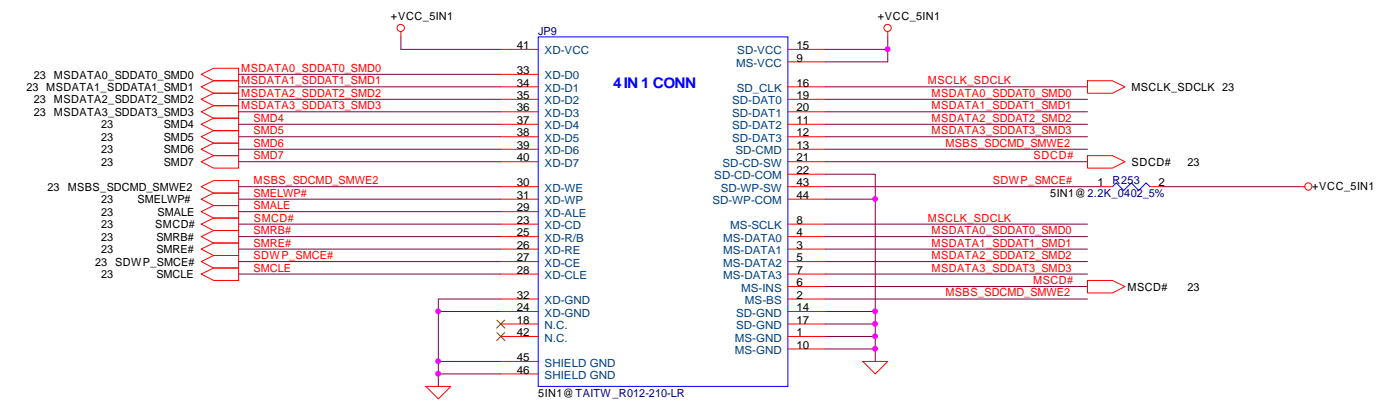
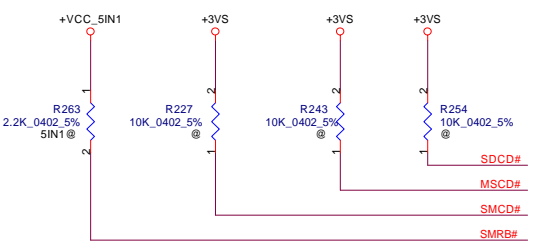
Place C755 near T17 and T18

5IN1 LED Side View

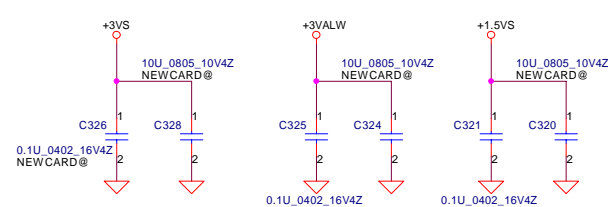
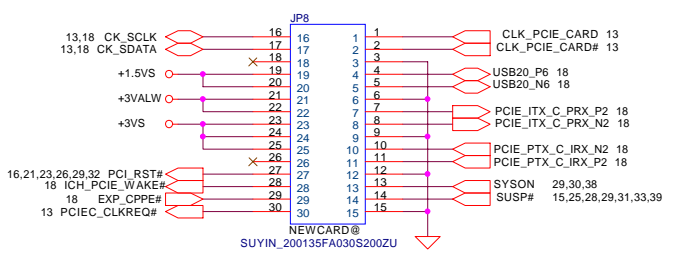


PCI1510 & PCI6411 UNMOUNT THOSE PARTS

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### New Card Connector



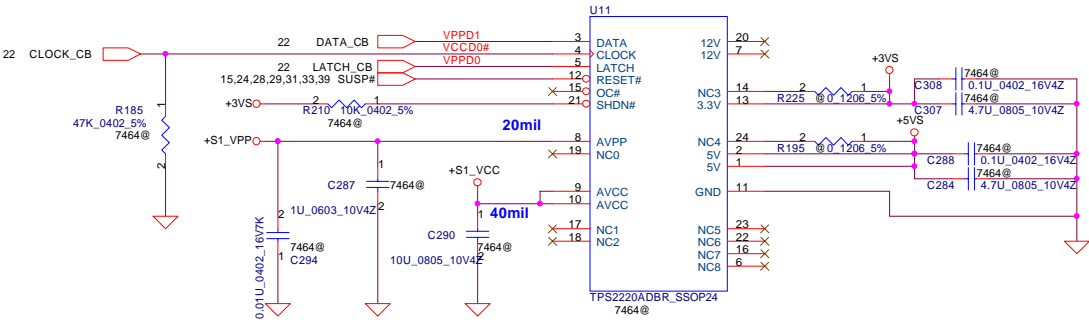
60mil I<sub>max</sub> = 1.35A  
 40mil I<sub>max</sub> = 0.275A  
 40mil I<sub>max</sub> = 0.75A

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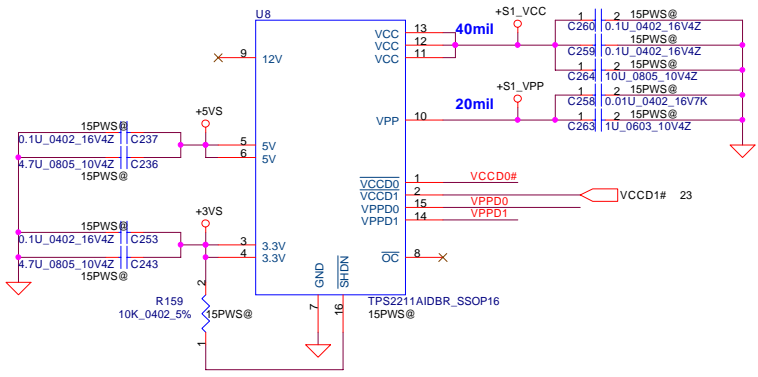


**Power Switch for PCMCIA**

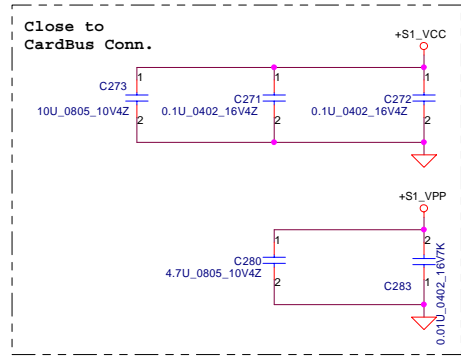
**Power Switch for PCMCIA (PCI7411 & PCI6411 only)**



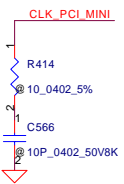
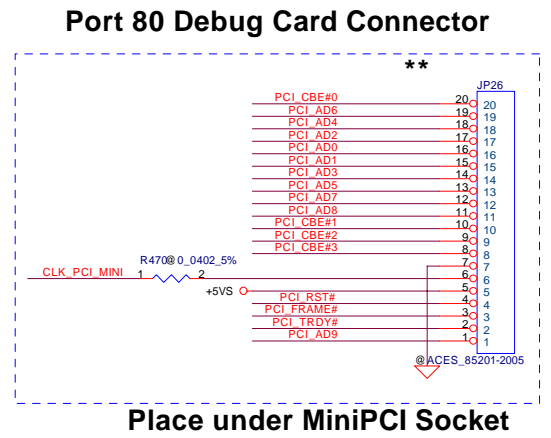
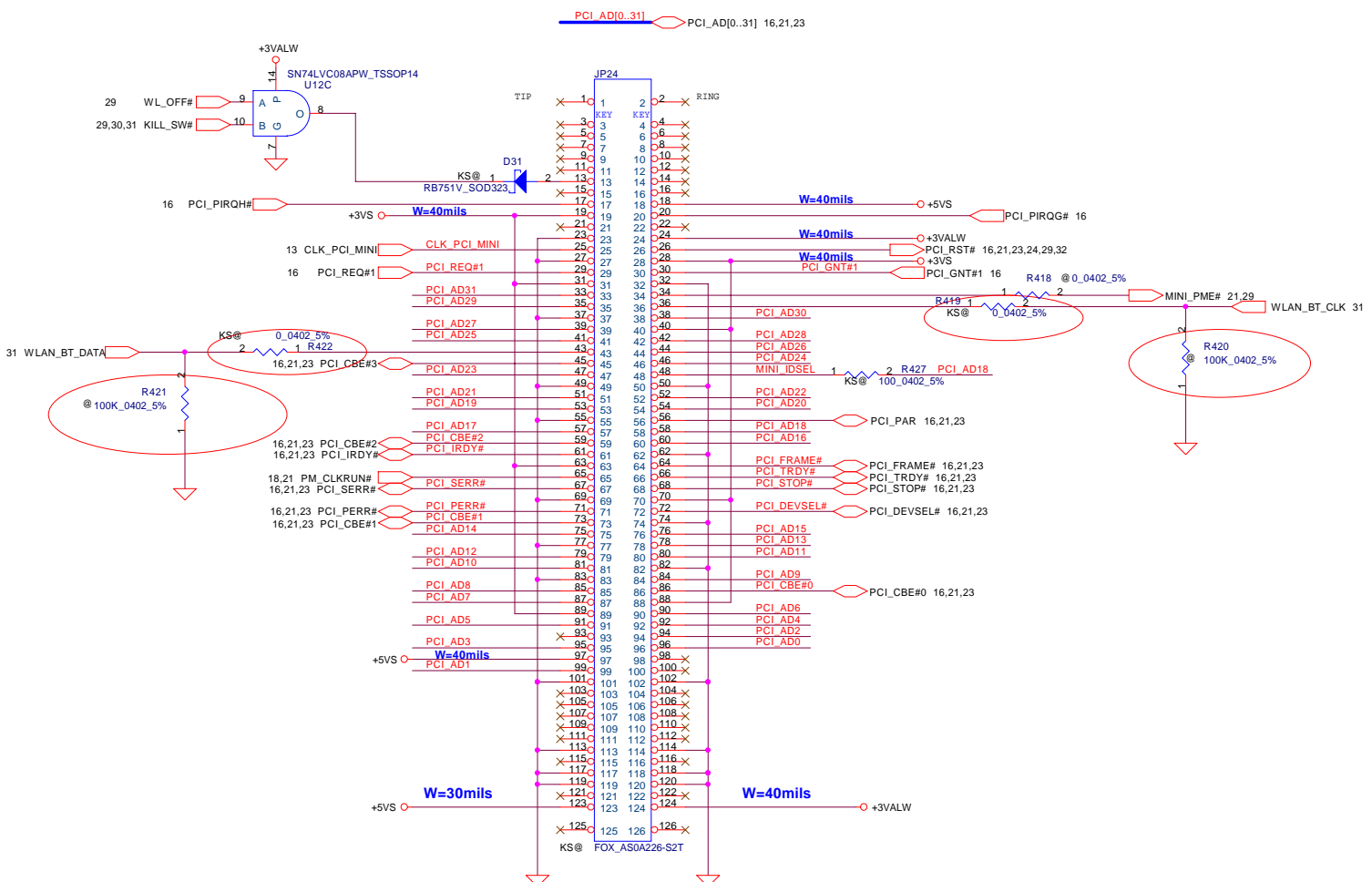
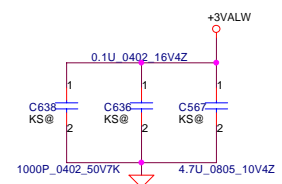
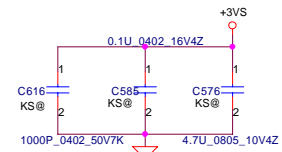
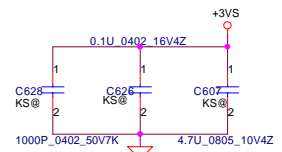
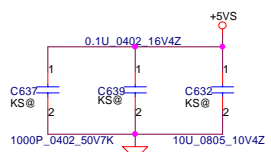
**Power Switch for PCMCIA (PCI1510 & PCI4510 only)**



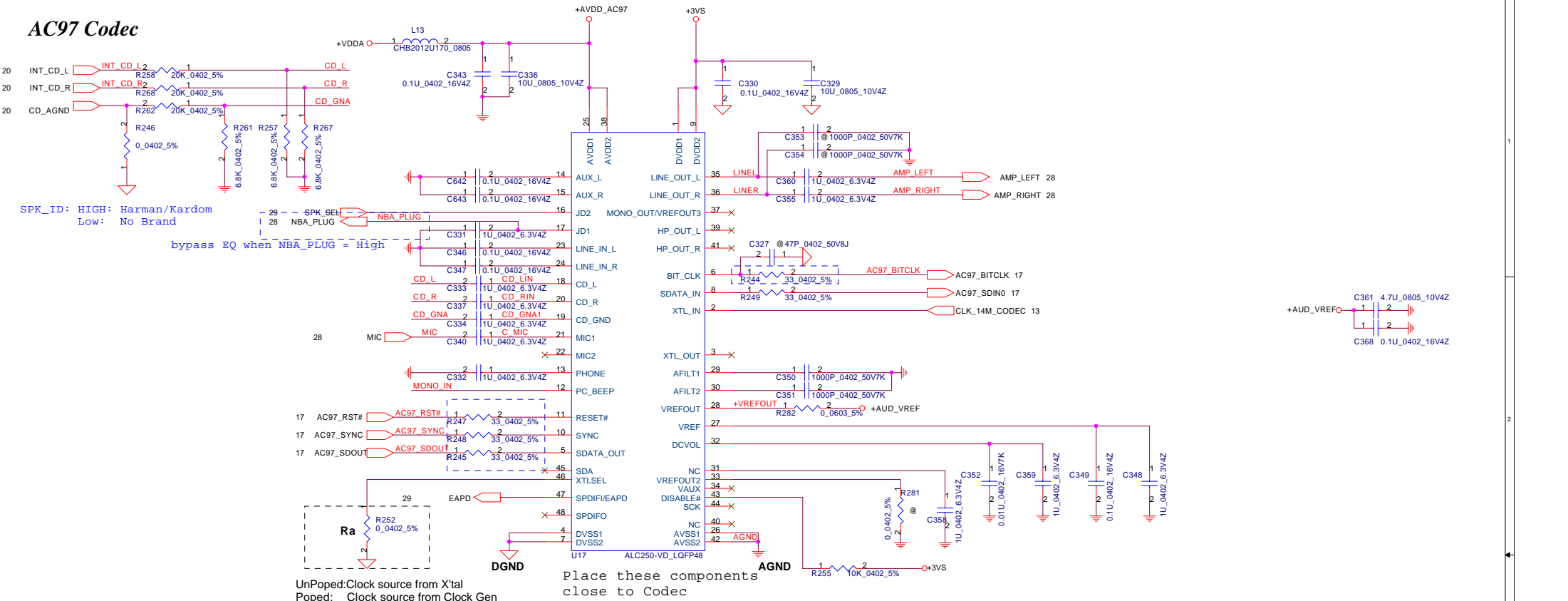
**CardBus Socket**



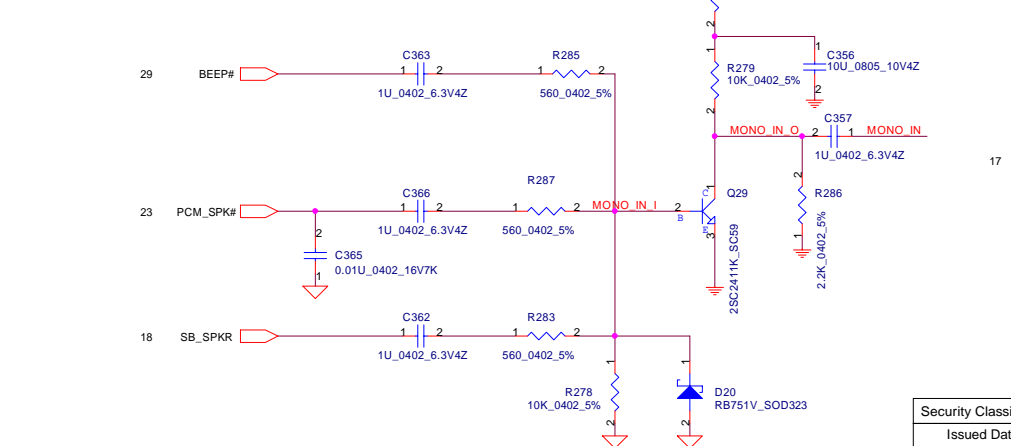
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Custom				1.0
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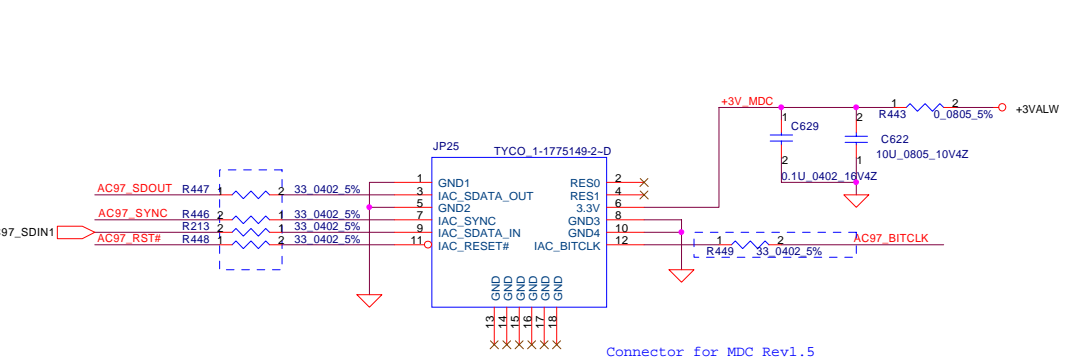
# AC97 Codec



## System Sound

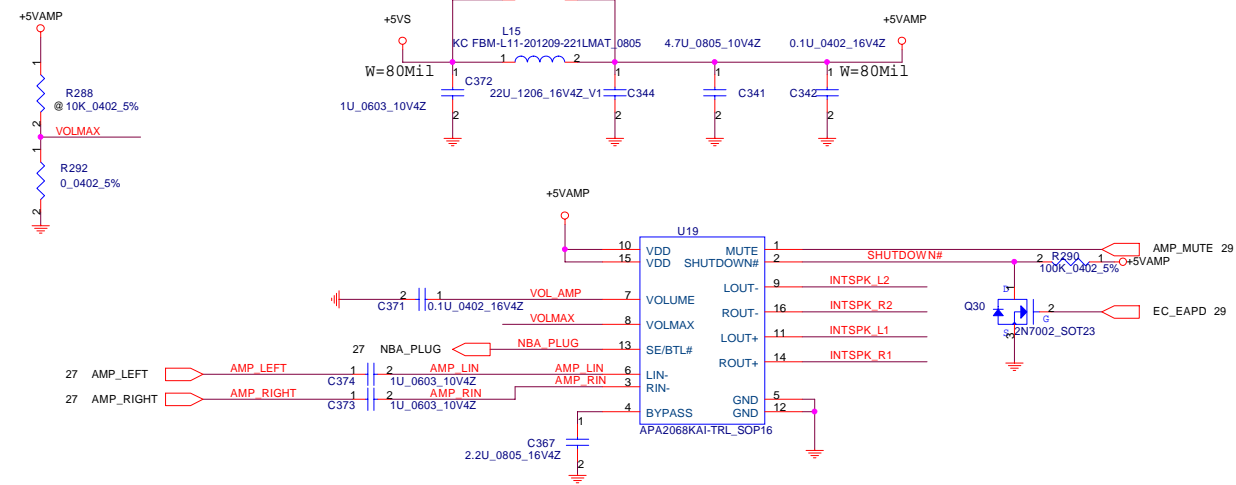


## MDC Connector

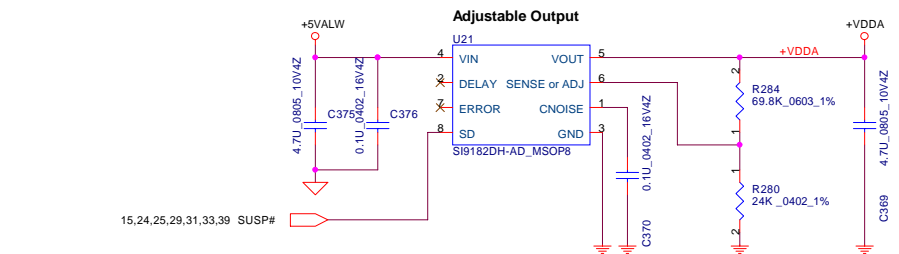


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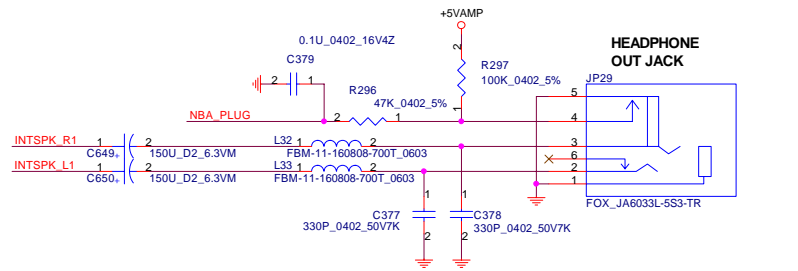
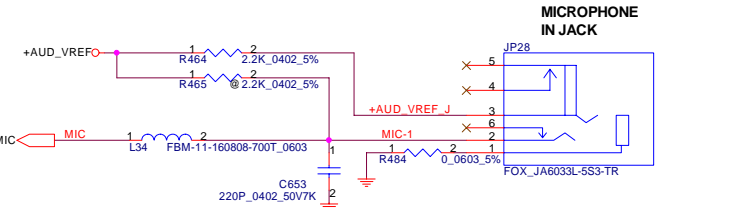
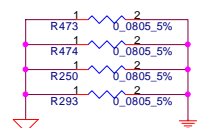
# Audio AMP



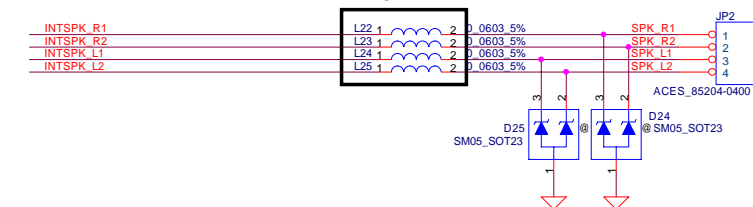
# Regulator for CODEC



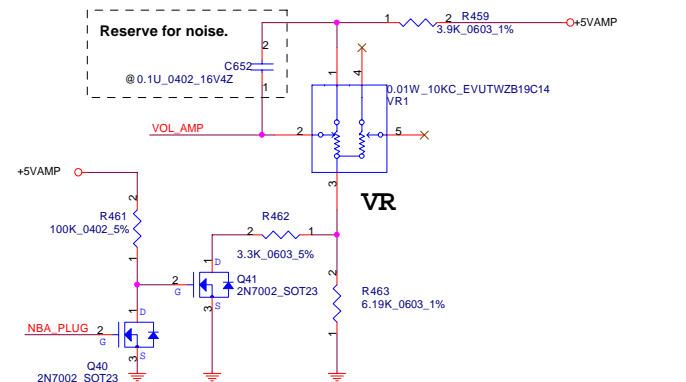
# Moat Bridge



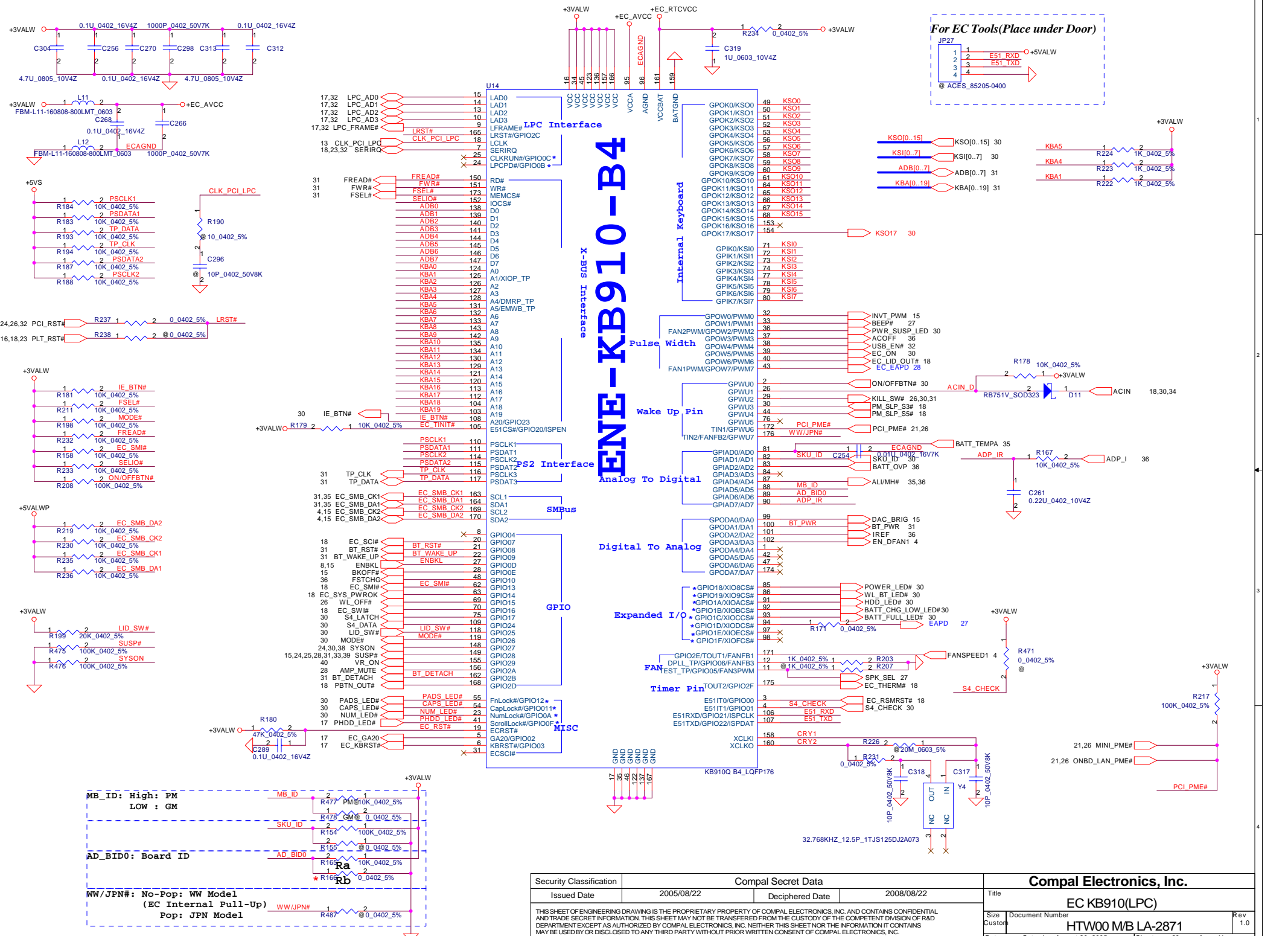
# Speaker Connector



# Variable Resistor



Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2005/08/22	Deciphered Date	2008/08/22	AMP/VR/Audio Jack		Size
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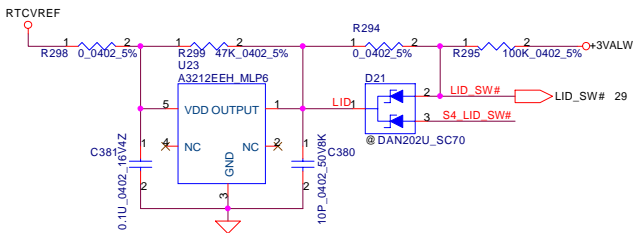


# ENE-KB910-B4

Security Classification	Compal Secret Data	
Issued Date	2005/08/22	Deciphered Date
		2008/08/22
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<b>Compal Electronics, Inc.</b>		
<b>EC KB910(LPC)</b>		
Title	HTW00 M/B LA-2871	
Size	Document Number	Rev
Custom		1.0
Date:	Saturday, August 20, 2005	Sheet 29 of 41

### Lid SW



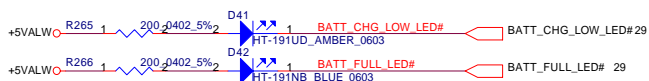
### WL&BT LED



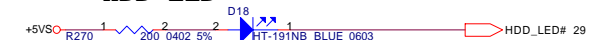
### POWER/ON(Green Pin2,1) Suspend (Amber Pin3,4) LED



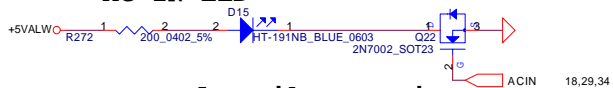
### BATTERY CHG(Green Pin2,1) BATTERY LOW(Amber Pin3,4) LED



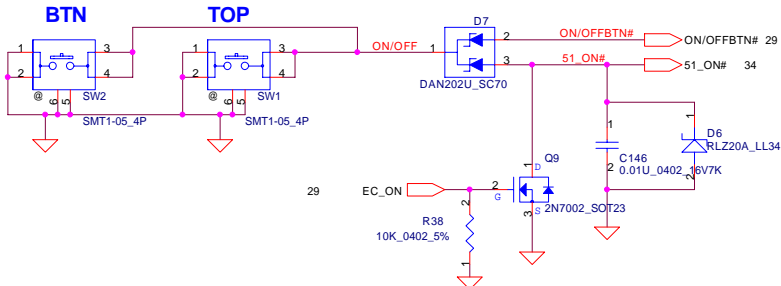
### HDD LED



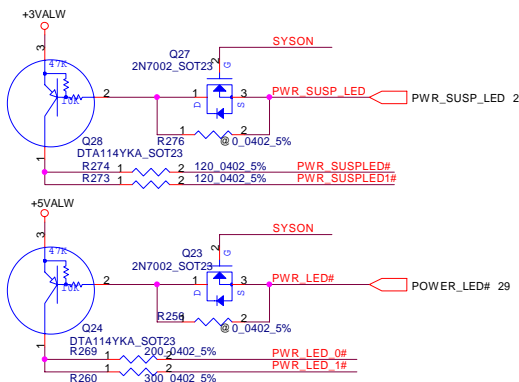
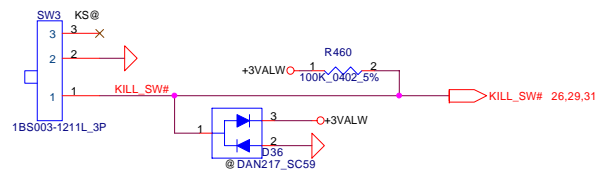
### AC IN LED



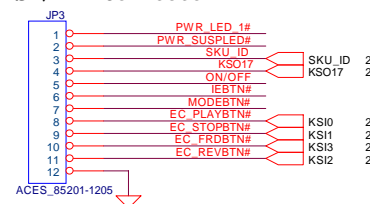
## ON/OFF BUTTON for debug only



### Kill SWITCH



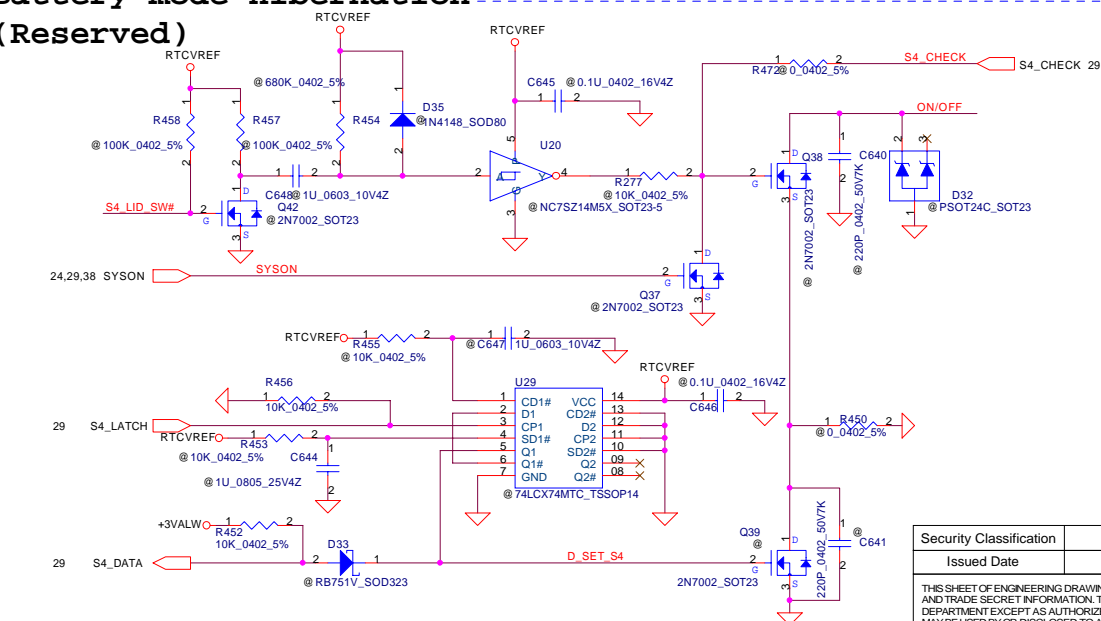
### SW/LED Connector



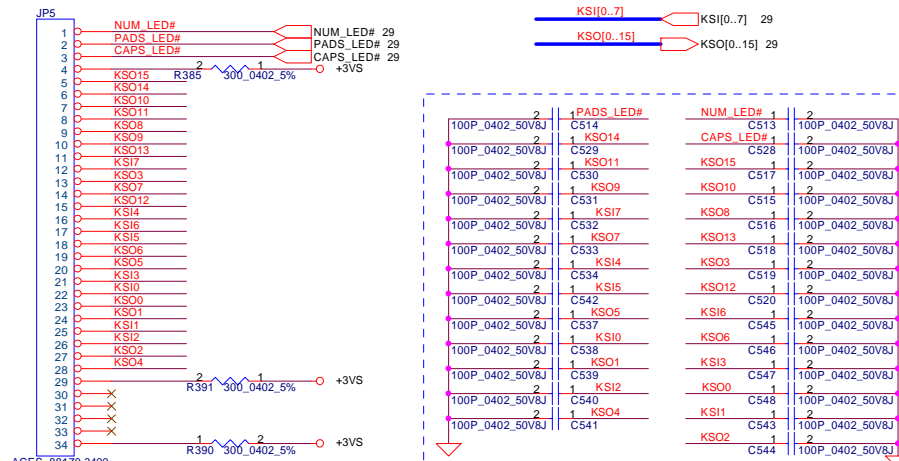
KSO17	C486	1	220P_0402_50V7K
ON/OFF	C485	1	220P_0402_50V7K
PWR_LED_1#	C488	1	220P_0402_50V7K
PWR_SUSPLED#	C487	1	220P_0402_50V7K
IEBTN#	C482	1	220P_0402_50V7K
MODEBTN#	C479	1	220P_0402_50V7K
EC_EVBTN#	C470	1	220P_0402_50V7K
EC_FRDBTN#	C473	1	220P_0402_50V7K
EC_PLAYBTN#	C478	1	220P_0402_50V7K
EC_STOPBTN#	C477	1	220P_0402_50V7K

For EMI Request

## Battery mode Hibernation (Reserved)



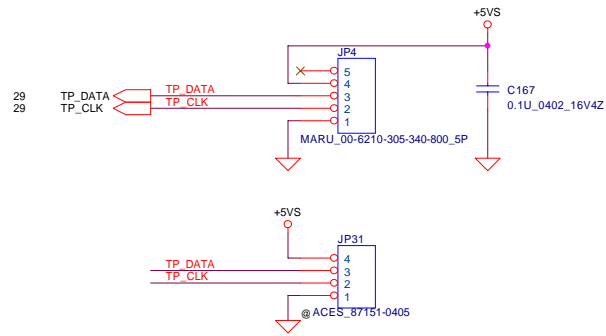
### KEYBOARD CONN.



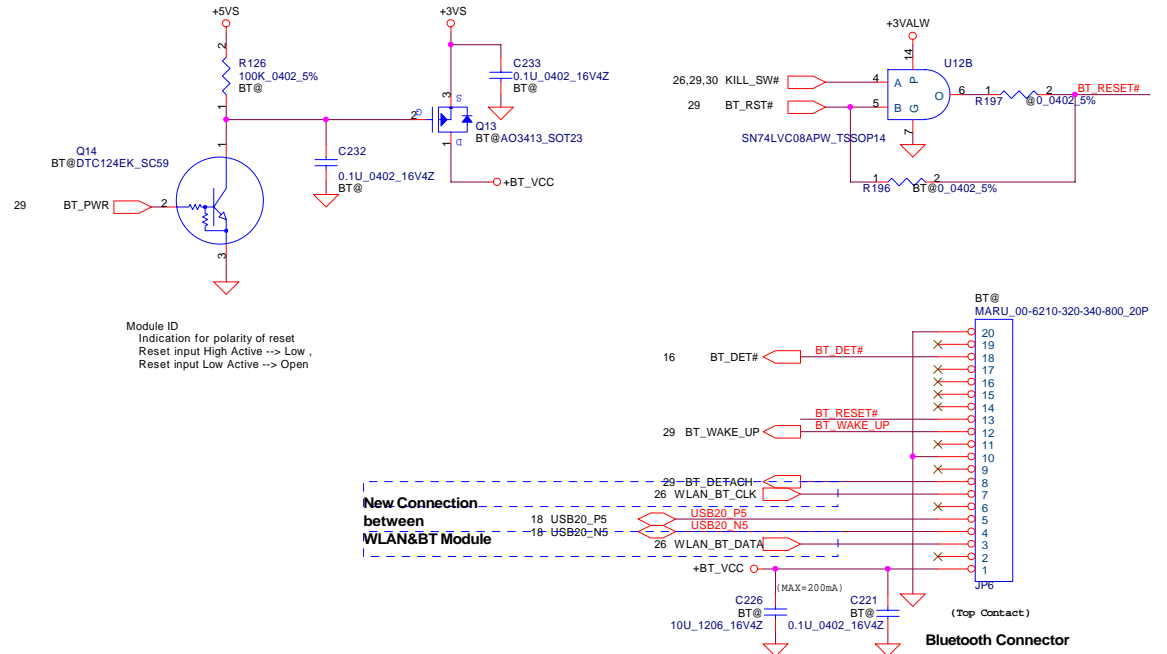
For EMI Request

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Size	Document Number	HTW00 M/B LA-2871		Rev 1.0
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**TP CONN.**

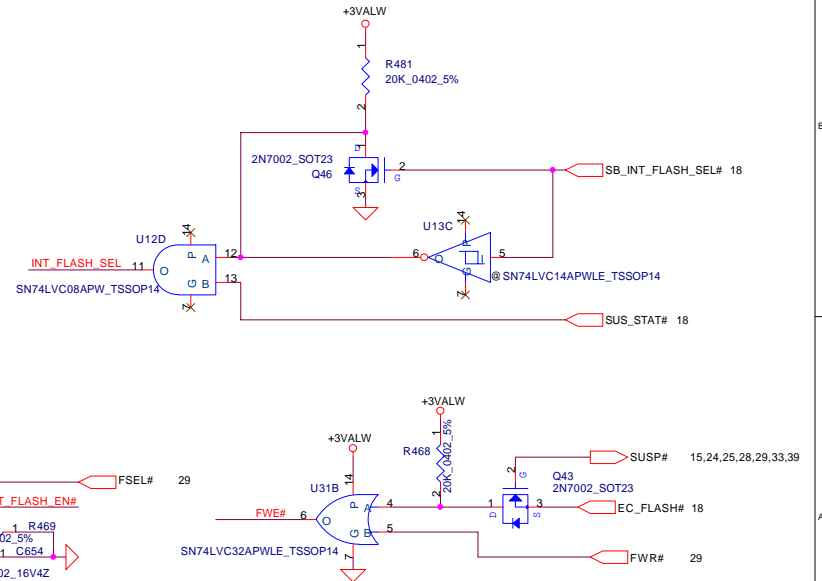
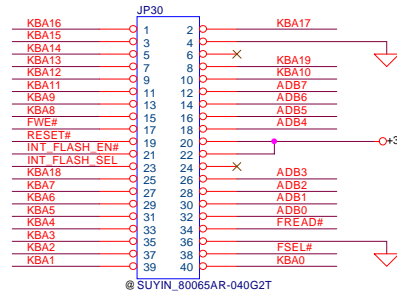
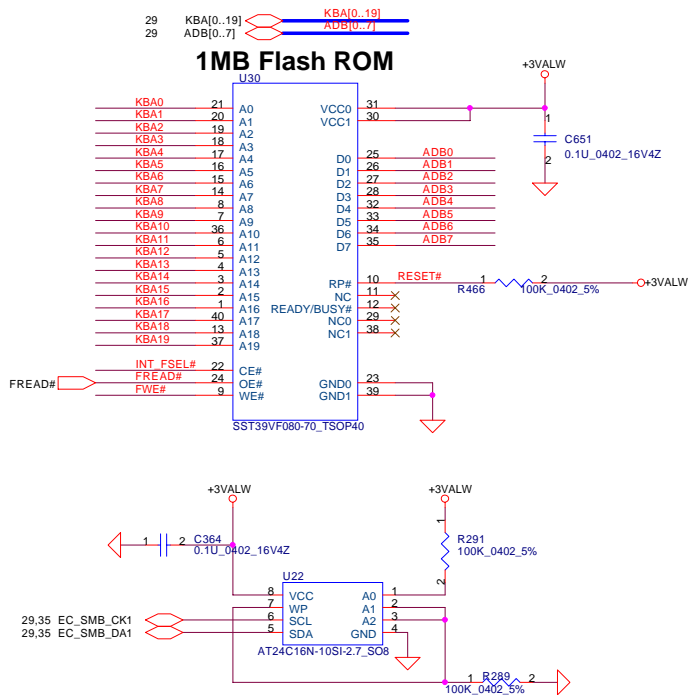


**BlueTooth Interface**

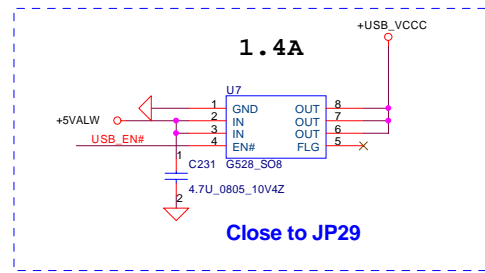
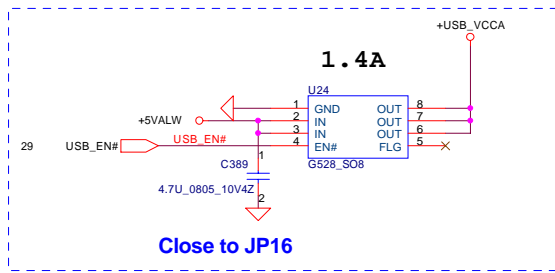


**1MB Flash ROM**

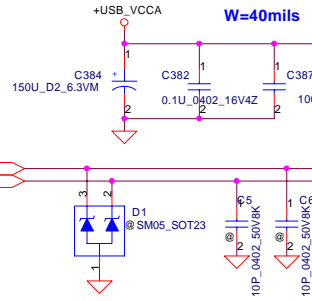
**1MB ROM Socket**



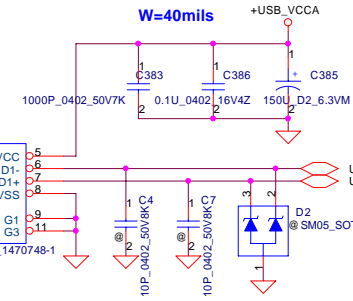
Security Classification	Compal Secret Data		Title	<b>Compal Electronics, Inc.</b>	
Issued Date	2005/08/22	Deciphered Date		2008/08/22	1MB BIOS/ TP Conn/ BT Conn
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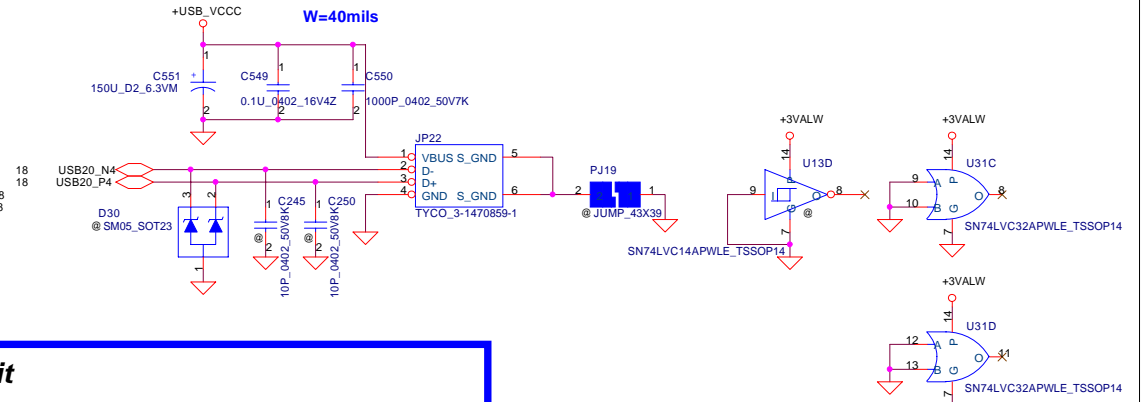
**USB CONN. 1**



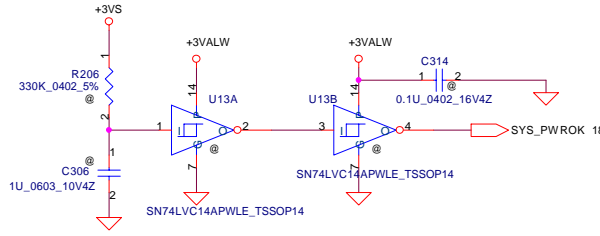
**USB CONN. 2**



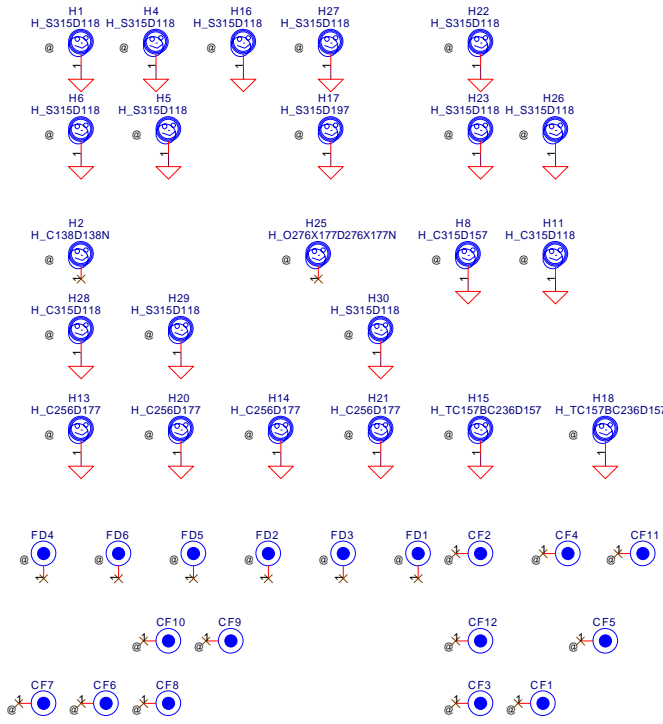
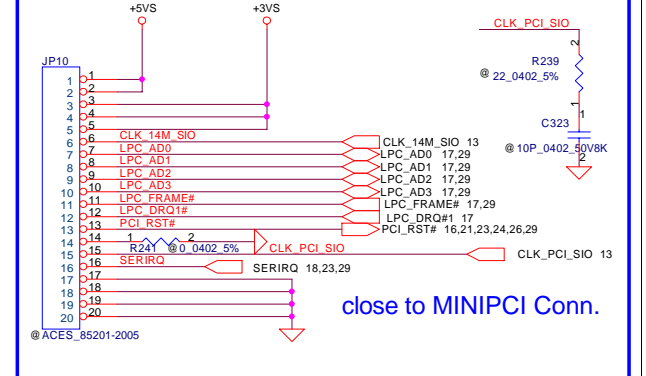
**USB CONN. 3**



**Power OK Circuit**



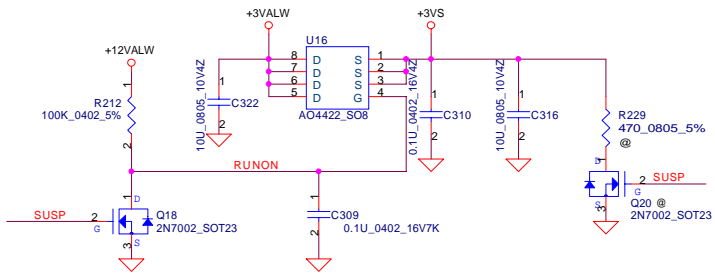
**LPC Debug Port**



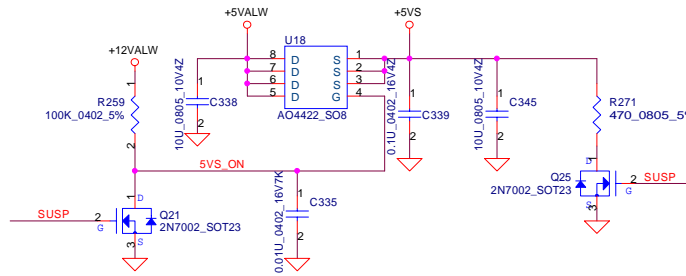
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/08/22	Deciphered Date	2008/08/22	Title	
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Date:		Saturday, August 20, 2005		Sheet 32 of 41	



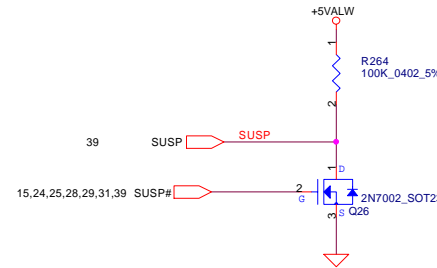
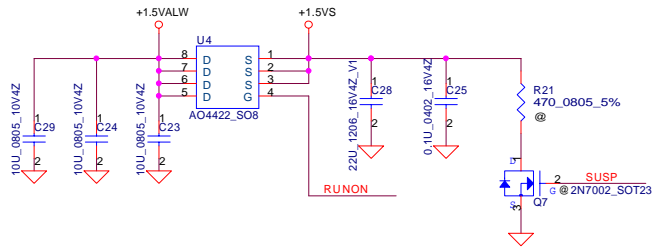
### +3VALW to +3VS Transfer



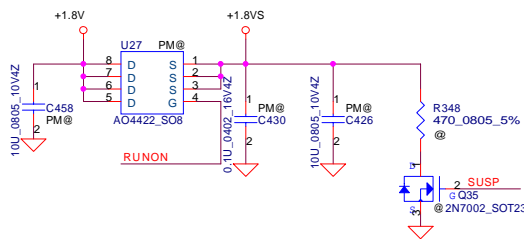
### +5VALW to +5VS Transfer



### +1.5VALW to +1.5VS Transfer

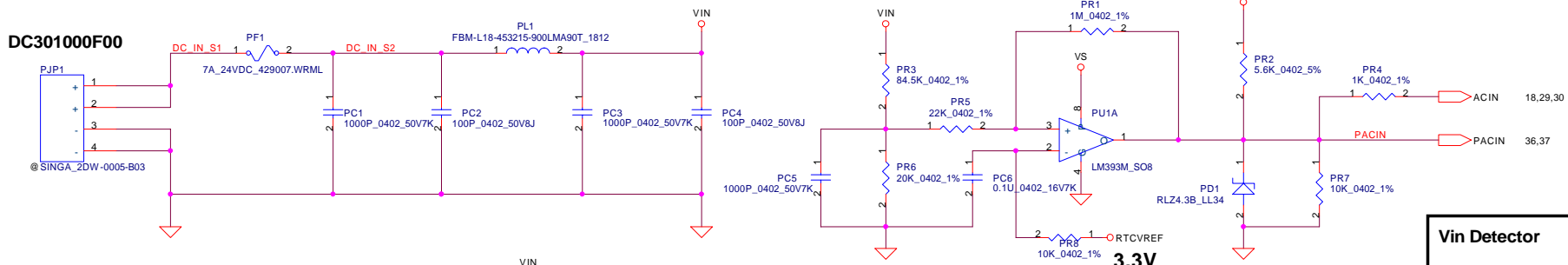


### +1.8V to +1.8VS Transfer

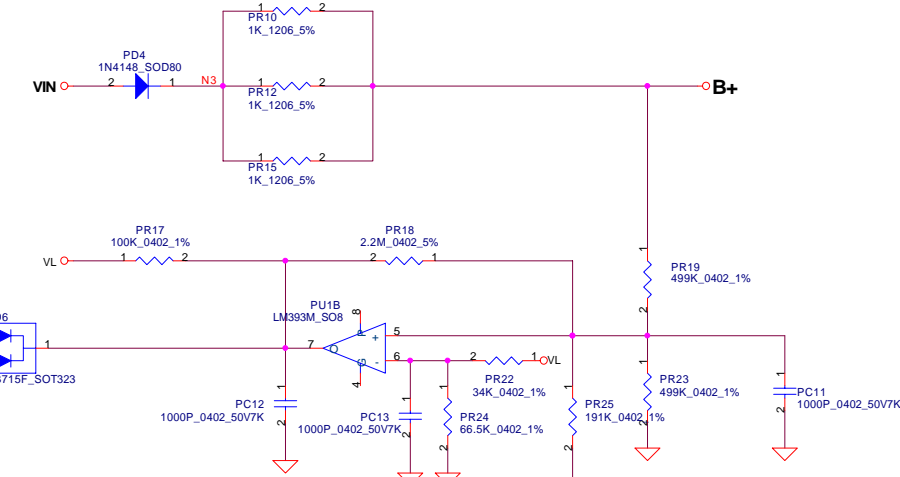
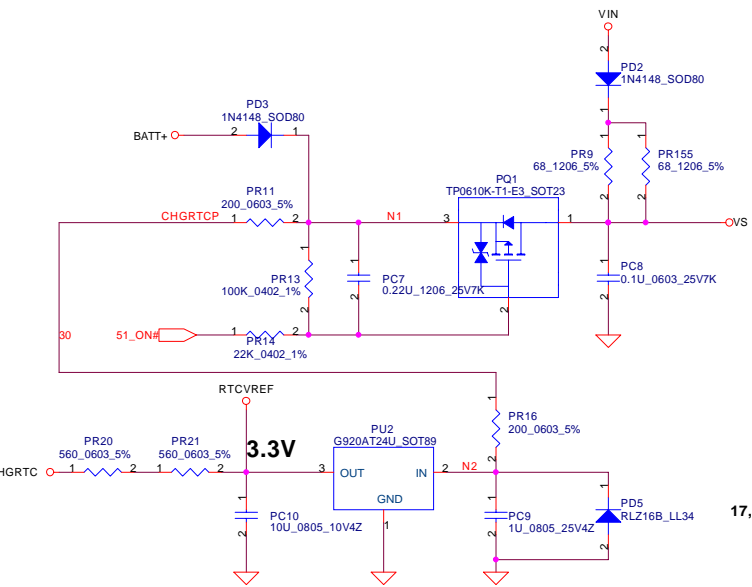


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Issued Date	2005/08/22	Deciphered Date	2008/08/22	Title
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Size	Document Number	HTW00 M/B LA-2871		Rev 1.0
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**DC301000F00**

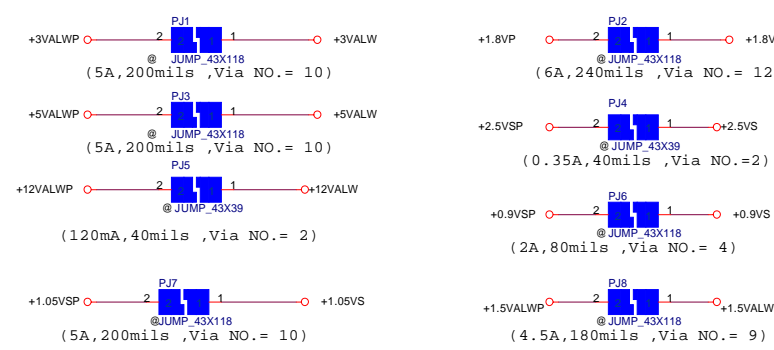


Vin Detector		
High	18.384	17.901 17.430
Low	17.728	17.257 16.976

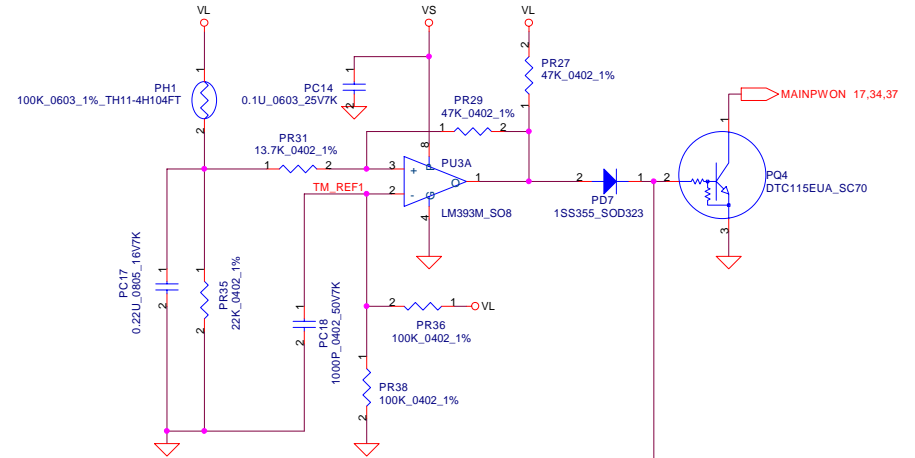
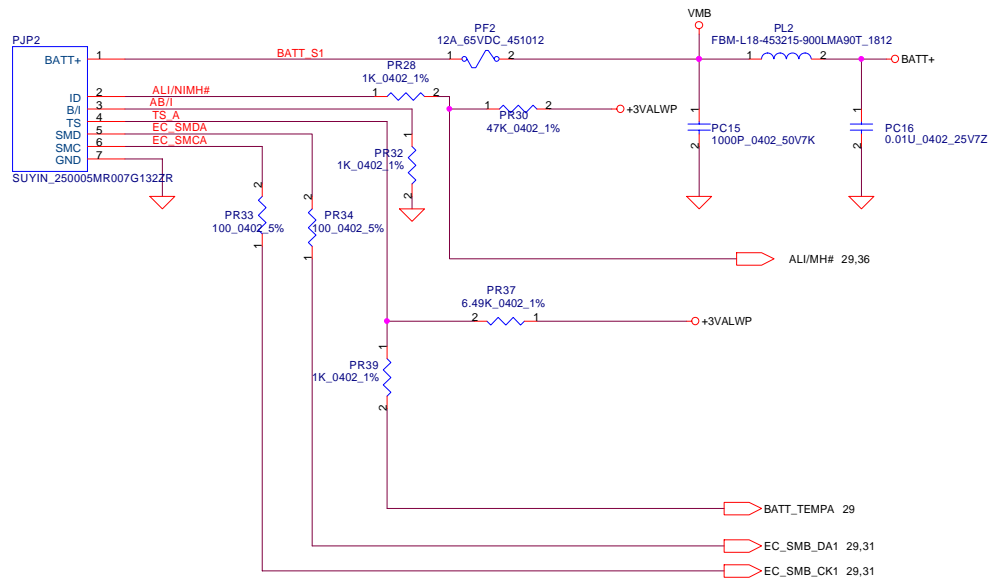


17,35,37 MAINPWON  
36 ACON

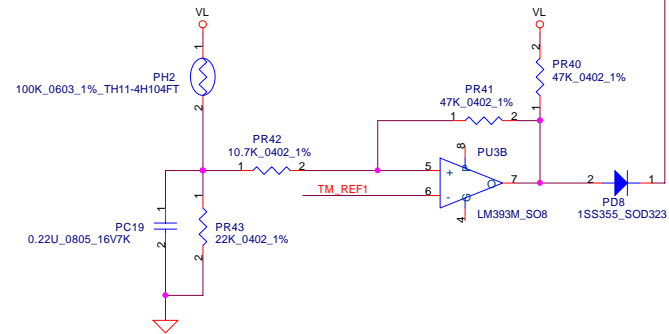
**Precharge detector  
15.97V/14.84V FOR  
ADAPTOR**



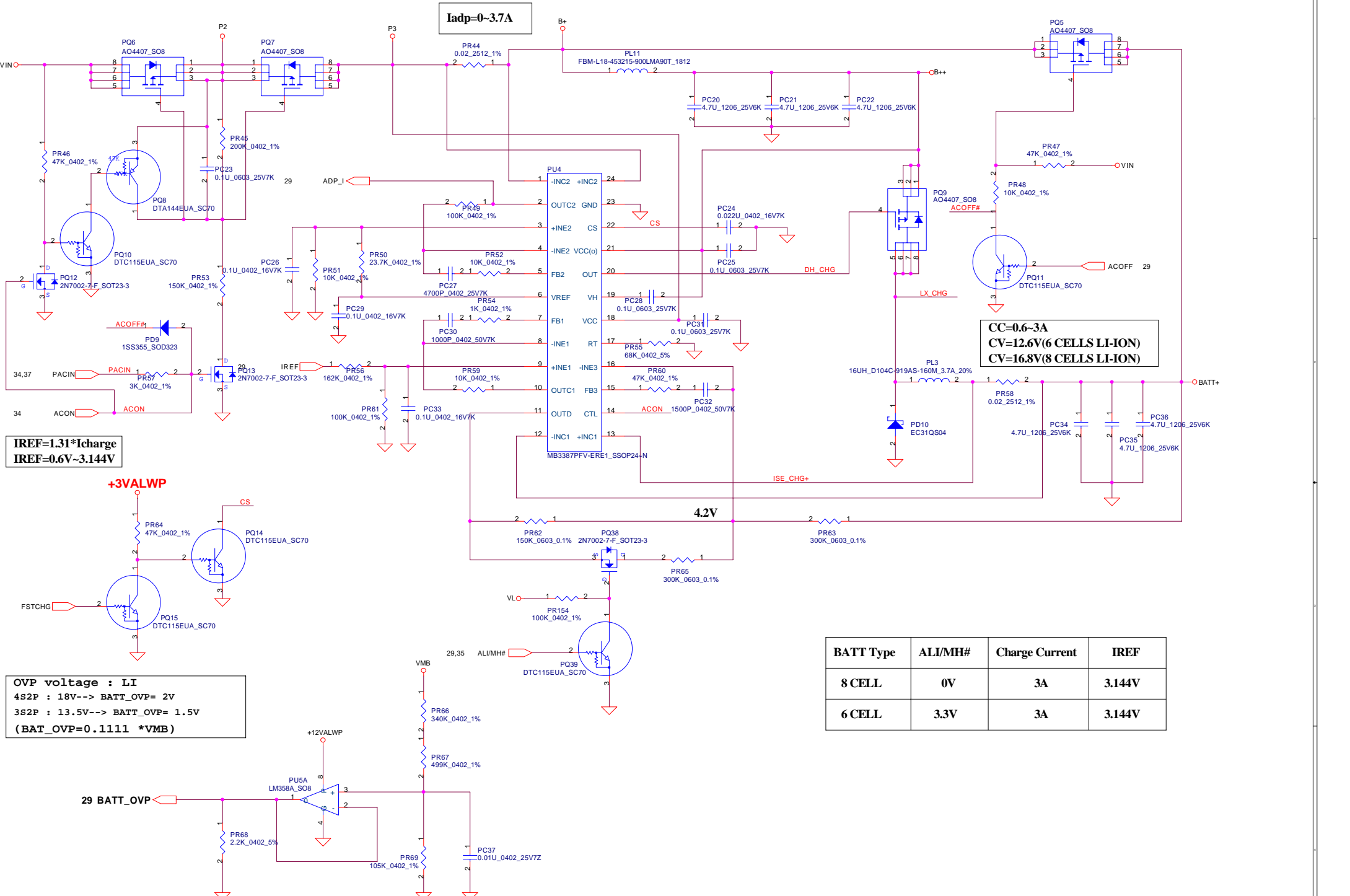
**PH1 under CPU botten side :**  
 CPU thermal protection at 84 degree C  
 Recovery at 45 degree C



**PH2 near main Battery CONN :**  
 BAT. thermal protection at 79 degree C  
 Recovery at 45 degree C



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Issued Date	2005/08/22	Deciphered Date	2008/08/22	Title	BATTERY CONN / OTP
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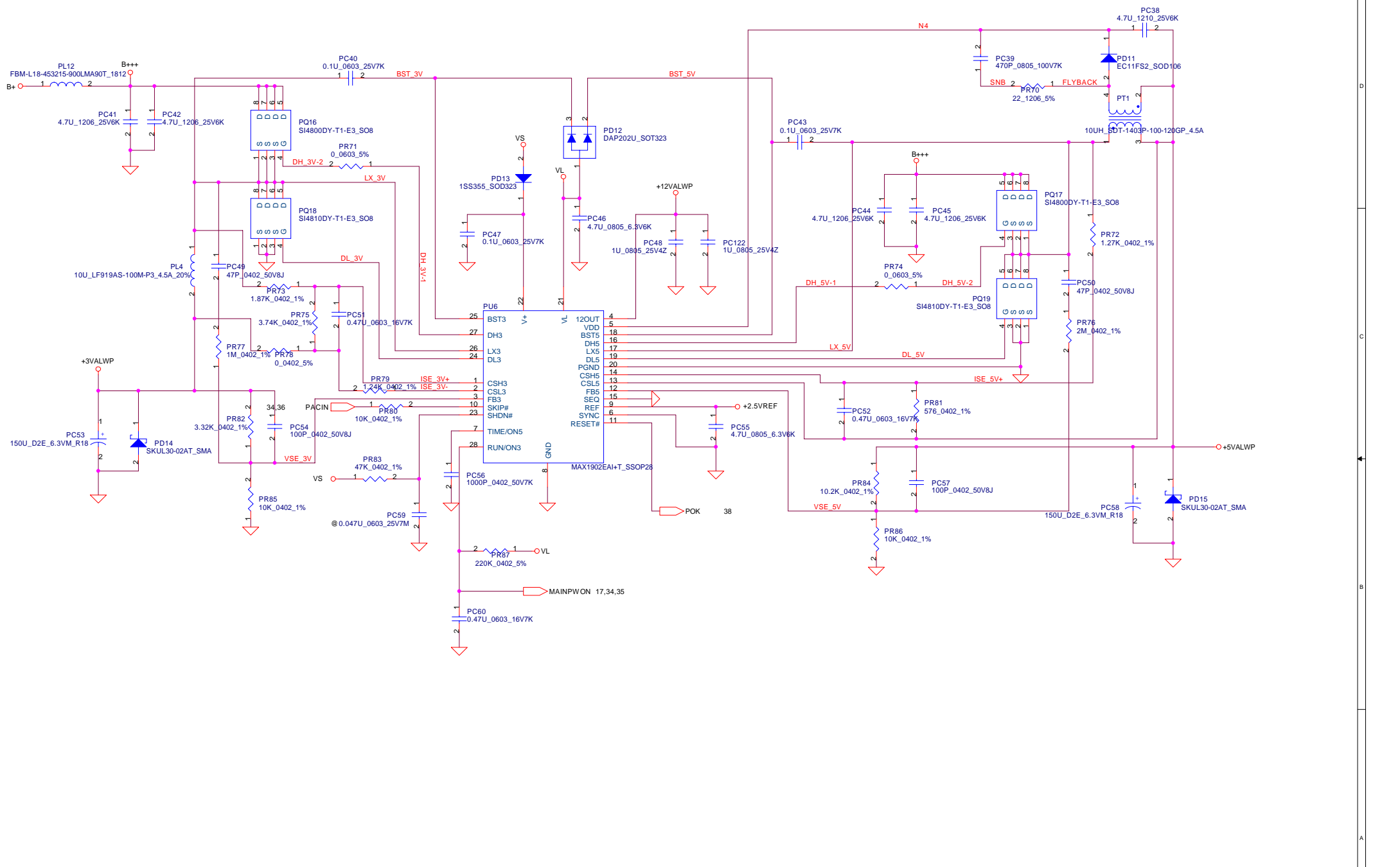


**IREF=1.31\*Icharge**  
**IREF=0.6V~3.144V**

**OVP voltage : LI**  
**4S2P : 18V--> BATT\_OVP= 2V**  
**3S2P : 13.5V--> BATT\_OVP= 1.5V**  
**(BATT\_OVP=0.1111 \*VMB)**

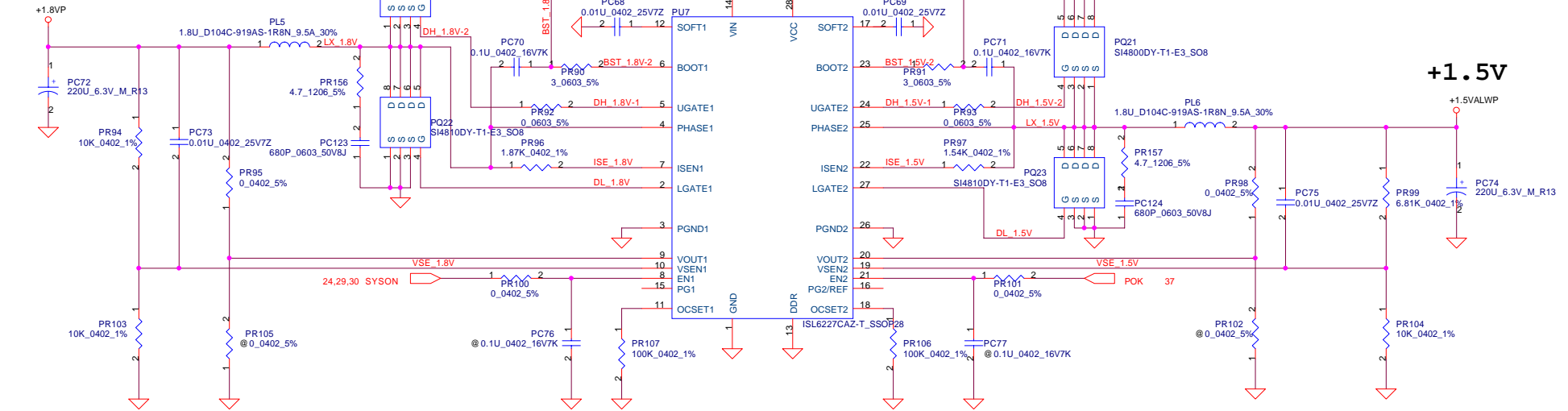
BATT Type	ALI/MH#	Charge Current	IREF
8 CELL	0V	3A	3.144V
6 CELL	3.3V	3A	3.144V

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Size	Document Number			Rev	
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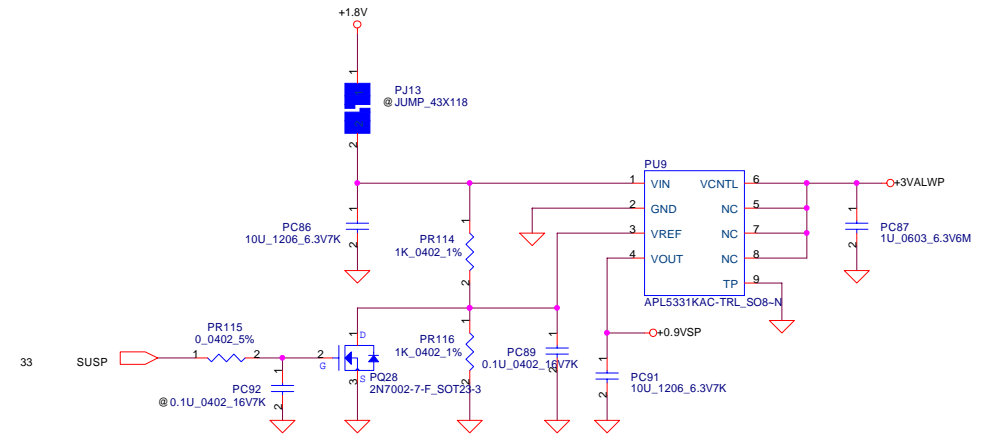
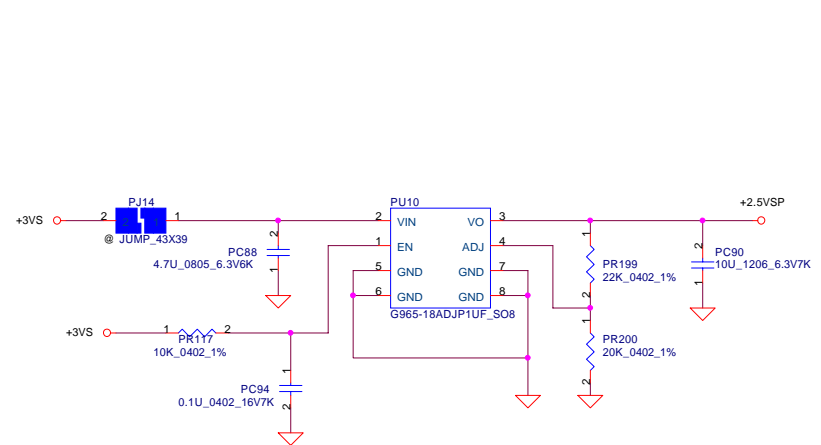
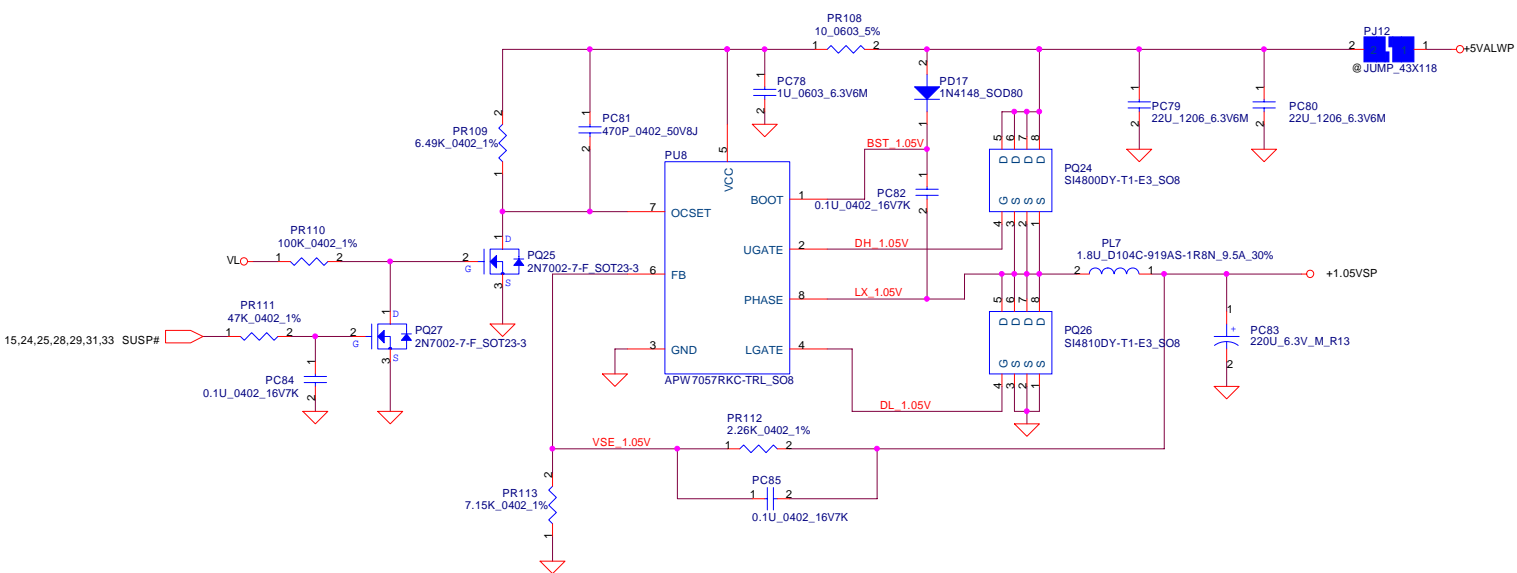


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**+1.8V**



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Issued Date	2005/08/22	Deciphered Date	2008/08/22	2.5V / 0.9V / 1.05V	
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# POWER PIR LIST

page	Reason for change	Modify list
DVT 36,37, 38,40	For EMI request to reduce the power board band	Add bead PL11,PL12,PL13(SM010020720), add snubber 4.7ohm(SD001470B80)PR131,PR151 and 680P(SE024681J80)PC108,PC120 on CPU CORE
		Add booster resistor 3ohm(SD013300B80) PR90,PR91 on 1.8V/1.5V and PR124,PR145 on CPU CORE
47	Reduce the high frequency noise	Change PC38 to 4.7U_1210(SE065475K80)
34	Add design margine	Add 68ohm(SD011680A80) PR155 and change PR9 to 68ohm
PVT 39	Change +2.5VSP enable signal for HW request	Change +2.5VSP enable signal to +3VS
40	For EMI request to reduce CPU power board band	Change PQ30,PQ34 to IRF7821(SB578210010); PQ31,PQ35 to IRF7832(SB578320010)
40	For cost down	del PC100 and PR122,PR123,PR125,PR127,PR129,PR130

# HW PIR LIST

HTW00 LA-2871 SCHEMATIC CHANGE LIST  
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	5/30	P29	ADD PULL DOWN 100K_0402_5% R475 ON SUSP#	TO PREVENT SUSP# FLOATING
2	5/30	P29	ADD PULL DOWN 100K_0402_5% R476 ON SYSON	TO PREVENT SYSON FLOATING
3	6/14	P17	CHANGE C241,C251 FROM 18PF TO 15PF	FINE TUNE RTC TIMING
4	7/01	P30	CHANGE LED TYPE FROM SIDE VIEW TO TOP VIEW	UPDATE LED LIBRARY
5	7/01	P30	CHANGE KB CONNECTOR EMI CAPS TO MOUNT	FOR EMI REQUEST
6	7/01	P27	ADD SPK_SEL CONNECTION BETWEEN EC AND CODEC	FOR CODEC EQ SELECTION FOR SPEAKER
7	7/01	P29	ADD MB_ID R477,R478 ON PIN88	FOR EC MB IDENTIFY
8	7/01	P17	CHANGE SATA DC COUPLING CAPS CAPACITANCE TO 3.9nf	TO MEET INTEL CRB RECOMMAND VALUE
9	7/01	P30	CHANGE LED RESISTOR R265, R266, R270, R272, RESISTANCE	TO INCREASE LED BRIGHTNESS
10	7/01	P20	ADD SATA HDD POWER CONTROL CIRCUIT	TO RESERVE BACKUP SOLUTION FOR SATA HDD RESET
11	7/01	P28	ADD R484 FOR MIC JACK GROUND PIN CLEAN	TO IMPROVE MIC SOUND QUALITY
12	7/01	P28	CHANGE U21 LDO POWER SOURCE FROM +5VALW TO +5VS	FOR POWER TRACE LAYOUT IMPROVE

HTW00 LA-2871 SCHEMATIC CHANGE LIST  
REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	8/6	P28	CHANGE U21 PIN 4 FROM +5VS TO +5VALW	TO PREVENT NOISE FROM HDD SPIN UP
2	8/6	P15	CHANGE R306, R307 FROM RES TO BEAD	FOR EMI REQUEST
3	8/6	P21	CHANGE U2 FROM H-50P (H=2mm) TO TS6121C (H=4mm)	FOR COST POINT OF VIEW
4	8/6	P23	CHANGE D19 LED COLOR FROM GREEN TO BLUE	CUSTOMER SPEC CHANGE
5	8/6	P09	ADD R488 0_0603 BETWEEN +2.5VS_CRTDAC TO +2.5VS	TO IMPROVE CRT VIDEO QUALITY
6	8/6	P29	ADD PULL HIGH RES R487 ON PIN176 FOR WW/JPN# SELECT	TO CONTROL M/B CONFUIRATION
7	8/6	P30	CHANGE D15,D18,D40,D42 LED COLOR FROM GREEN TO BLUE	CUSTOMER SPEC CHANGE

HTW00 LA-2871 SCHEMATIC CHANGE LIST  
REVISION CHANGE: 0.3 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	8/22	P20	CHANGE C661,C662,Q44,Q45,Q47,Q48,R411,R479,R480,R482,R483 FROM MOUNT TO RESERVE	REMOVE SATA-HDD POWER RESET FUNCTION FOR SW REQUEST
		P18	CHANGE D38,R485 FROM MOUNT TO RESERVE	
2	8/22	P28	CHANGE R459 RESISTANCE FROM 4.53K TO 3.9K CHANGE R463 RESISTANCE FROM 4.22K TO 6.19K CHANGE R462 RESISTANCE FROM 4.87K TO 3.3K	TO REDUCE HEAD PHONE GAIN SETTING
3	8/22	P31	CHANGE JP4 AND JP6 VENDOR FROM ACES TO MANUNIX	FOR CUSTOMER'S REQUEST
4	8/22	P31	RESERVE JP31	FOR TEST ABILITY

PROPRIETARY NOTE

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Issued Date	2005/08/22	Deciphered Date	2008/08/22			
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