KSWAA/KTWAA

Liverpool 10M/10MG

Sunderland 10M/10MG

LA-4982P REV 1.0 Schematic

Intel Penryn/ Cantiga/ ICH9M

2009-07-27 Rev. 1.0

Security Classification	Compal Secret Data		
Issued Date	2009/07/22	Deciphered Date	2012/07/22

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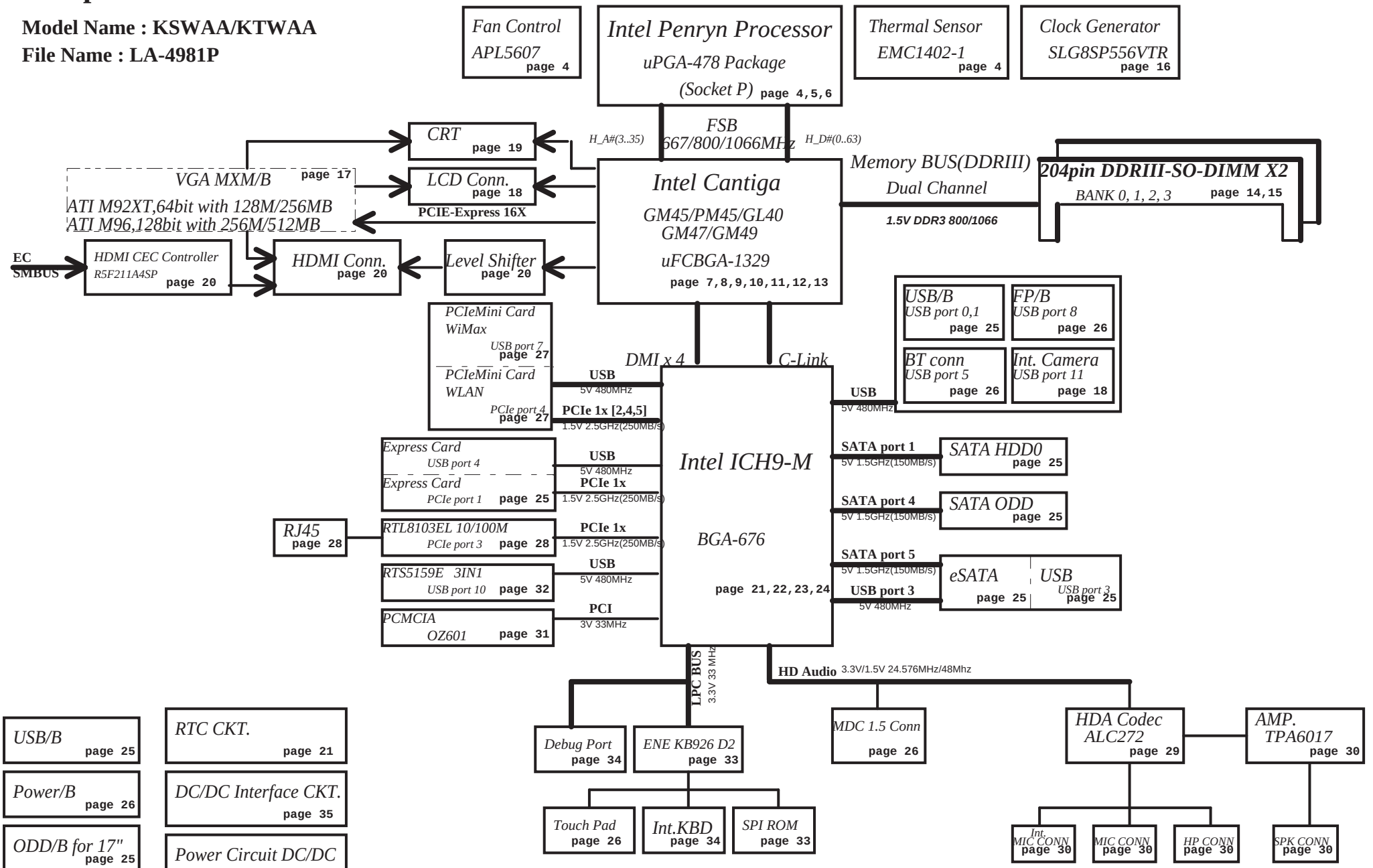
Compal Confidential

Model Name : KSWAA/KTWAA
File Name : LA-4981P



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8V power rail for VRAM	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+3VS_HDP	3.3V power rail for G-sensor	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

External PCI Devices

DEVICE	PCI DEVICE ID	IDSEL#	REQ/GNT#	PIRQ
CARD BUS	D4	AD20	1	A/B

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

BTO Option Table

Function	Express Card/ PCMCIA		Bluetooth	RJ11	Camera	3D Sensor
description	(E)	(A)	(B)	(R)	(X)	(S)
explain	Express Card	PCMCIA	Bluetooth	MDC	Camera	3D Sensor
BTO	NEW@	PCM@	BT@	MDC@	CAM@	GSENSOR@

Function	HDMI				
description	(Y)				
explain	Intel(UMA)	ATI VGA/B		COMMON	
BTO	IHDMI@	NIHDMI@	HDMI@	H@	

EC SM Bus1 address

Power	Device	Address
+5VL	EC KB926 D2	
+5VL	Smart Battery	0001 011X b
+5VL	HDMI-CEC	0011 010x b

EC SM Bus2 address

Power	Device	Address
+3VS	EC KB926 D2	
+3VS	CPU THM Sen SMSC SMC1402	1001 101Xb
+3VS	VGA THM Sen ADM1032ARMZ	1001 100Xb
	VGA on die thermal sensor	1001 111Xb (No used)

ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb
+3VS	Express Card	

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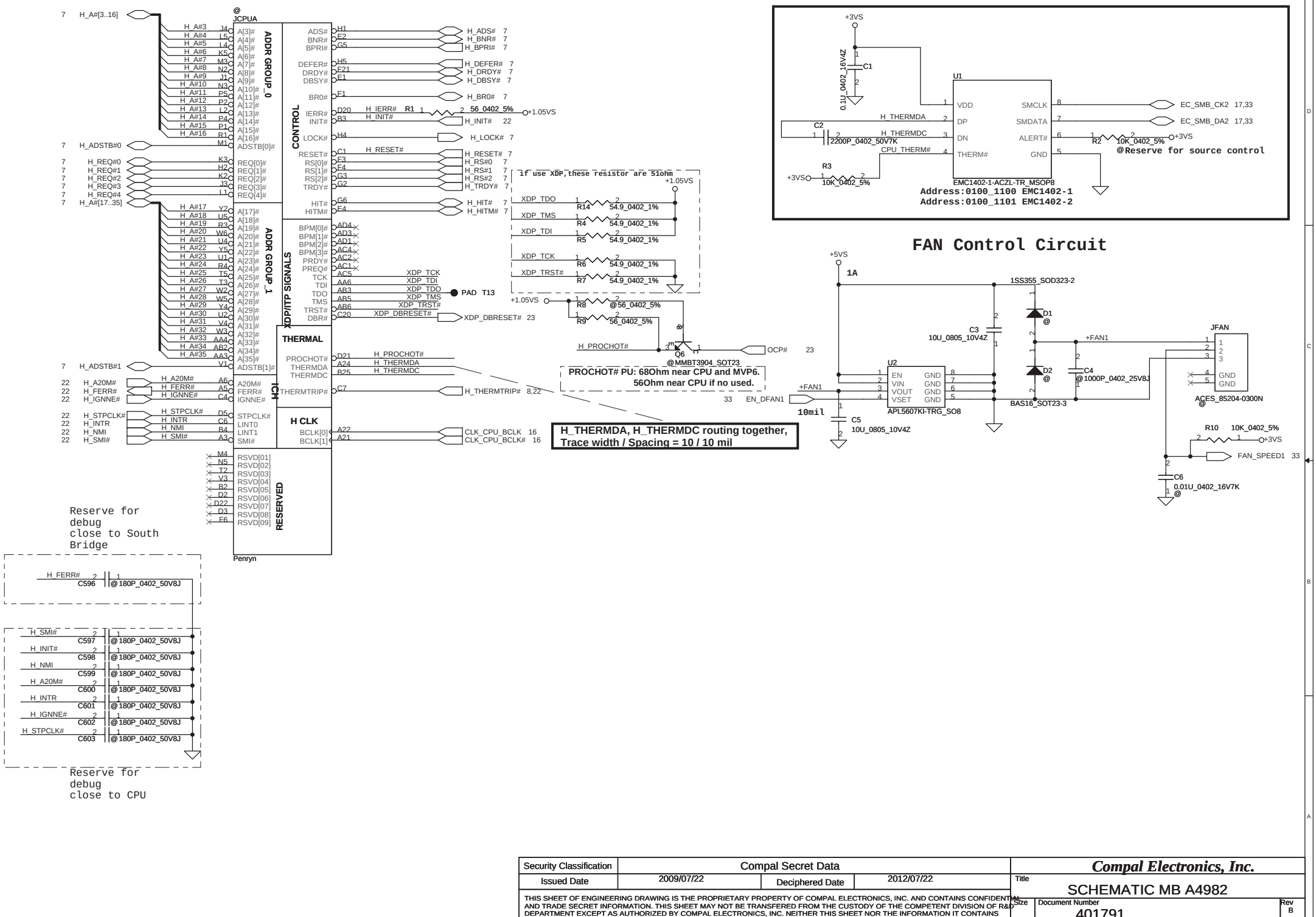

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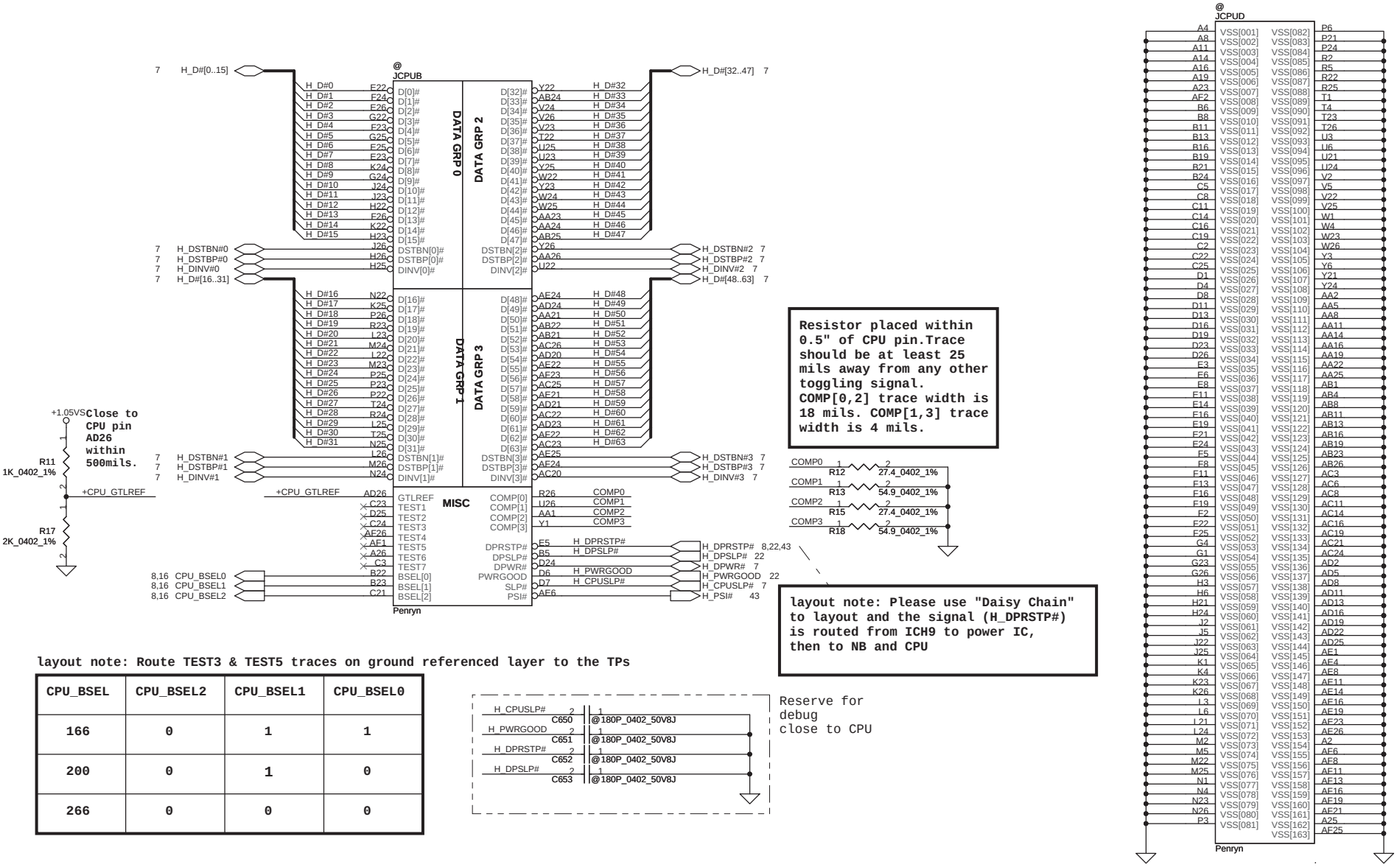

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

layout note: Please use "Daisy Chain" to layout and the signal (H_DPRSTP#) is routed from ICH9 to power IC, then to NB and CPU

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Reserve for debug close to CPU

H_CPUSLP# C650 @180P_0402_50V8J
H_PWRGOOD C651 @180P_0402_50V8J
H_DPRSTP# C652 @180P_0402_50V8J
H_DPSLP# C653 @180P_0402_50V8J

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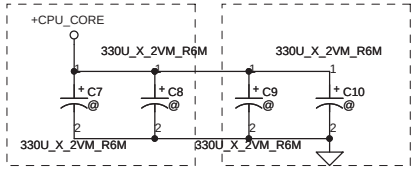
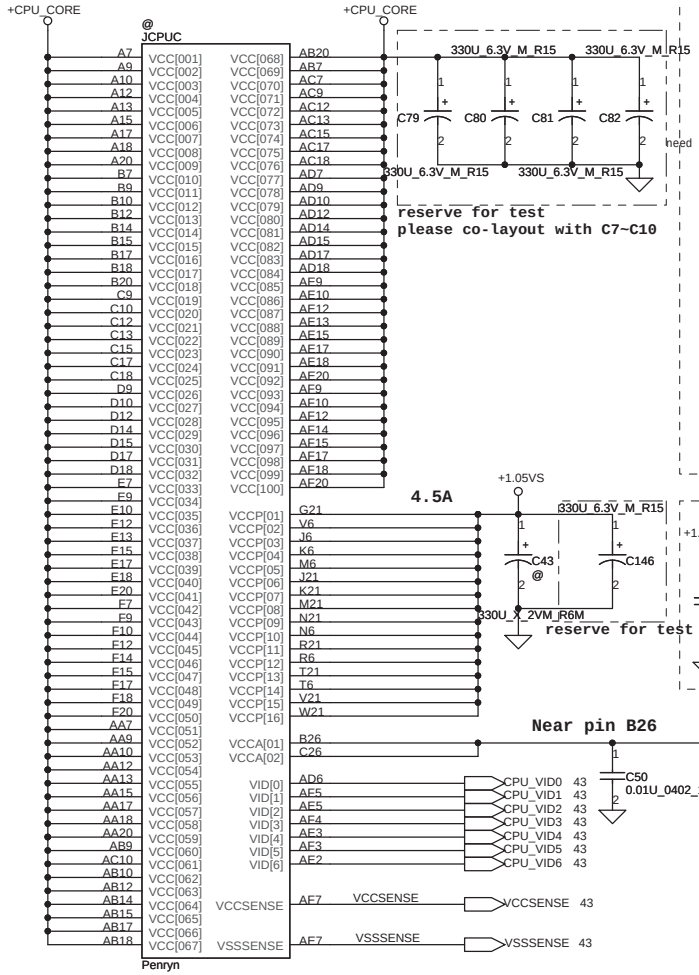
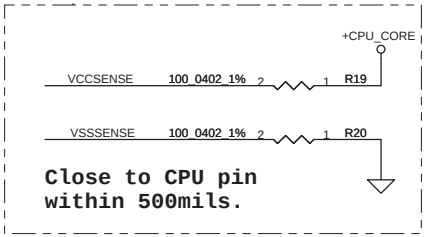
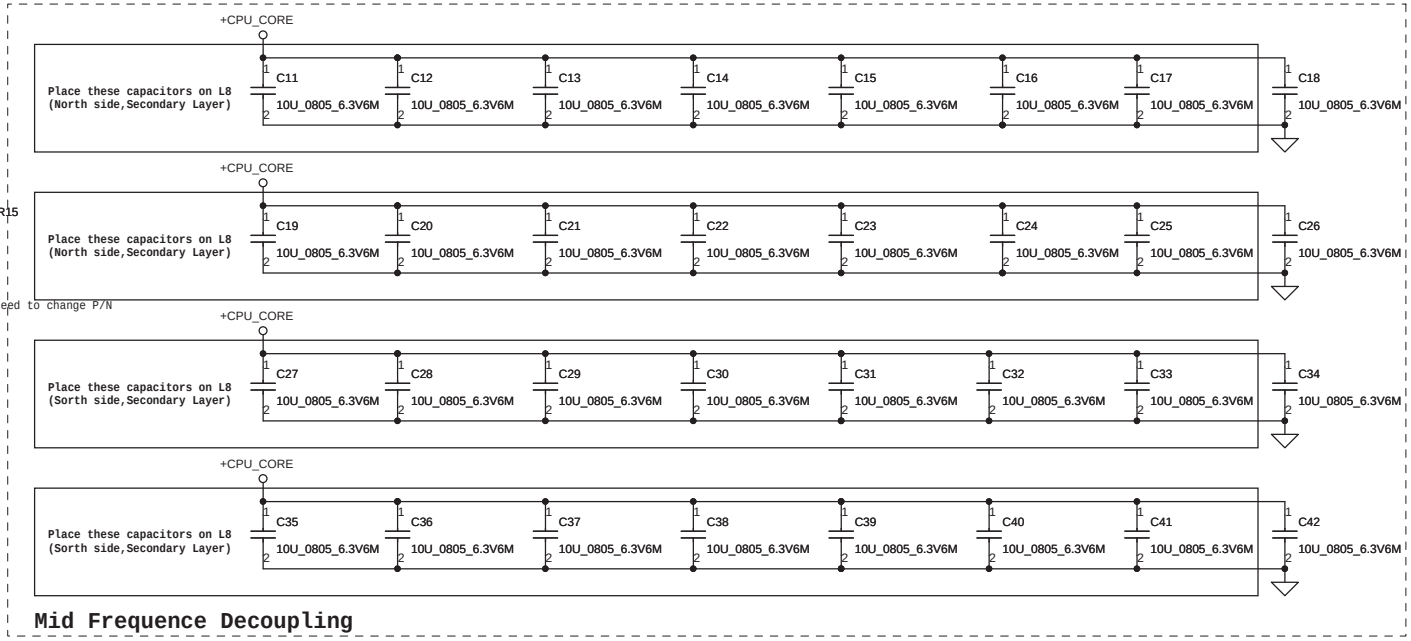
Near CPU CORE regulator

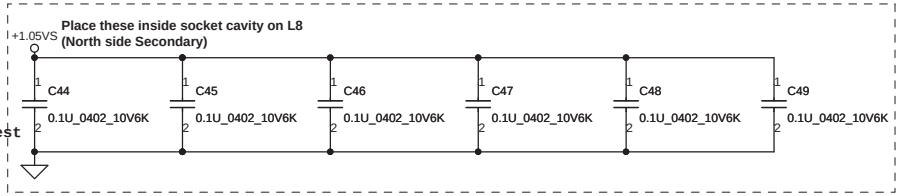
ESR <= 1.5m ohm
Capacitor > 1980uF

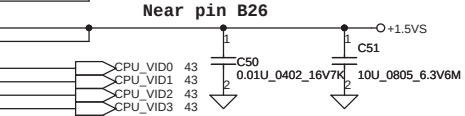












Length match within 25 mils.
The trace width/space/other is 14/7/25.

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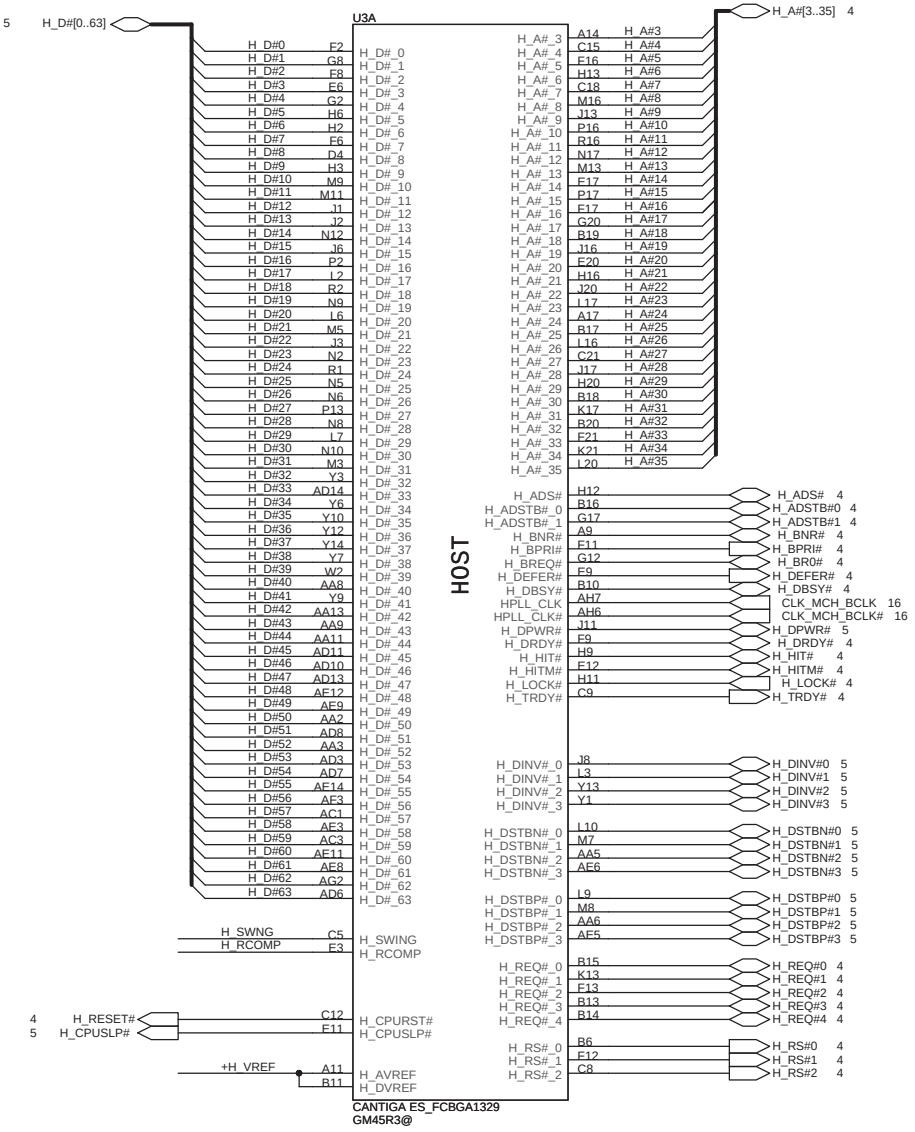
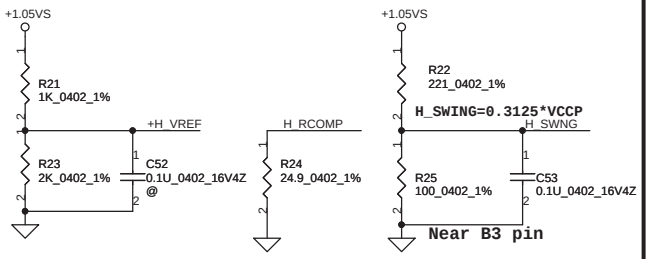


Layout Note:
H_RCOMP / +H_VREF / H_SWNG
trace width and spacing is 10/20
within 100 mils from NB



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Strap Pin Table

CFG[2:0]		011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6	Internal pull-up	0 = iTPM Host Interface is enabled can support disble by SW. 1 = iTPM Host Interface is Disabled *(Default)
CFG7	Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9	Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10	Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12]	Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16	Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19	Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable *(Default)
CFG20 (PCIE/SDVO select)	Internal pull-down	0 = Only PCIE or [SDVO/DP/HDMI] is operational. * (Default) 1 = PCIE/[SDVO/DP/HDMI] are operating simu.

U3B

RSVD: M36 RSVD1, N36 RSVD2, R33 RSVD3, T33 RSVD4, AH9 RSVD5, AH10 RSVD6, AH12 RSVD7, AH13 RSVD8, K12 RSVD9, AL34 RSVD10, AK34 RSVD11, AN35 RSVD12, AM35 RSVD13, T24 RSVD14, R31 RSVD15, B2 RSVD16, M1 RSVD17, AY21 RSVD20, BG23 RSVD22, BE23 RSVD23, BH18 RSVD24, BE18 RSVD25

DDR CLK/ CONTROL/ COMPENSATION: SA_CK_0 AP24 DDRA_CLK0 14; SA_CK_1 AT21 DDRA_CLK1 14; SB_CK_0 AV24 DDRB_CLK0 15; SB_CK_1 AU20 DDRB_CLK1 15; SA_CK#_0 AR24 DDRA_CLK0# 14; SA_CK#_1 AR21 DDRA_CLK1# 14; SB_CK#_0 AU24 DDRB_CLK0# 15; SB_CK#_1 AV20 DDRB_CLK1# 15; SA_CKE_0 BC28 DDRA_CKE0 14; SA_CKE_1 AY28 DDRA_CKE1 14; SB_CKE_0 AY36 DDRB_CKE0 15; SB_CKE_1 BB36 DDRB_CKE1 15; SA_CS#_0 BA17 DDRA_SCS0# 14; SA_CS#_1 AY16 DDRA_SCS1# 14; SB_CS#_0 AV16 DDRB_SCS0# 15; SB_CS#_1 AR13 DDRB_SCS1# 15; SA_ODT_0 BD17 DDRA_ODT0 14; SA_ODT_1 AY17 DDRA_ODT1 14; SB_ODT_O BE15 DDRB_ODT0 15; SB_ODT_1 AY13 DDRB_ODT1 15

SM_RCOMP BG22 SMRCOMP R29 80.6_0402_1%; SM_RCOMP# BH21 SMRCOMP# R30 80.6_0402_1%

SM_RCOMP_VOH BF28 +SM_RCOMP_VOH; SM_RCOMP_VOL BH28 +SM_RCOMP_VOL

SM_VREF AV42 +SM_VREF; SM_PWROK AR36 SM_PWROK R32 @ 0_0402_5%; SM_REXT BF17 SM_REXT R33 499_0402_1%; SM_DRAMRST# BC36 SM_DRAMRST# 14,15

SM_DRAMRST# would be needed for DDR3 only

For Cantiga 80 Ohm

20mil

C58 0.1U_0402_16V4Z @

+1.5V: R26 1K_0402_1%; R31 1K_0402_1%; R34 1K_0402_1%

+SM_RCOMP_VOH: C54 0.01U_0402_16V7K, C55 2.2U_0603_6.3V6K, R27 3.01K_0402_1%

+SM_RCOMP_VOL: C56 0.01U_0402_16V7K, C57 2.2U_0603_6.3V6K, R28 1K_0402_1%

SM_PWROK R101 0_0402_5% DDR3_SM_PWROK 42

CLK: DPLL_REF_CLK B38 CLK_DREF_96M; DPLL_REF_CLK# A38 CLK_DREF_96M#; DPLL_REF_SSCLK F41 CLK_DREF_SSC; DPLL_REF_SSCLK# F41 CLK_DREF_SSC#

CLK_DREF_96M R575 PM@ 0_0402_5%; CLK_DREF_96M# R576 PM@ 0_0402_5%; CLK_DREF_SSC R577 PM@ 0_0402_5%; CLK_DREF_SSC# R578 PM@ 0_0402_5%

Please place these resistors close to related balls

PEG_CLK F43 CLK_MCH_3GPLL 16; PEG_CLK# E43 CLK_MCH_3GPLL# 16

DMI: DMI_RXN_0 AF41 DMI_ITX_MRX_N0 21; DMI_RXN_1 AE37 DMI_ITX_MRX_N1 21; DMI_RXN_2 AE47 DMI_ITX_MRX_N2 21; DMI_RXN_3 AH39 DMI_ITX_MRX_N3 21

DMI_RXP_0 AE40 DMI_ITX_MRX_P0 21; DMI_RXP_1 AE38 DMI_ITX_MRX_P1 21; DMI_RXP_2 AE48 DMI_ITX_MRX_P2 21; DMI_RXP_3 AH40 DMI_ITX_MRX_P3 21

DMI_TXN_0 AF35 DMI_MTX_IRX_N0 21; DMI_TXN_1 AF43 DMI_MTX_IRX_N1 21; DMI_TXN_2 AF46 DMI_MTX_IRX_N2 21; DMI_TXN_3 AH42 DMI_MTX_IRX_N3 21

DMI_TXP_0 AD35 DMI_MTX_IRX_P0 21; DMI_TXP_1 AE44 DMI_MTX_IRX_P1 21; DMI_TXP_2 AE46 DMI_MTX_IRX_P2 21; DMI_TXP_3 AH43 DMI_MTX_IRX_P3 21

Lane reversal

+1.05VS: R38 1K_0402_5%; R41 54.9_0402_1%; +3VS: R42 1K_0402_5%

MCH_TSATN# Q7 MMBT3904_SOT23-3 MCH_TSATN_EC# 33

CFG: 5,16 CPU_BSEL0 R35 1K_0402_5% MCH_CLKSEL0 T25 CFG_0; 5,16 CPU_BSEL1 R36 1K_0402_5% MCH_CLKSEL1 R25 CFG_1; 5,16 CPU_BSEL2 R37 1K_0402_5% MCH_CLKSEL2 P25 CFG_2

T14 PAD P20 CFG_3; T15 PAD P24 CFG_4

R39 @2.21K_0402_1% MCH_CFG_5 C25 CFG_5; R40 @2.21K_0402_1% MCH_CFG_6 N24 CFG_6; R43 @2.21K_0402_1% MCH_CFG_7 M24 CFG_7

E21 CFG_8; R44 @2.21K_0402_1% MCH_CFG_9 C23 CFG_9; R45 @2.21K_0402_1% MCH_CFG_10 C24 CFG_10

N21 CFG_11; R46 @2.21K_0402_1% MCH_CFG_12 P21 CFG_12; R47 @2.21K_0402_1% MCH_CFG_13 T21 CFG_13

R20 CFG_14; +3VS R48 @2.21K_0402_1% MCH_CFG_16 M20 CFG_15; I21 CFG_16

H21 CFG_17; T16 PAD P29 CFG_18; R49 4.02K_0402_1% MCH_CFG_19 R28 CFG_19; R50 @4.02K_0402_1% MCH_CFG_20 T28 CFG_20

PM: +3VS R52 10K_0402_5% PM_EXTTS# R

23 PM_SYNC# R51 0_0402_5% PM_SYNC#_R R29 PM_SYNC#

5,22,43 H_DPRSTP# B7 PM_DPRSTP#

14,15 PM_EXTTS# R53 0_0402_5% PM_EXTTS#_R N33 PM_EXT_TS#_0

GMCH_PWROK P32 PM_EXT_TS#_1

17,21,27,28,33,34 PLT_RST# R54 100_0402_5% MCH_RSTIN# AT40 PWROK

4,22 H_THERMTRIP# R55 0_0402_5% NB_THERMTRIP# AT11 RSTIN#

23,43 PM_DPRSLPVR R56 0_0402_5% DPRSLPVR T20 THERMTRIP#

R32 DPRSLPVR

Use VGATE for GMCH_PWROK

23,33,43 VGATE R58 @0_0402_5% GMCH_PWROK

23,33 ICH_PWROK R59 0_0402_5%

GRAPHICS VID: GFX_VID_0 B33; GFX_VID_1 B32; GFX_VID_2 G33; GFX_VID_3 F33; GFX_VID_4 E33

GFX_VR_EN C34

Strap Pin Table

SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled *(Default) 1 = SDVO interface enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled 1 = Digital display (iHDMI/DP) interface enabled *(Default)

ME: CL_CLK AH37 CL_CLK0 23; CL_DATA AH36 CL_DATA0 23; CL_PWROK AN36 ICH_PWROK; CL_RST# AJ35 CL_RST#0 23; CL_VREF AH34 +CL_VREF

Width:Spacing 12mil:12mil

+CL_VREF=0.355V

+1.05VS: R57 1K_0402_1%; CL_VREF should be 0.35 V; R60 499_0402_1%

C59 0.1U_0402_16V4Z

R61 PM@ 0_0402_5%; R62 PM@ 0_0402_5%

NC: DDPC_CTRLCLK N28; DDPC_CTRLDATA M28; SDVO_CTRLCLK G36 SDVO_SCLK; SDVO_CTRLDATA F36 SDVO_SDATA; CLKREQ# K36 CLKREQ_3GPLL# 16; ICH_SYNC# H36 MCH_ICH_SYNC# 23

SDVO_SCLK SDVO_SCLK 20; SDVO_SDATA SDVO_SDATA 20

MISC: TSATN# B12 MCH_TSATN#

+3VS: SDVO_SCLK R61 GM@ 2.2K_0402_5%; SDVO_SDATA R62 IHDMI@ 2.2K_0402_5%; R579 GM@ 0_0402_5%; R580 PM@ 0_0402_5%

the strap pin will impact no IHDMI SKU if mount R62

HDA: HDA_BCLK B28 AZ_BITCLK_MCH 22; HDA_RST# B30 AZ_RST_MCH# 22; HDA_SDI B29 AZ_SDIN2_MCH_R; HDA_SDO C29 AZ_SDOUT_MCH 22; HDA_SYNC A28 AZ_SYNC_MCH 22

R63 33_0402_5% IHDMI@ AZ_SDIN2_MCH 22

NC_1 BG48, NC_2 BF48, NC_3 BD48, NC_4 BC48, NC_5 BH47, NC_6 BG47, NC_7 BE47, NC_8 BH46, NC_9 BF46, NC_10 BG45, NC_11 BH44, NC_12 BH43, NC_13 BH6, NC_14 BH5, NC_15 BG4, NC_16 BH3, NC_17 BF3, NC_18 BH2, NC_19 BG2, NC_20 BE2, NC_21 BG1, NC_22 BF1, NC_23 BD1, NC_24 BC1, NC_25 F1, NC_26 A47

CANTIGA ES_FCBGA1329

GM45R3@

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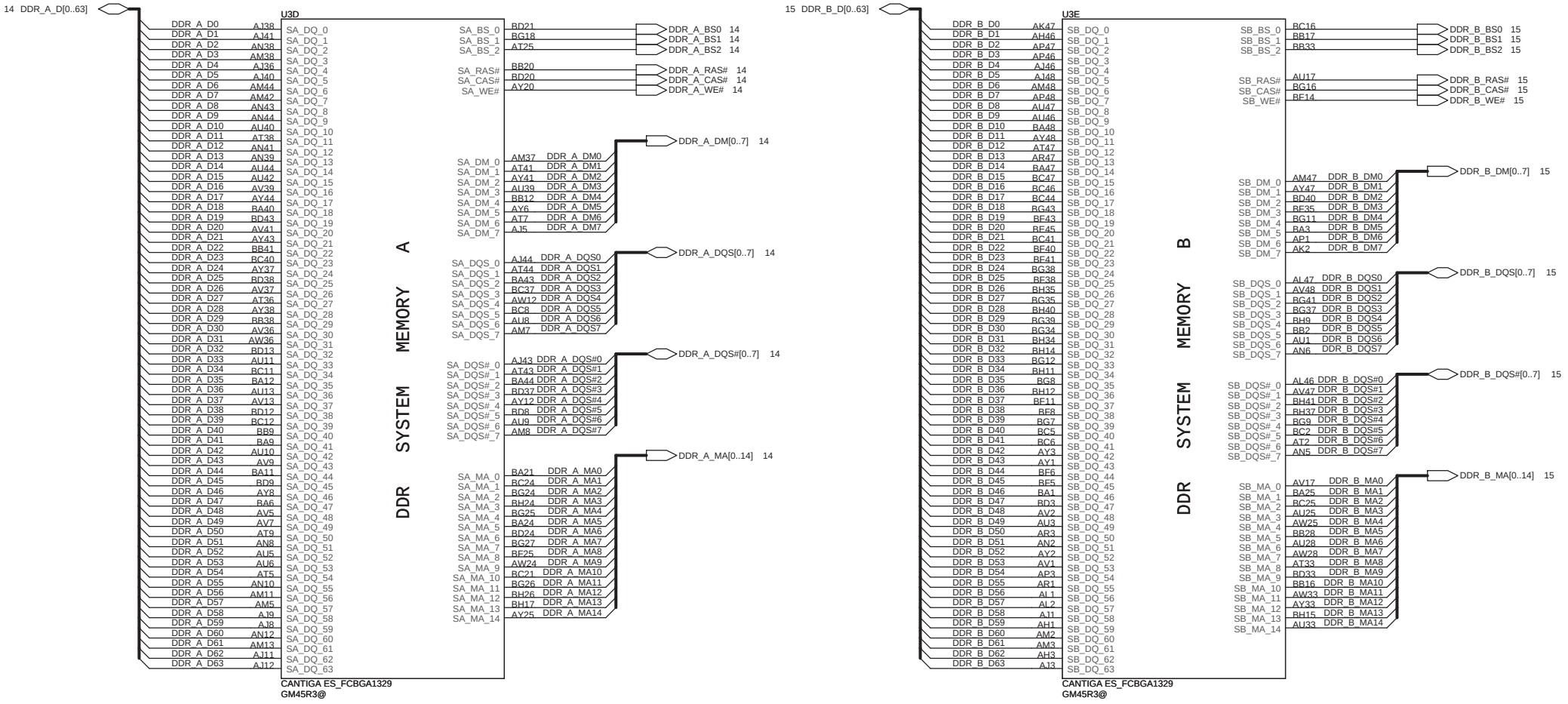

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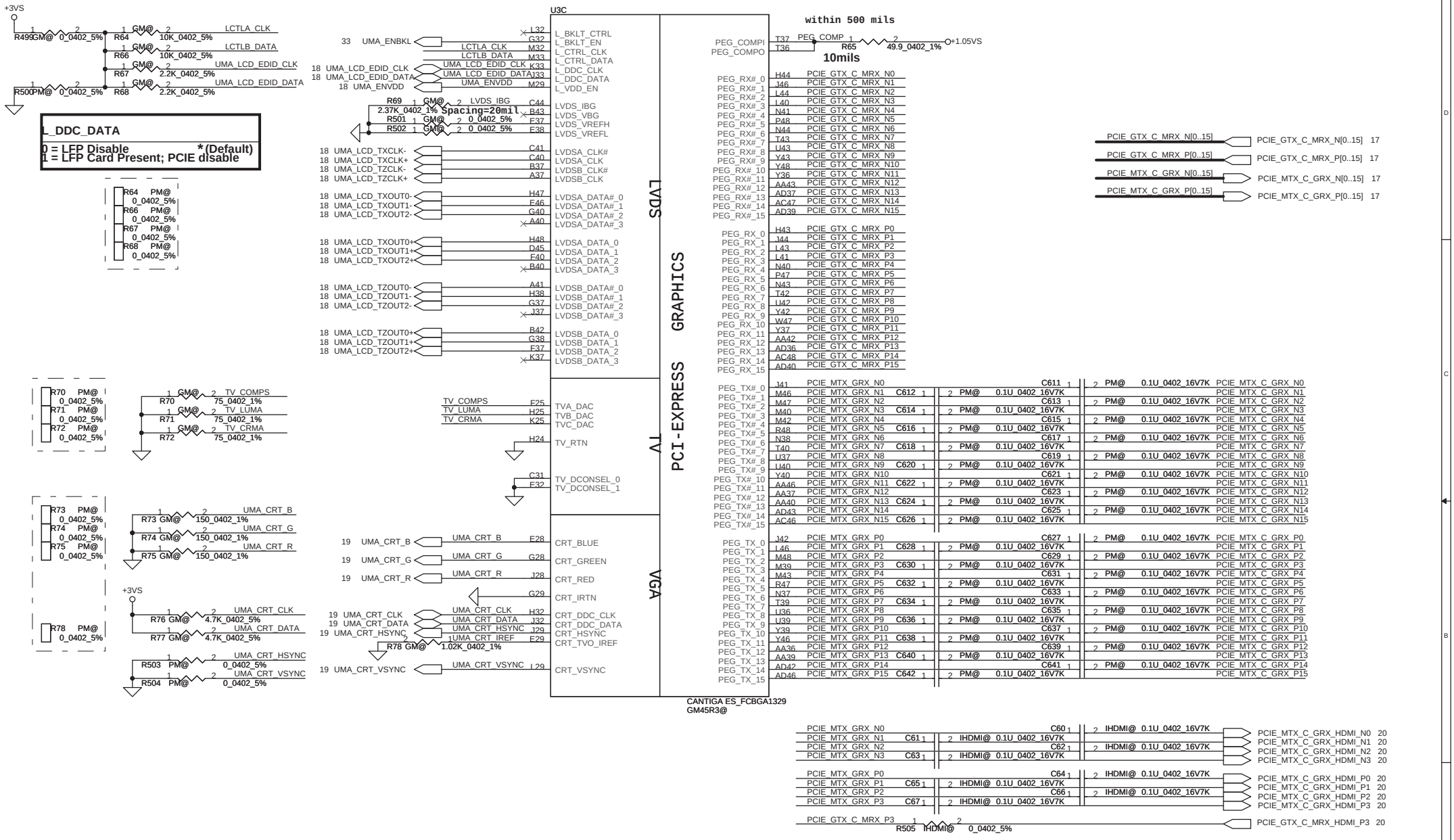

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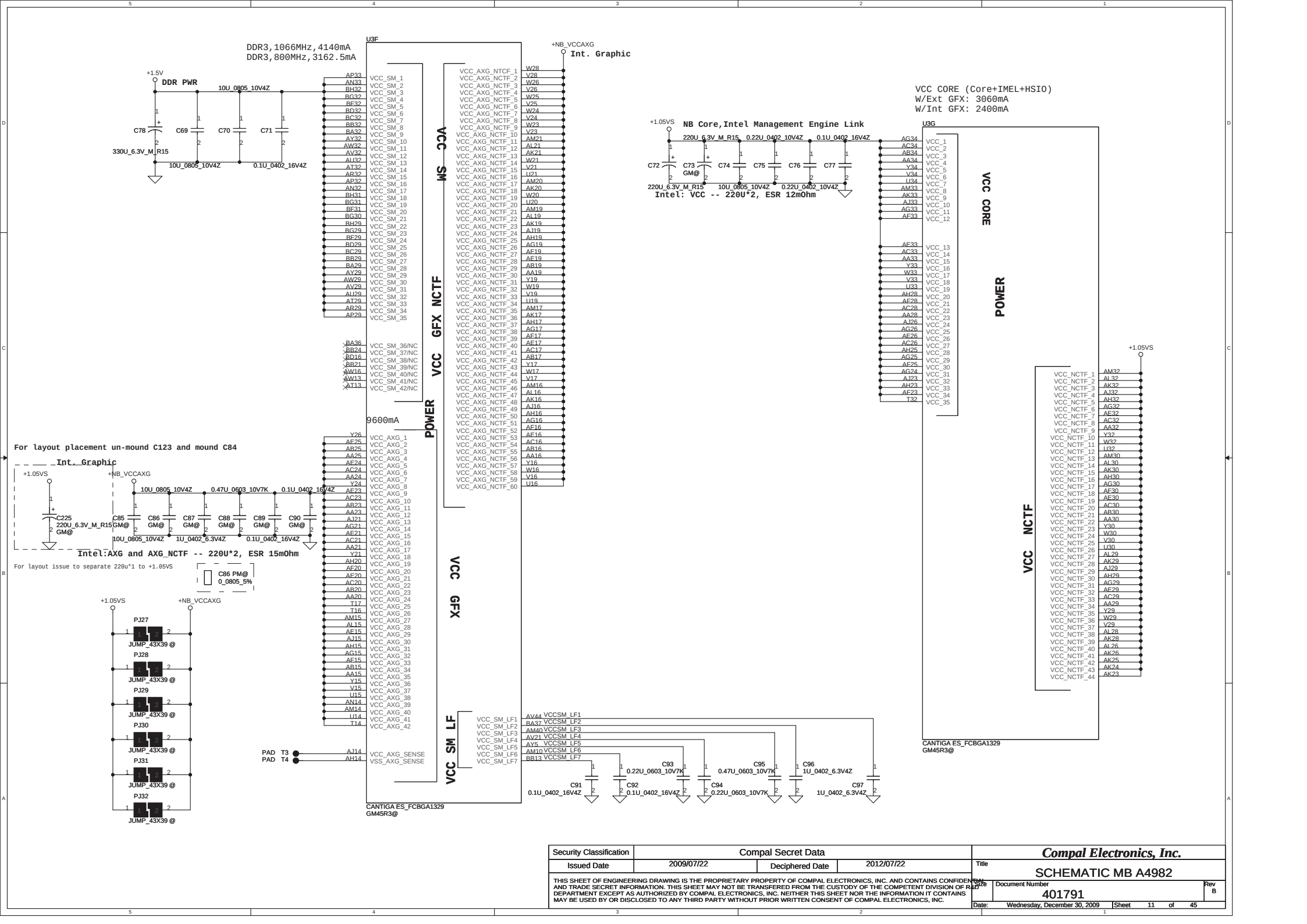

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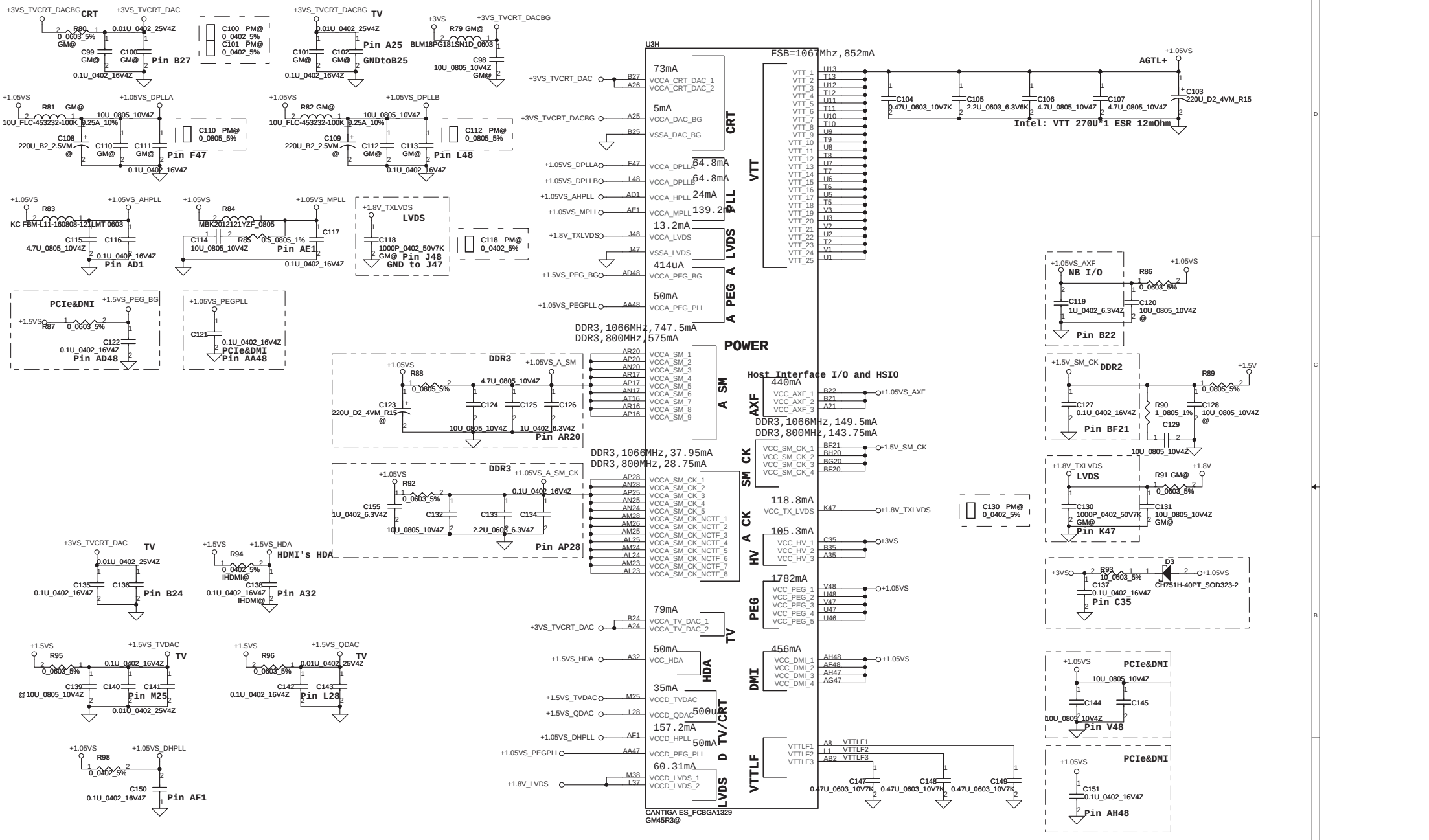

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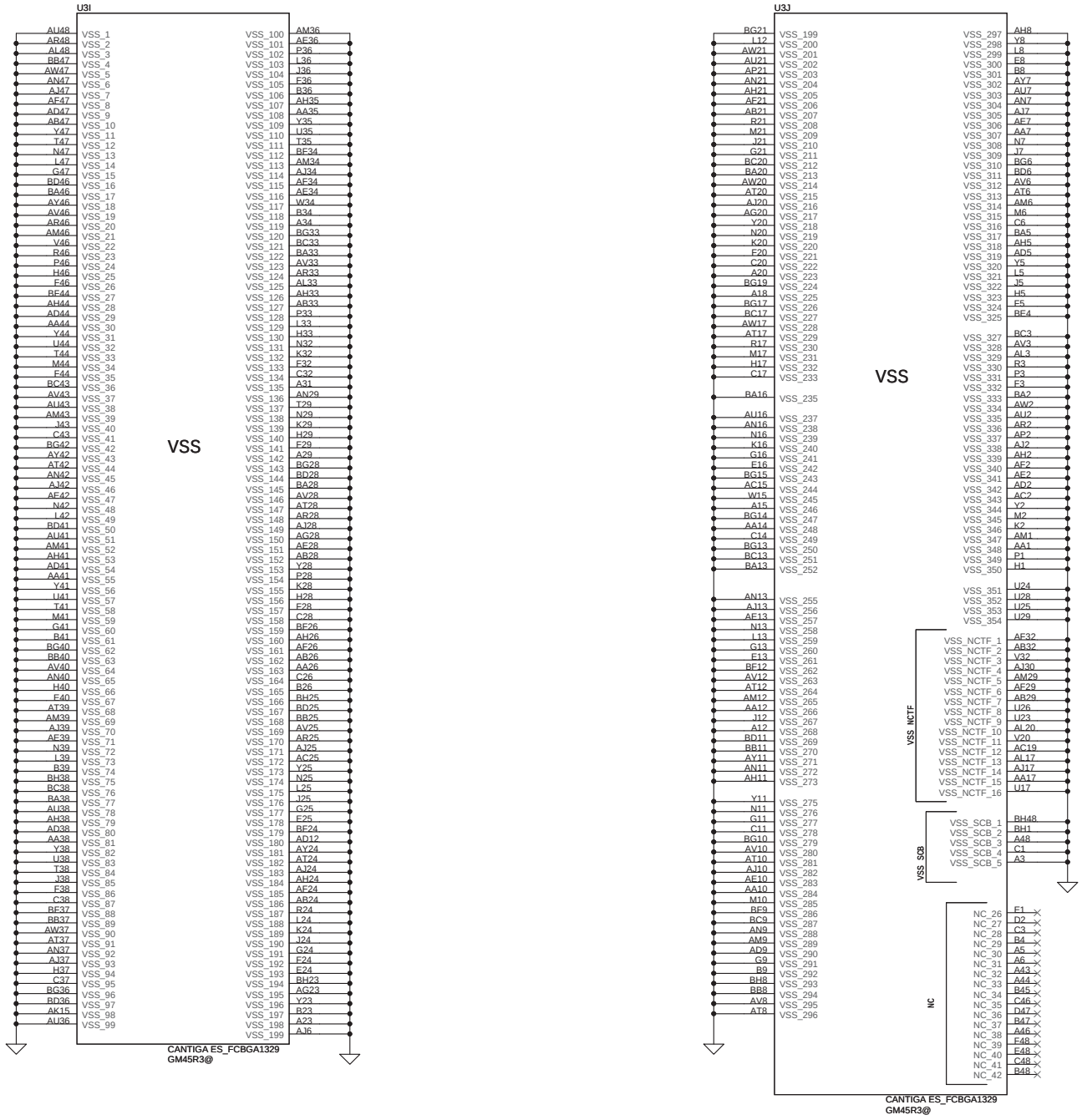

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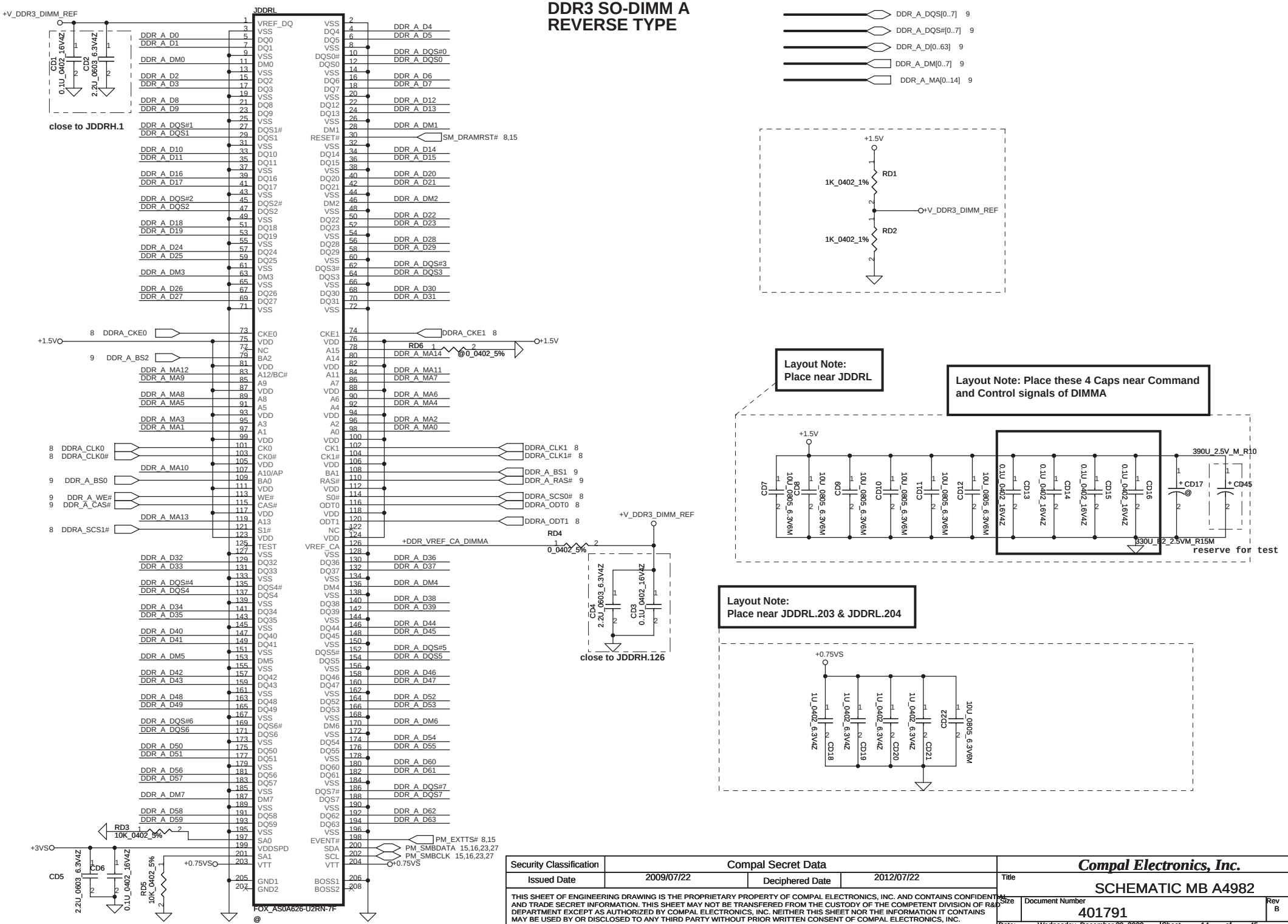
DDR3 SO-DIMM A
REVERSE TYPE



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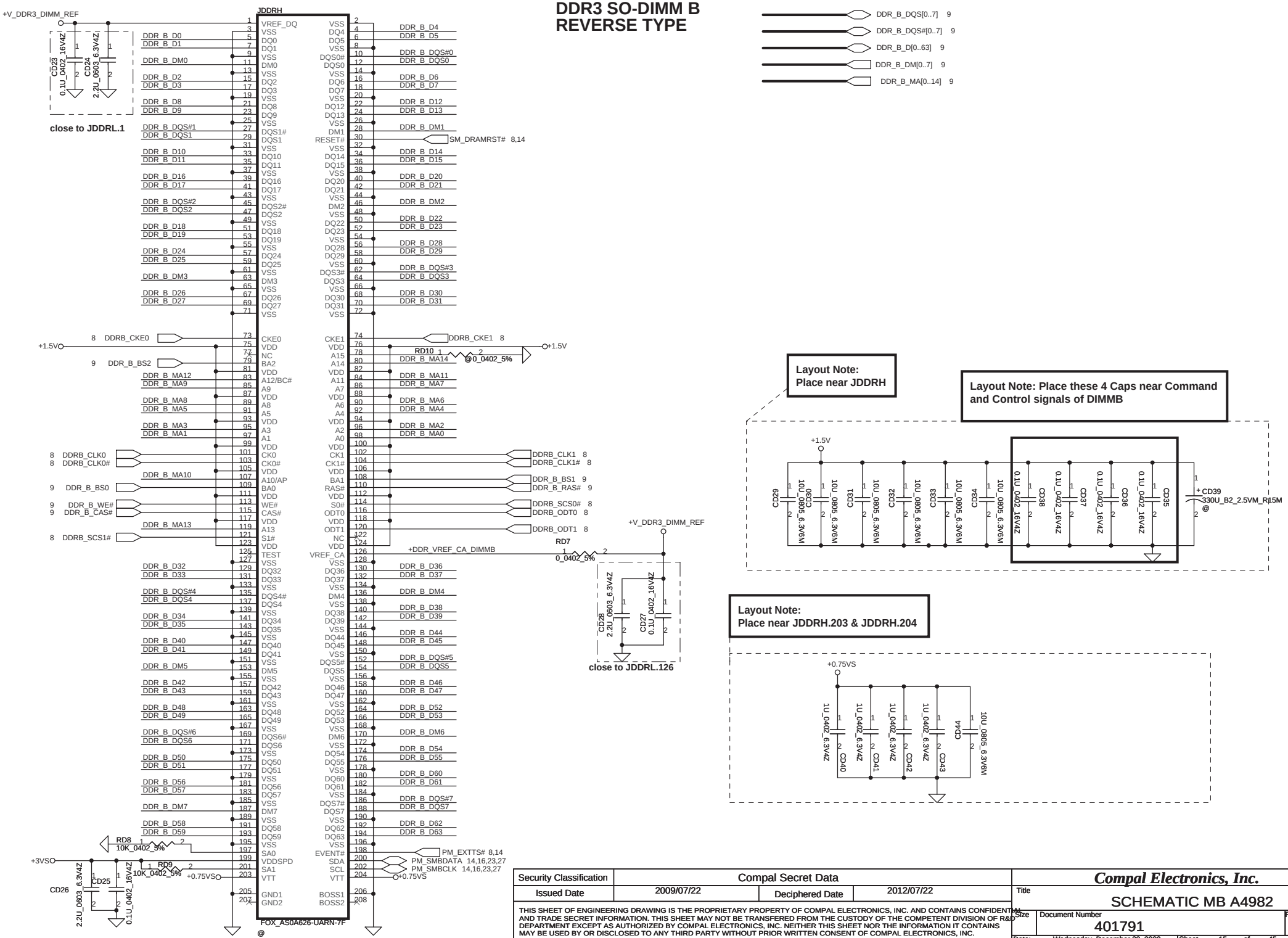
DDR3 SO-DIMM B
REVERSE TYPE



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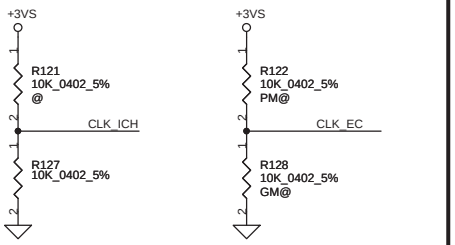
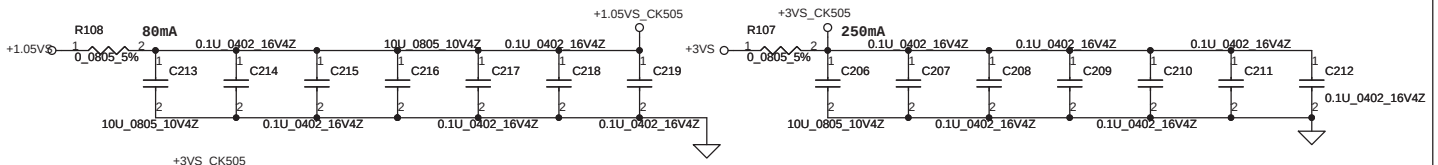
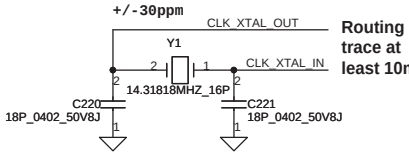
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

CLK_ICH	0 = SRC8/SRC8# (100MHz) 1 = ITP/ITP# (266MHz)
CLK_EC	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)

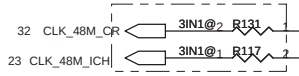


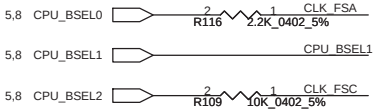


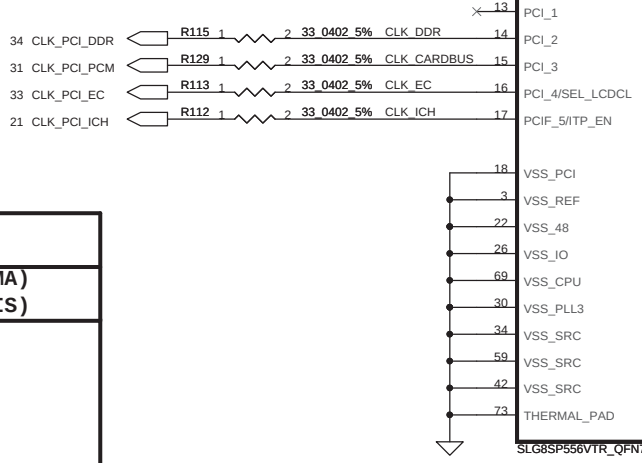


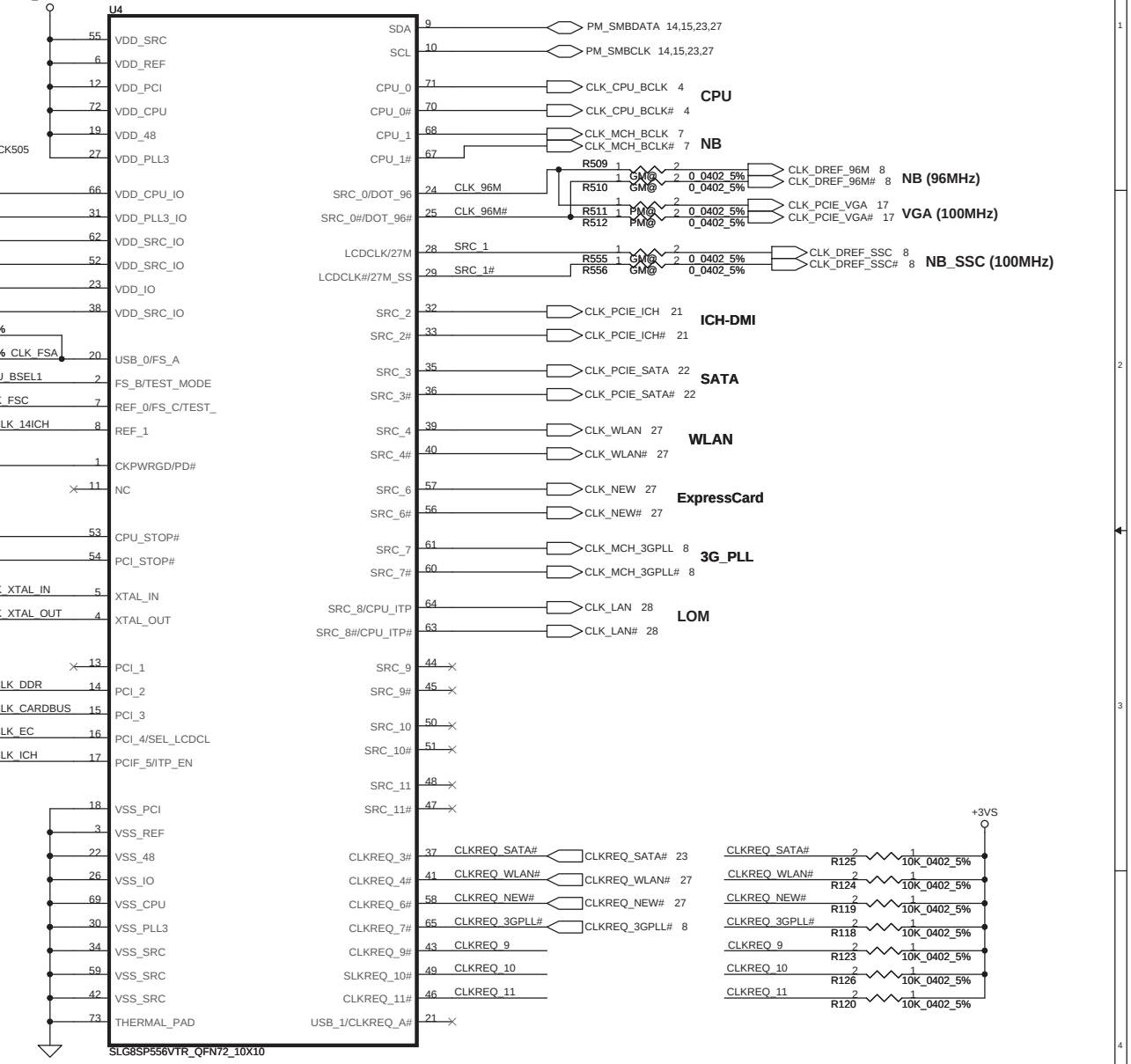
Routing the trace at least 10mil

place 22ohm for damping resistor when loading is two device,









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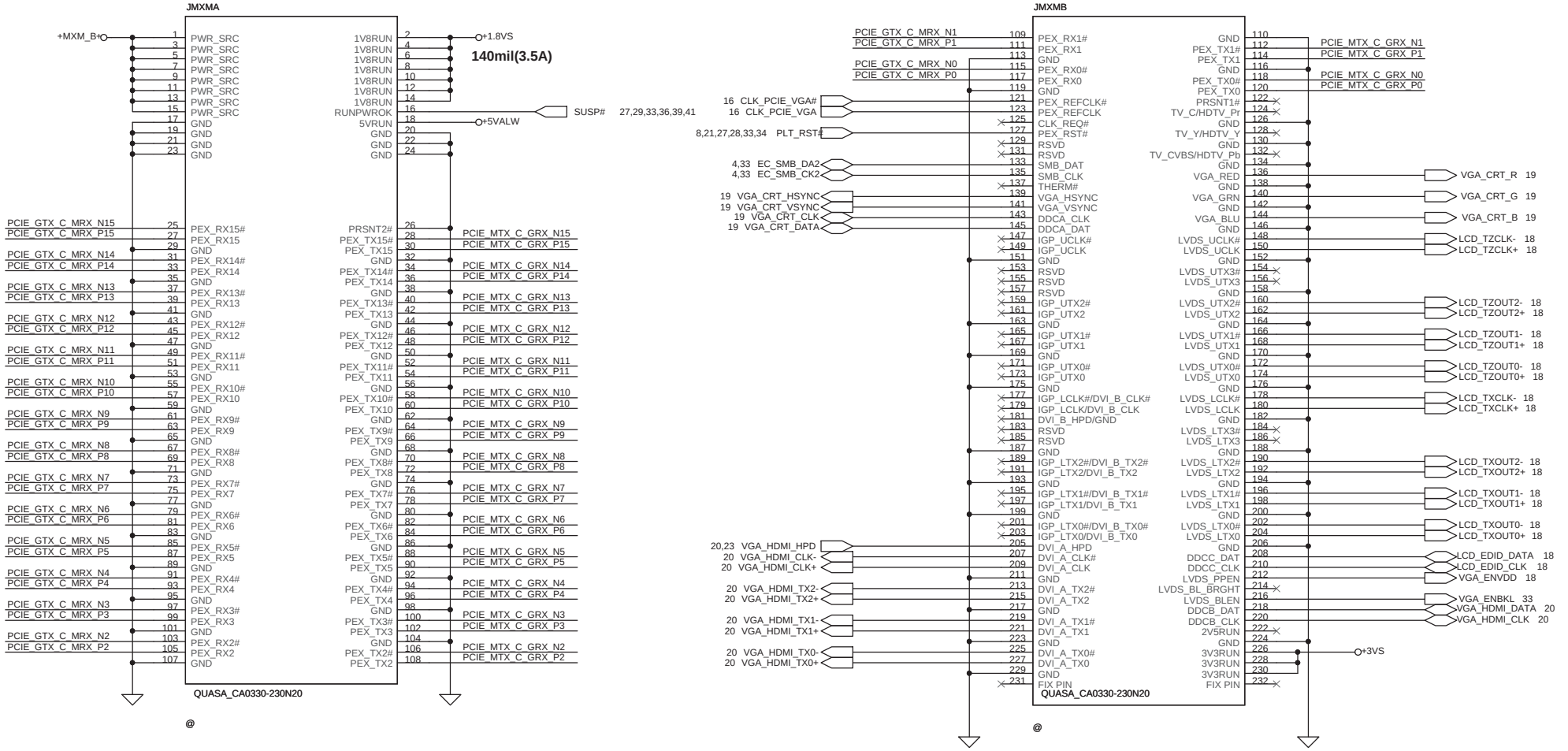
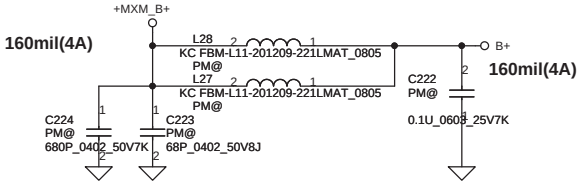
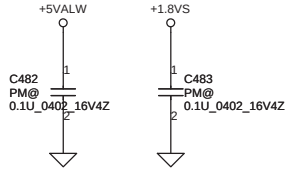
10 PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15]
10 PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15]
10 PCIE_GTX_C_MRX_N[0..15] → PCIE_GTX_C_MRX_N[0..15]
10 PCIE_GTX_C_MRX_P[0..15] → PCIE_GTX_C_MRX_P[0..15]







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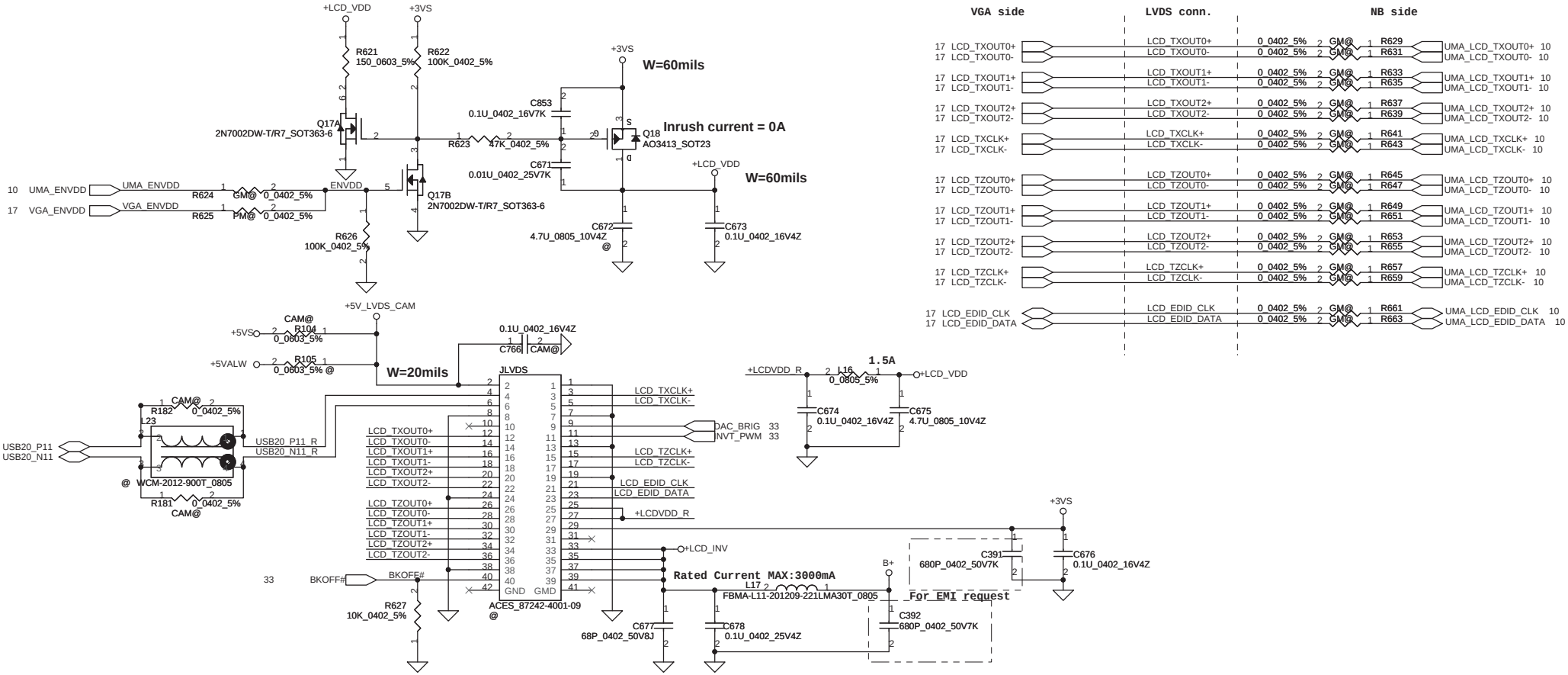
LCD/PANEL BD. Conn.



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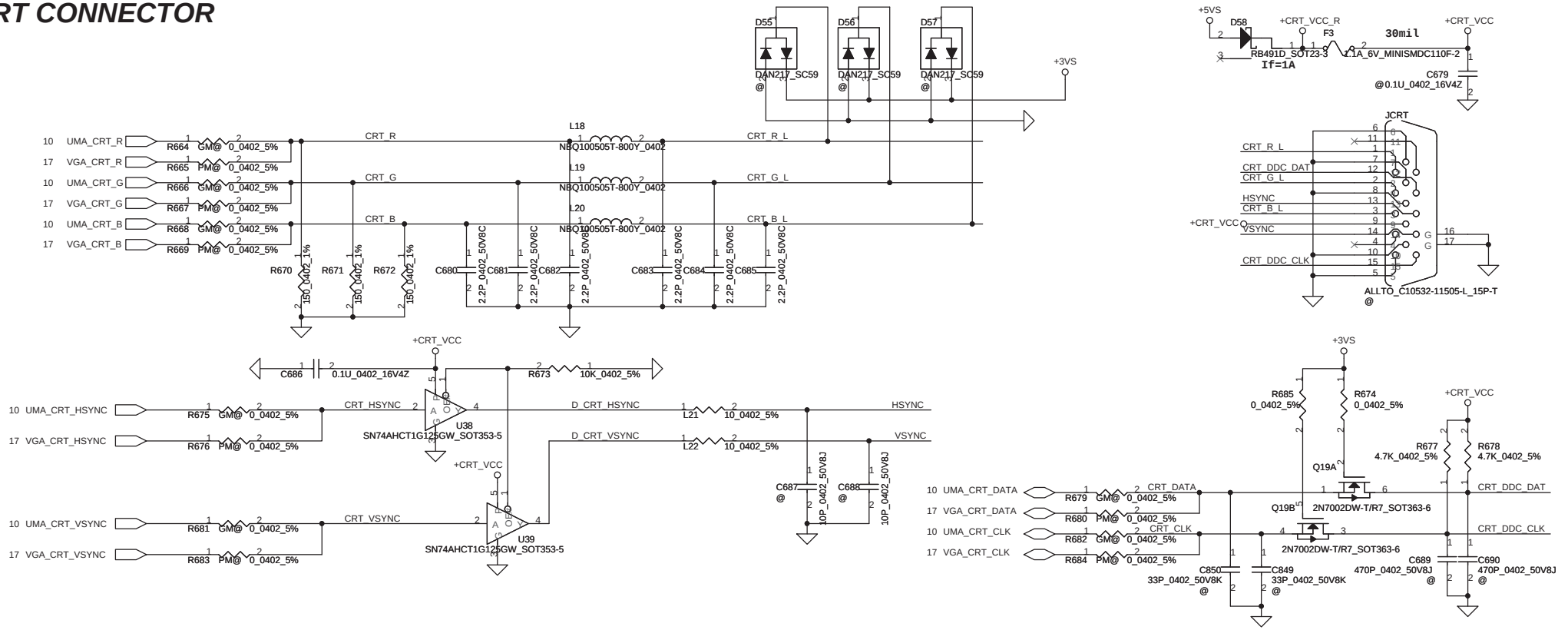
CRT CONNECTOR



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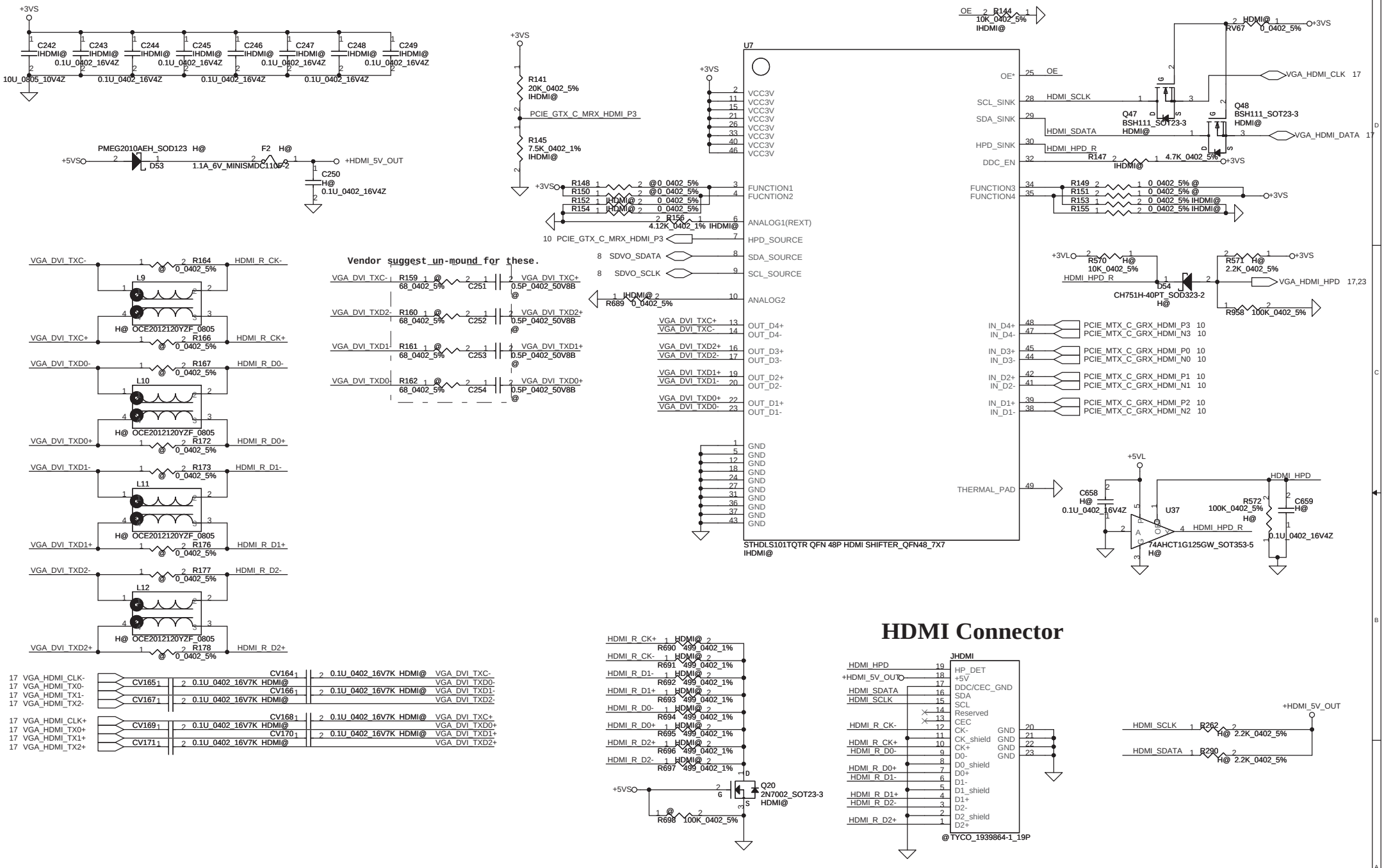

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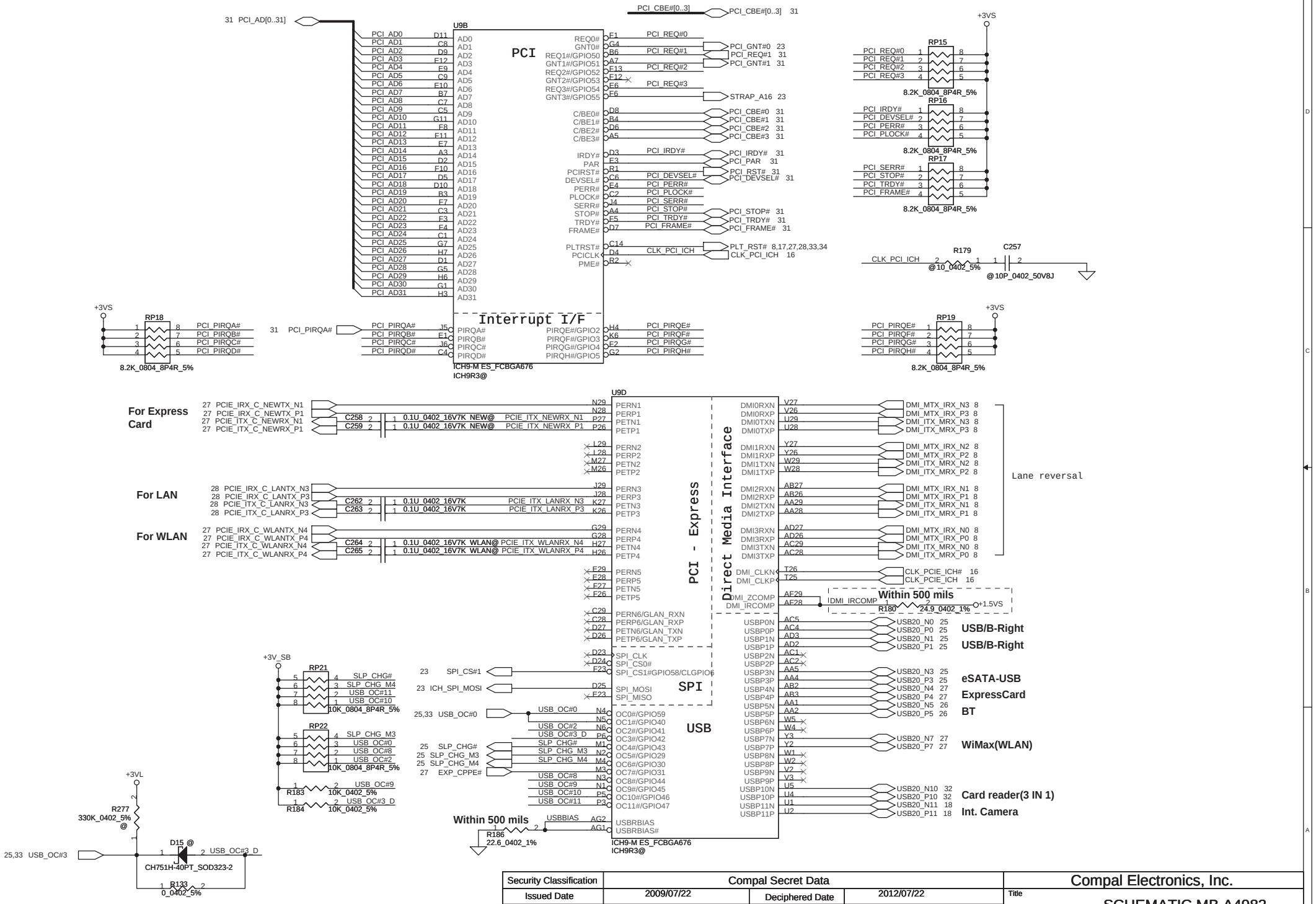

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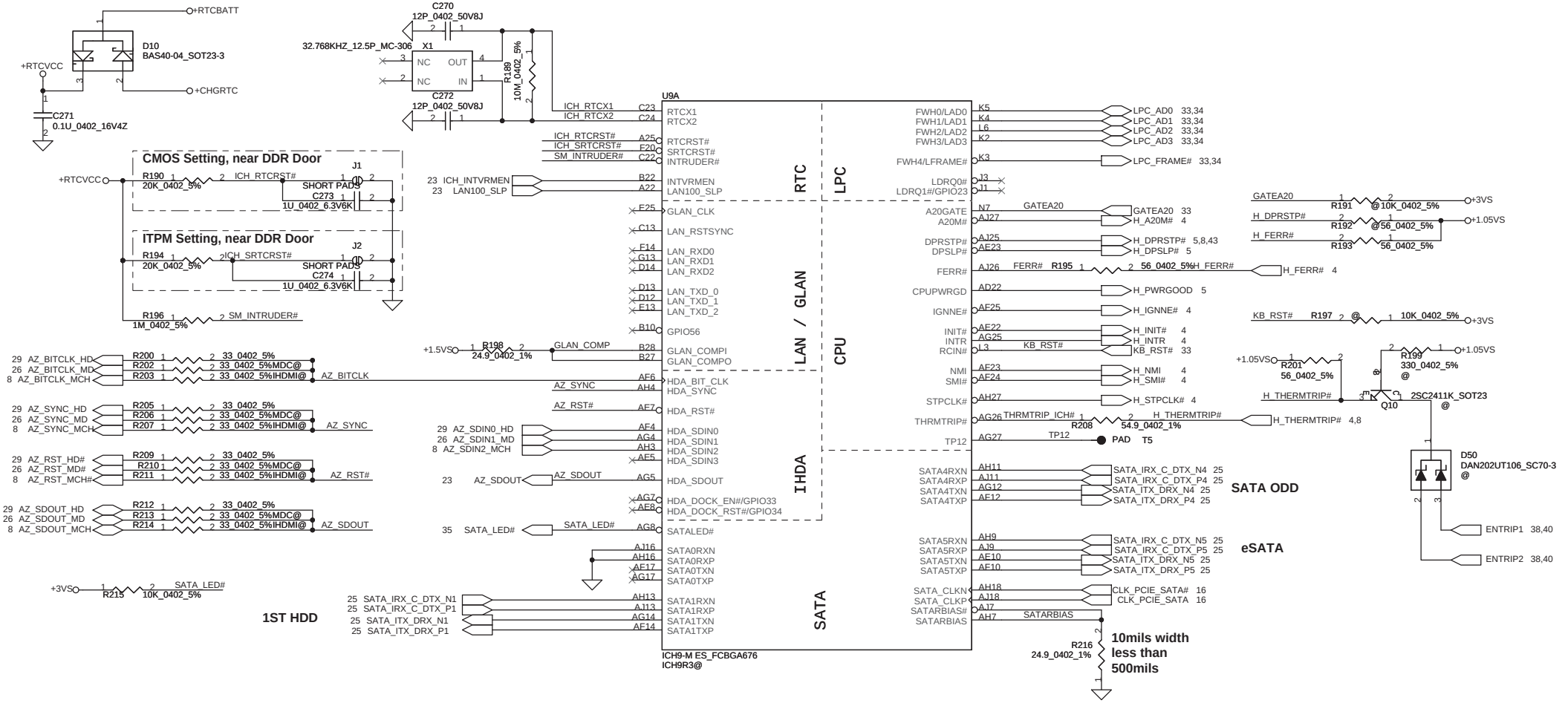

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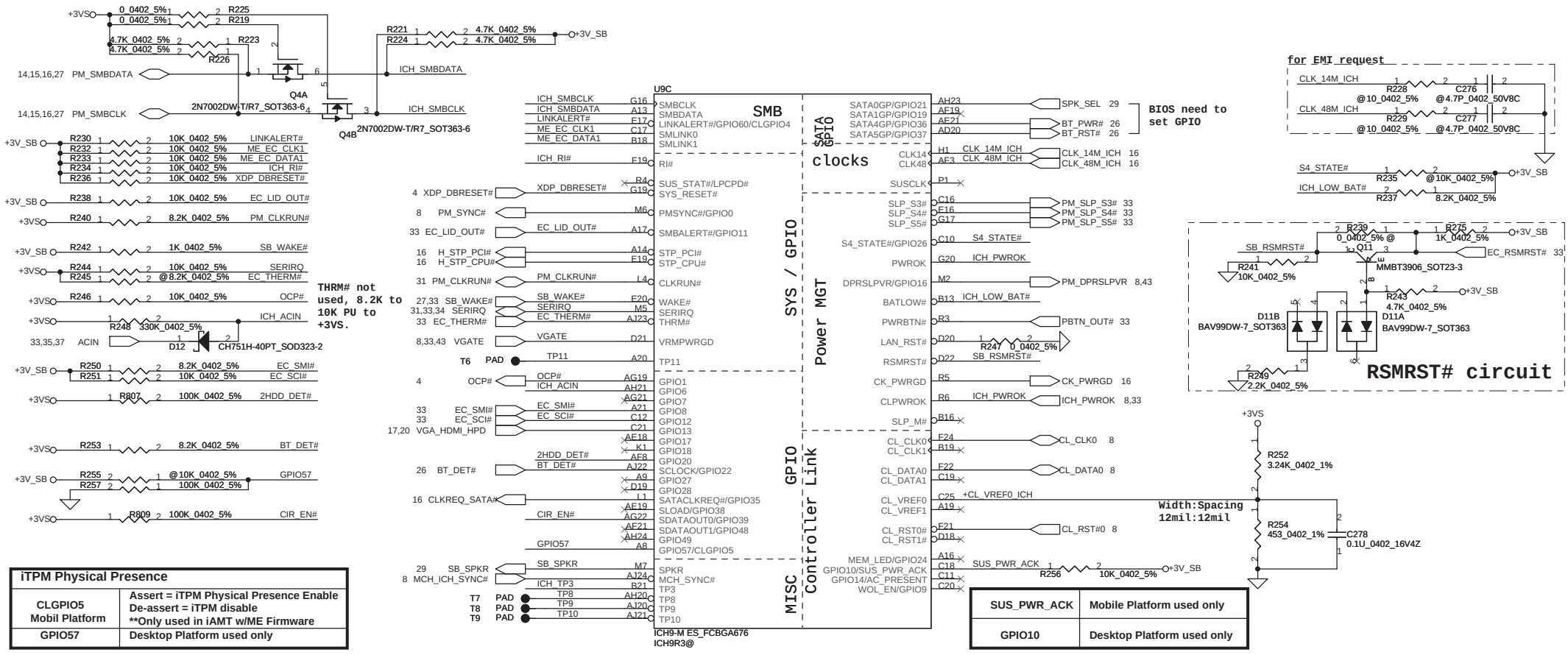

iTPM Physical Presence	
CLGPIO5 Mobil Platform	Assert = iTPM Physical Presence Enable De-assert = iTPM disable **Only used in iAMT w/ME Firmware
GPIO57	Desktop Platform used only

SUS_PWR_ACK	Mobile Platform used only
GPIO10	Desktop Platform used only

ICH9M Strap Pin

Internal TPM Strap(Internal pull-down)	
SPI_MOSI	Low= Disable High= iTPM enable by MCH strap*

No Reboot Strap (Internal pull-up)	
SB_SPKR	Low= *Default High= "No Reboot"

Boot BIOS Strap (Internal pull-up)		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	0	RESERVED
0	1	SPI
1	0	PCI
1	1	LPC* (Default)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default* (Internal pull-up)

Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

DMI Termination Voltage	
GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

XOR Chain Entrance Strap		
ICH_TP3 (Internal pull-up)	HDA_SDOUT (Internal pull-down)	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

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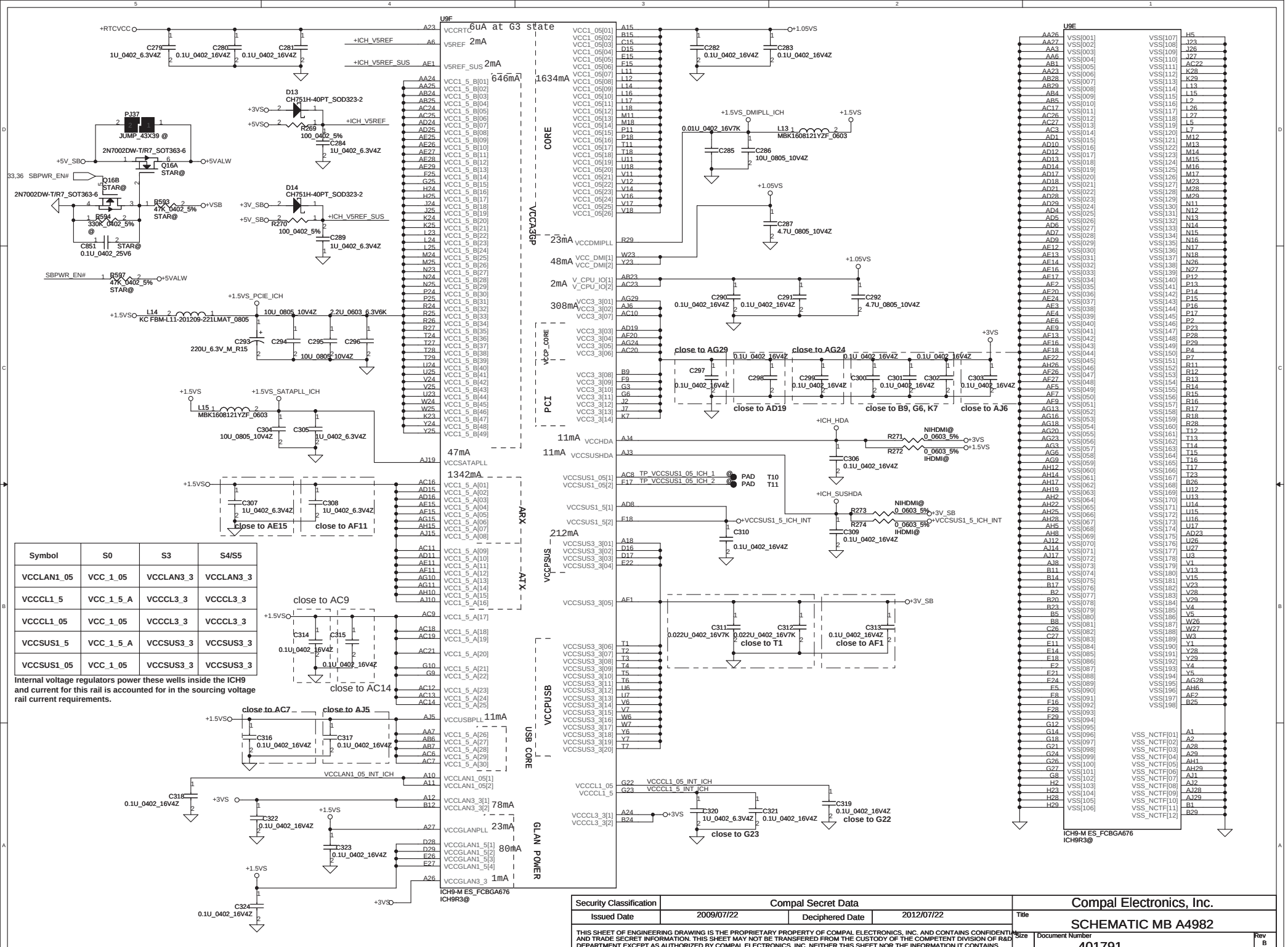

Symbol	S0	S3	S4/S5
VCCLAN1_05	VCC_1_05	VCCLAN3_3	VCCLAN3_3
VCCCL1_5	VCC_1_5_A	VCCCL3_3	VCCCL3_3
VCCCL1_05	VCC_1_05	VCCCL3_3	VCCCL3_3
VCCSUS1_5	VCC_1_5_A	VCCSUS3_3	VCCSUS3_3
VCCSUS1_05	VCC_1_05	VCCSUS3_3	VCCSUS3_3

Internal voltage regulators power these wells inside the ICH9 and current for this rail is accounted for in the sourcing voltage rail current requirements.

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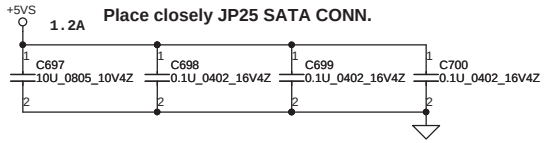
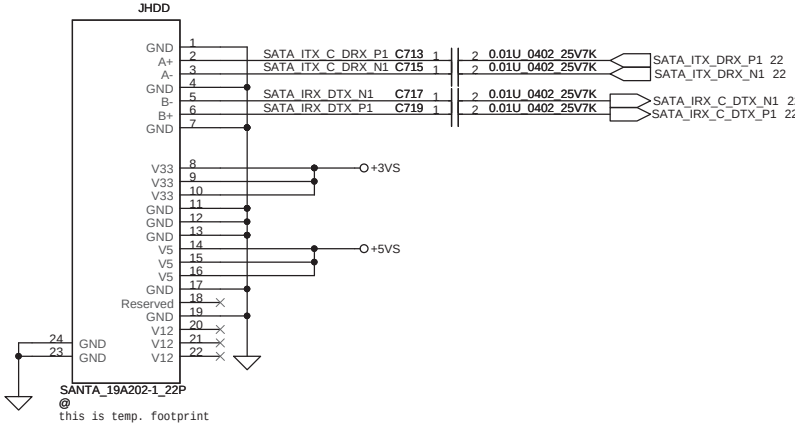
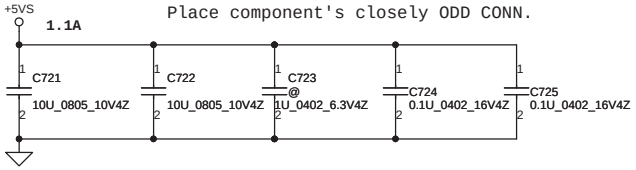
SATA HDD Conn.



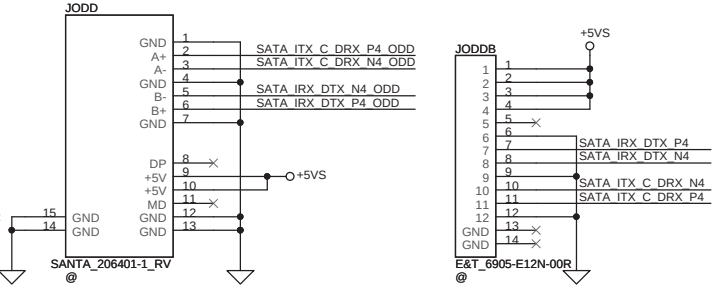


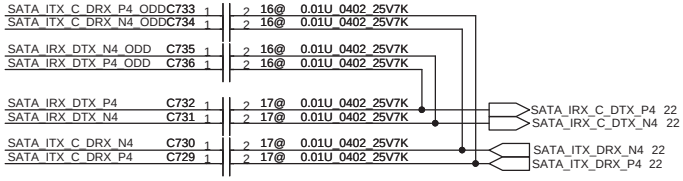
SATA ODD Conn



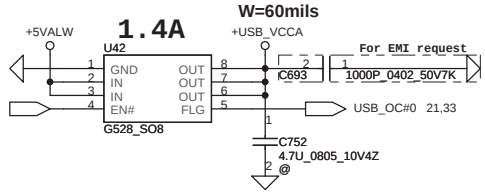
for 16" use

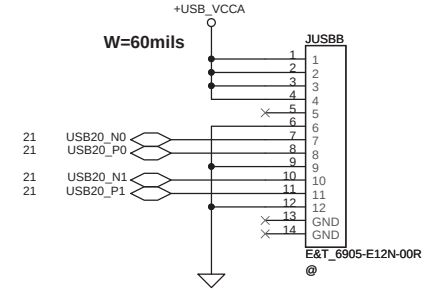
for 17" expansion using



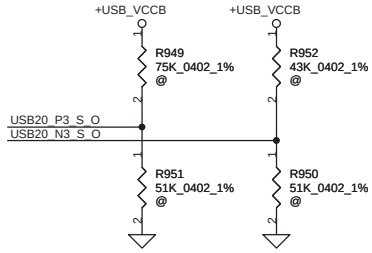


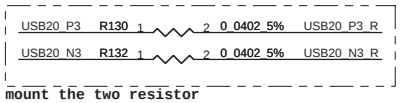
USB Board

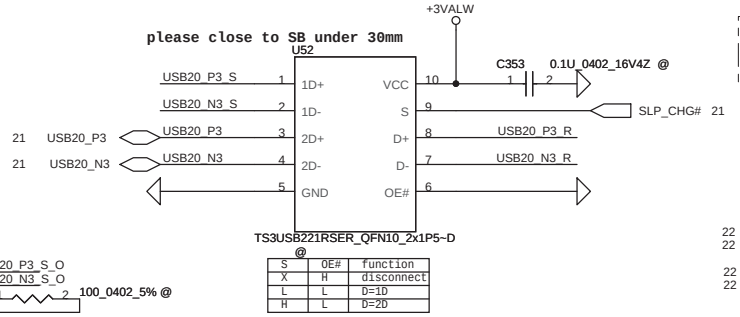


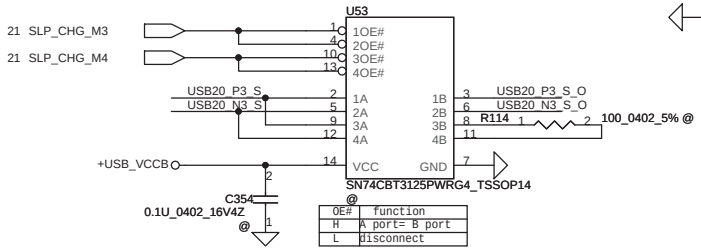


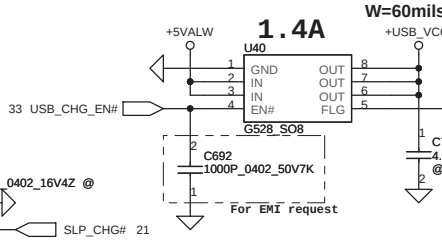
eSATA/USB

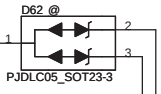


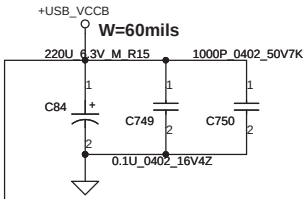




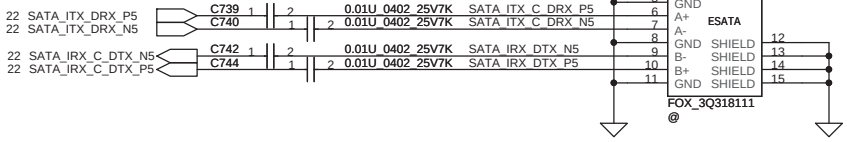








eSATA/USB Conn



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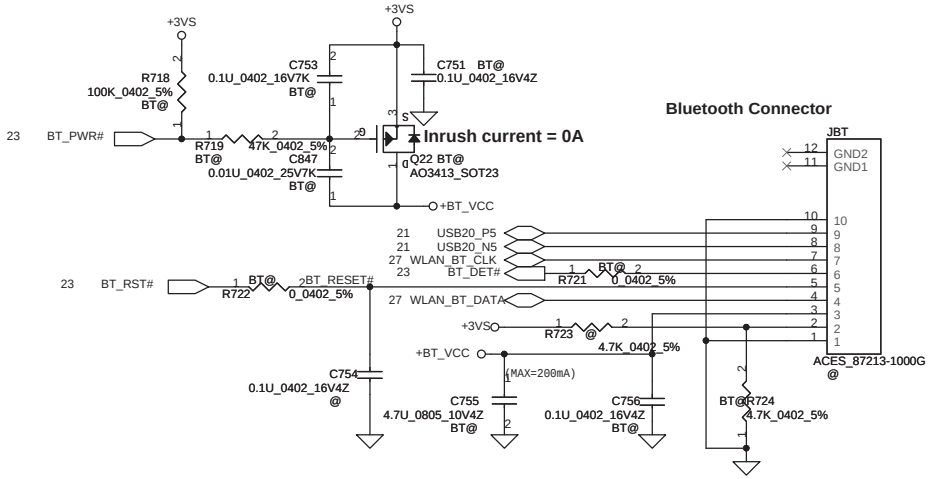
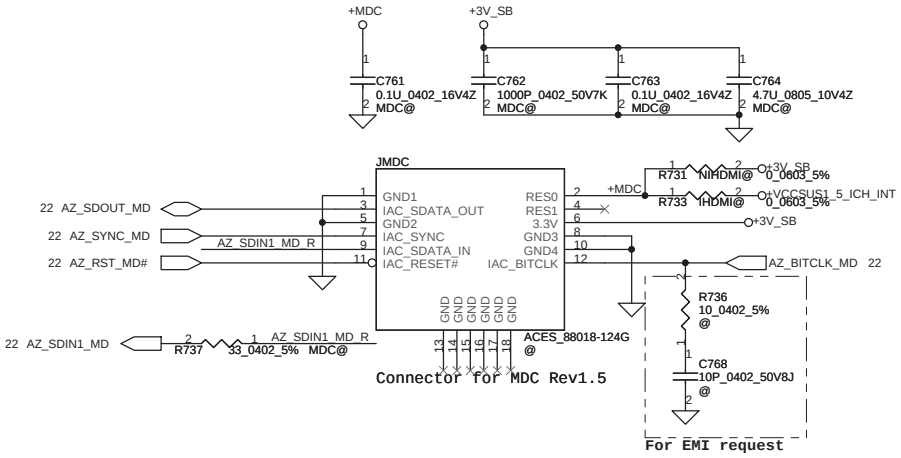
BlueTooth Interface

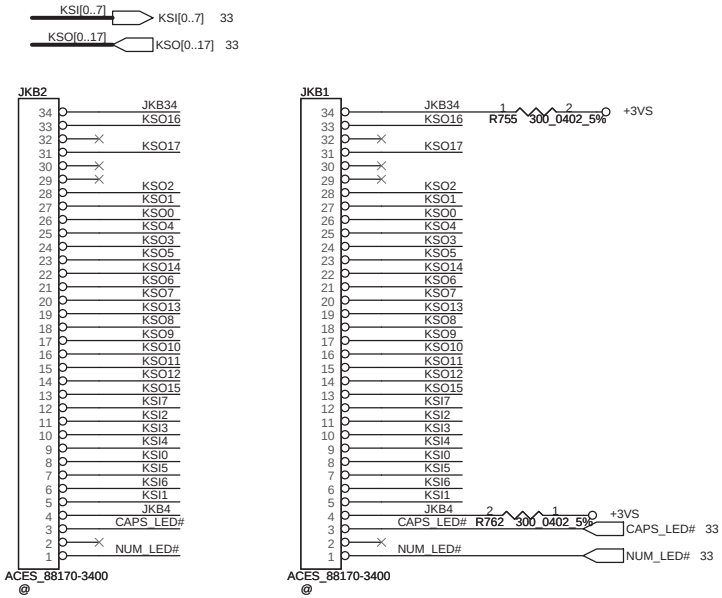


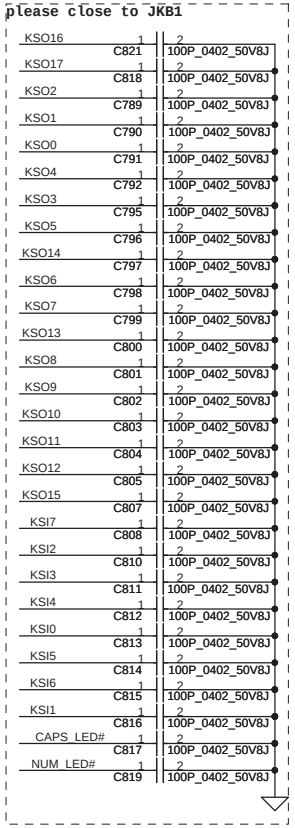
MDC 1.5 Conn.



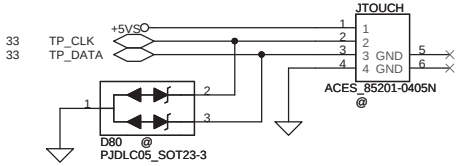
KEYBOARD CONN. for 17"

KEYBOARD CONN. for 16"

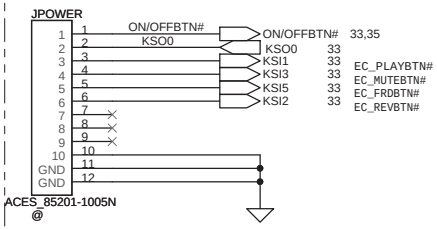


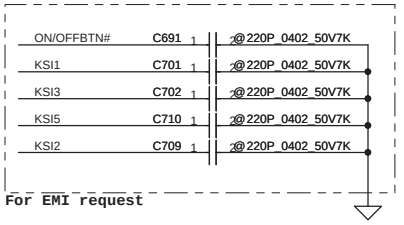


Touch/B Connector



SW/B Connector





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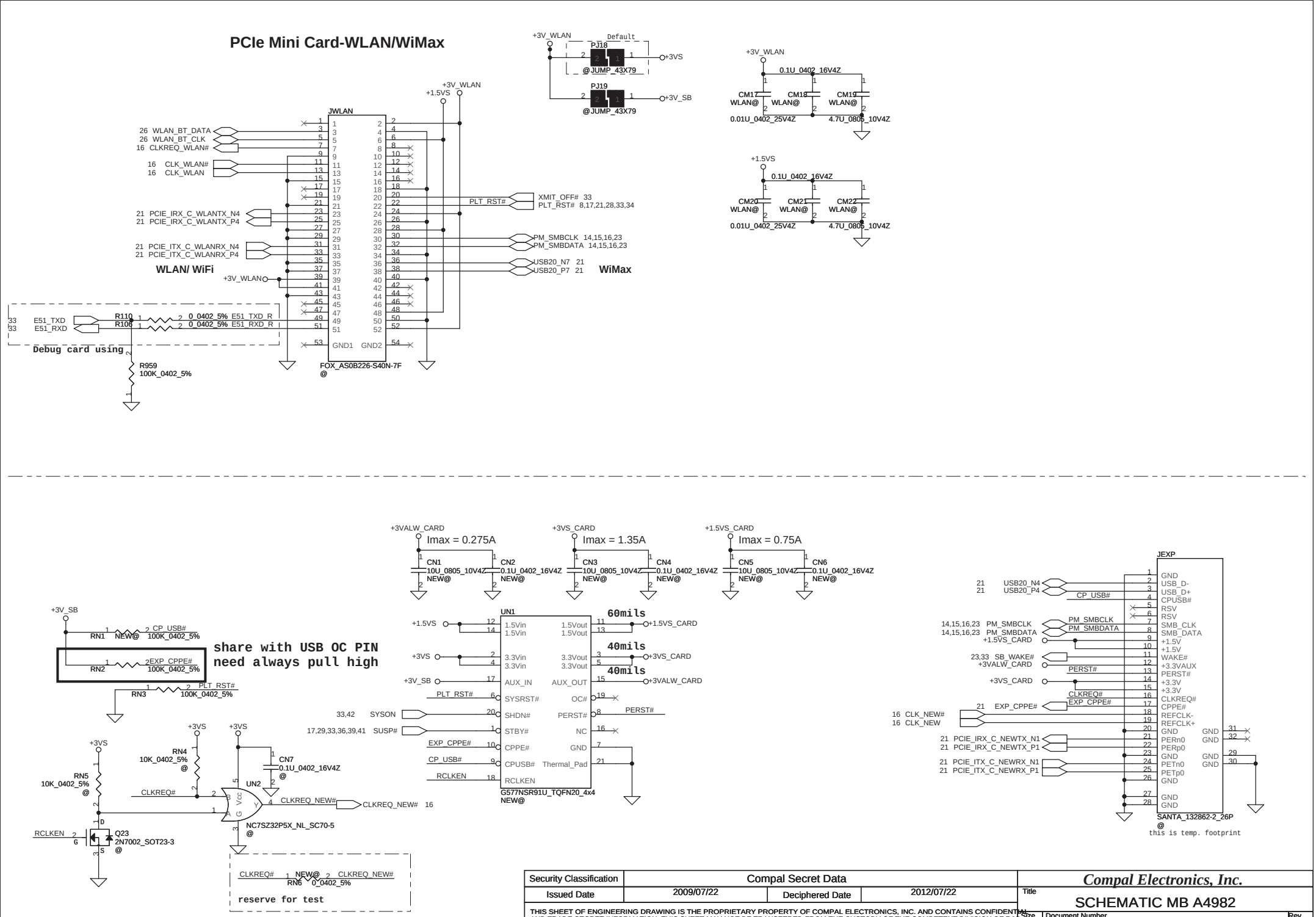

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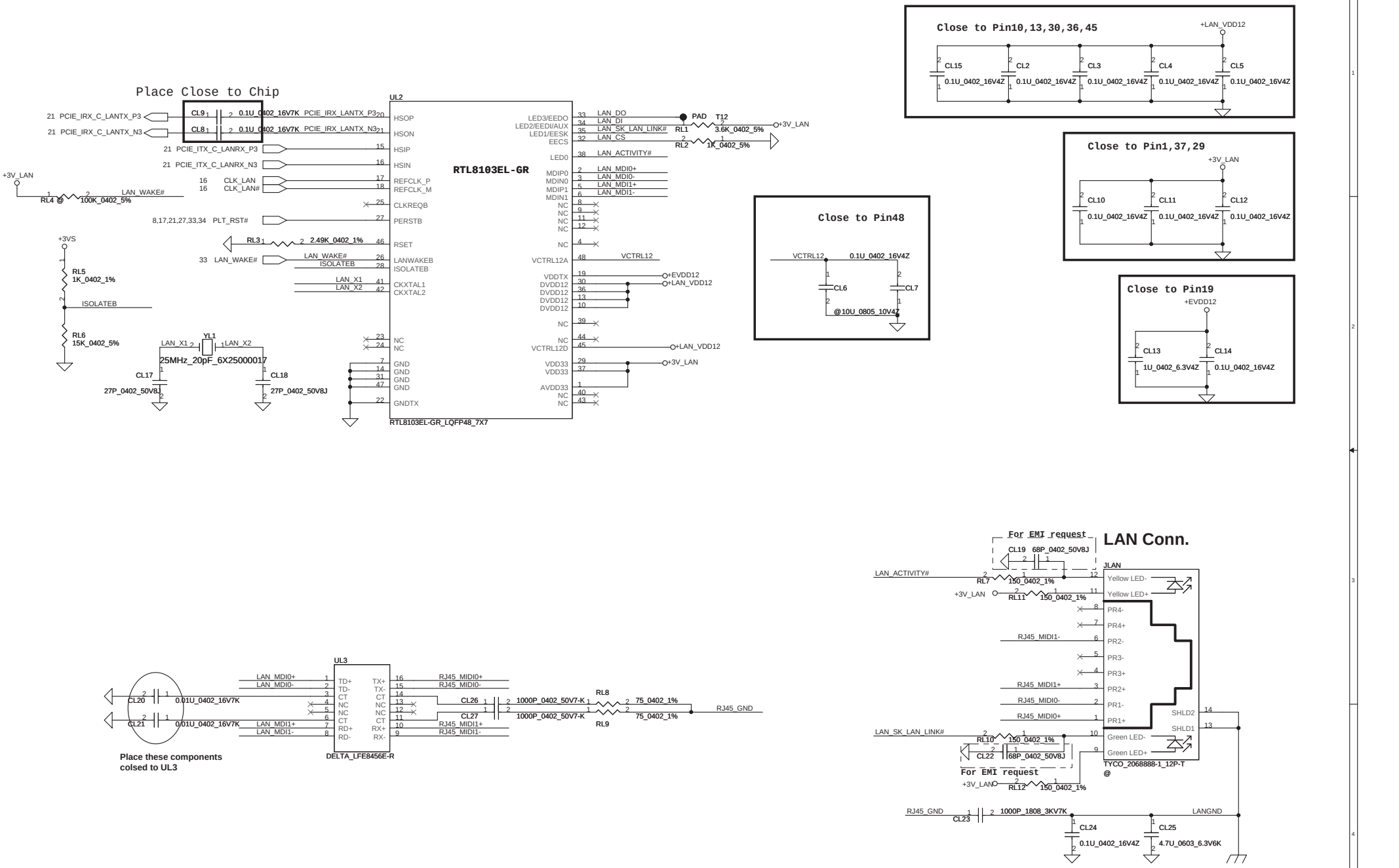

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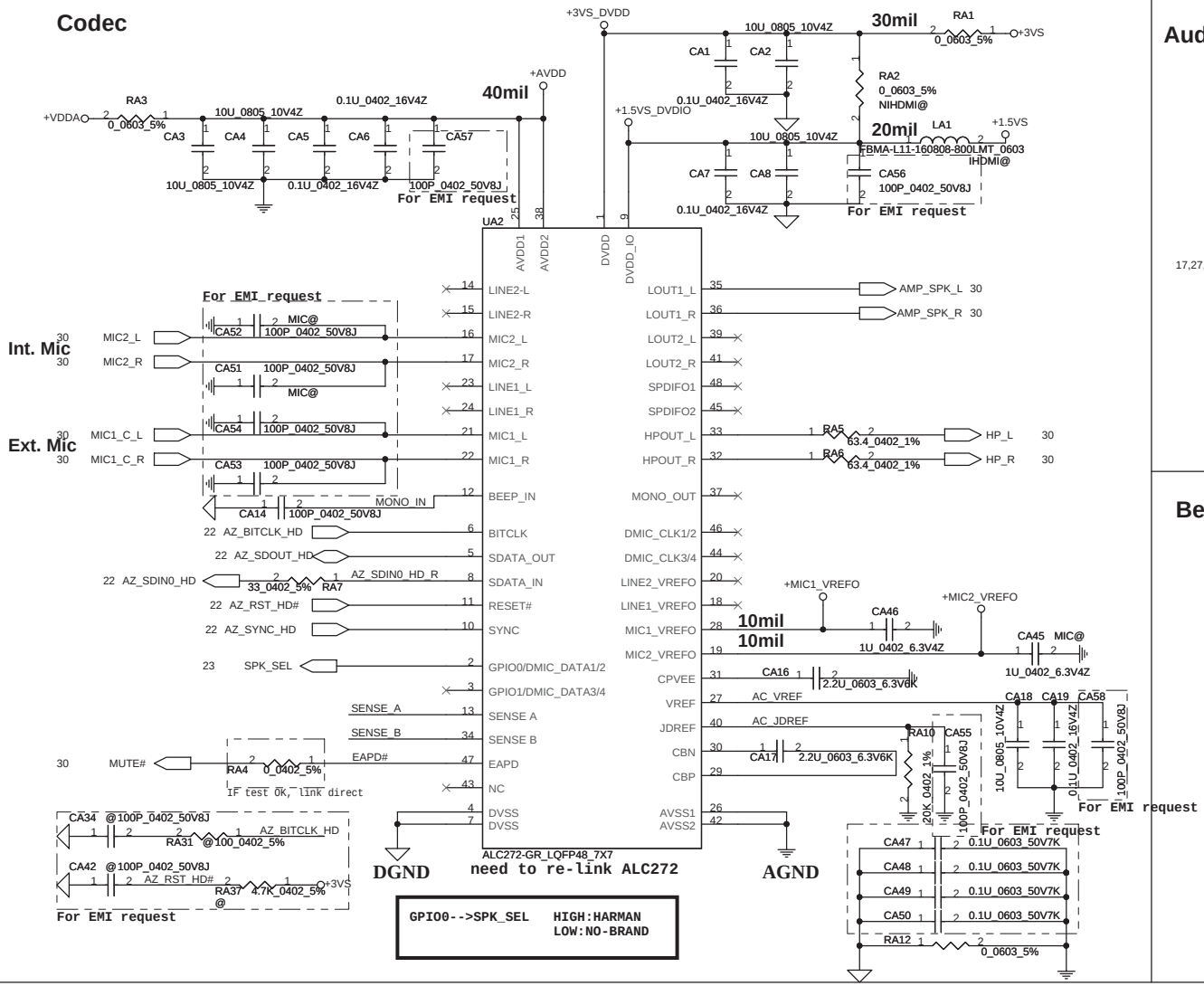
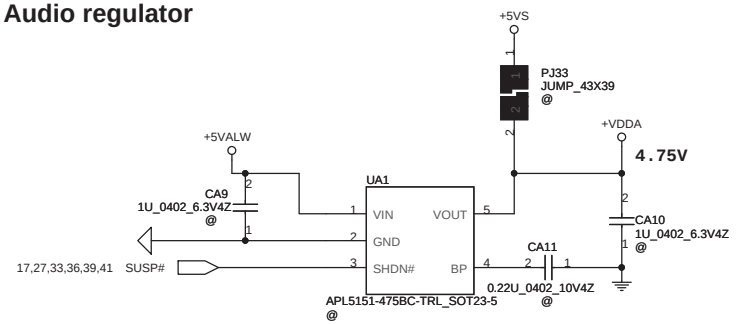
Codec

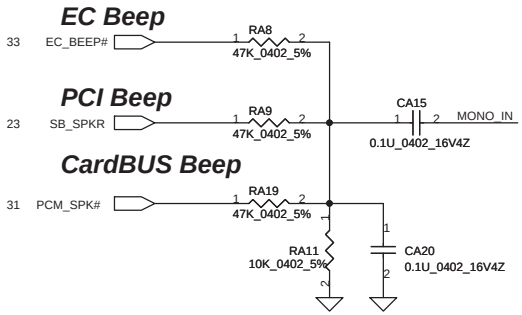


GPIO0-->SPK_SEL HIGH:HARMAN
LOW:NO-BRAND

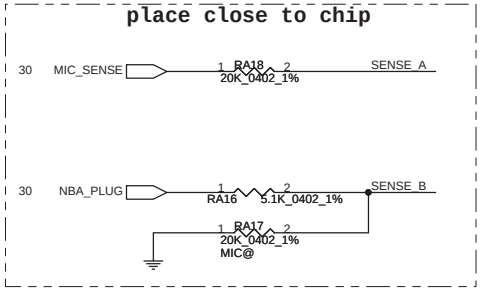
Audio regulator



Beep sound



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



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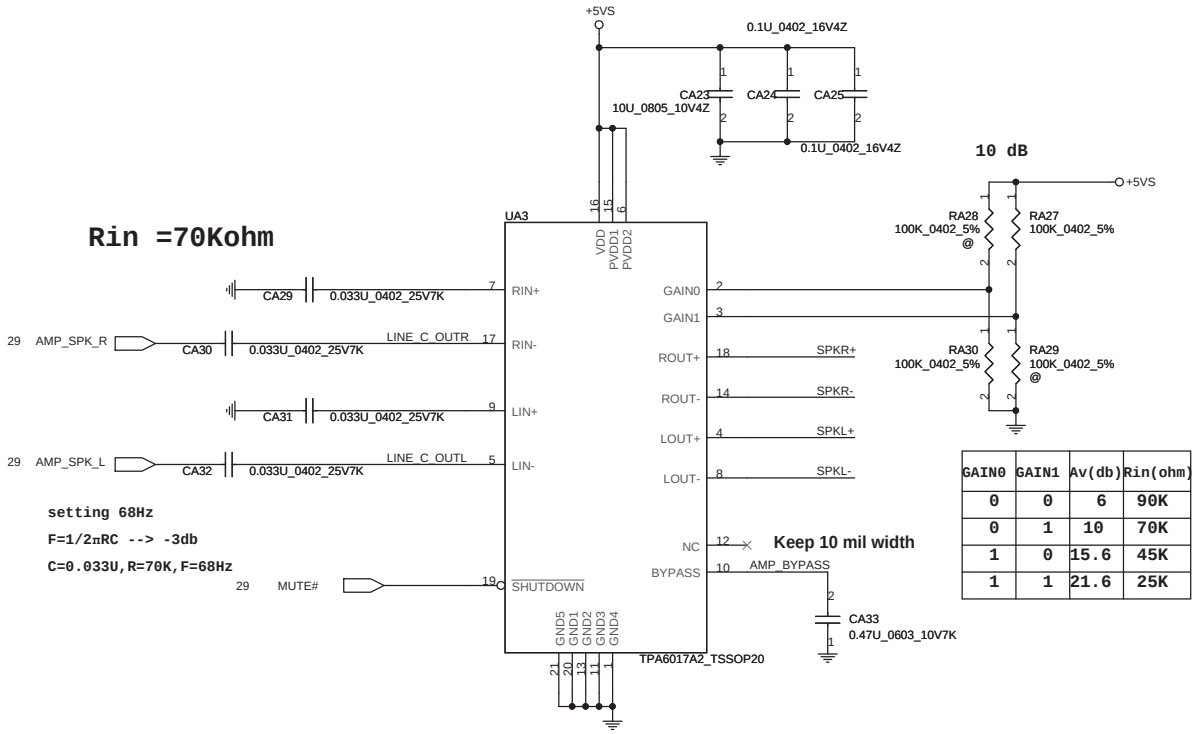
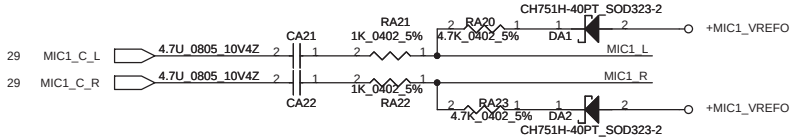
TPA6017 Medium Range Amplifier

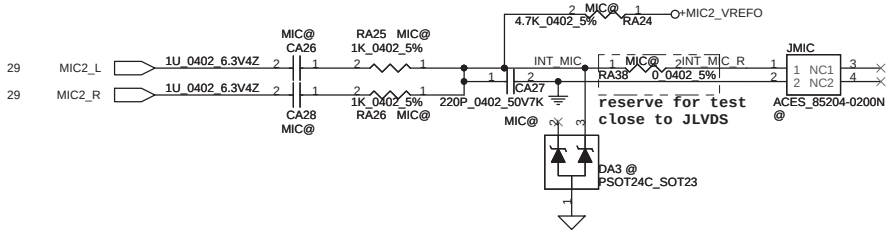


GAIN0	GAIN1	Av(db)	Rin(ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

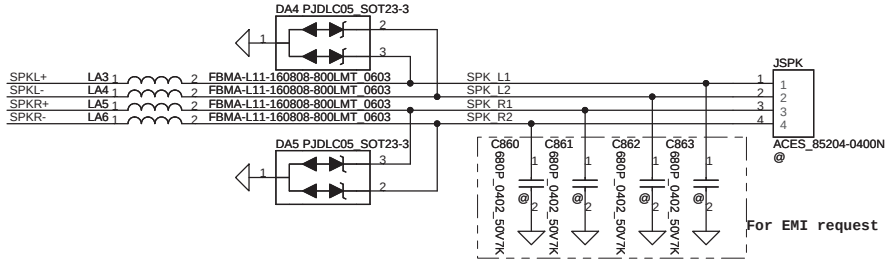
Ext. Mic



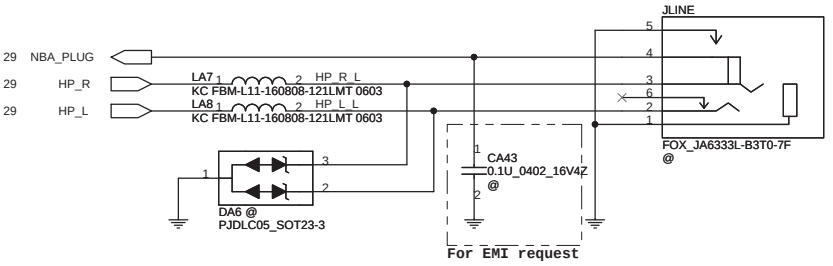
Int. Mic



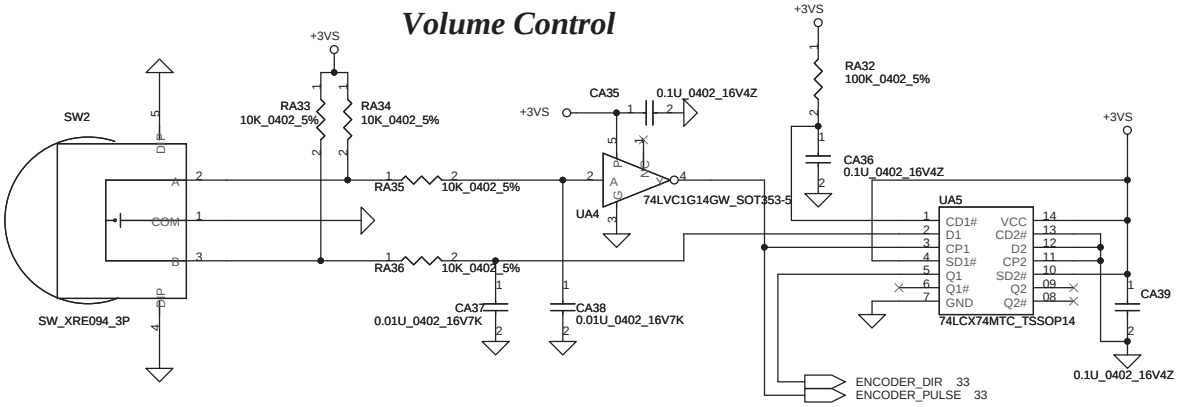
Speaker Connector



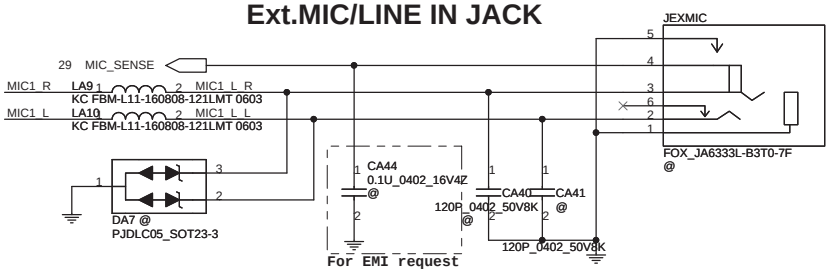
HeadPhone/LINE Out JACK



Volume Control



Ext.MIC/LINE IN JACK



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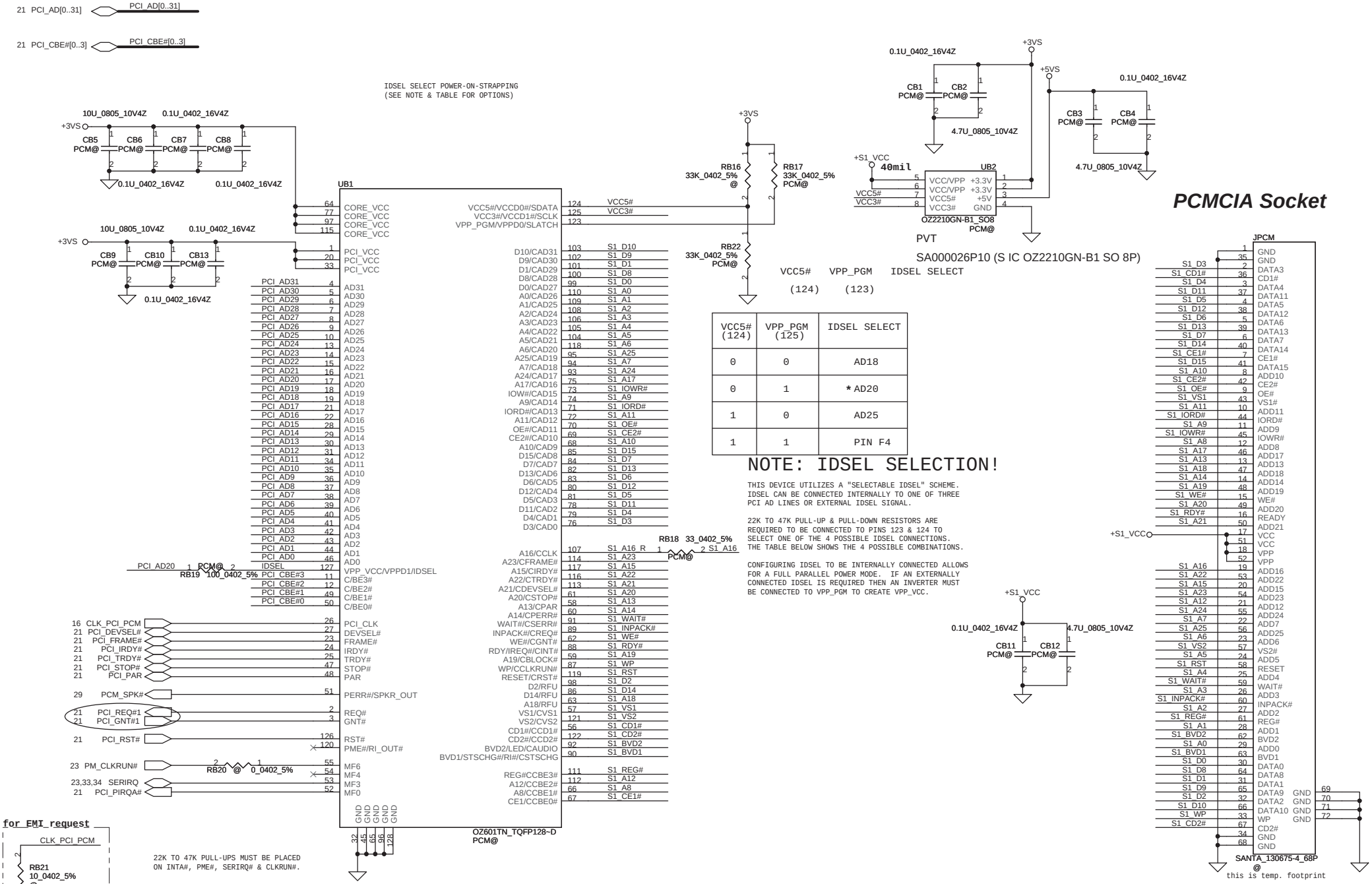

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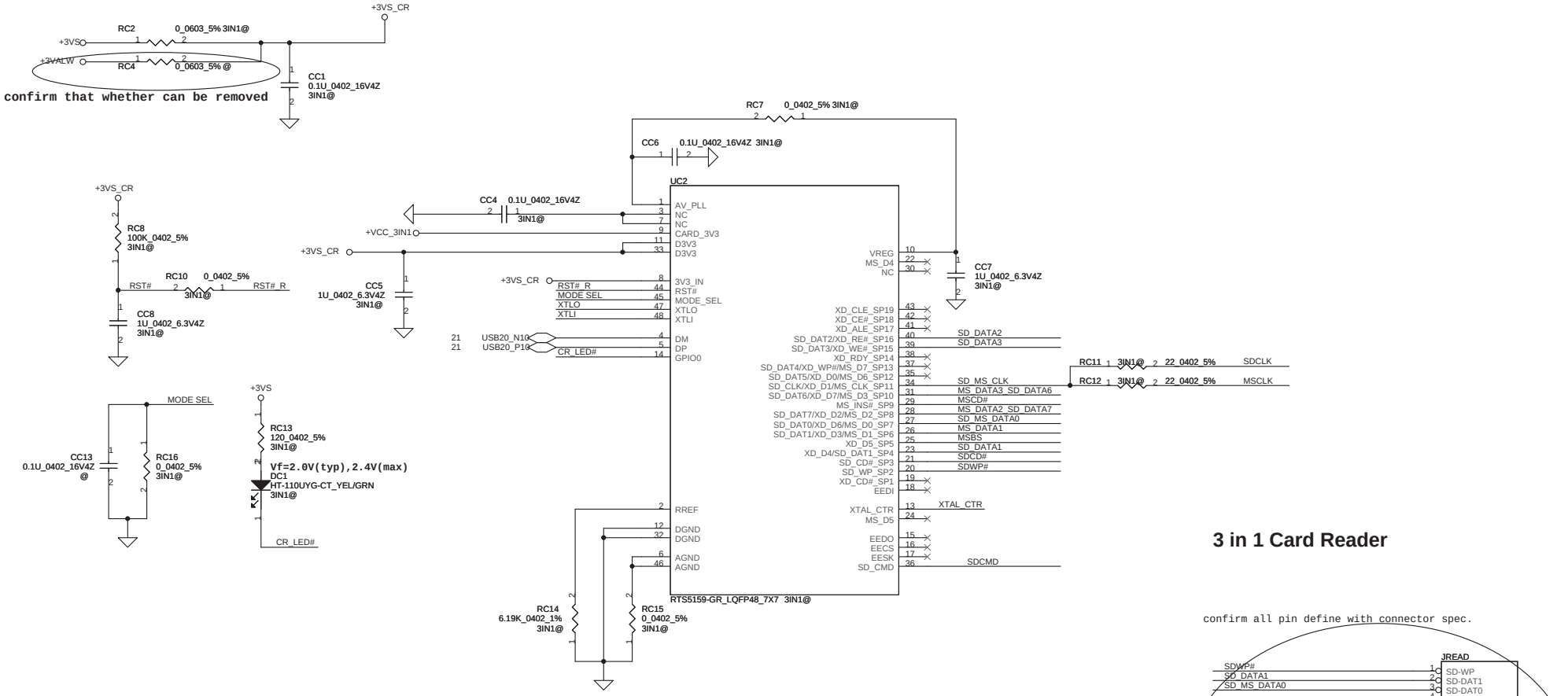

R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

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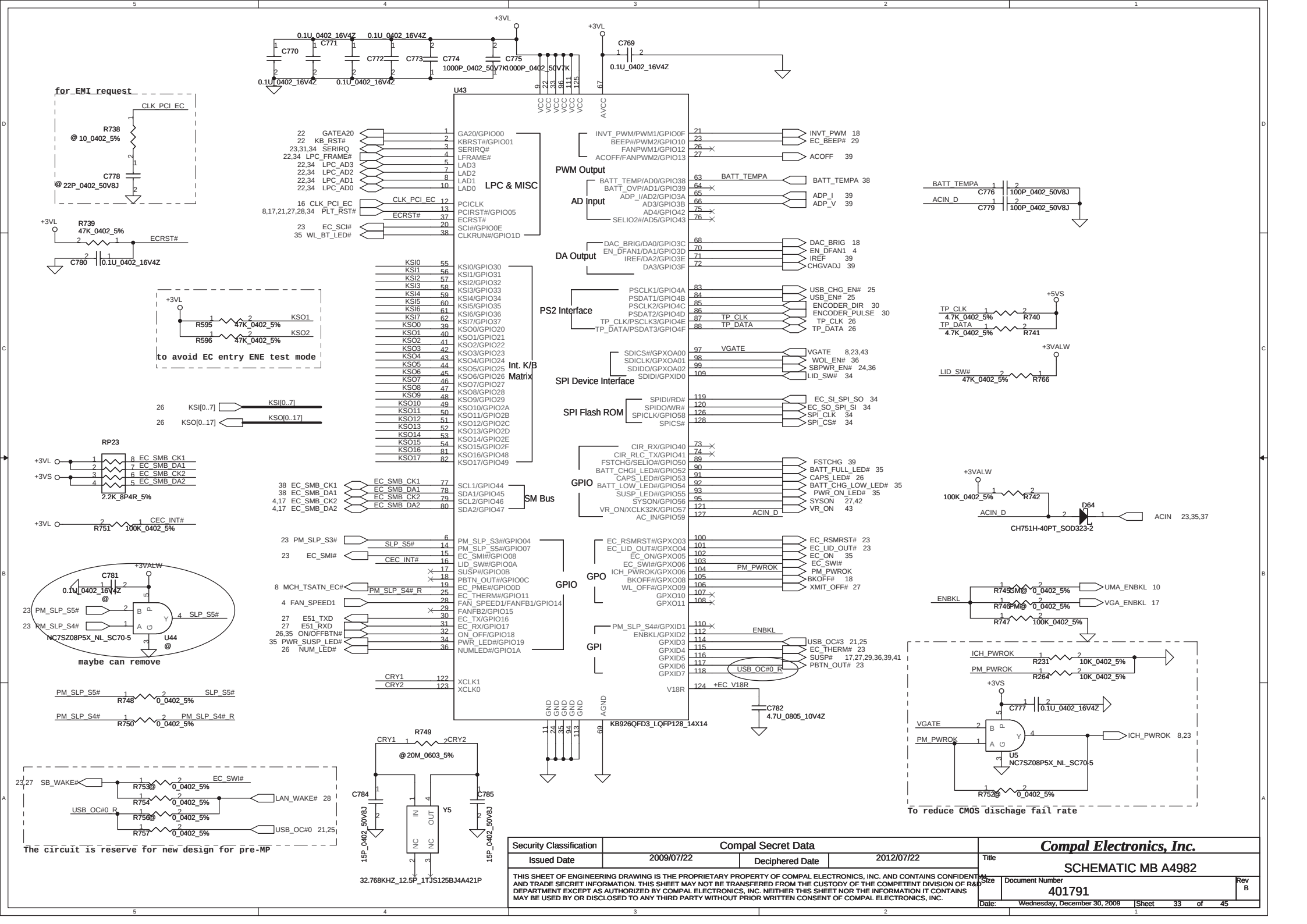
U43
KB926QFD3_LQFP128_14X14
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
for EMI request
to avoid EC entry ENE test mode
maybe can remove
The circuit is reserve for new design for pre-MP
To reduce CMOS dischage fail rate
32.768KHZ_12.5P_1TJS125BJ4A421P
CH751H-40PT_SOD323-2
NC7SZ08P5X_NL_SC70-5
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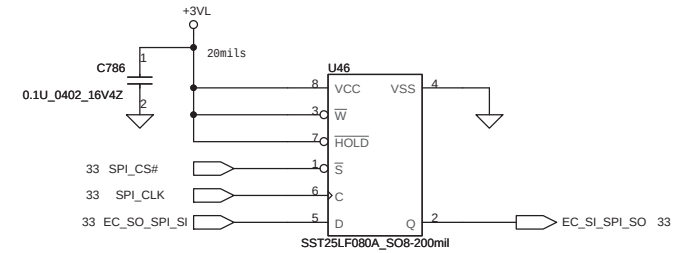
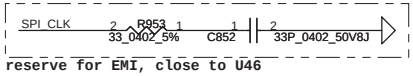
SPI Flash (16Mb*1)

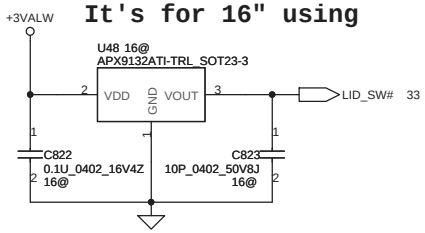




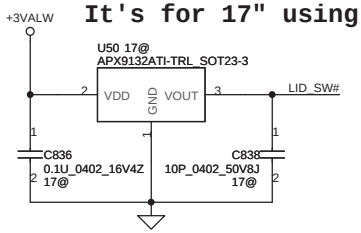
reserve for EMI, close to U46

Lid SW

It's for 16" using

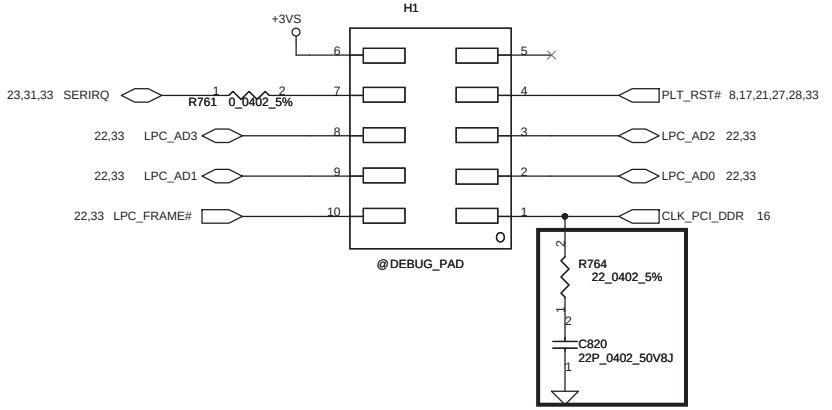


It's for 17" using



LPC Debug Port

Please place the PAD under DDR DIMM.



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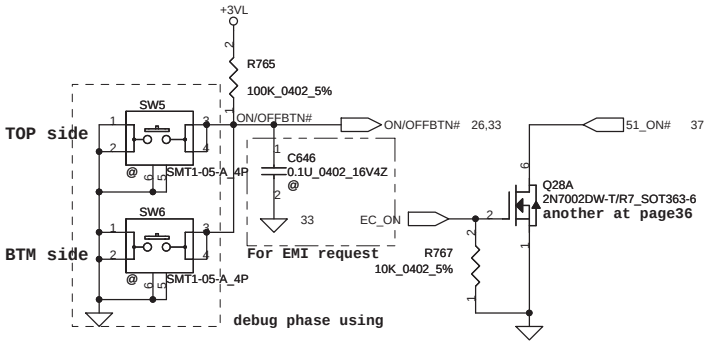
Power Button

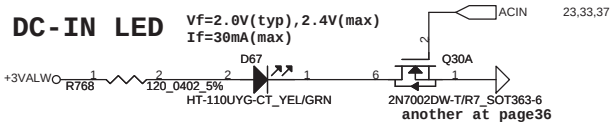


ISPD

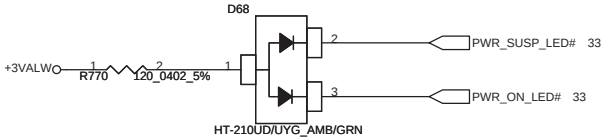
PCB	ZZZ PCB ZKU LA-4982P REV1	NB_PM_R3	U3 CANTIGA PM PMR3@	NB_PM_R1	U3 CANTIGA PM PMR1@		
DC-IN 16	PJP1 PJP1 KSWAA45@	NB_GL40_R3	U3 CANTIGA GL40 GL40R3@	NB_GL40_R1	U3 CANTIGA GL40 GL40R1@		
DC-IN 17	PJP1 PJP1 KTWAA45@	NB_GM45_R1	U3 CANTIGA GM45 GM45R1@	SB_R1	U9 ICH9-M ES ICH9R1@		

DC-IN LED

Vf=2.0V(typ),2.4V(max)
If=30mA(max)

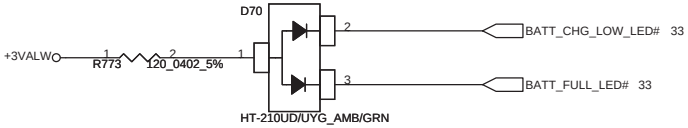


POWER/SUSPEND LED



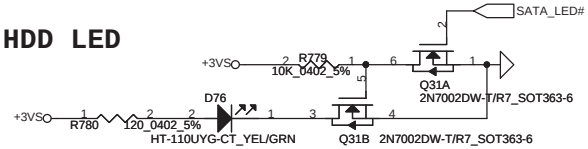
BATT CHARGE/FULL LED

Vf=1.9V(typ),2.4V(max) for amber
Vf=2.0V(typ),2.4V(max) for green
If=30mA(max)

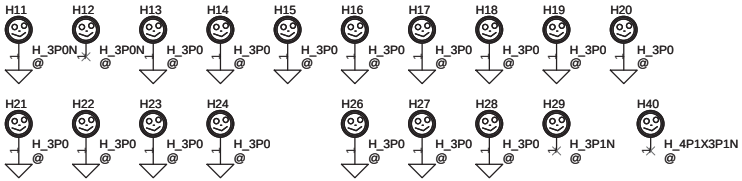


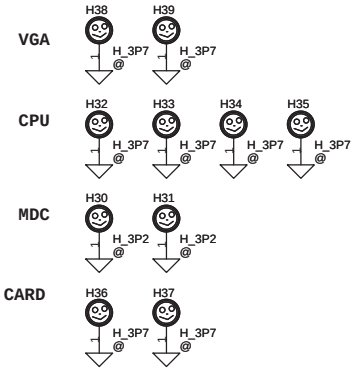
WL&BT LED

HDD LED



Screw Hole





PCB Fedical Mark PAD

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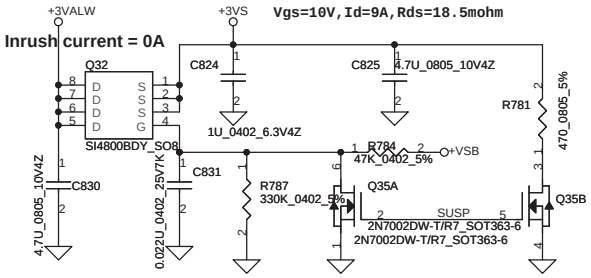
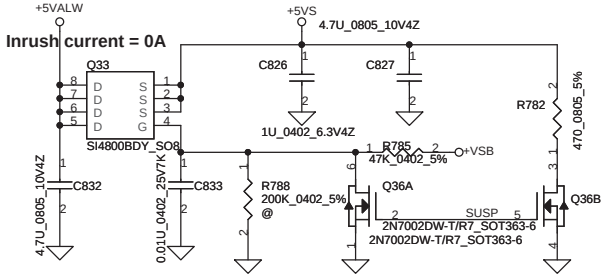
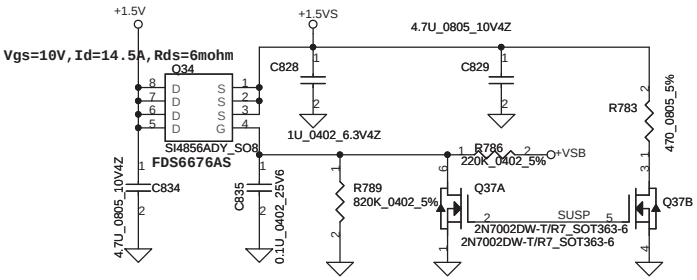
+3VALW TO +3VS



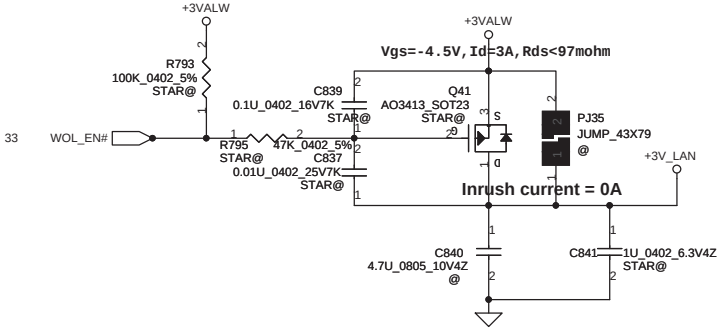
+5VALW TO +5VS



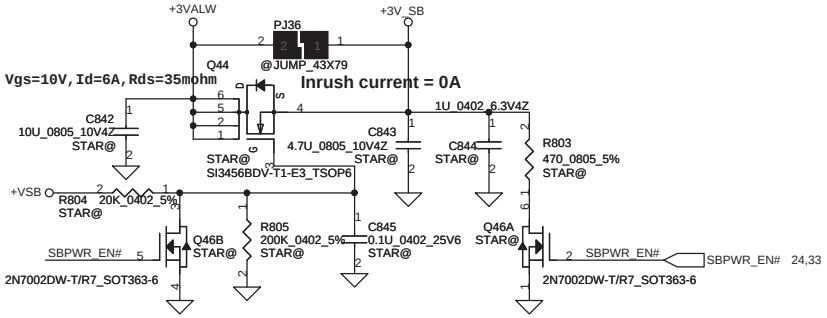
+1.5V to +1.5VS

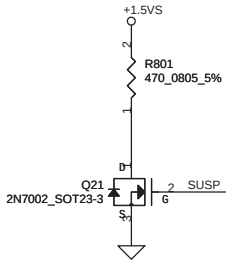


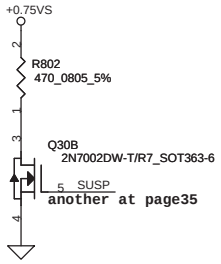
+3VALW TO +3V_LAN

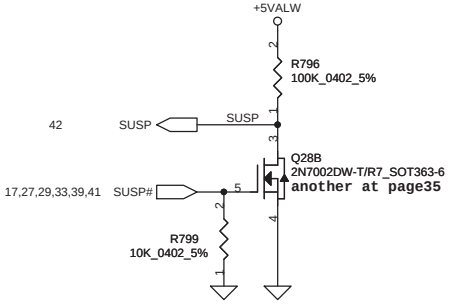


+3VALW TO +3V_SB









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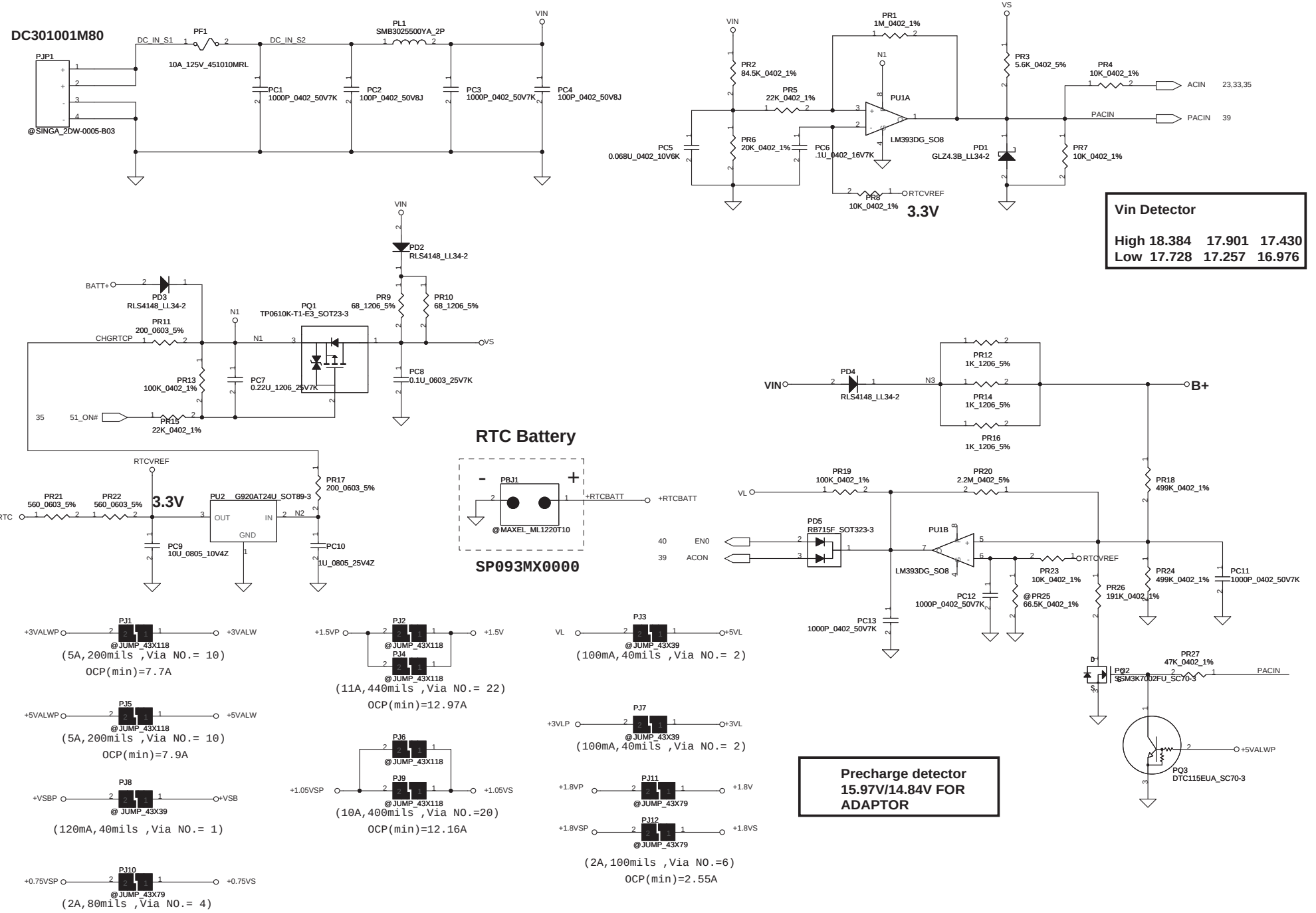

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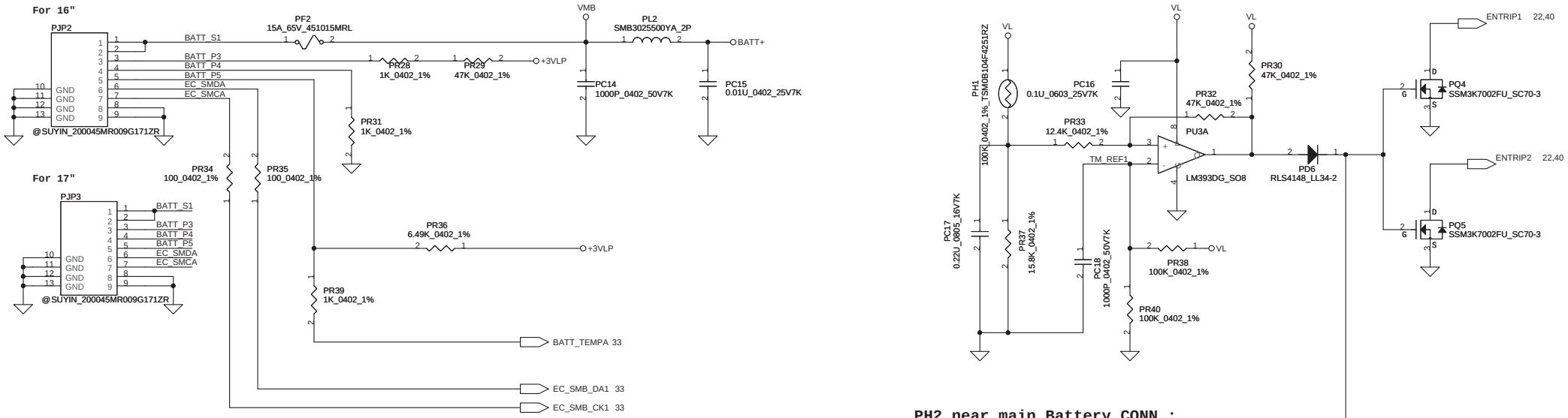
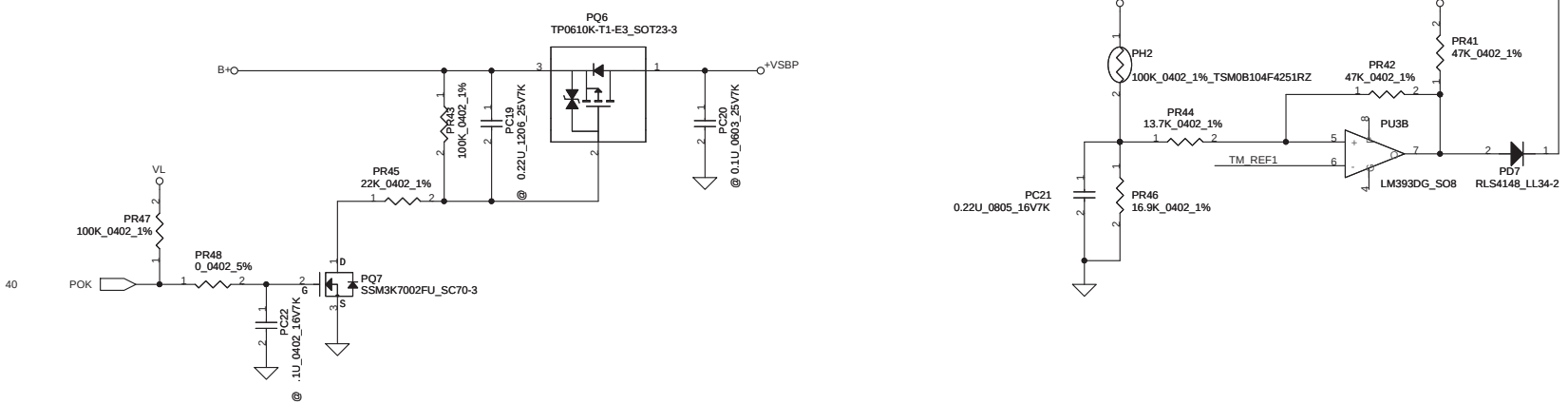
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 90 degree C
Recovery at 53 degree C



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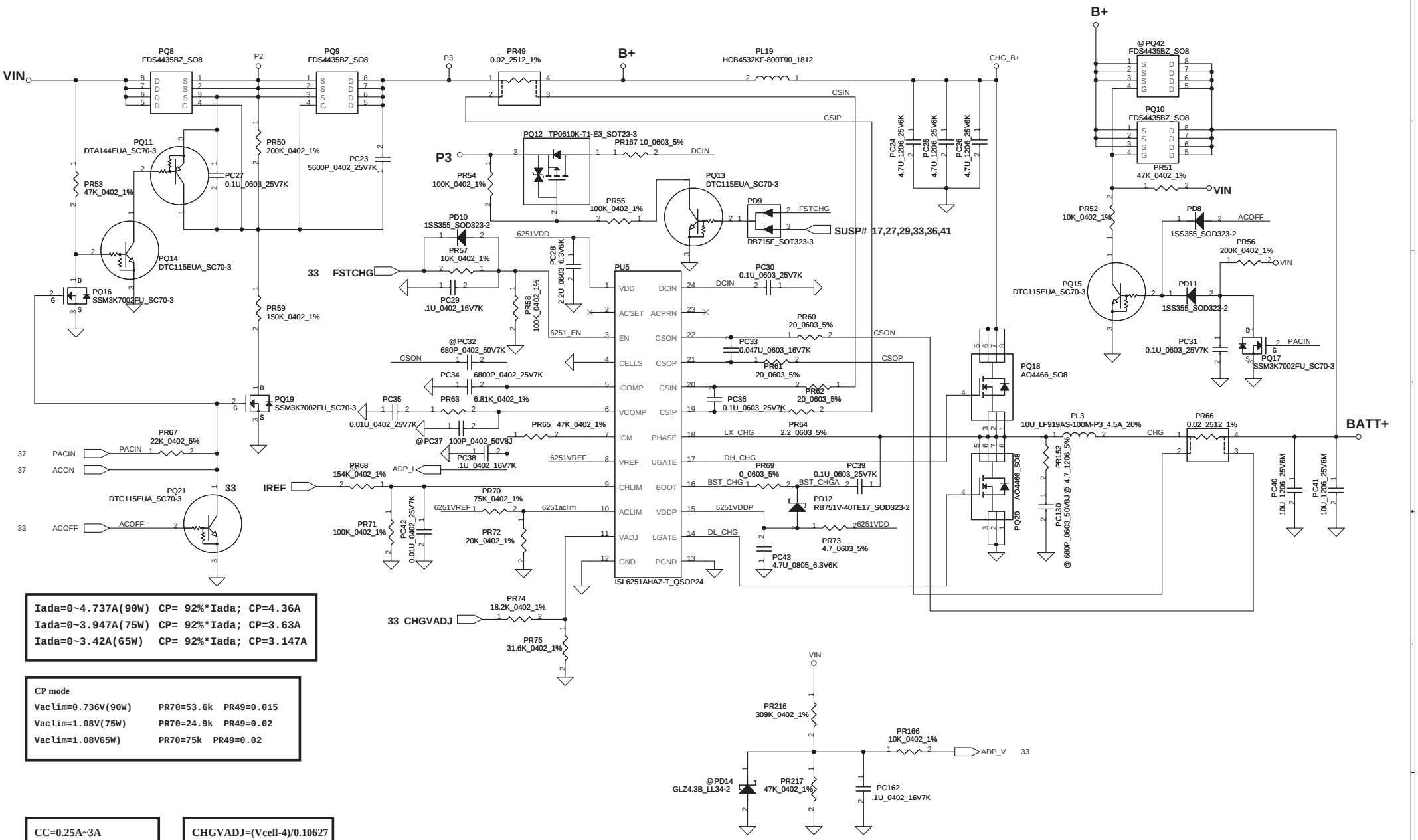

Iada=0~4.737A(90W) CP= 92%*Iada; CP=4.36A
Iada=0~3.947A(75W) CP= 92%*Iada; CP=3.63A
Iada=0~3.42A(65W) CP= 92%*Iada; CP=3.147A

CP mode		
Vaclim=0.736V(90W)	PR70=53.6k	PR49=0.015
Vaclim=1.08V(75W)	PR70=24.9k	PR49=0.02
Vaclim=1.08V65W)	PR70=75k	PR49=0.02

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CELLS	VDD	GND	Float
CELL number	4	3	2

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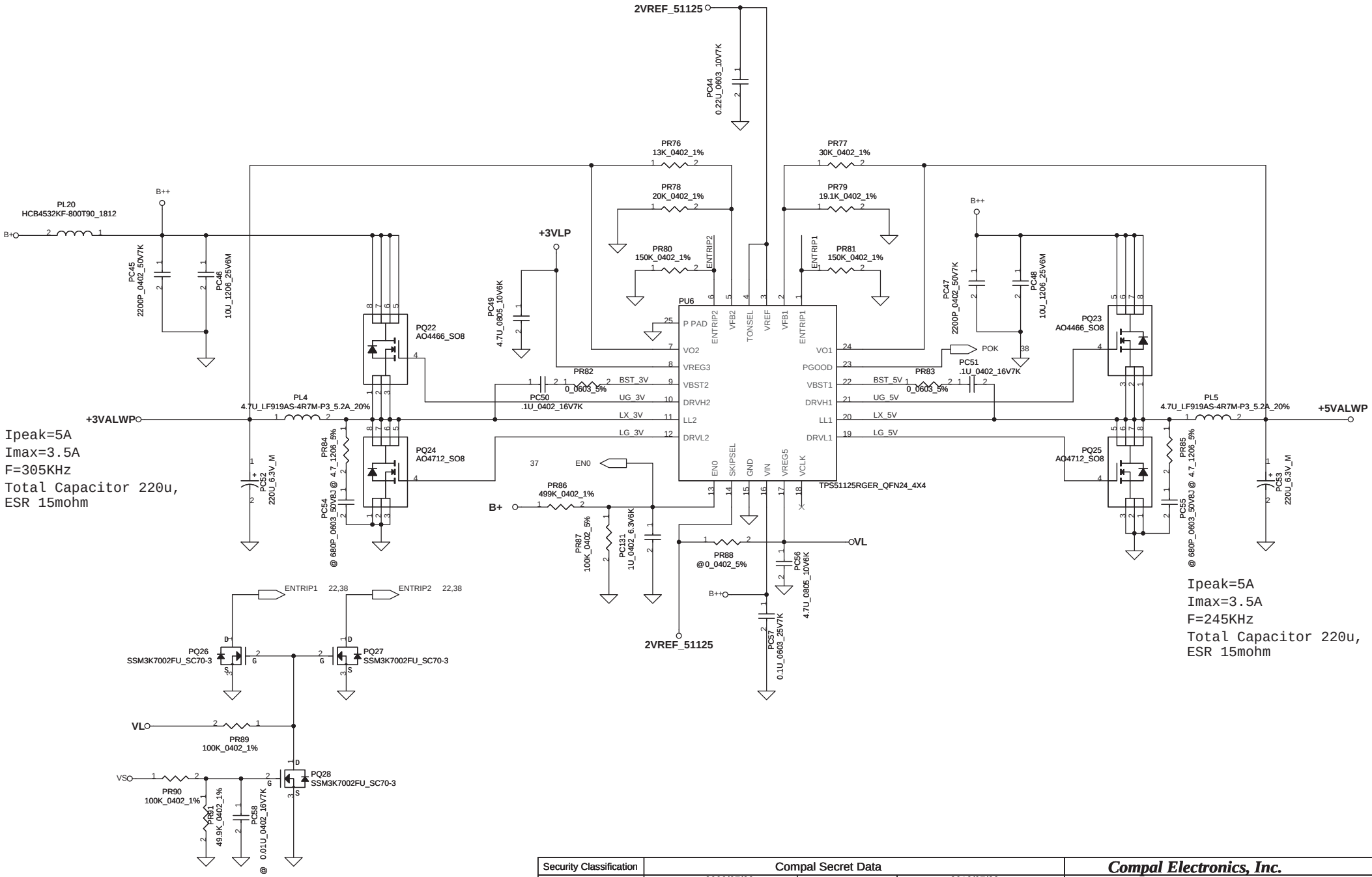

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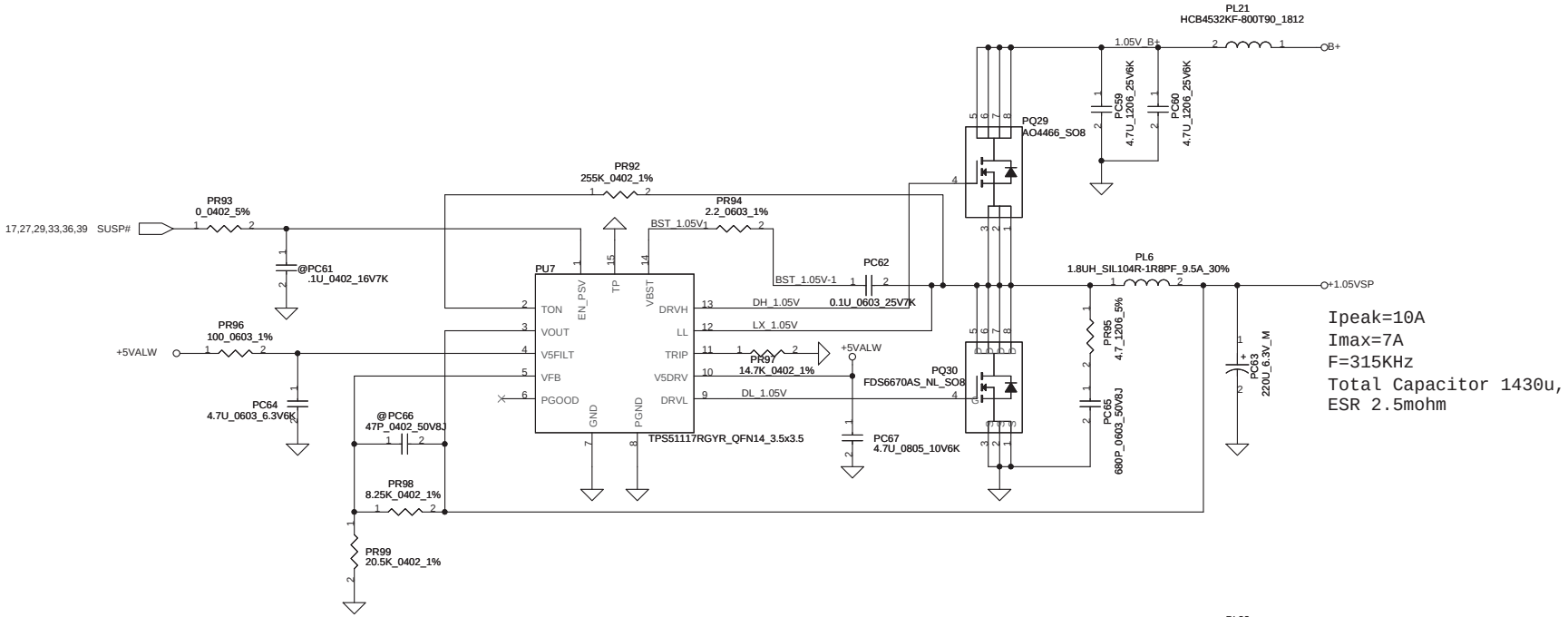
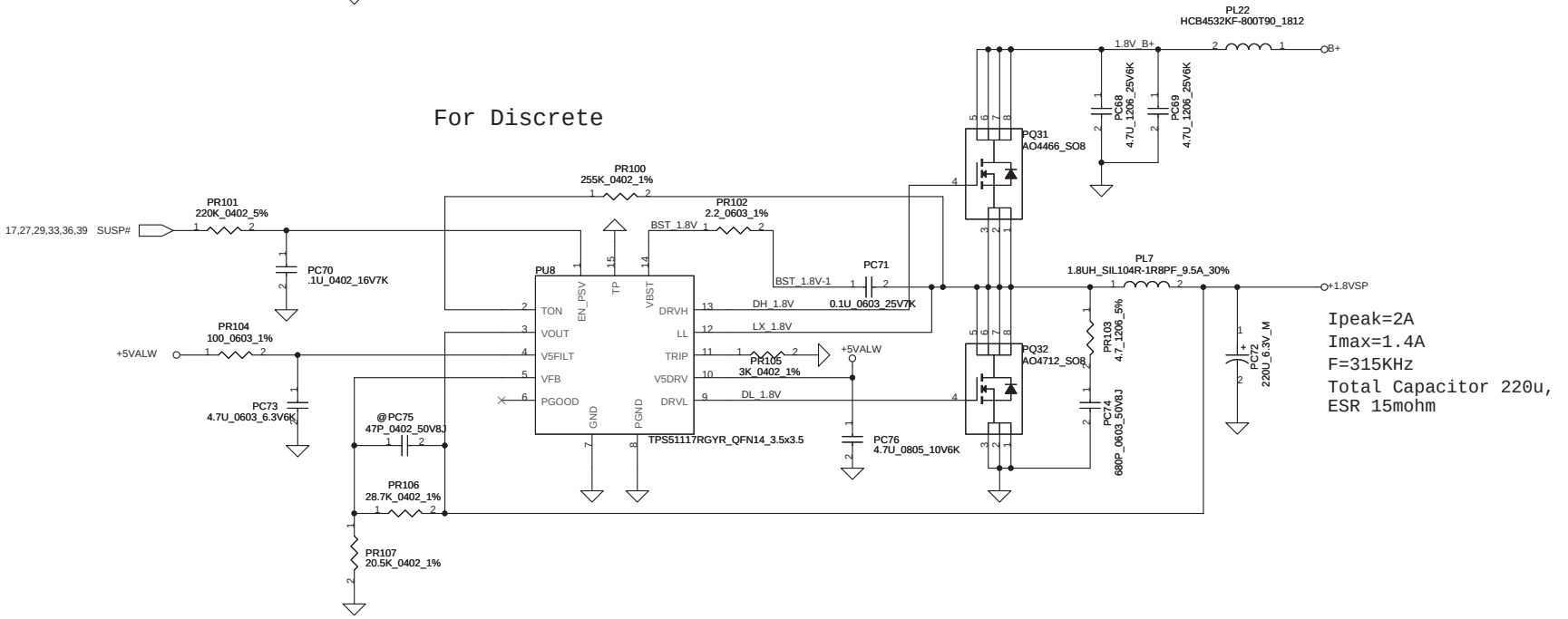


Ipeak=10A
Imax=7A
F=315KHz
Total Capacitor 1430u,
ESR 2.5mohm

For Discrete



Ipeak=2A
Imax=1.4A
F=315KHz
Total Capacitor 220u,
ESR 15mohm

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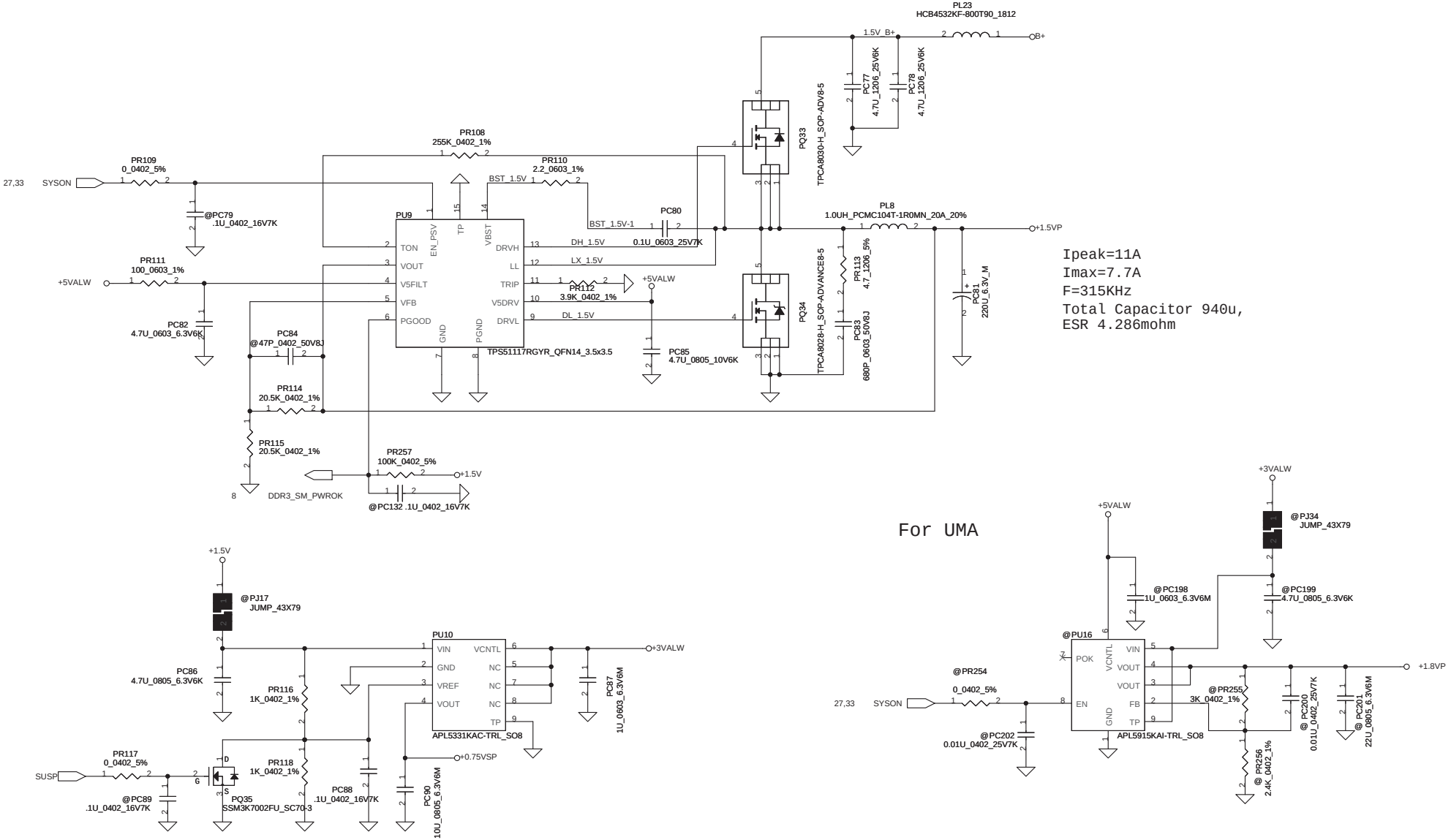

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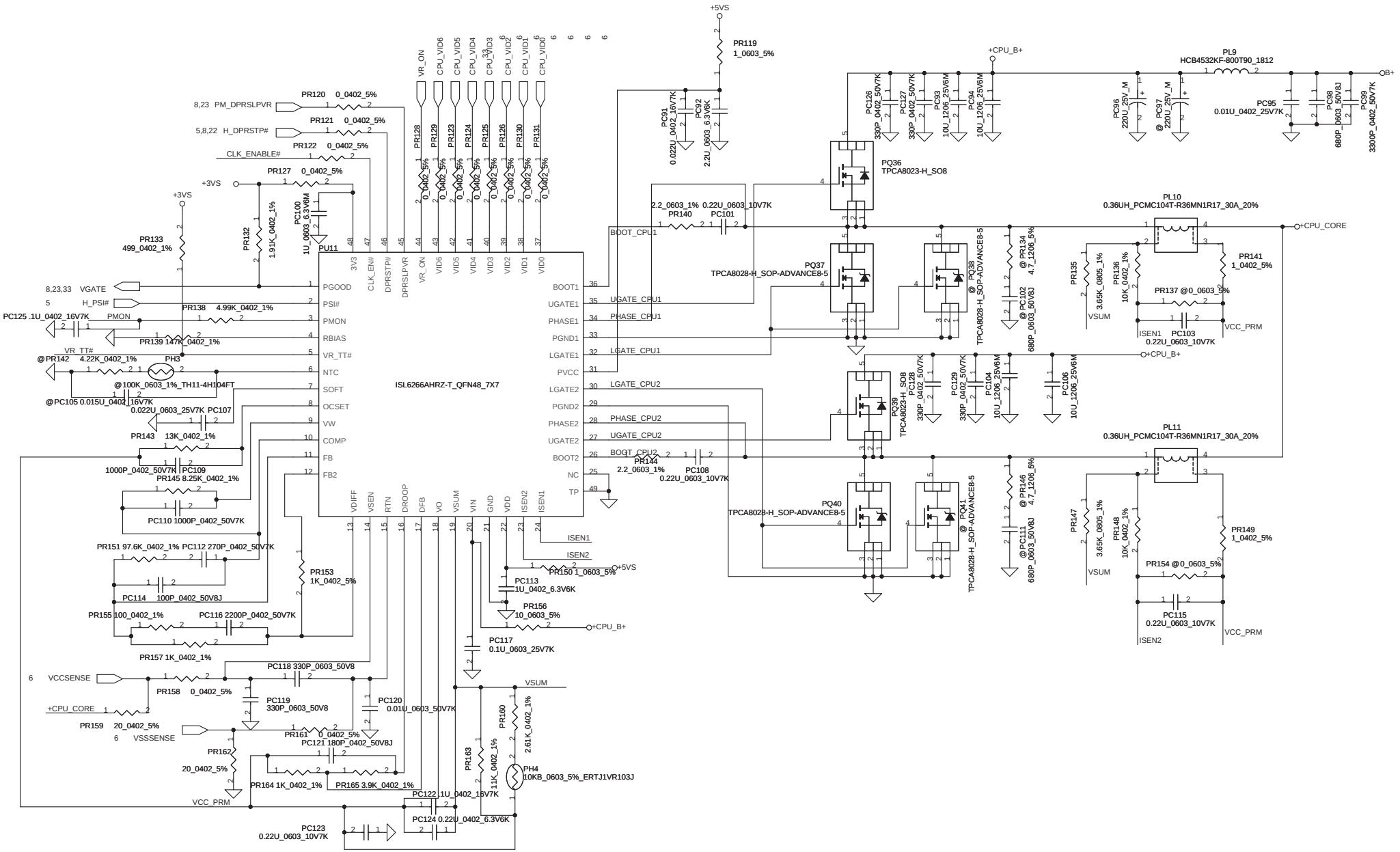

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT		P42-+CPU_CORE	change PU11 ISL6262 to ISL6266	change CPU_CORE IC
			Change PR145 6.81k to 8.25k	modify the parameter for ISL6266
			Change PC112 470P to 270P	
			Change PC114 220P to 100P	
			Change PC116 1000P to 2200P	
			Change PR155 255 to 100	
			Change PC118 0.018U to 330P	
			Change PC119 0.018U to 330P	
			Change PC120 0.018U to 0.01U	
			Change upop component PC96 to PC97	
EVT		P40-1.05V/1.5V	Change PR97 13.7k to 14.7k	Modify trip resistor for ocp
EVT		P41-1.8VP/0.9VSP	Change PR112 15.4k to 18k	Modify trip resistor for ocp
EVT		P38-CHARGER	Add PC162 0.1U	Add detect adapter function
			Add PR216 309k	
			Add PR217 47k	
			Add PD14 GLZ4.3B	
EVT		P38-CHARGER	Change PR49 0.02 to 0.015	Set CP for 90W(X6366051L02)
			Change PR70 24k to 53.6k	
			Change PQ8,PQ9,PQ10,PQ42 FDS4435 to AO4407A	For 90W(X6366051L02)
			Change PR69 2.2 to 0	
EVT		P38-CHARGER	Change PR70 24k to 24.9k	Set CP for 75W(X6366051L01)
DVT		P36-DCIN/DECTOR	Delete PD13	Precharge detector circuit modify
			ENTRIP1 signal change to EN0	
			ENTRIP2 signal change to ACON	
			Change PR23 34k to 10k	
			Add @ lable to PR25 66.5k	
DVT		P39-3VALWP/5VALWP	Add EN0 signal from PU6 pin 13	Precharge detector circuit modify
DVT		P38-CHARGER	Change PR70 24k to 75k	Set CP for 65W(X6366051L03)
DVT		P42-+CPU_CORE	Add PC126,PC127,PC128,PC129 330PF	For EMI solution
			Add PR134,PR146 4.7 ohm	
			Add PC102,PC111 680PF	
			Change PR140,PR144 0ohm to 2.2ohm	
DVT		P38-CHARGER	Change PR71 100k to 120k	Modify charging current for 12 cell
			Change PL3 16U to 10U	
DVT		P42-+CPU_CORE	Change PR145 8.25k to 11.3k	Modify switching frequency
PVT		P38-CHARGER	Change PL3 Part NO SH000003080 to SH162100M10	SH000003080 footprint is wrong
PVT		P36-DCIN/DECTOR	Change PU1 8 pin connect to N1	For precharge function
PVT		P38-CHARGER	Add PR166 10k Ohm	Modify ADP_V circuit(2009/02/18)
PVT		P38-CHARGER	Remove PD14	Modify ADP_V circuit(2009/02/18)
PVT		P38-CHARGER	Change PR74 18.2k to 15.4k	Change CHGVADJ voltage dividers value(2009/02/18)
PVT		P42-+CPU_CORE	Change PC126,PC127,PC128,PC129 (SE068331K80) to (SE00000FD80)	Change temperature tolerance K(10%) to J(5%)(2009/02/23)
PREMP		P38-CHARGER	Add PR167 10_0603_5%	Add 10 Ohm to DCIN circuit(2009/03/12)
PREMP		P38-CHARGER	Add PL19 HCB4532KF-800T90_1812 and delete PJ12	Add bead on B+ node(2009/03/12)
PREMP		P39-3VALWP/5VALWP	Add PL20 HCB4532KF-800T90_1812 and delete PJ13	Add bead on B+ node(2009/03/12)
PREMP		P40-1.05V/1.5V	Add PL21 HCB4532KF-800T90_1812 and delete PJ14	Add bead on B+ node(2009/03/12)
			Add PL22 HCB4532KF-800T90_1812 and delete PJ15	Add bead on B+ node(2009/03/12)
PREMP		P41-1.8VP/0.9VSP	Add PL23 HCB4532KF-800T90_1812 and delete PJ16	Add bead on B+ node(2009/03/12)
PREMP		P39-3VALWP/5VALWP	Change PR79 19.6k to 19.1k	Modify 5V to 5.14V(2009/04/08)
PREMP		P38-CHARGER	Change PR65 100 to 47k	For CPU throtting setting(2009/04/08)
PREMP			Change PR82,PR83,PR94,PR102,PR110 SD014000080 (0 +-1% 0603) to SD013000080 (0 +-5% 0603)	Component not haven 0_+-1%, change to 0_5%(2009/04/08)
PREMP		P42-+CPU_CORE	Change PC126,PC127,PC128,PC129 (SE0000FD80) to (SE074331K80)	Change property NPO to X7R(2009/04/08)
PREMP		P41-1.05VSP/1.8VP	Change PR96 422 ohm to 100 ohm	Avoid 2nd source RT8209B can not power on(2009/07/27)
			Change PC64 1U to 4.7U	
PREMP		P42-1.5VP/0.75VSP	Change PR111 422 ohm to 100 ohm	Avoid 2nd source RT8209B can not power on(2009/07/27)
			Change PC82 1U to 4.7U	
PREMP		P42-1.5VP/0.75VSP	Change PR112 14.7k to 3.9k	Set 1.5V OCP to 13.25A(2009/07/27)
PREMP		P40-3VALWP/5VALWP	Change PC52, PC53 SF22001M200 to SF000001H00	SF22001M200 is forbids to use (2009/08/04)
PREMP		P41-1.05VSP/1.8VP	Change PC63, PC72 SF22001M200 to SF000001H00	SF22001M200 is forbids to use (2009/08/04)
PREMP		P42-1.5VP/0.75VSP	Change PC81 SF22001M200 to SF000001H00	SF22001M200 is forbids to use (2009/08/04)
MP		P42-1.5VP/0.75VP	Change High,Low side Mosfet and Choke.	(2009/06/18)
			Add bead on B+ node	
MP		P38-BATTERY CONN / OTP	Change PR33 13.7k to 12.4k	Change resistor for OTP (2009/09/01)
			Change PR37 15.4k to 15.8k	

PIR (Product Improve Record)

KSWAA LA-4982P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	7/22	15	delete C604~C610,C643~C645	Change reference plane of control from VCC to GND
2	7/24	35	change PCB P/N to DAZ07300200	For load BOM
3	7/27	14	add CD45 and un-mount CD17,CD39 on DDR 1.5V	design change

Compal Electronics, Inc.

Title: SCHEMATIC MB A4982

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