

NSWAA/NTWAA

Liverpool 10G

Sunderland 10G

LA-5322P REV 1.0 Schematic

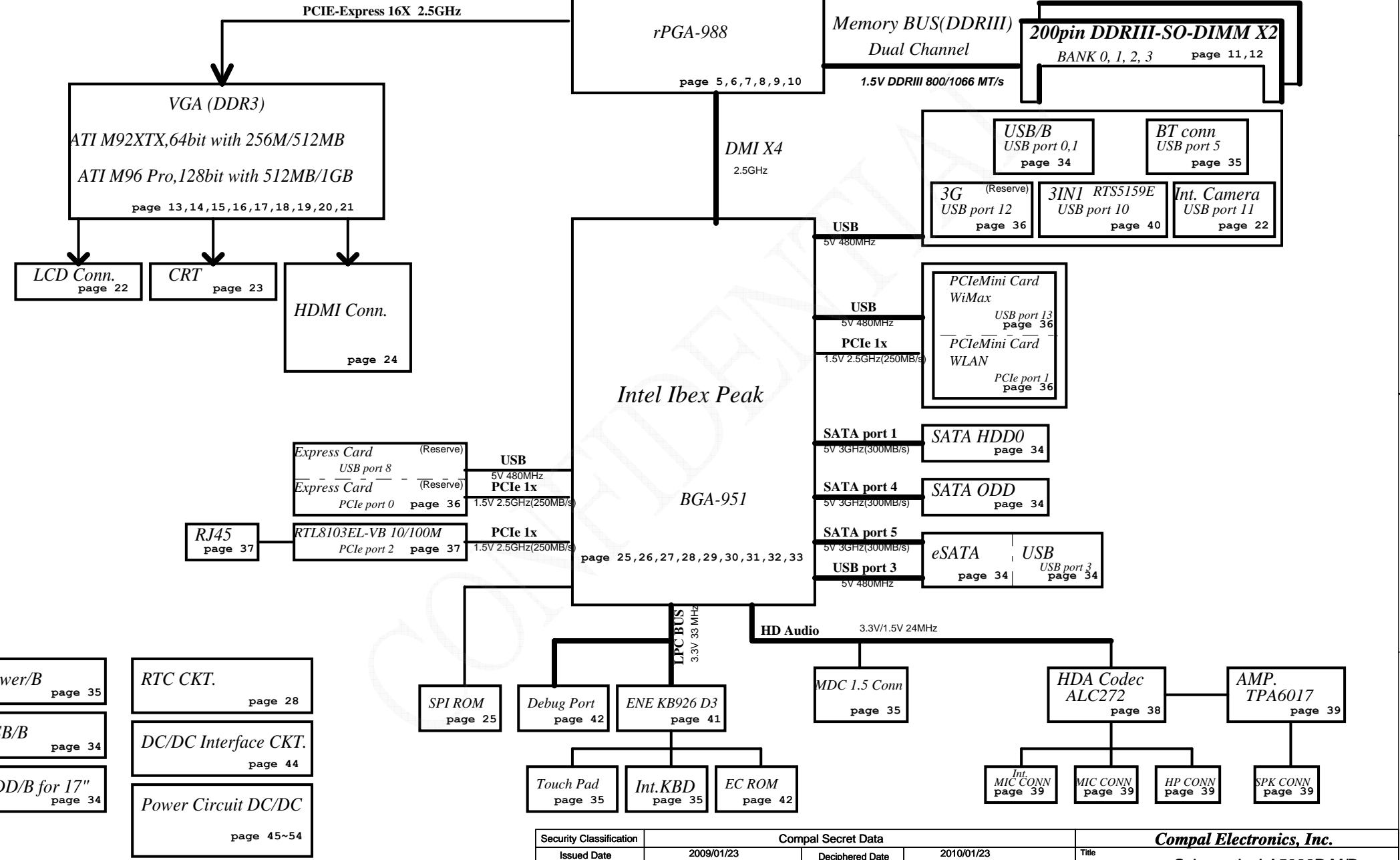
Intel Arrandale /IBEX PEAK

2009-12-22 Rev 1.0

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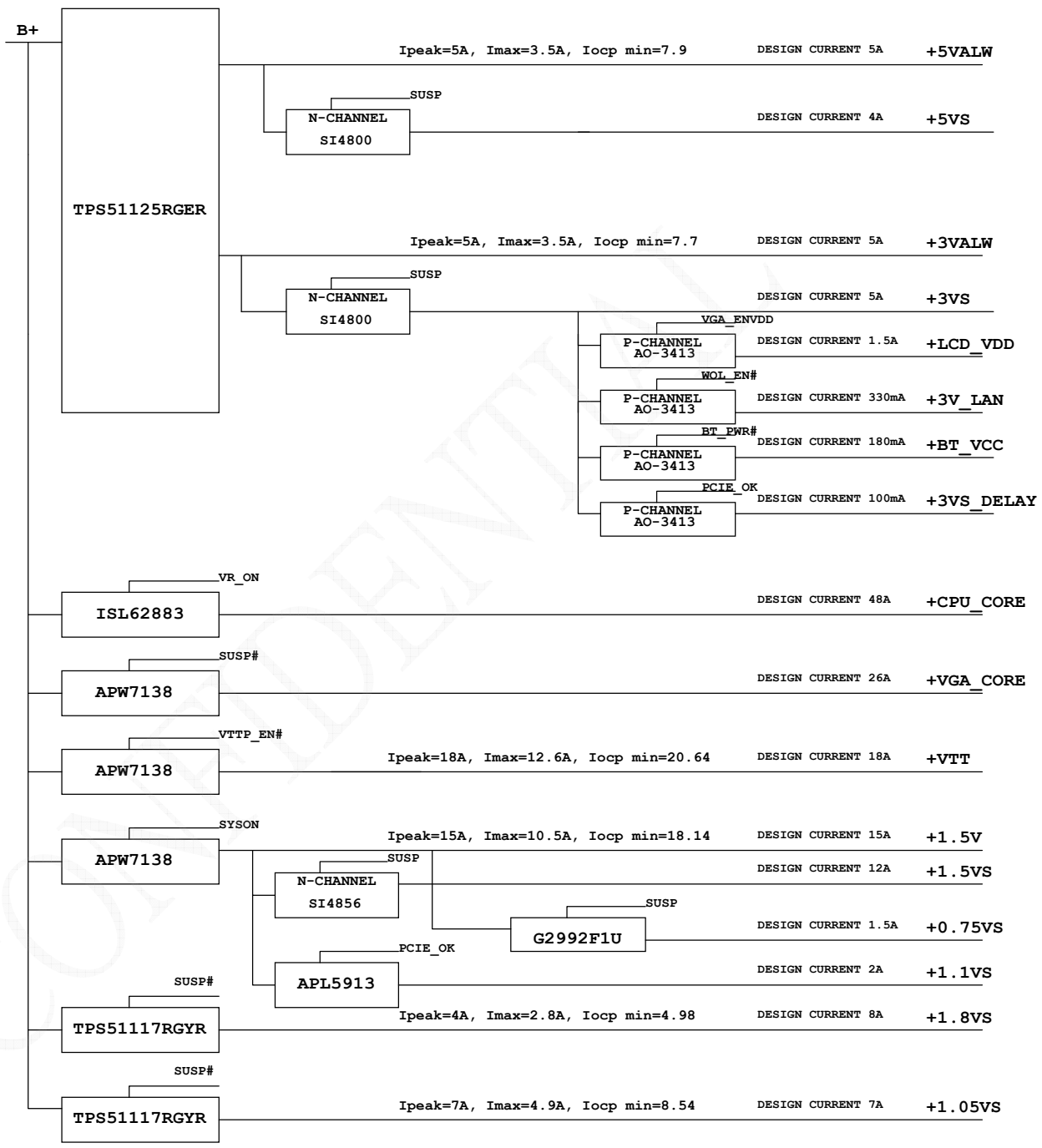
Compal Confidential

Model Name : NSWAA/NTWAA
File Name : LA-5322P



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NSWAA Liverpool Intel Arrandale (Discrete)
 NTWAA Sunderland Intel Arrandale (Discrete)



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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVC	+B	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

BTO Option Table

Function	Bluetooth	RJ11	Express Card	MIC	HDMI	Panel	M1/M3	
description	(B)		(E)		(Y)			
explain	Bluetooth	MDC	New Card	MIC	HDMI	16"	17"	M1 M3
BTO	BT@	MDC@	NEW@	MIC@	HDMI@	16@	17@	M1@ M3@

Function	Mini Card	VRAM			GPU	
description						
explain	WIRELESS	256M	512M	1G	M92 XTX	M96 Pro
BTO	WLAN@	2PCS@	4PCS@	8PCS@	M92XTX@	M96PRO@

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

EC SM Bus1 address

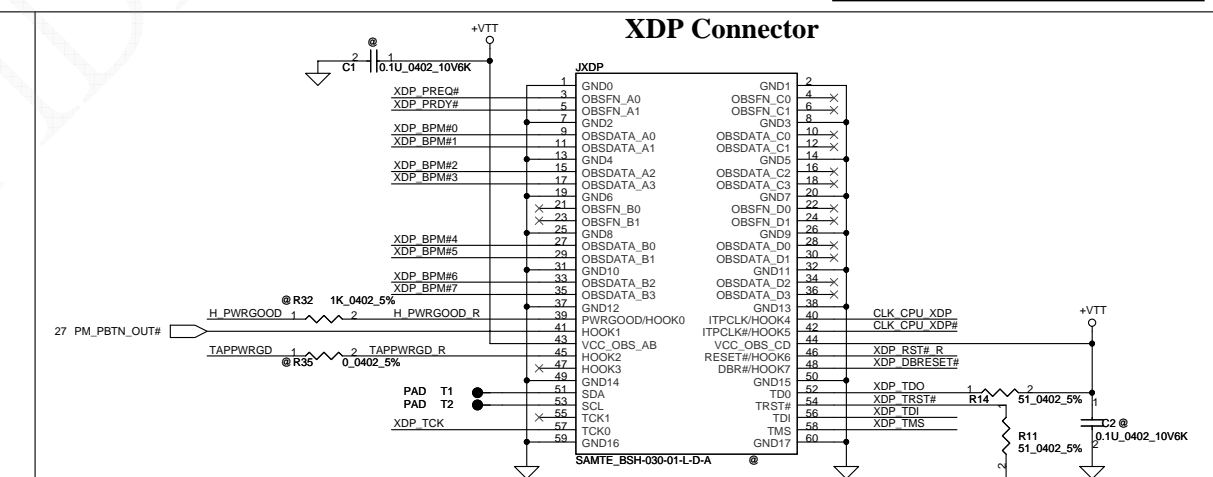
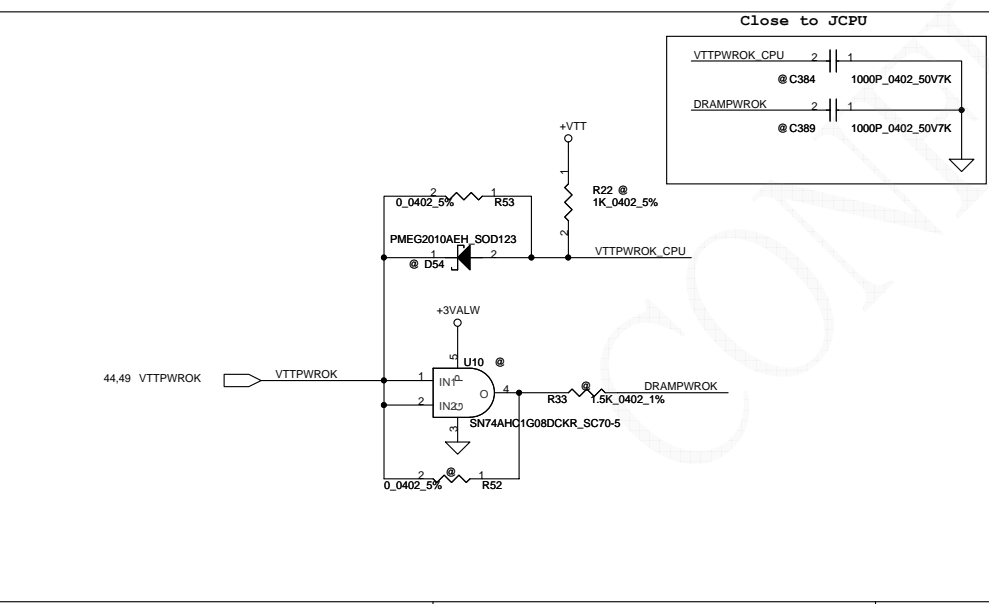
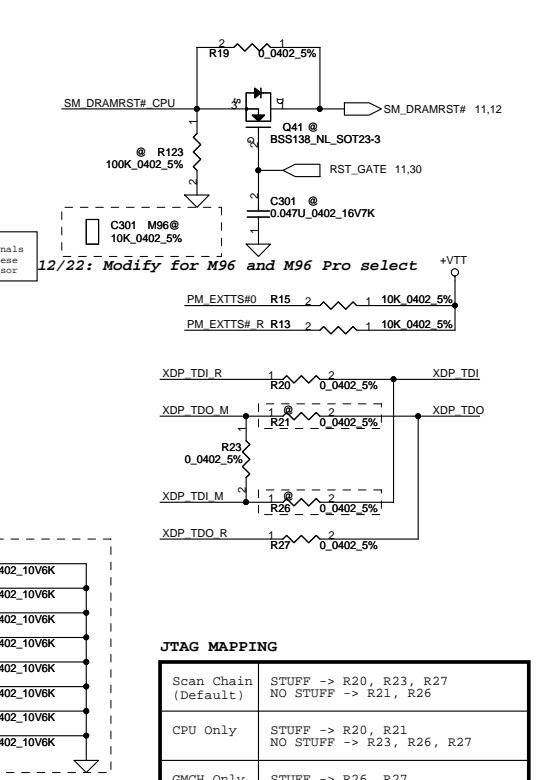
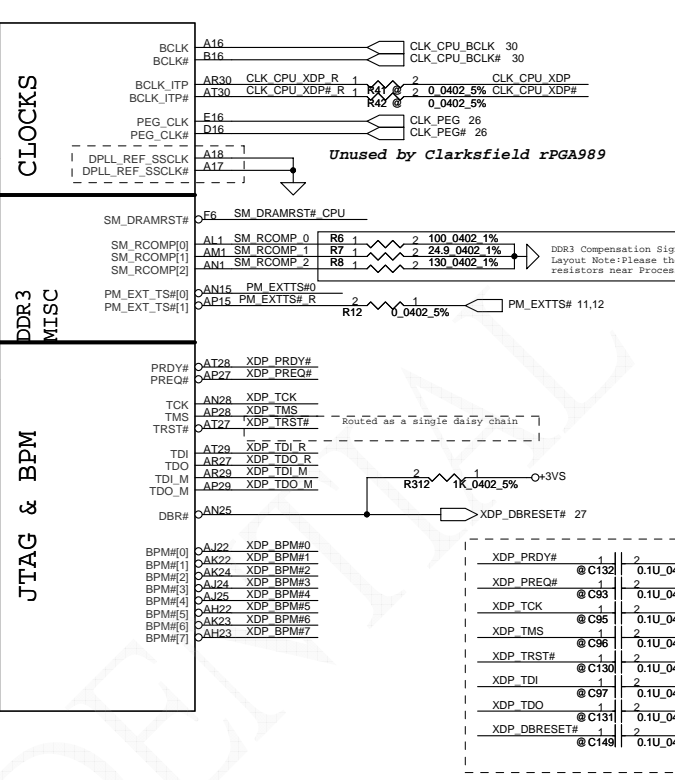
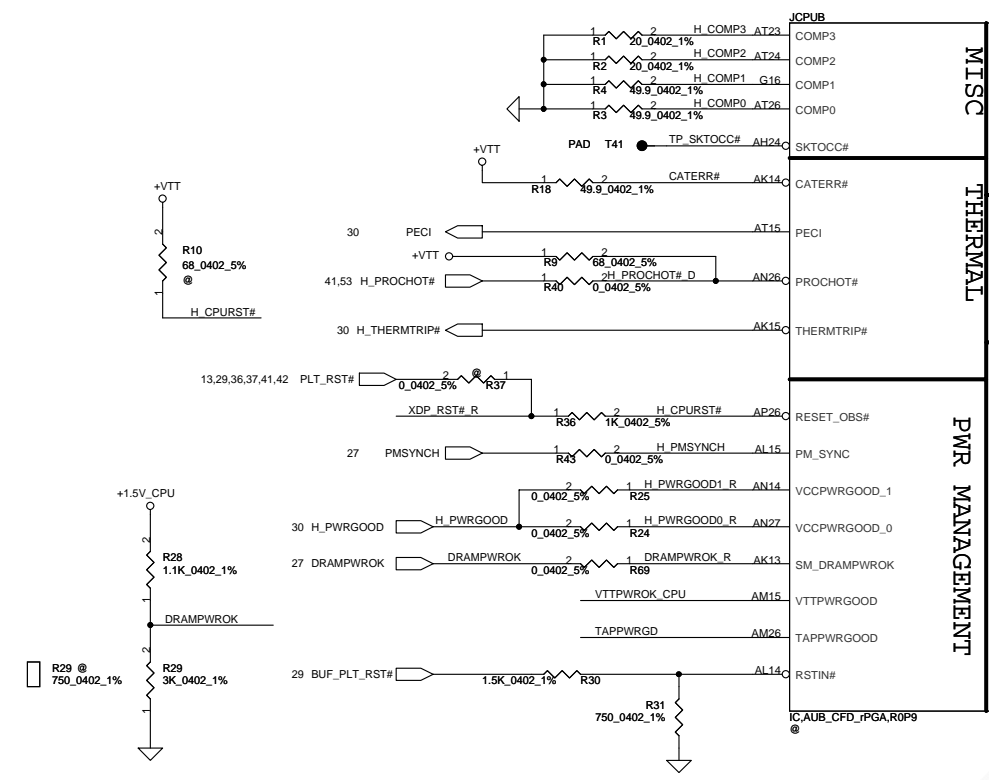
EC SM Bus2 address

Power	Device	Address	Power	Device	Address
+3VALW	EC KB926 D3		+3VS	EC KB926 D3	
+3VALW	Smart Battery	0001 011x b	+3VS	VGA THM Sensor ADM1032ARMZ	1001 110x b
			+3VS	PCH	0100 110x b

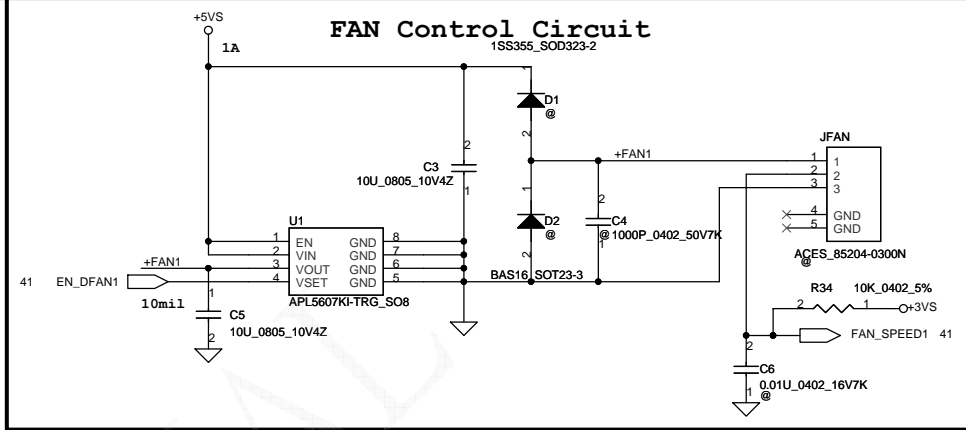
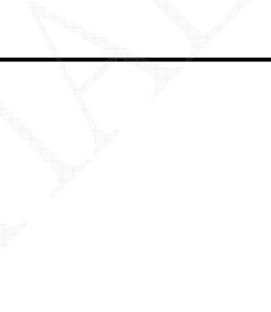
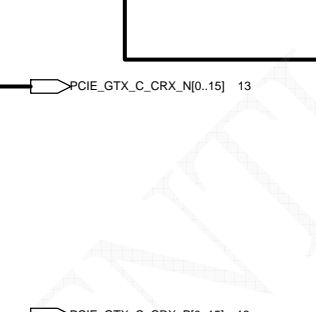
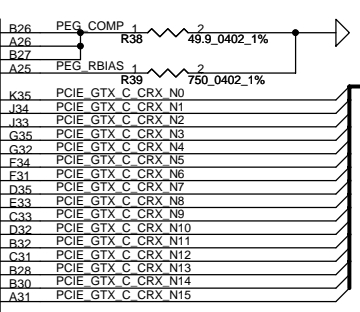
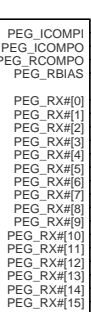
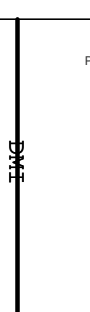
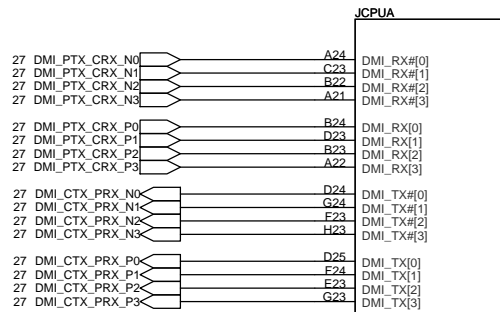
PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMM0	1001 000x b
+3VS	DDR DIMM1	1001 010x b
+3VS	Express	
+3VS	WLAN/Wimax/3G	

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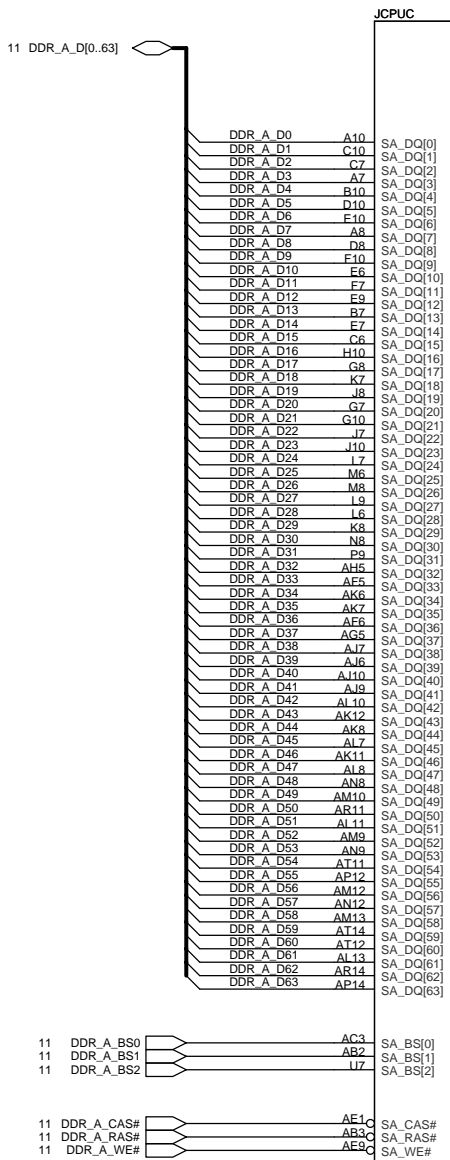


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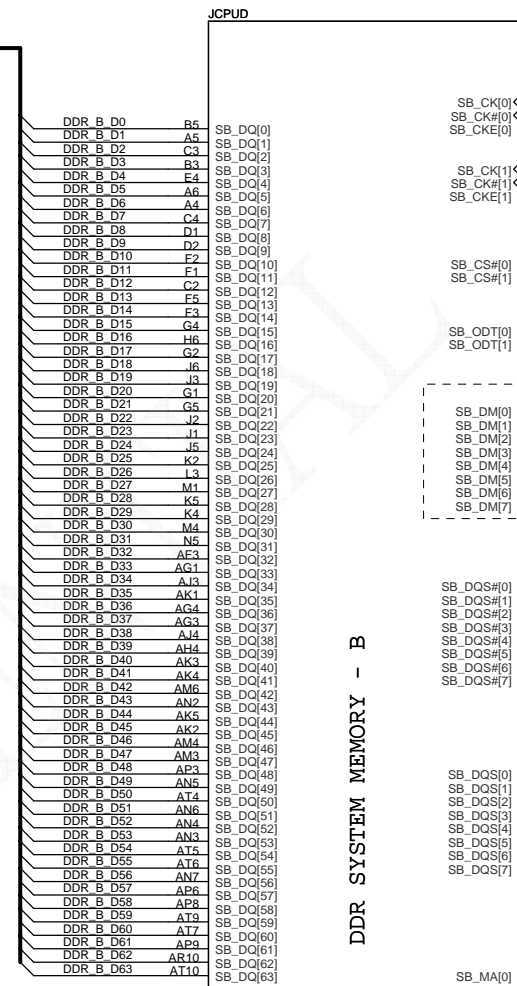
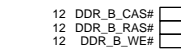
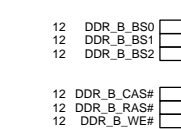
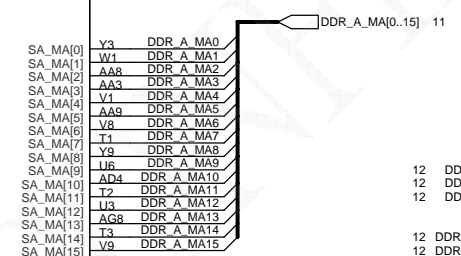
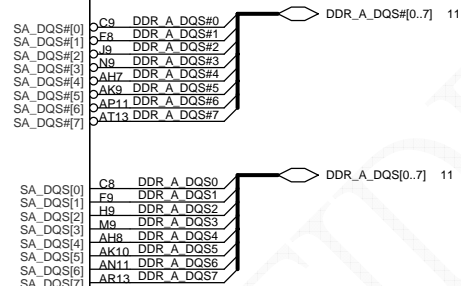
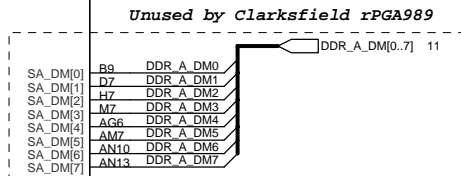
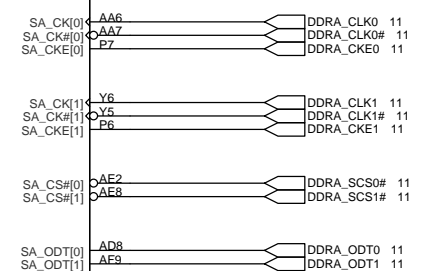


IC_AUB_CFD_PGA_R0P9
©

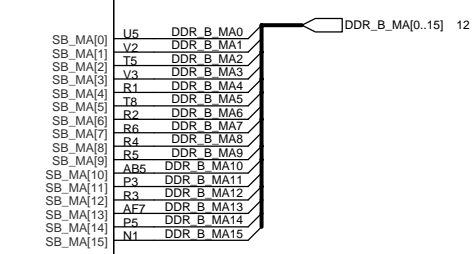
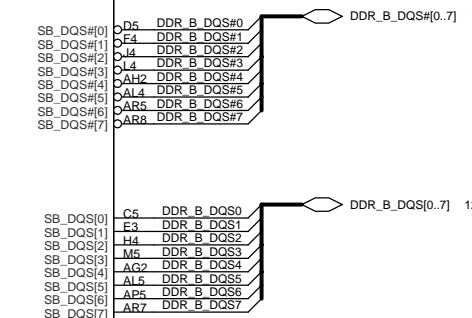
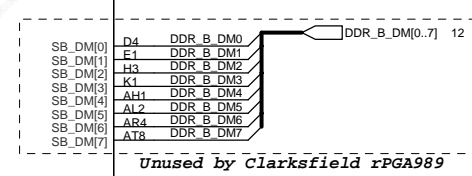
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DDR SYSTEM MEMORY A



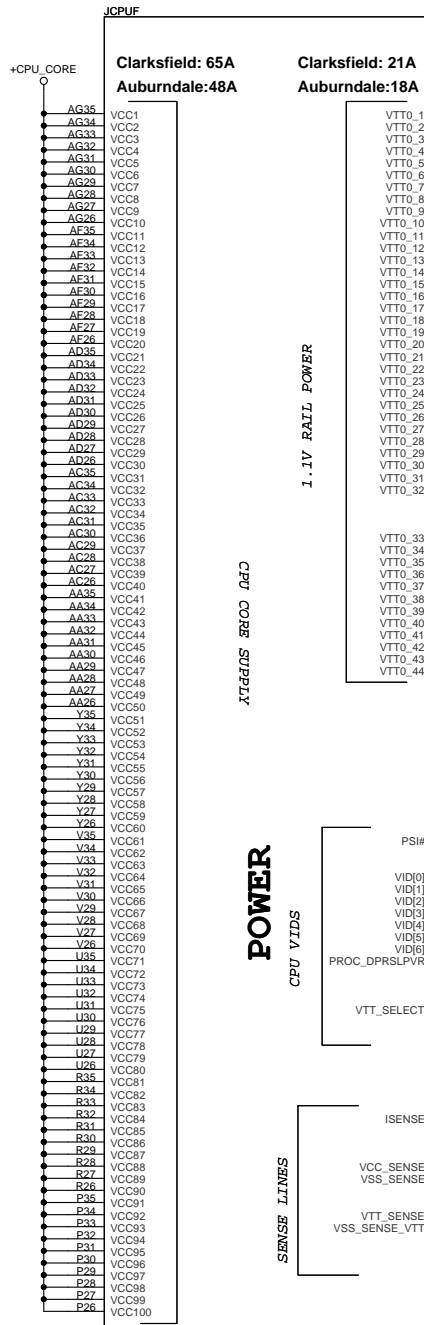
DDR SYSTEM MEMORY - B



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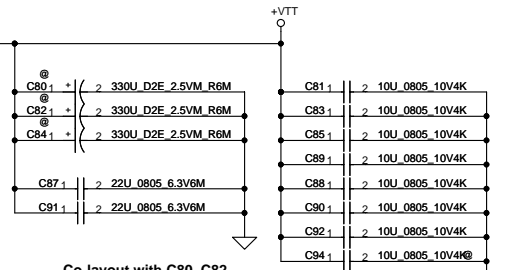
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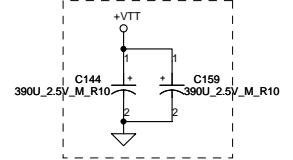


Material Note (+VTT) :
 330uF/ 6mohm, number are 3,
 power x1, HW x2

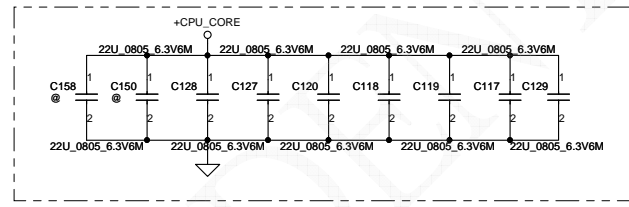
(Place these capacitors under CPU socket Edge, top layer)



Co-layout with C80, C82



5/25: Add for power team request.



CRB default setting:
 VID[6:0]=[0100111]

VTT Rail
 Auburndale +1.1VS_VTT=1.05V
 Clarkfield +1.1VS_VTT=1.1V

H_VTTSELECT = low, 1.1V
H_VTTSELECT = high, 1.05V

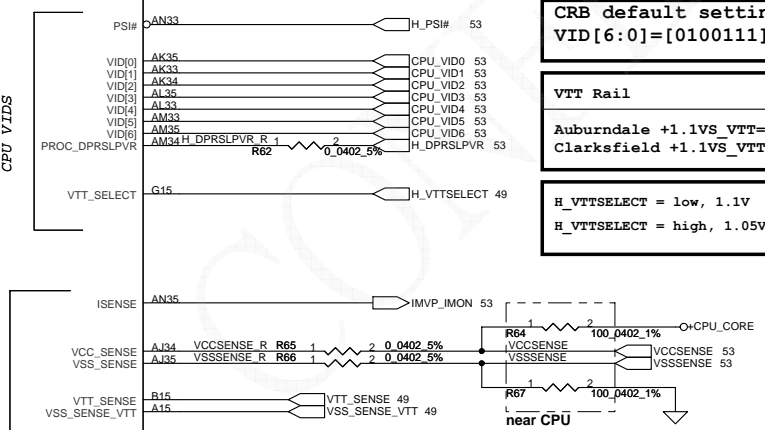
1.1V RAIL POWER

CPU CORE SUPPLY

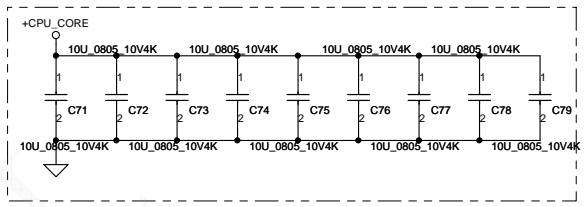
POWER

CPU VIDS

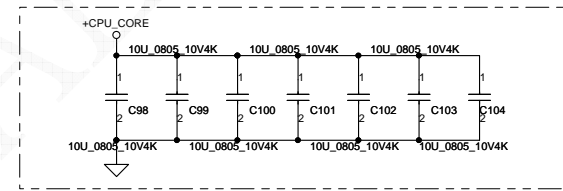
SENSE LINES



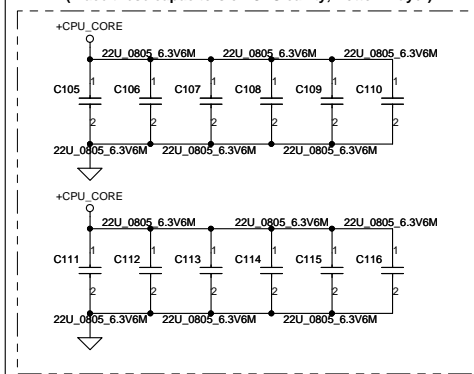
(Place these capacitors between inductor and socket on Bottom)



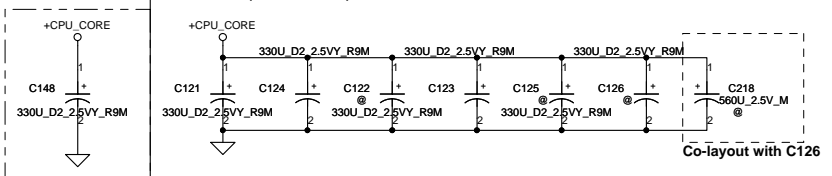
(Place these capacitors under CPU socket, top layer)



(Place these capacitors on CPU cavity, Bottom Layer)

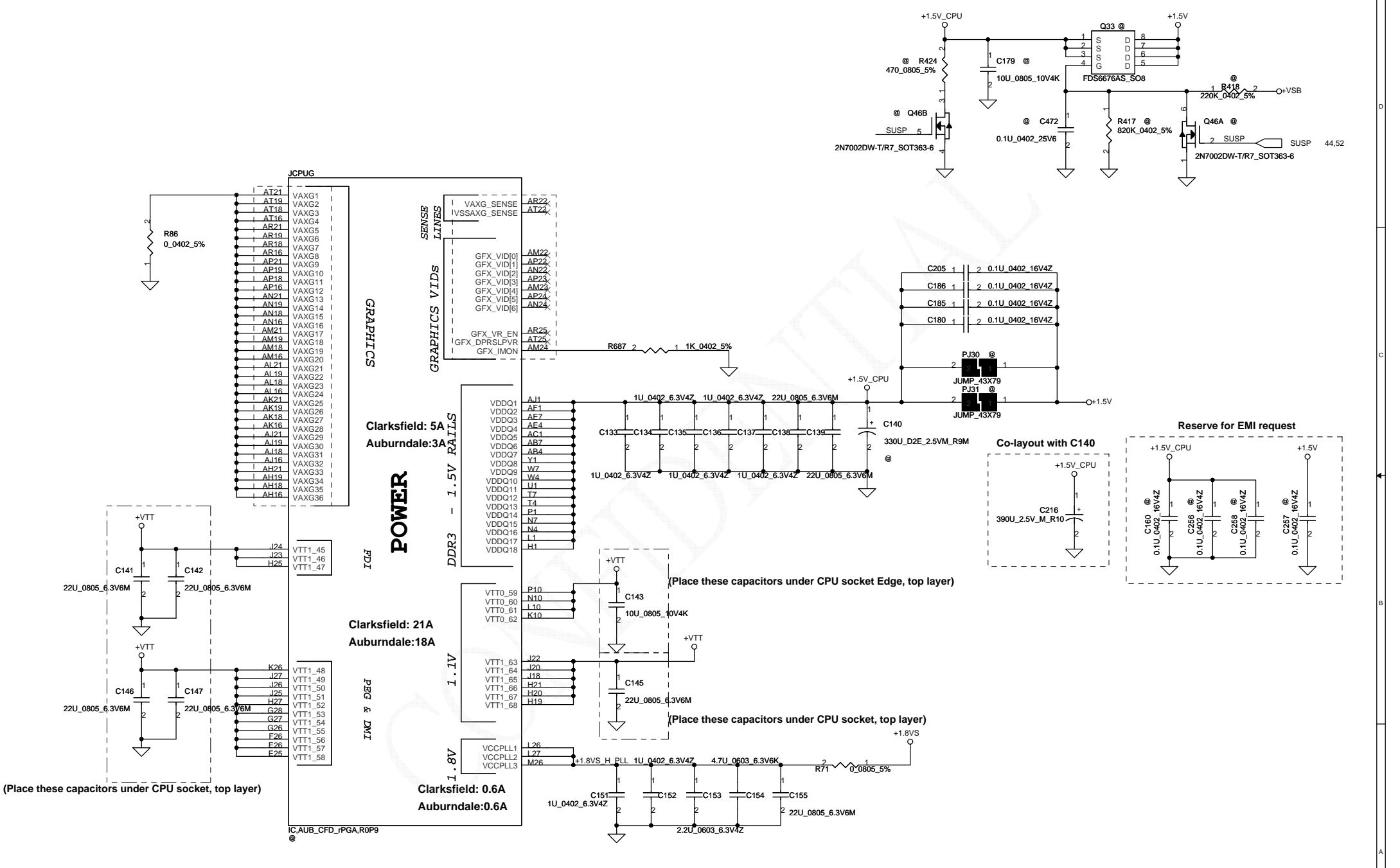


TOP side (under inductor)

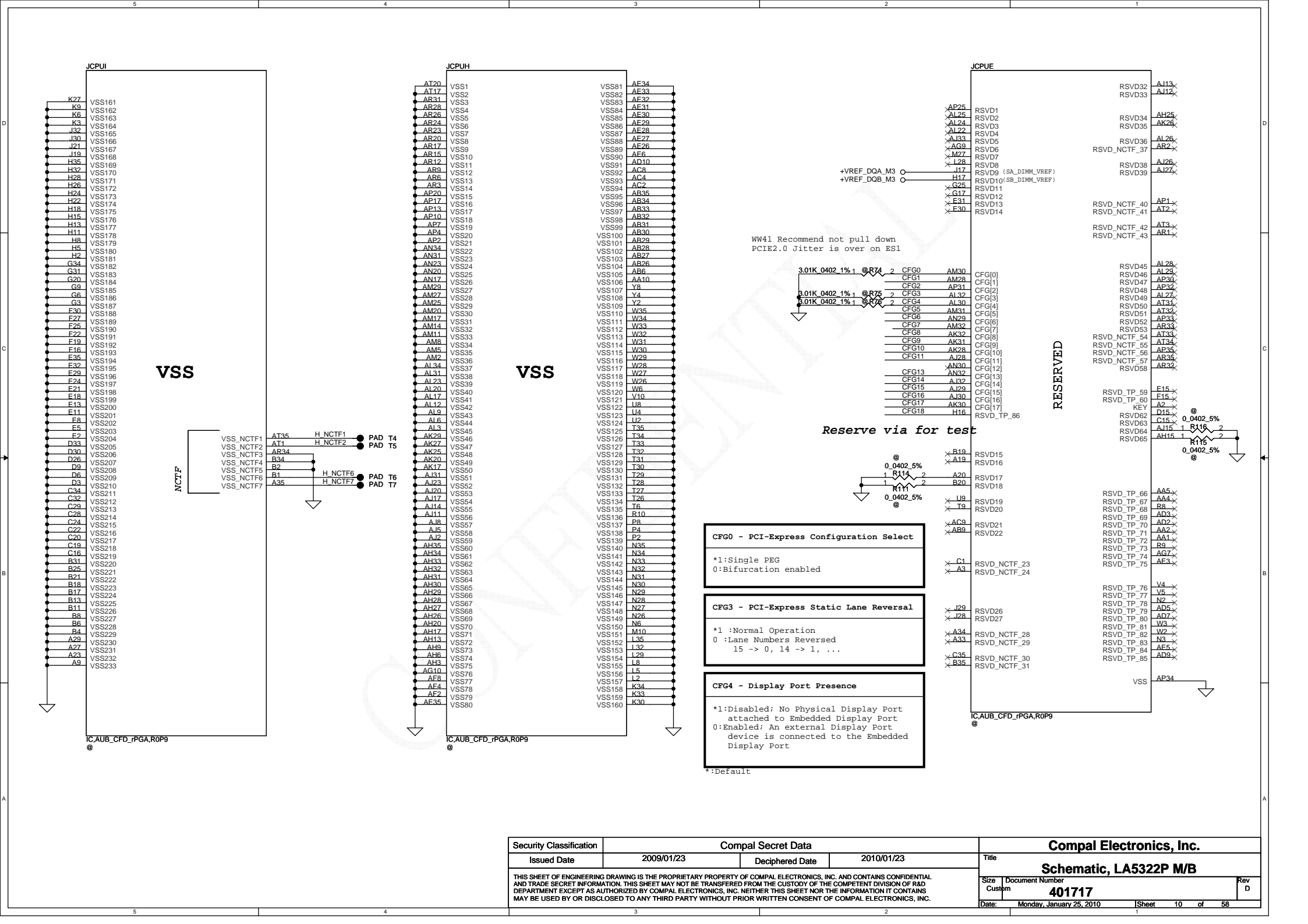


9/11: Add for power team request.

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WW41 Recommend not pull down
PCIe2.0 Jitter is over on ES1

Reserve via for test

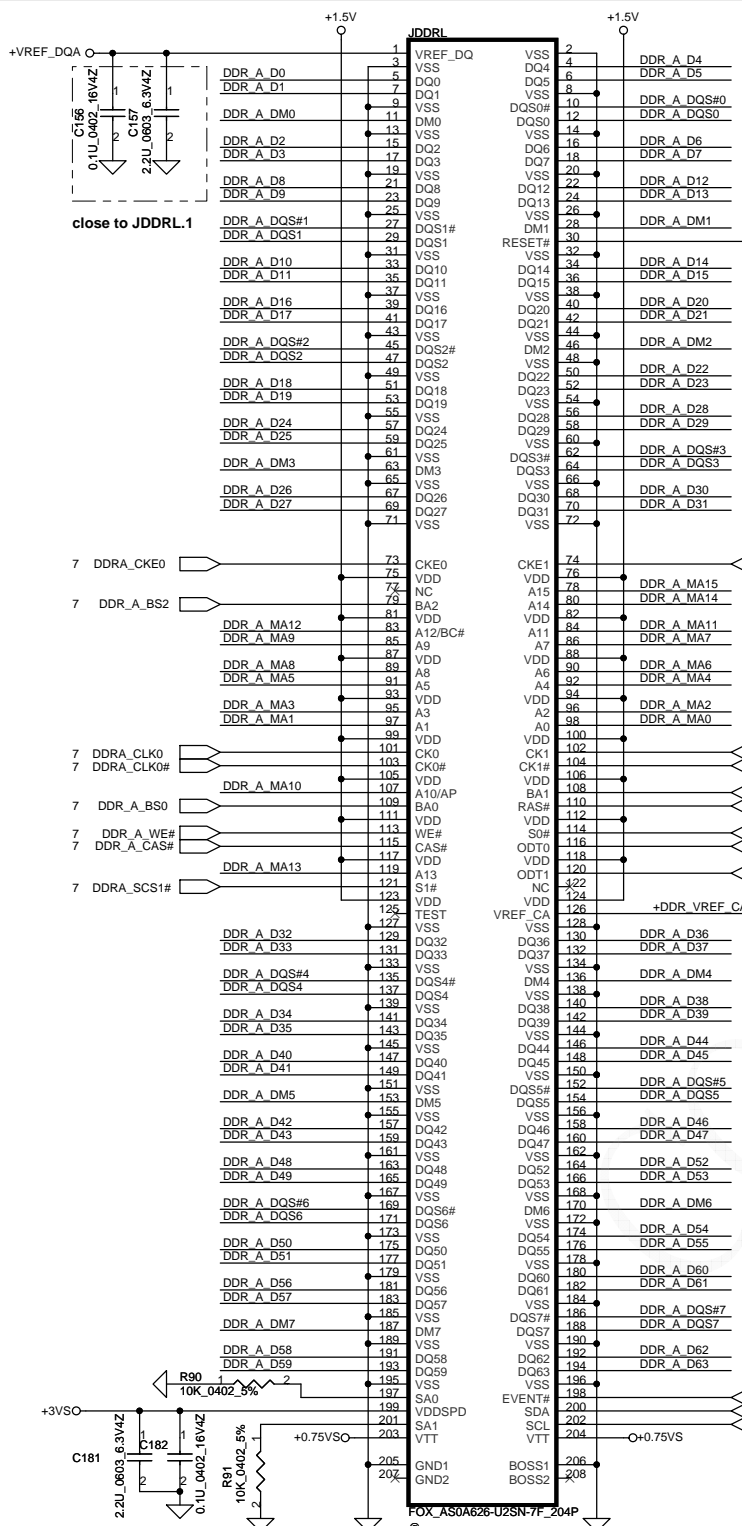
CFG0 - PCI-Express Configuration Select
*1: Single PEG
0: Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal
*1: Normal Operation
0: Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

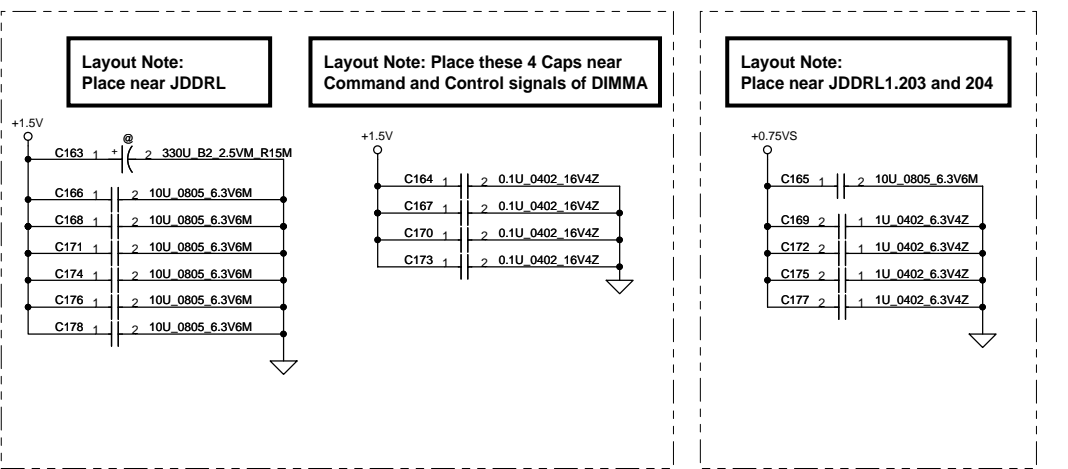
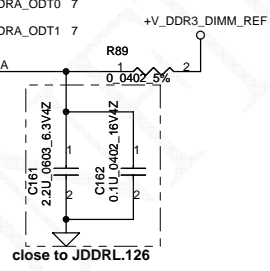
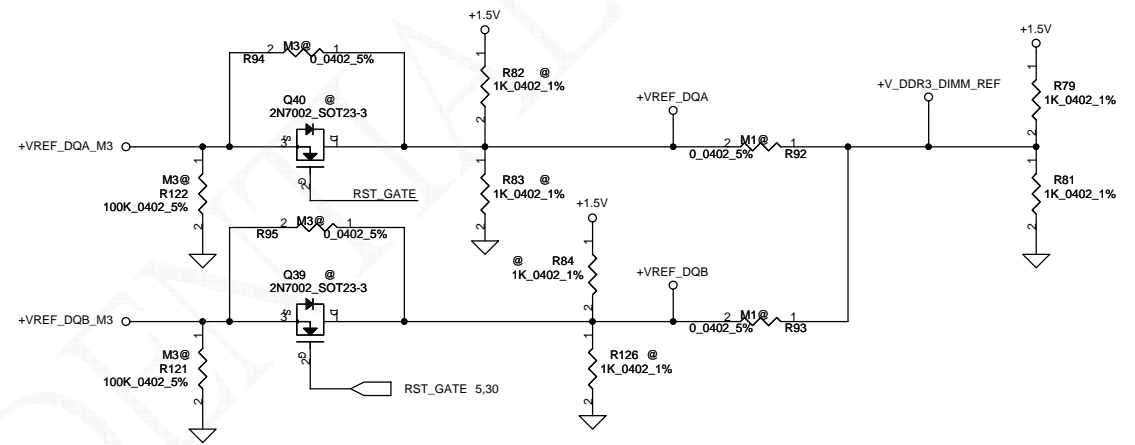
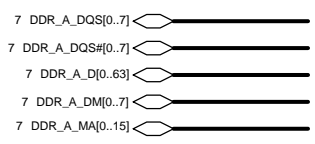
CFG4 - Display Port Presence
*1: Disabled; No Physical Display Port attached to Embedded Display Port
0: Enabled; An external Display Port device is connected to the Embedded Display Port

**Default

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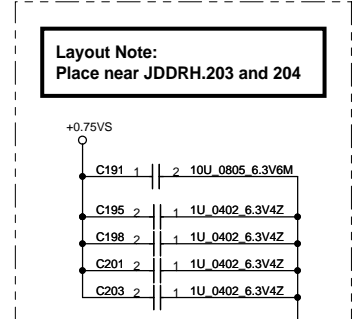
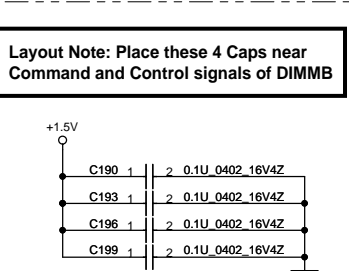
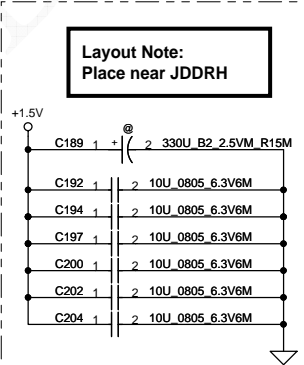
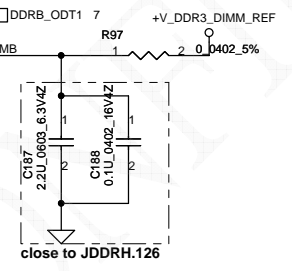
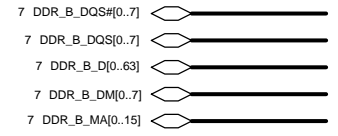
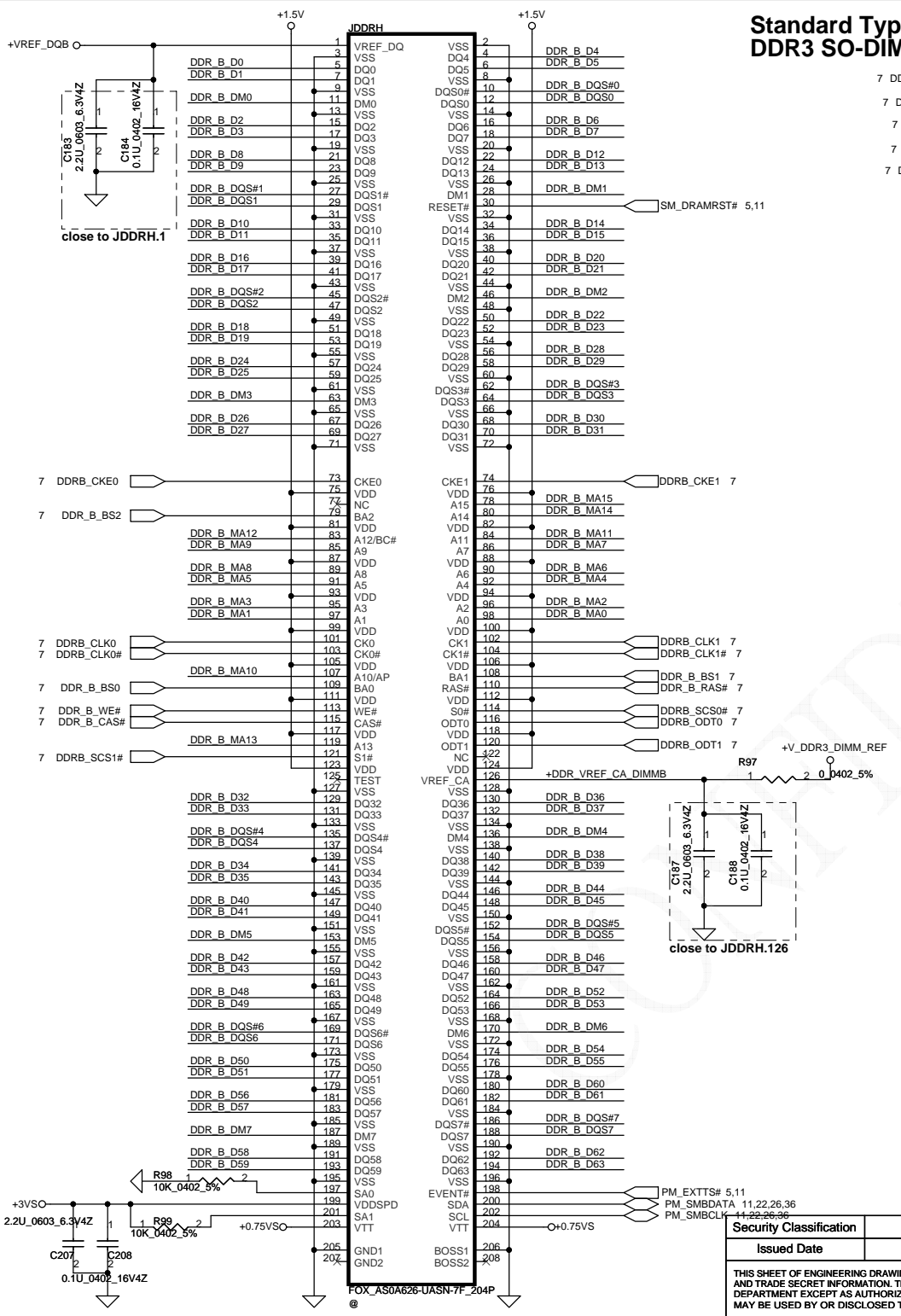


DDR3 SO-DIMM A Standard Type



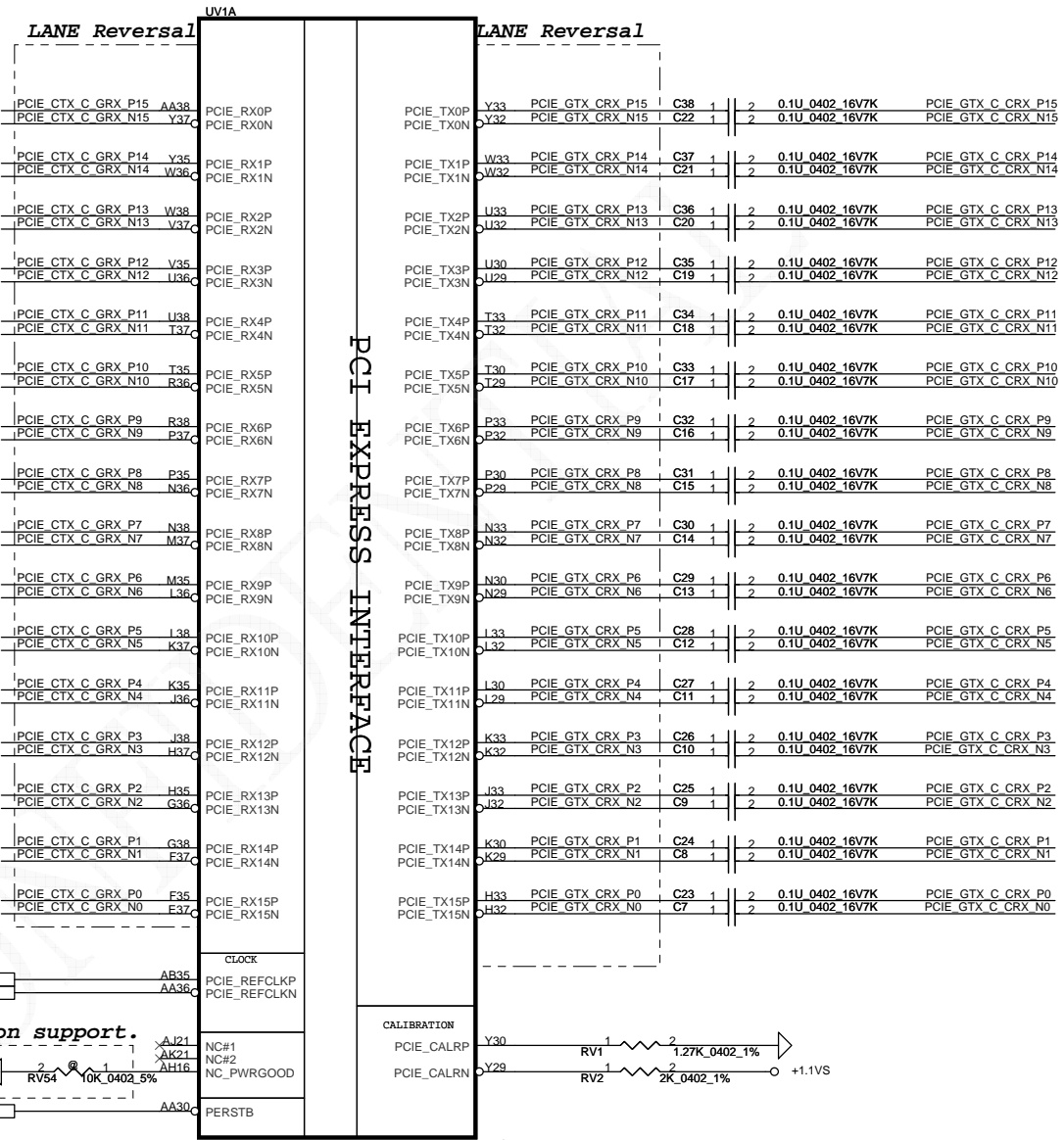
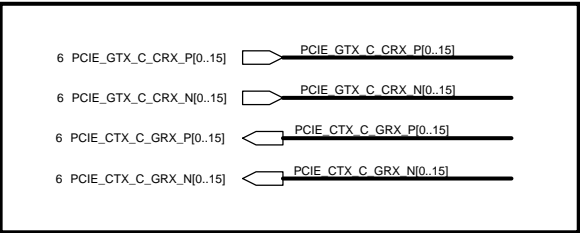
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Standard Type DDR3 SO-DIMM B

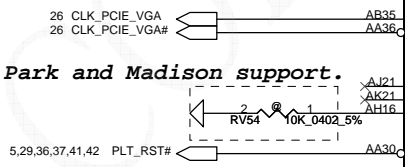


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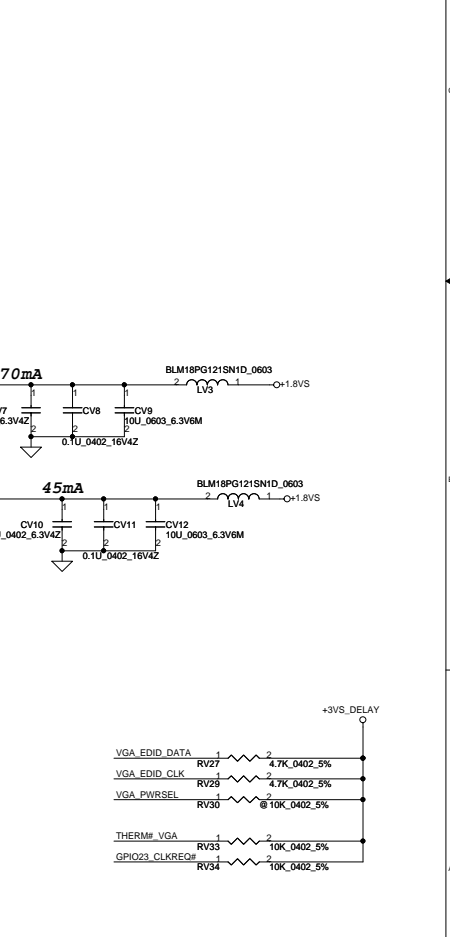
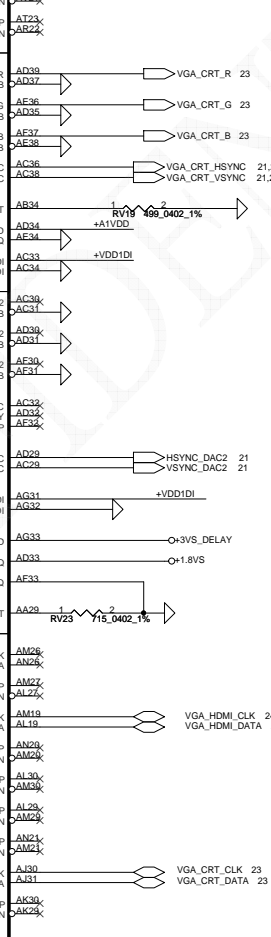
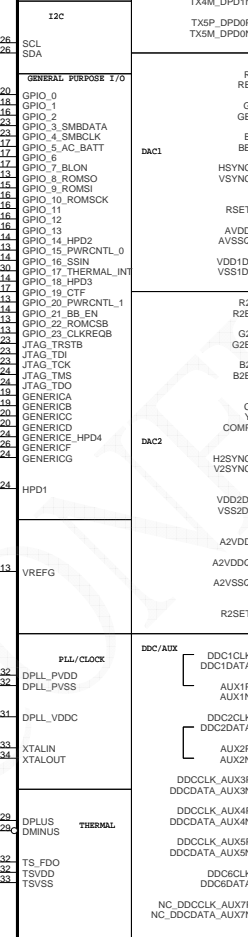
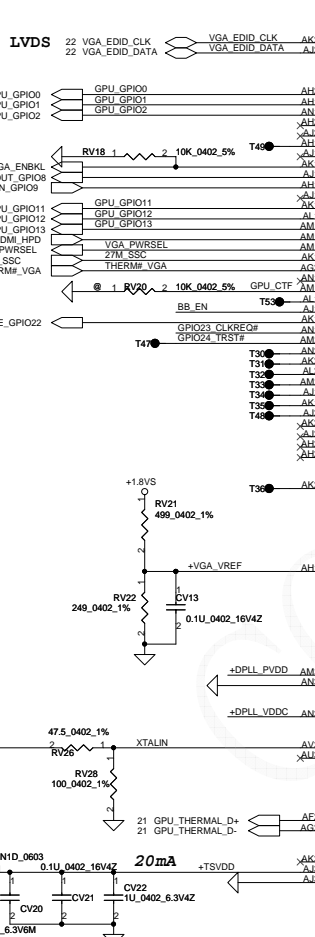
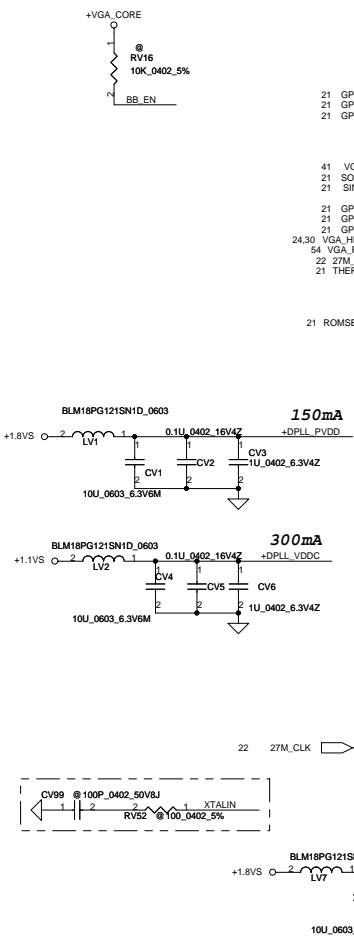


Reserve for Park and Madison support.

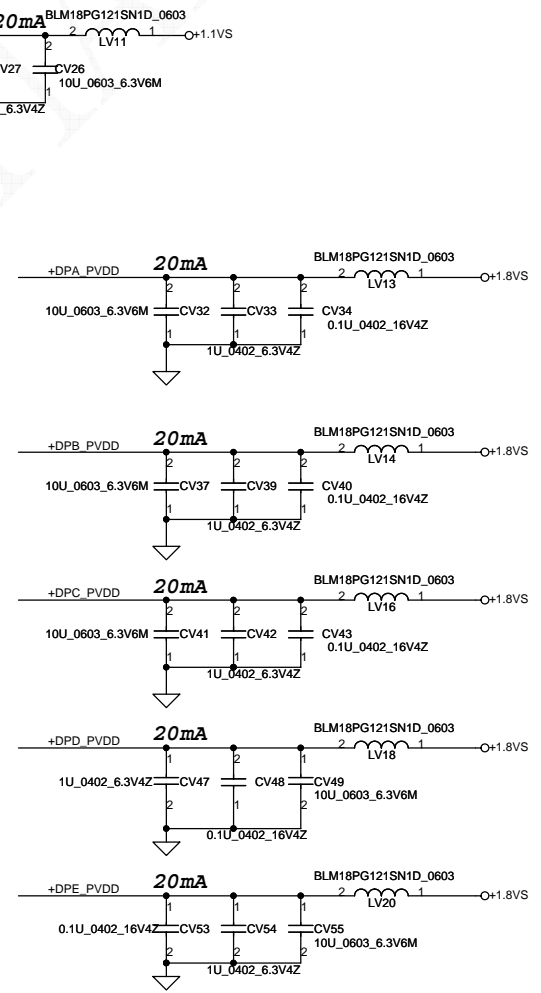
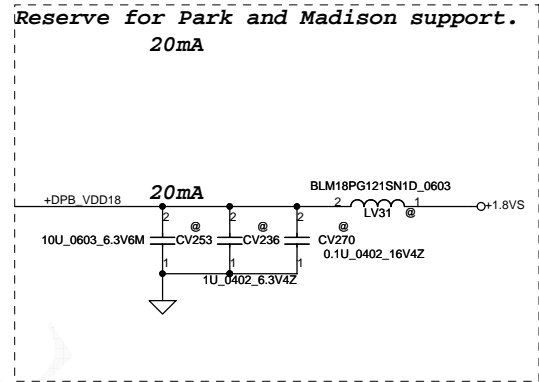
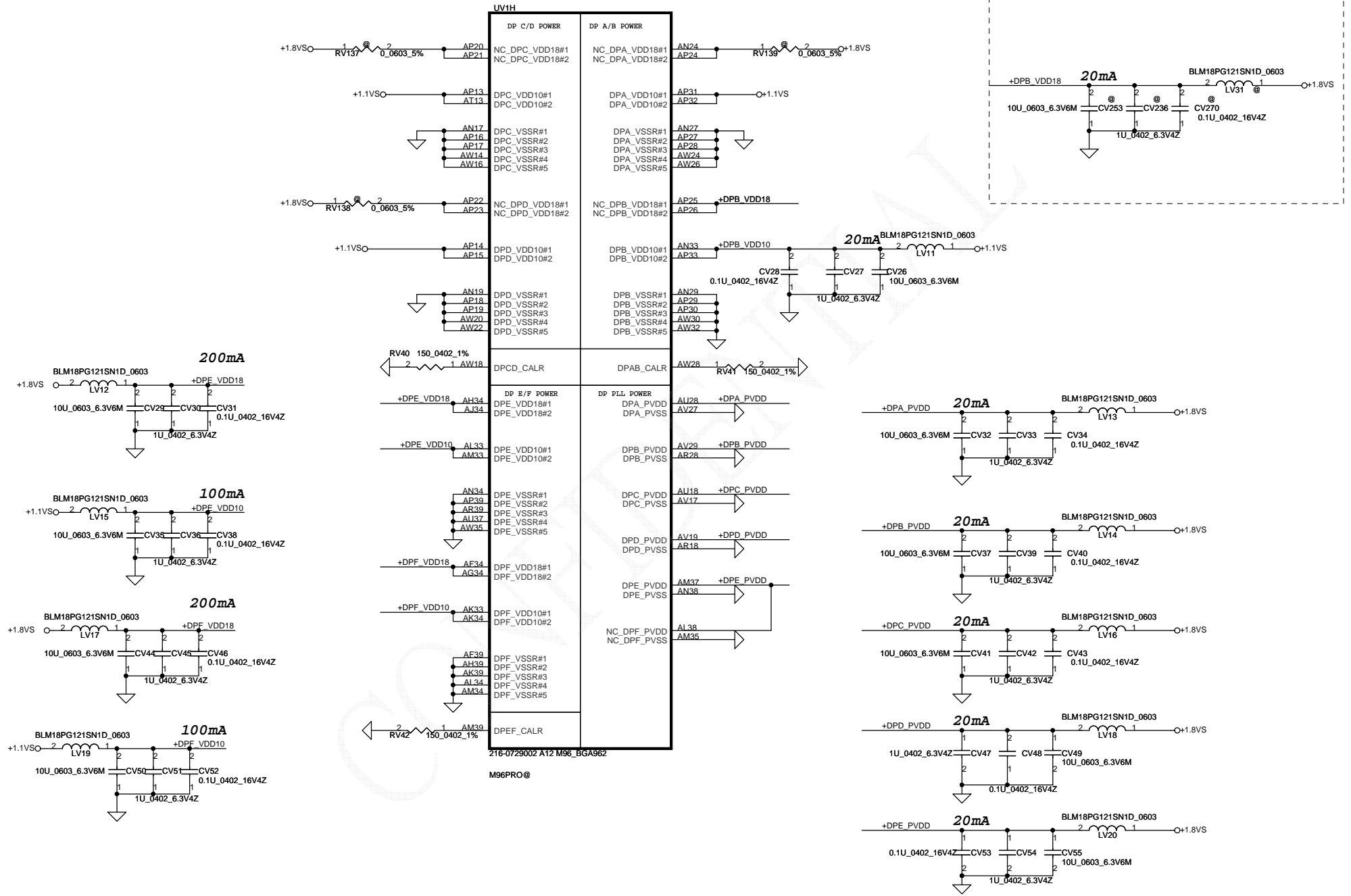


216-0729002 A12 M96_BGA962

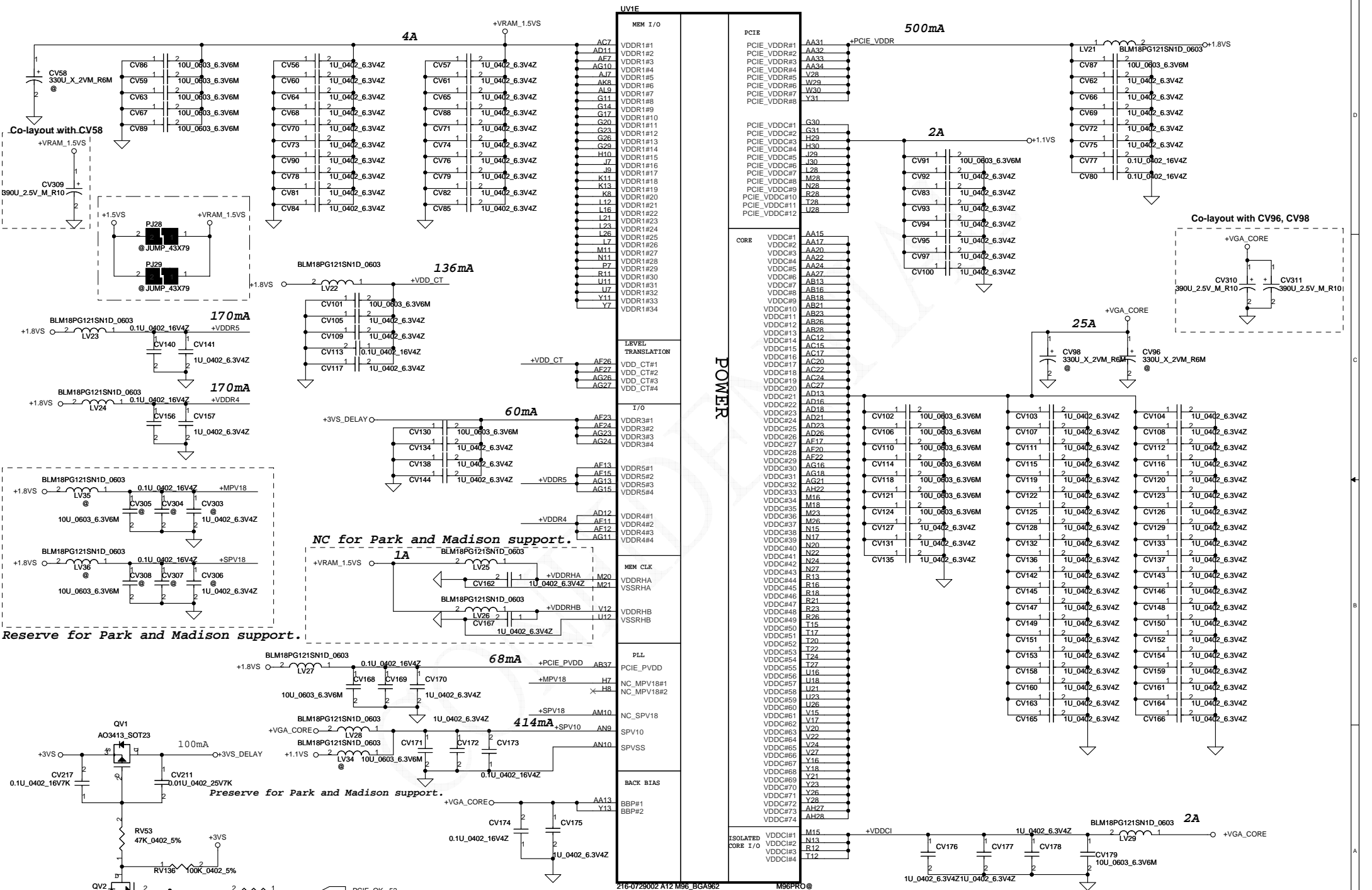
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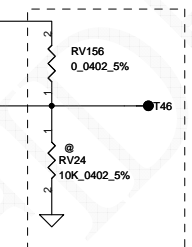
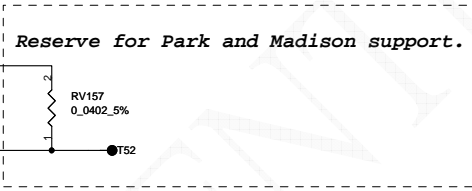
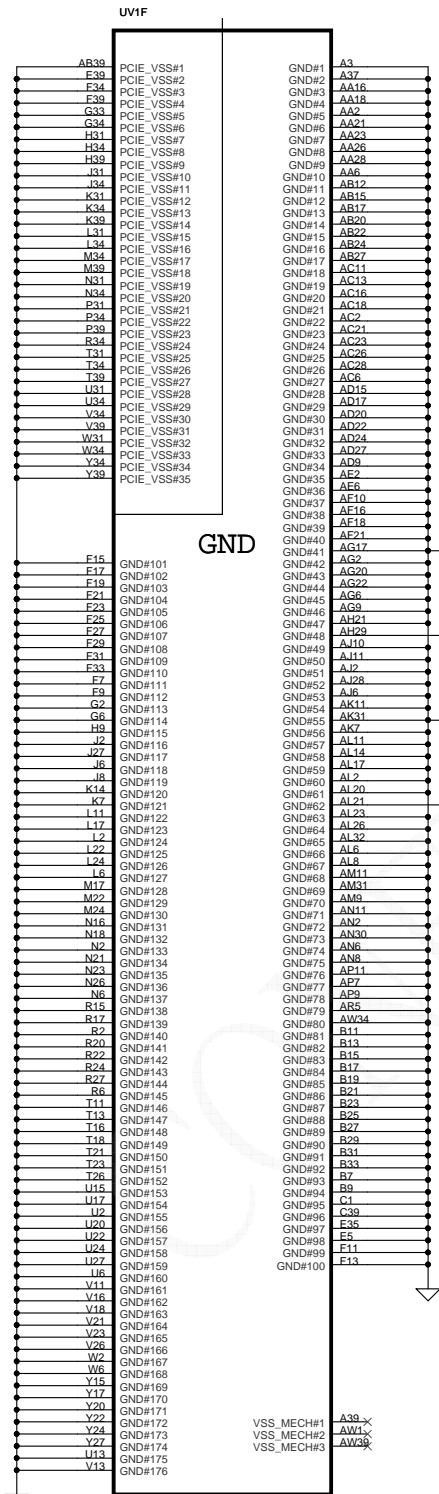
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MEM I/O	LEVEL TRANSLATION	I/O	MEM CLK	PLL	BACK BIAS	ISOLATED CORE I/O
VDDR1#1	VDD_CT#1	VDDR3#1	VDDR4#1	PCIE_PVDD	BBP#1	VDDCI#1
VDDR1#2	VDD_CT#2	VDDR3#2	VDDR4#2	NC_MPV18#1	BBP#2	VDDCI#2
VDDR1#3	AG26	VDDR3#3	VDDR4#3	NC_MPV18#2		VDDCI#3
VDDR1#4	AG27	VDDR3#4	VDDR4#4	NC_SPV18		VDDCI#4
VDDR1#5				SPV10		
VDDR1#6				SPVSS		
VDDR1#7						
VDDR1#8						
VDDR1#9						
VDDR1#10						
VDDR1#11						
VDDR1#12						
VDDR1#13						
VDDR1#14						
VDDR1#15						
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VDDR1#26						
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VDDR1#28						
VDDR1#29						
VDDR1#30						
VDDR1#31						
VDDR1#32						
VDDR1#33						
VDDR1#34						



Reserve for Park and Madison support.

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M96PRO@

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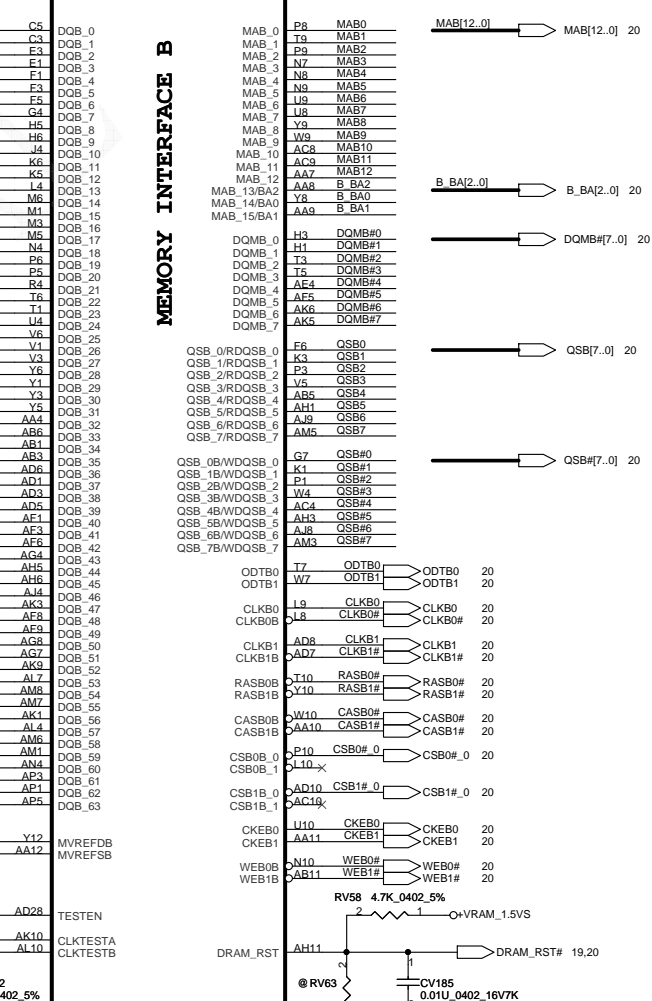
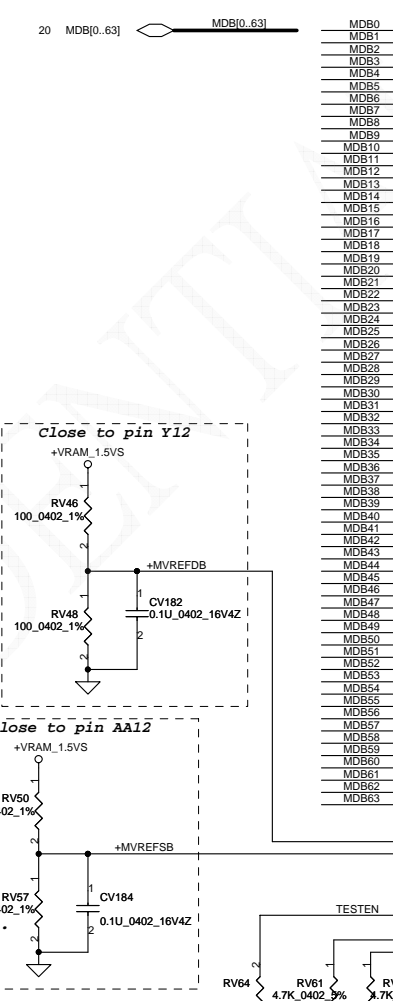
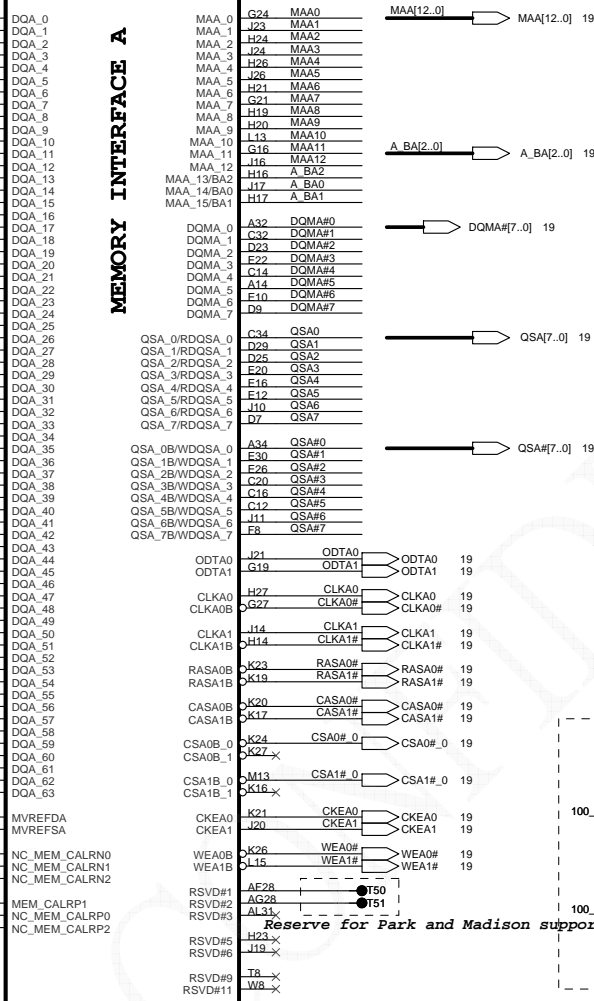
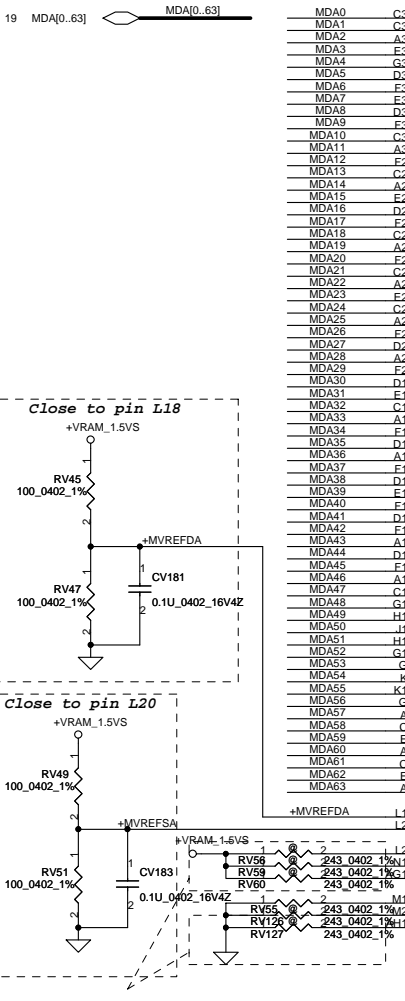
M92-M2 uses memory group B only

MEMORY INTERFACE A

MEMORY INTERFACE B

UVIC

UVIP



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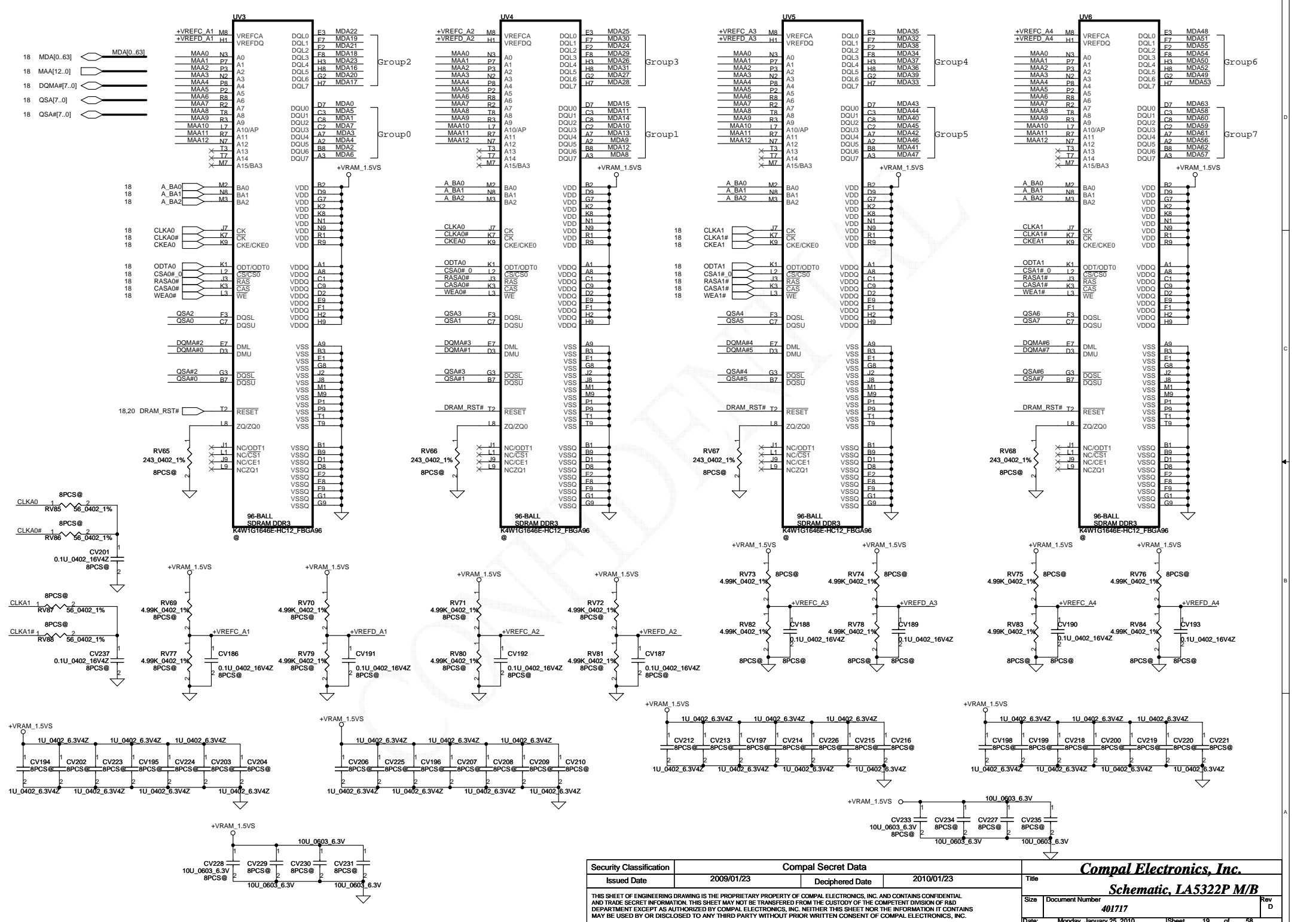
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M96PRO

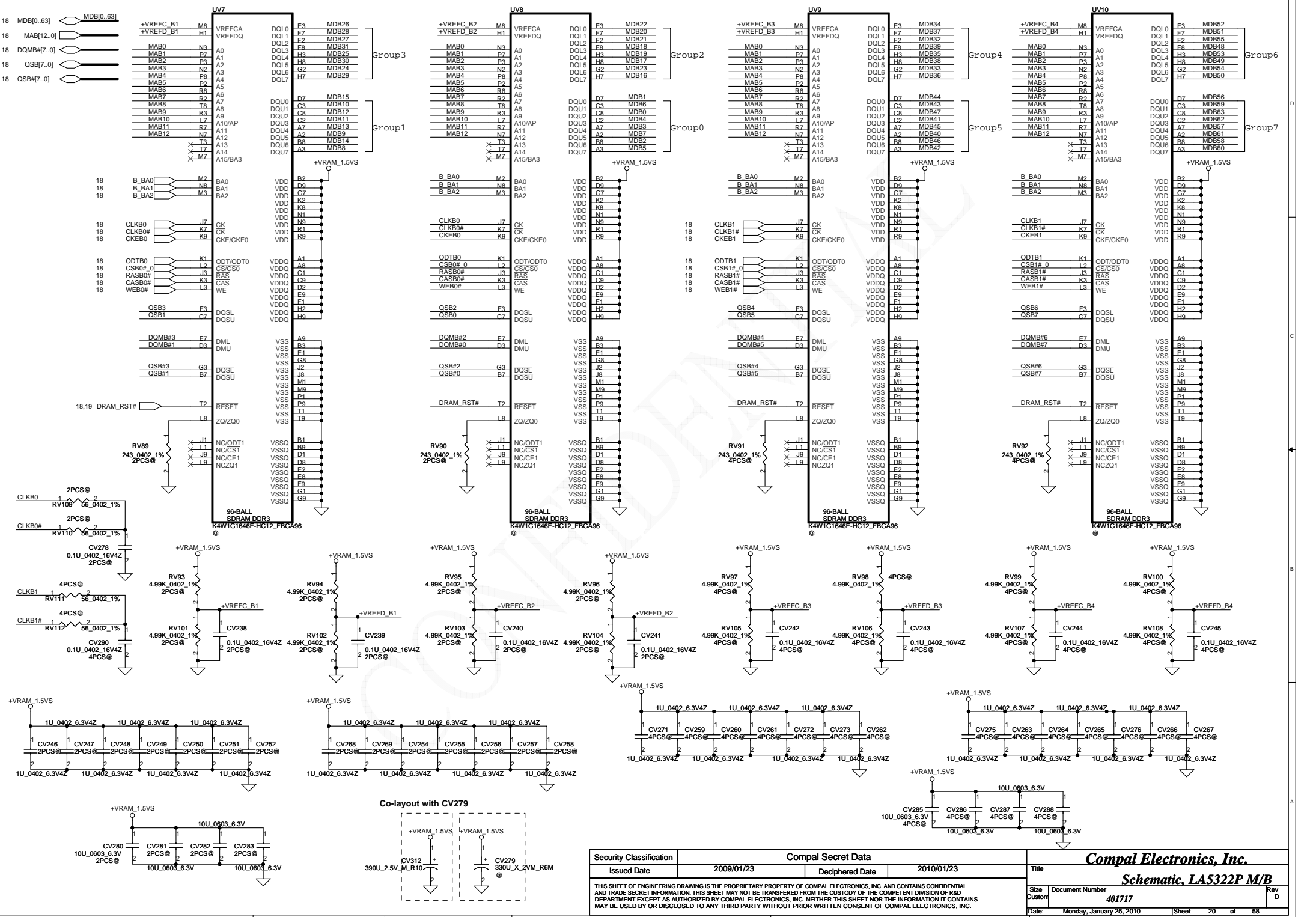
M96PRO

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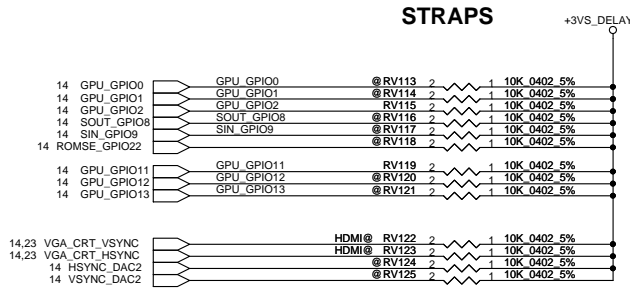
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GPU by the system BIOS		GPU by VBIOS	
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)	
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]	
0 0 0	128MB	1 0 0	
0 0 1	256MB	(M25P05A)	
0 1 0	64MB		



CONFIGURATION STRAPS

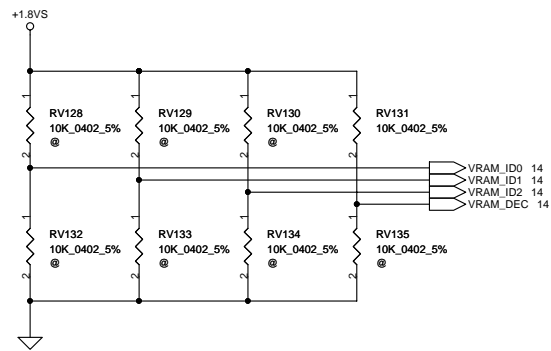
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA Controller ENABLED	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable External BIOS device	0
ROMIDCFG(2:0)	GPIO[13:11]	ROM Configurations	0 0 1
VIP_DEVICE_STRAP_ENA	VSYNC_DAC2	IGNORE VIP DEVICE STRAPS	0
AUD[1]	HSYNC	AUD[1] AUD[0] 0 0 No audio function	1 1
AUD[0]	VSYNC	0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	
RSVD	HSYNC_DAC2		0
RSVD	GENERICC		0

AMD RESERVED CONFIGURATION STRAPS

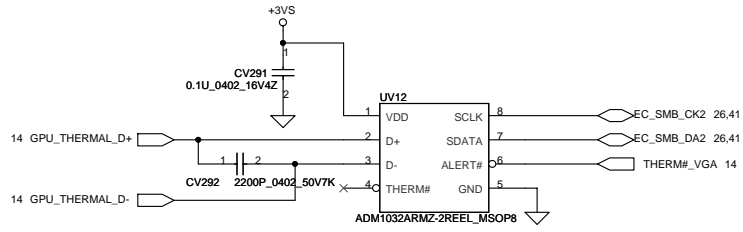
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

HSYNC_DAC2	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO_28_TDO	GPIO21_BB_EN



STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 2,1,0
VRAM_ID[2:0]	DVPDATA (3,2,1)	M92-M2 XT	512M 64Mx16 (x4)	HYN H5TQ1G63BFR-12C	SA000032400	0 0 0
		M96-M2	1G 64Mx16 (x8)	HYN H5TQ1G63BFR-12C	SA000032400	0 0 1
		M92-M2 XT	256M 64Mx16 (x2)	HYN H5TQ1G63BFR-12C	SA000032400	0 1 0
		M96-M2	1G 64Mx16 (x8)	SAM K4W1G1646E-HC12	SA000035700	0 1 1
		M92-M2 XT	512M 64Mx16 (x4)	SAM K4W1G1646E-HC12	SA000035700	1 0 0
		M92-M2 XT	256M 64Mx16 (x2)	SAM K4W1G1646E-HC12	SA000035700	1 0 1

External VGA Thermal Sensor

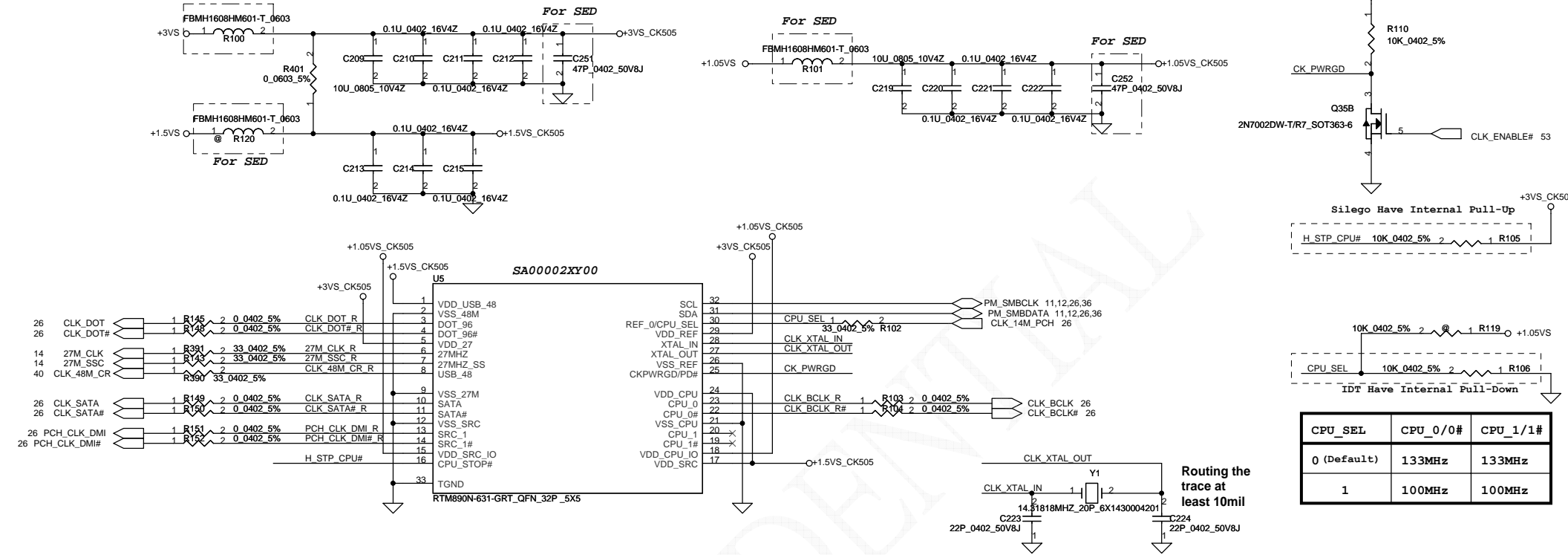


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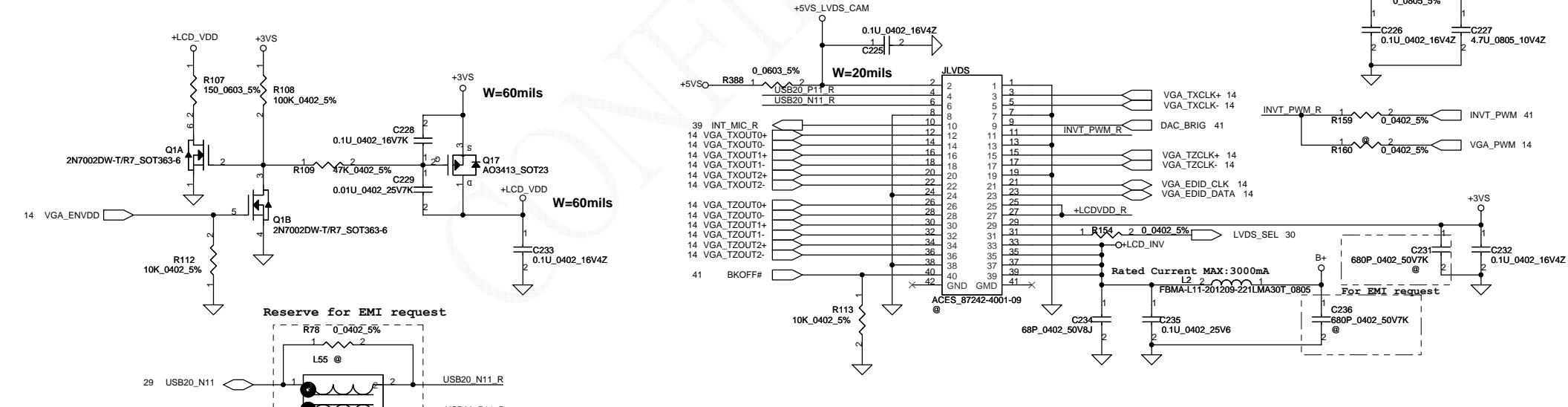
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Clock Generator

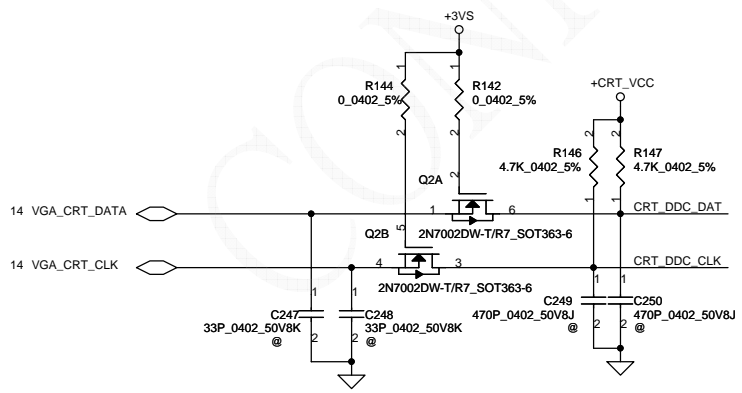
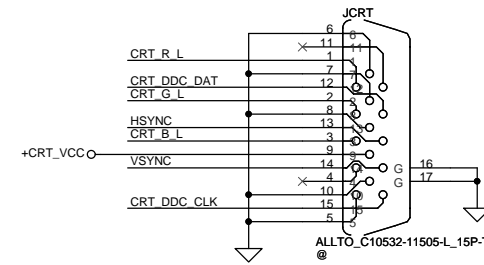
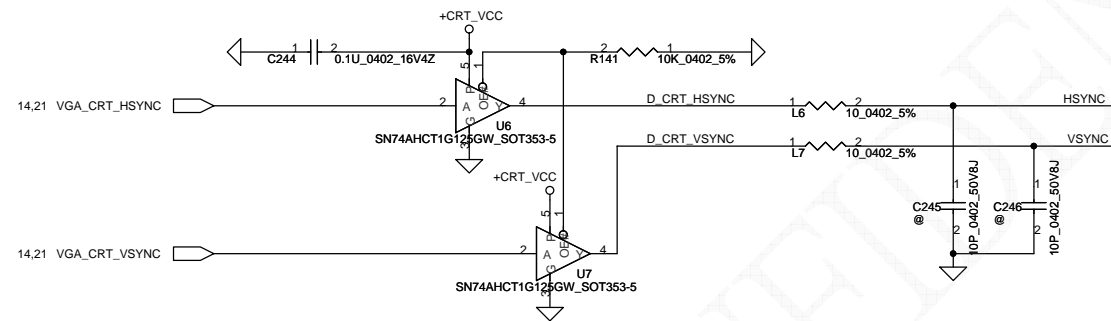
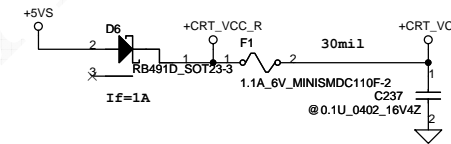
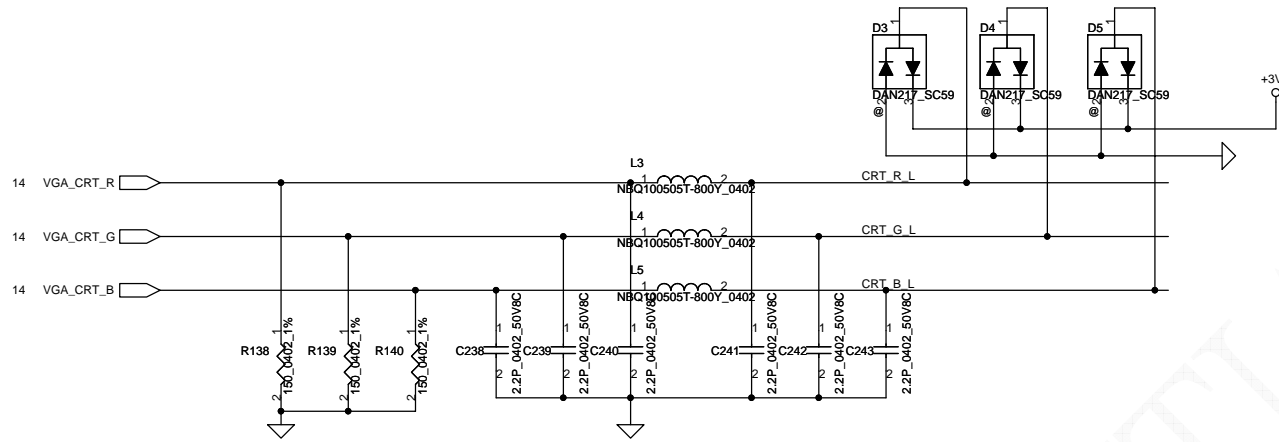


LCD/PANEL BD. Conn.

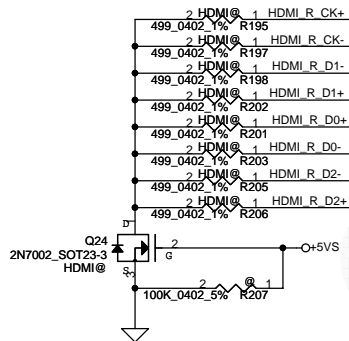
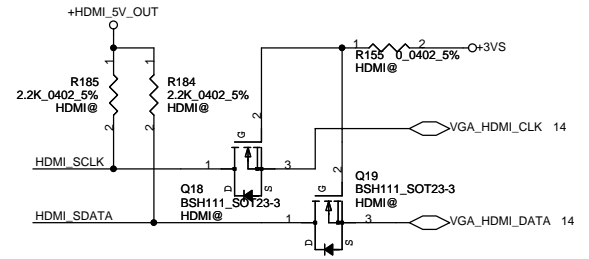
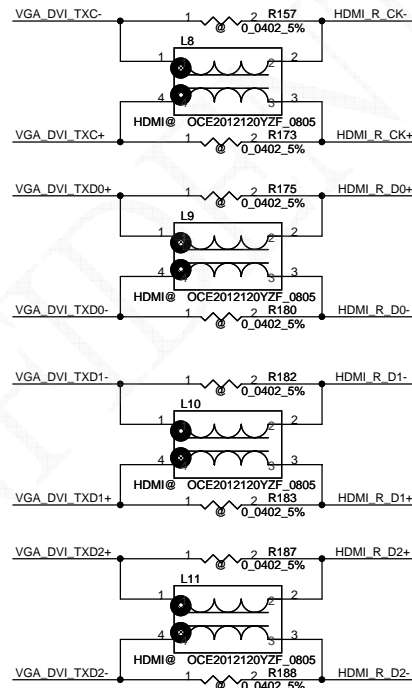
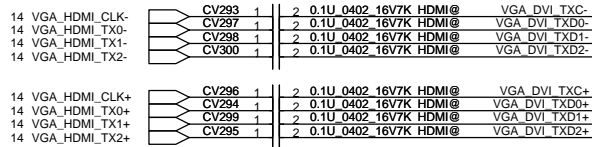
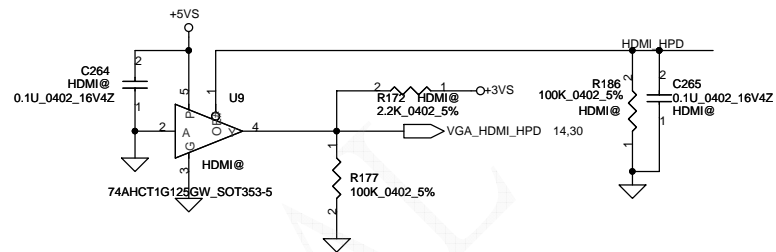
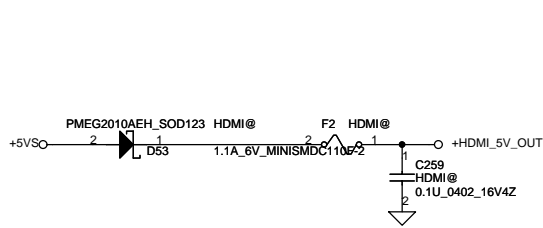


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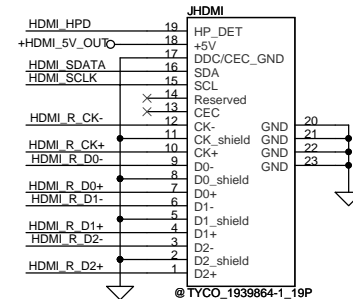
CRT CONNECTOR



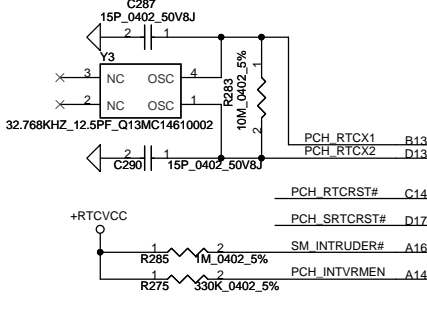
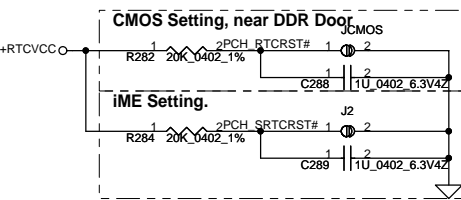
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HDMI Connector



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Integrated SUS 1.05V VRM Enable

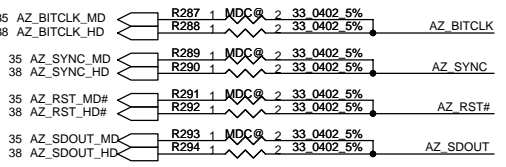
PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)
--------------	---

HDA_SYNC
This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
*L=>On Die PLL is supplied by 1.8V

HDA_SDO
This signal has a weak internal pull down.
This signal can't PU

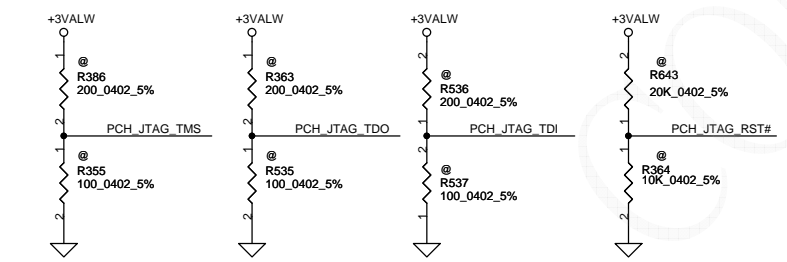
Flash Descriptor Security Override

HDA_DOCK_EN#	Low = Enabled High = Disabled*
--------------	-----------------------------------



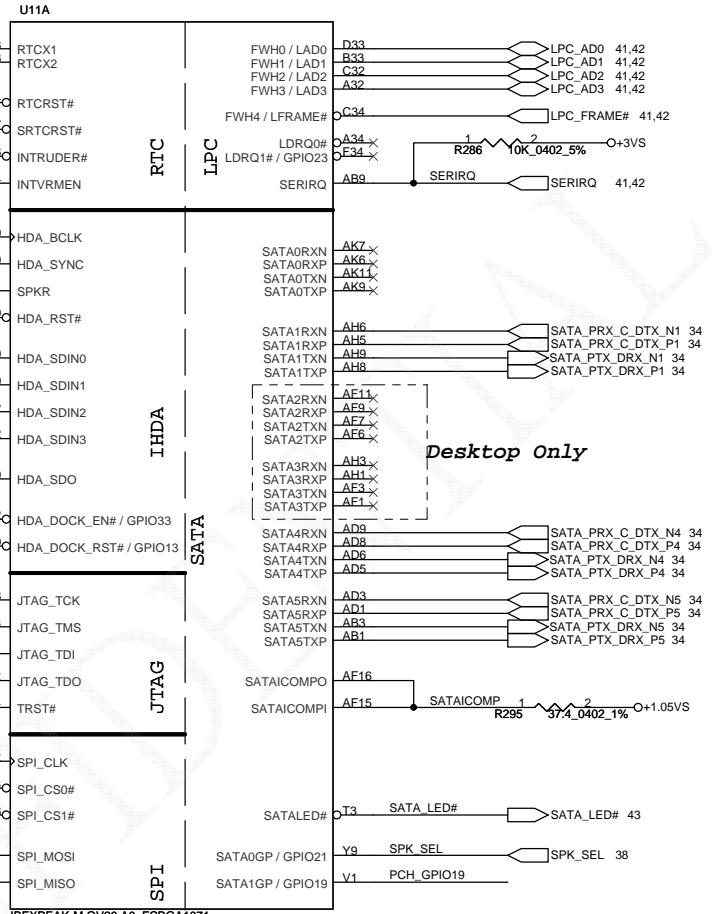
ITPM Enabled Internal: Pull down 20k

SPI_MOSI	High = Enabled Low = Disabled (Default)
----------	--



06/01 change R156 from 4.7K to 51 ohm

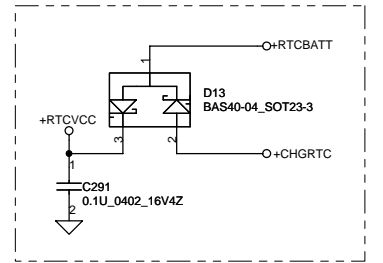
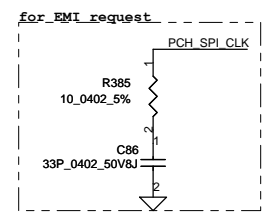
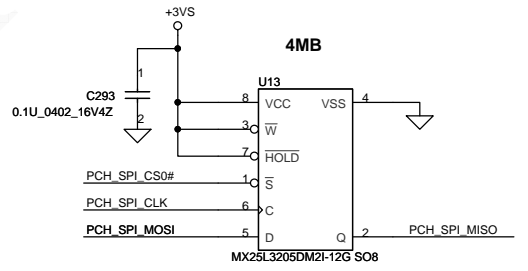
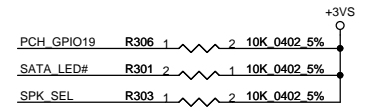
PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_RST#	R536	200ohm	200ohm	20kohm	No Install
	R537	100ohm	100ohm	10kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20kohm	20kohm	No Install	No Install
	R353	10kohm	10kohm	No Install	No Install



1ST HDD

SATA ODD

eSATA



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For NewCard

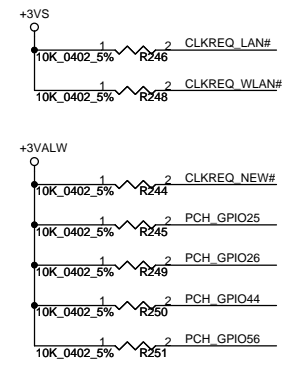
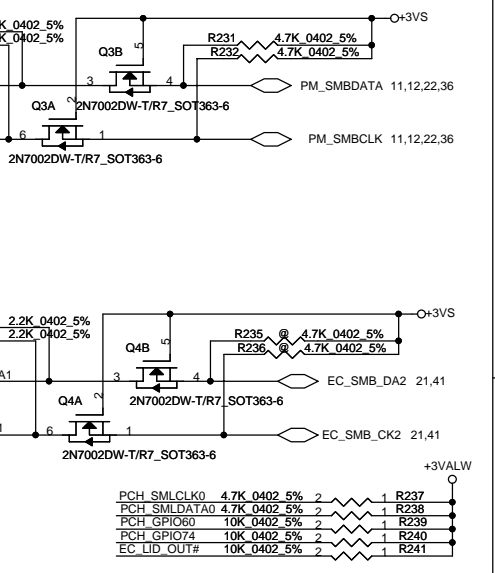
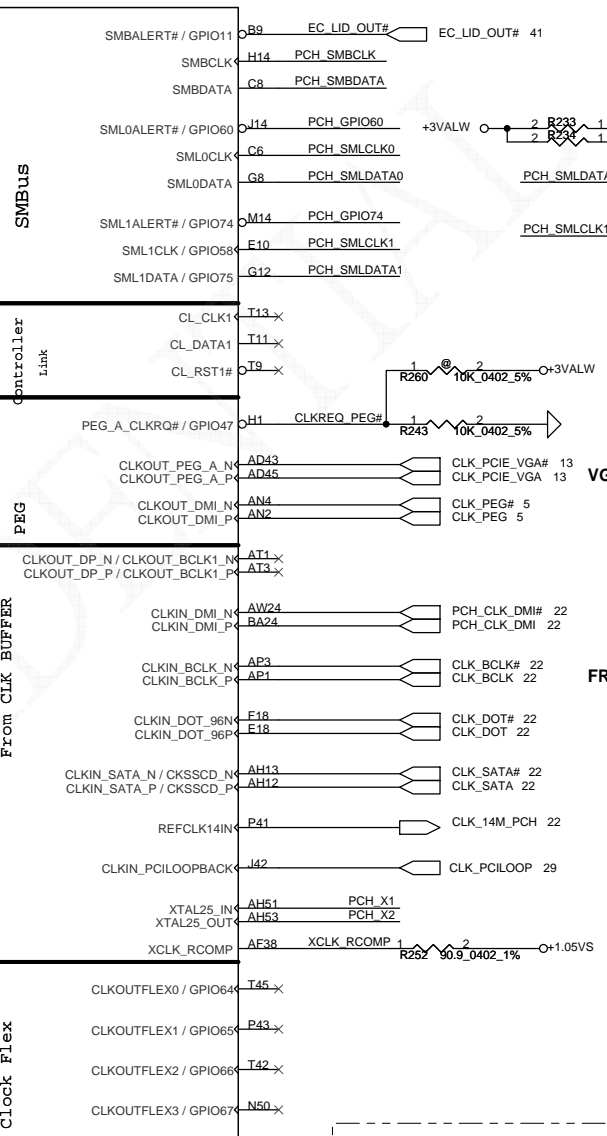
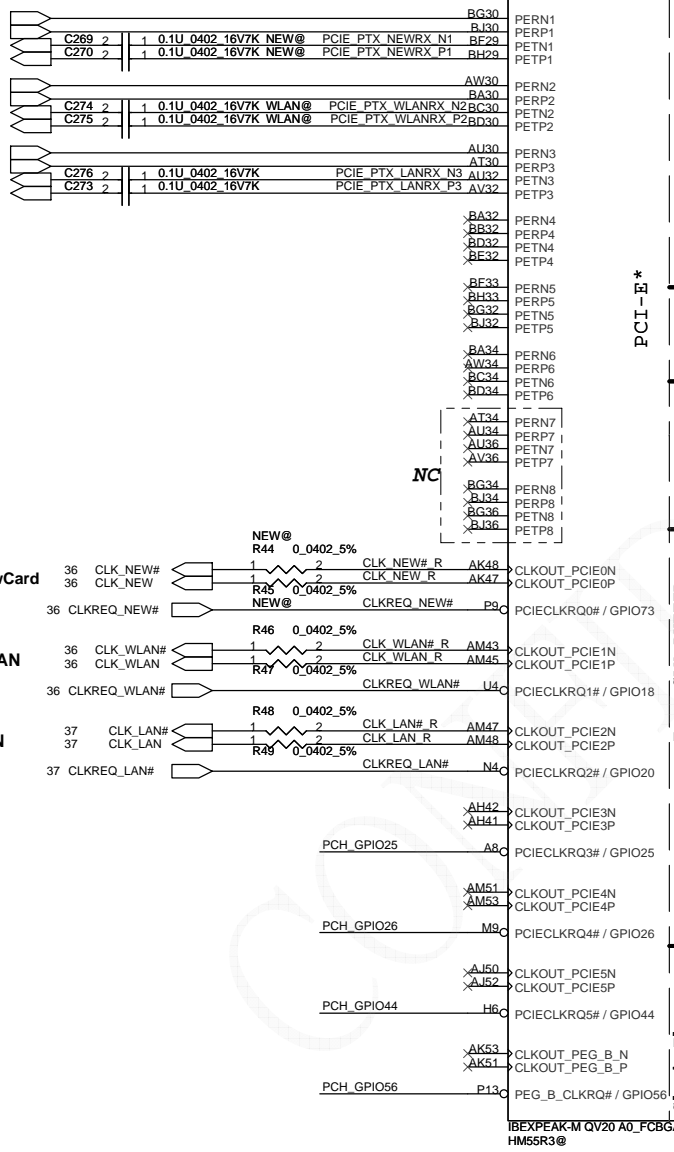
36 PCIE_PRX_NEWTX_N1
36 PCIE_PRX_NEWTX_P1
36 PCIE_PTX_C_NEWRX_N1
36 PCIE_PTX_C_NEWRX_P1

For WLAN

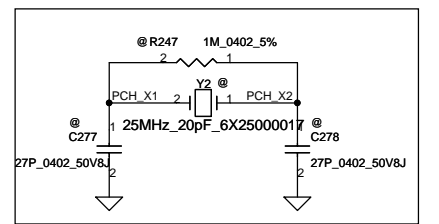
36 PCIE_PRX_WLANTX_N2
36 PCIE_PRX_WLANTX_P2
36 PCIE_PTX_C_WLANRX_N2
36 PCIE_PTX_C_WLANRX_P2

For LAN

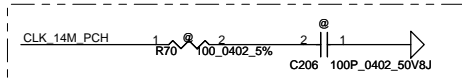
37 PCIE_PRX_C_LANTX_N3
37 PCIE_PRX_C_LANTX_P3
37 PCIE_PTX_C_LANRX_N3
37 PCIE_PTX_C_LANRX_P3



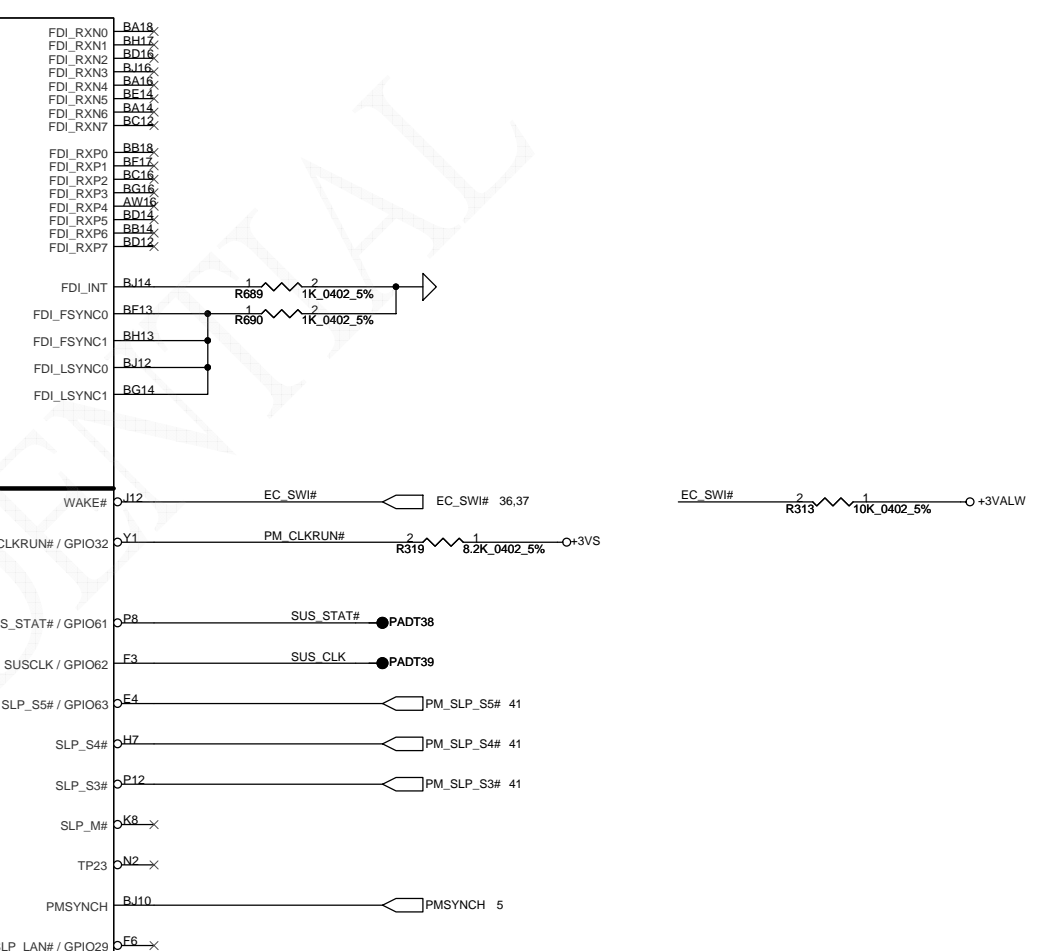
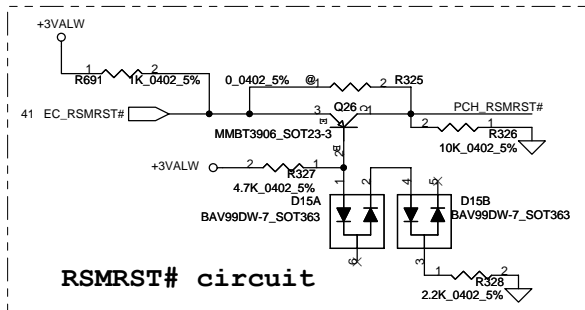
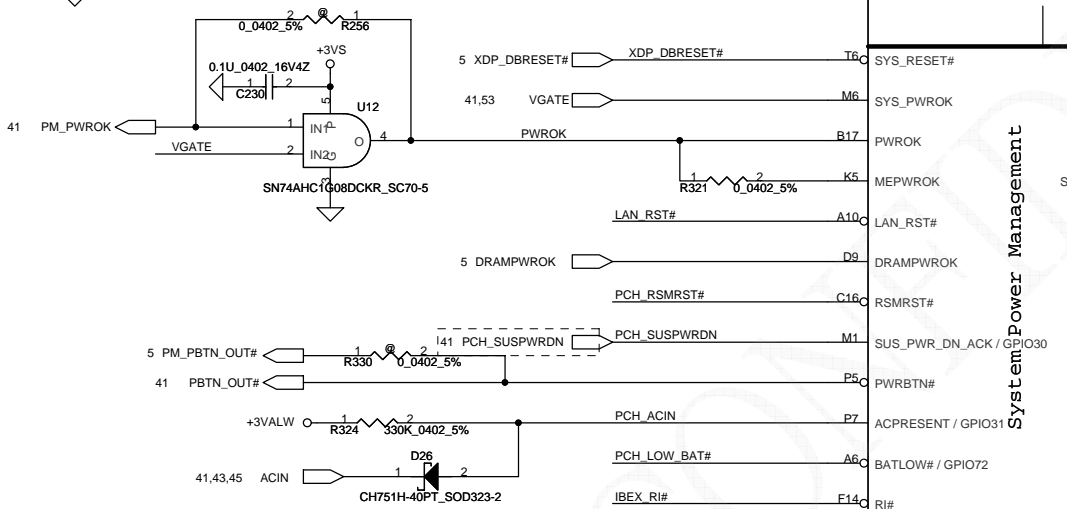
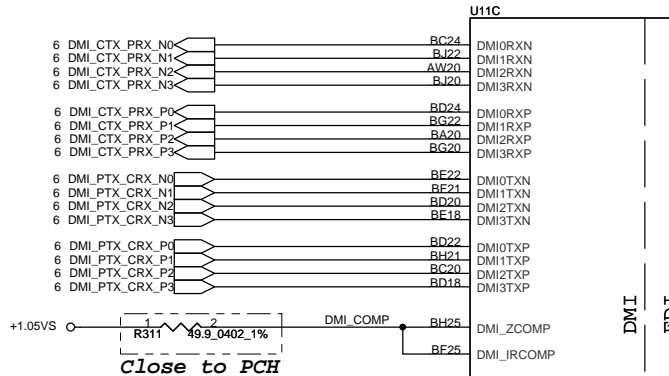
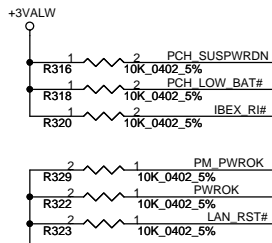
FROM CLK GEN FOR: 133/100/96/14.318 MHZ



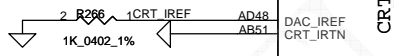
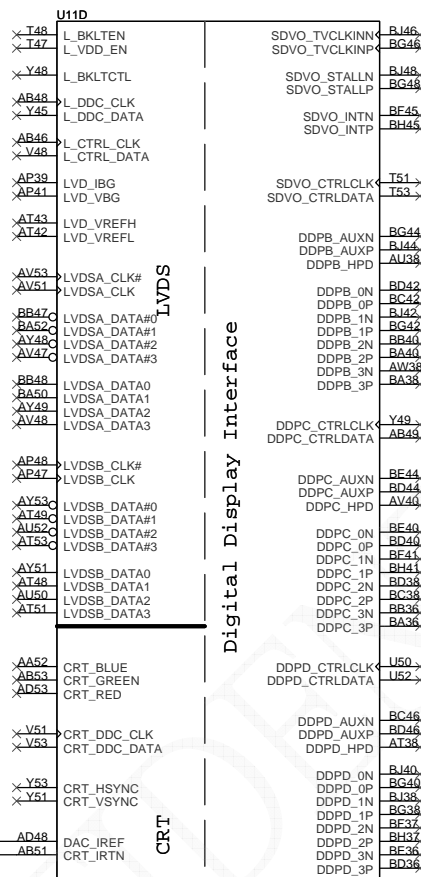
Note: Stuff 0 ohm if 25MHz crystal un-stuff



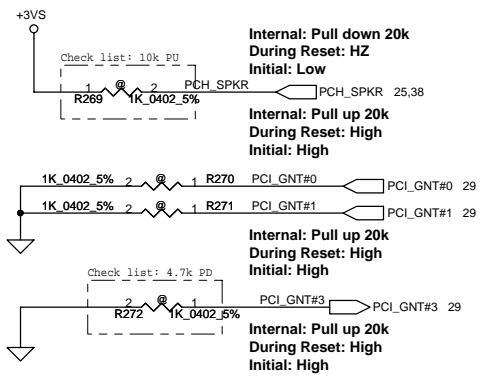
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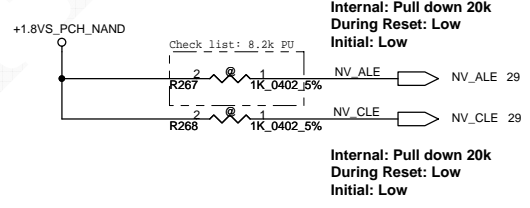
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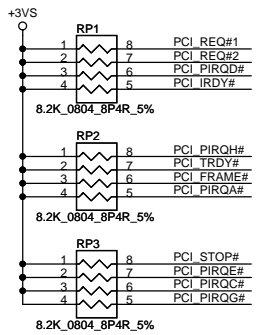
PCH Strap Pin



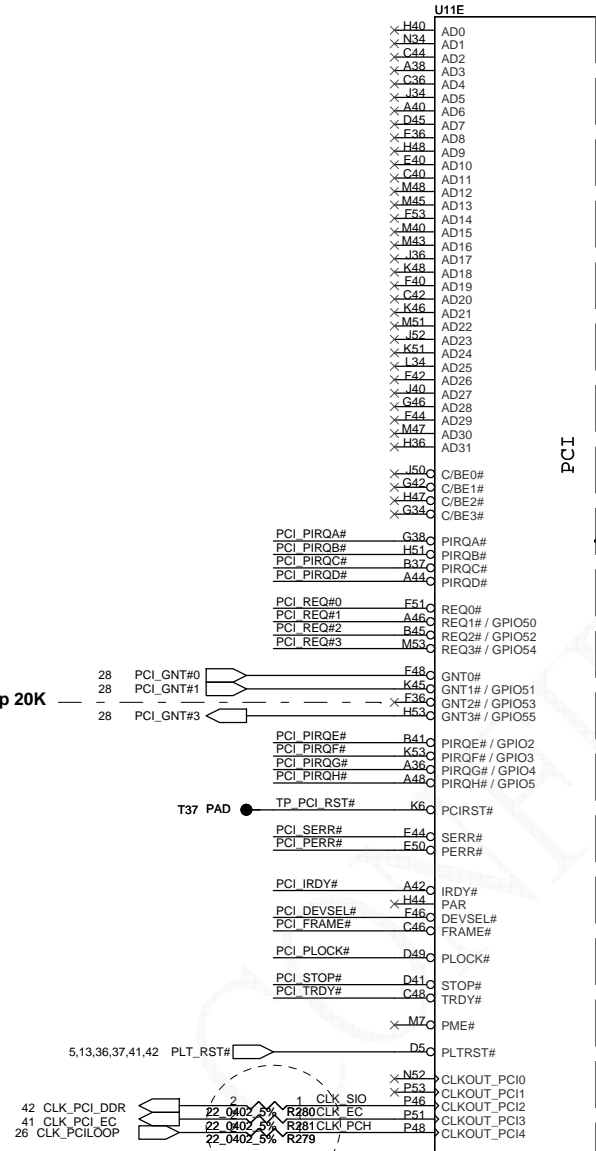
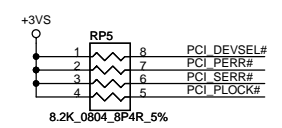
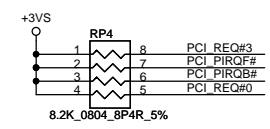
NO REBOOT Strap		
PCH_SPKR	Low= Disable	High= Enable
Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI
A16 Swap Override Strap		
PCI_GNT#3	Low= A16 swap override Enable	High= A16 swap override Disable



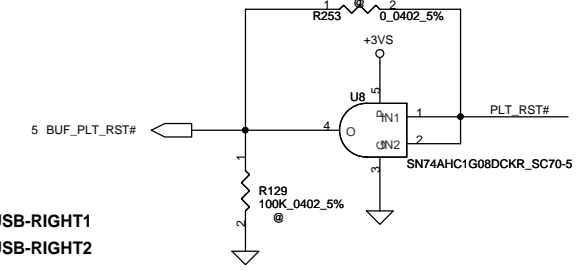
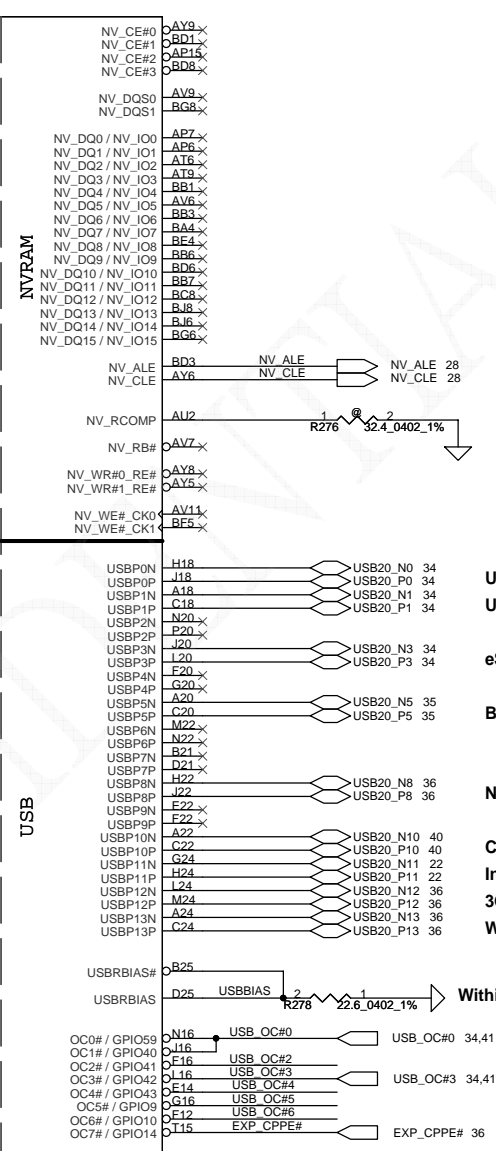
Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)
DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc



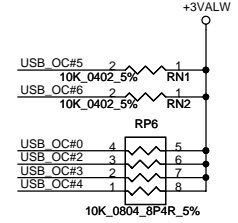
GNT2#: Not pull low, internal pull up 20K



Change to 47 ohm?



- USB-RIGHT1
- USB-RIGHT2
- eSATA-USB
- BT
- NewCard
- Card reader(3 in 1)
- Int. Camera
- 3G
- WiMax(WLAN)



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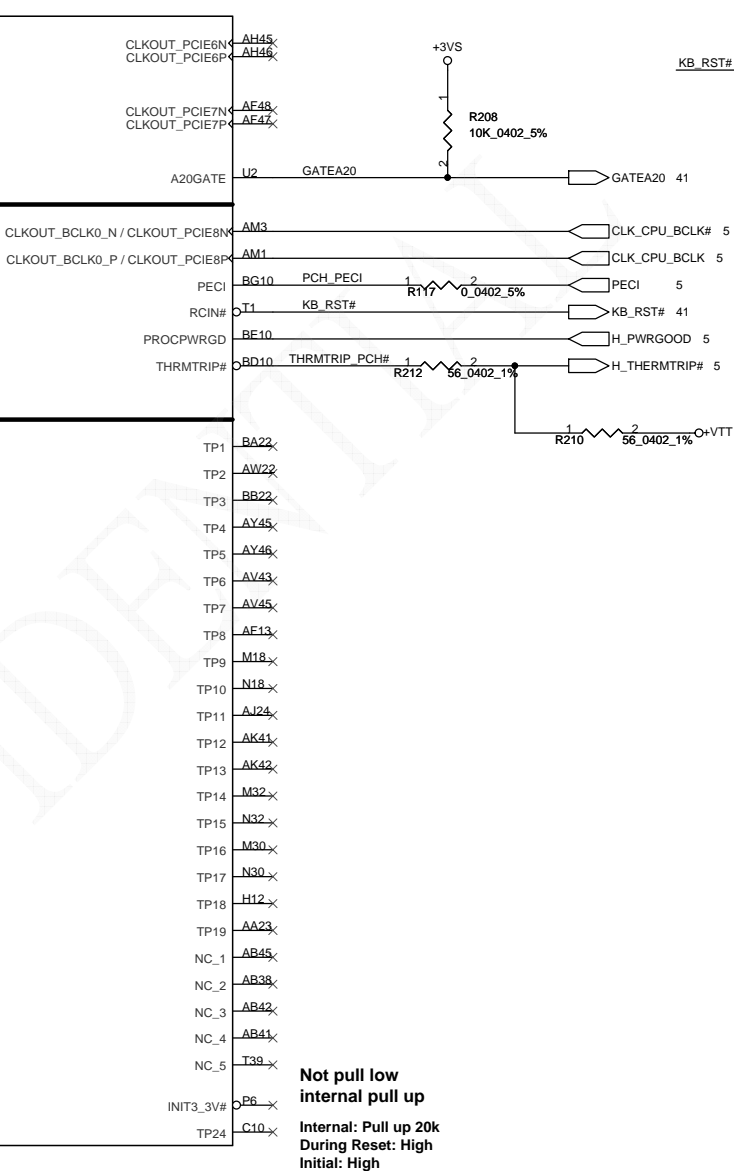
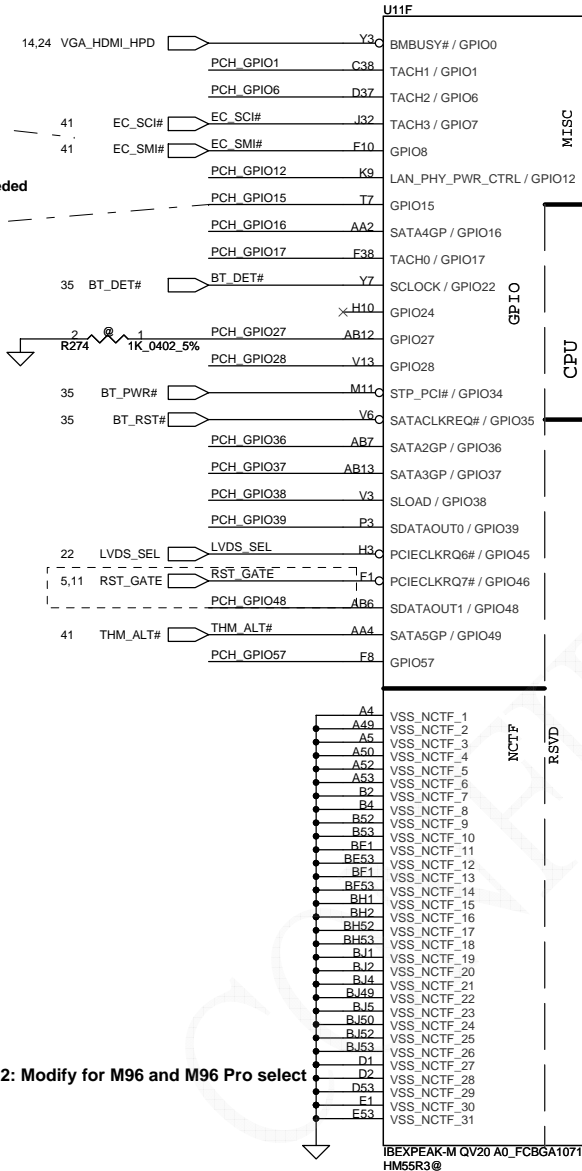
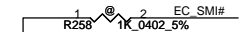
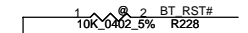
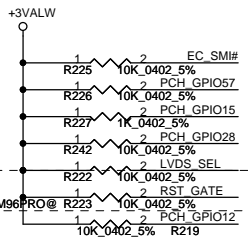
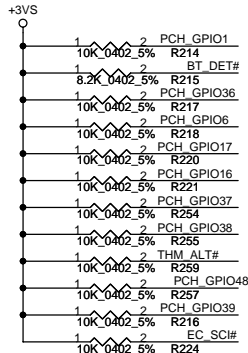
**GPIO8
Not pull down**

Internal: Pull up 20k
During Reset: High
Initial: High

**GPIO15
a Strong pull up may be needed
for GPIO Functionality**
Internal: Pull down 20k
During Reset: Low
Initial: Low

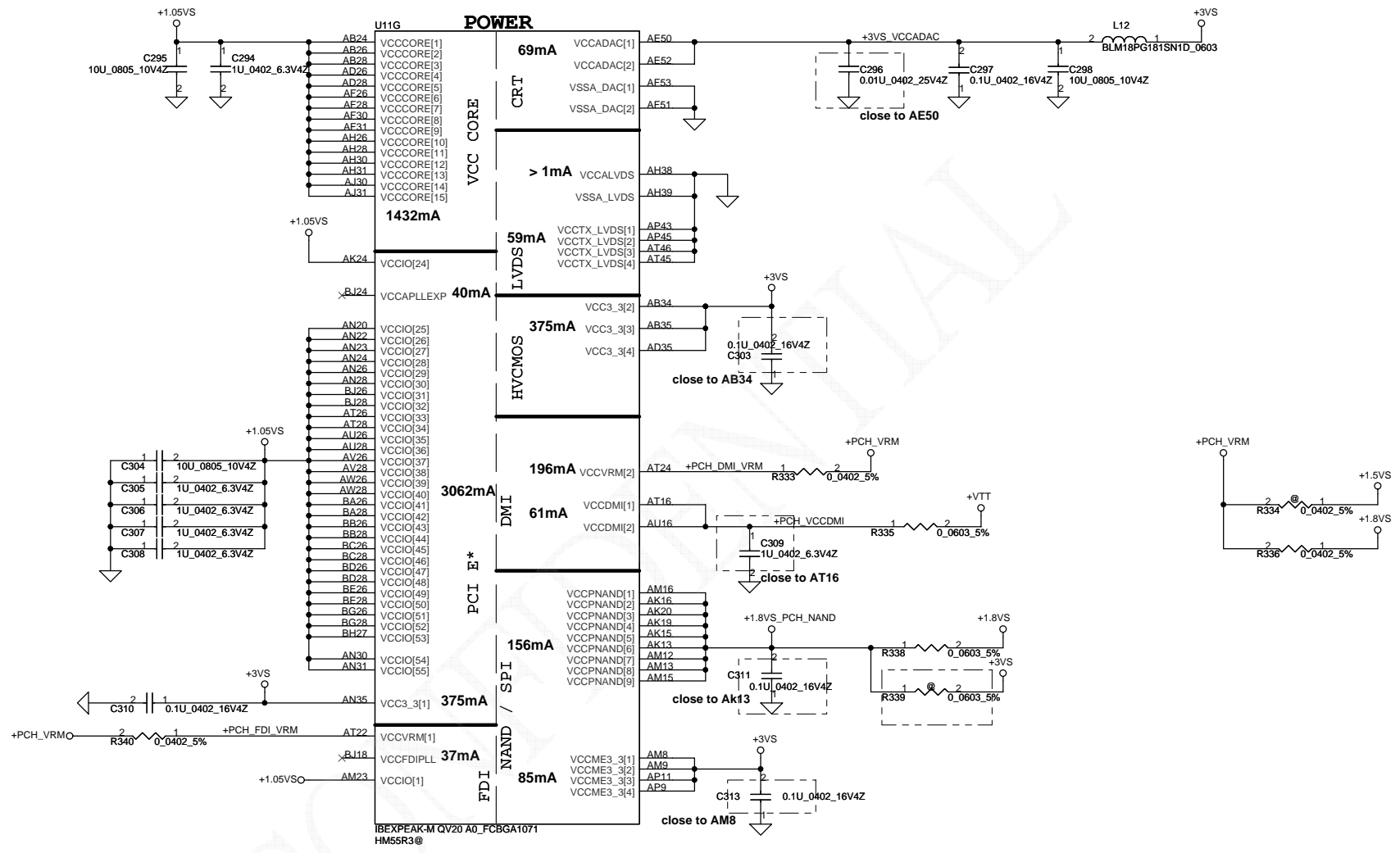
On-Die PLL VR

PCH_GPIO27 High = Enabled (Default)
Low = Disabled



**Not pull low
internal pull up**
Internal: Pull up 20k
During Reset: High
Initial: High

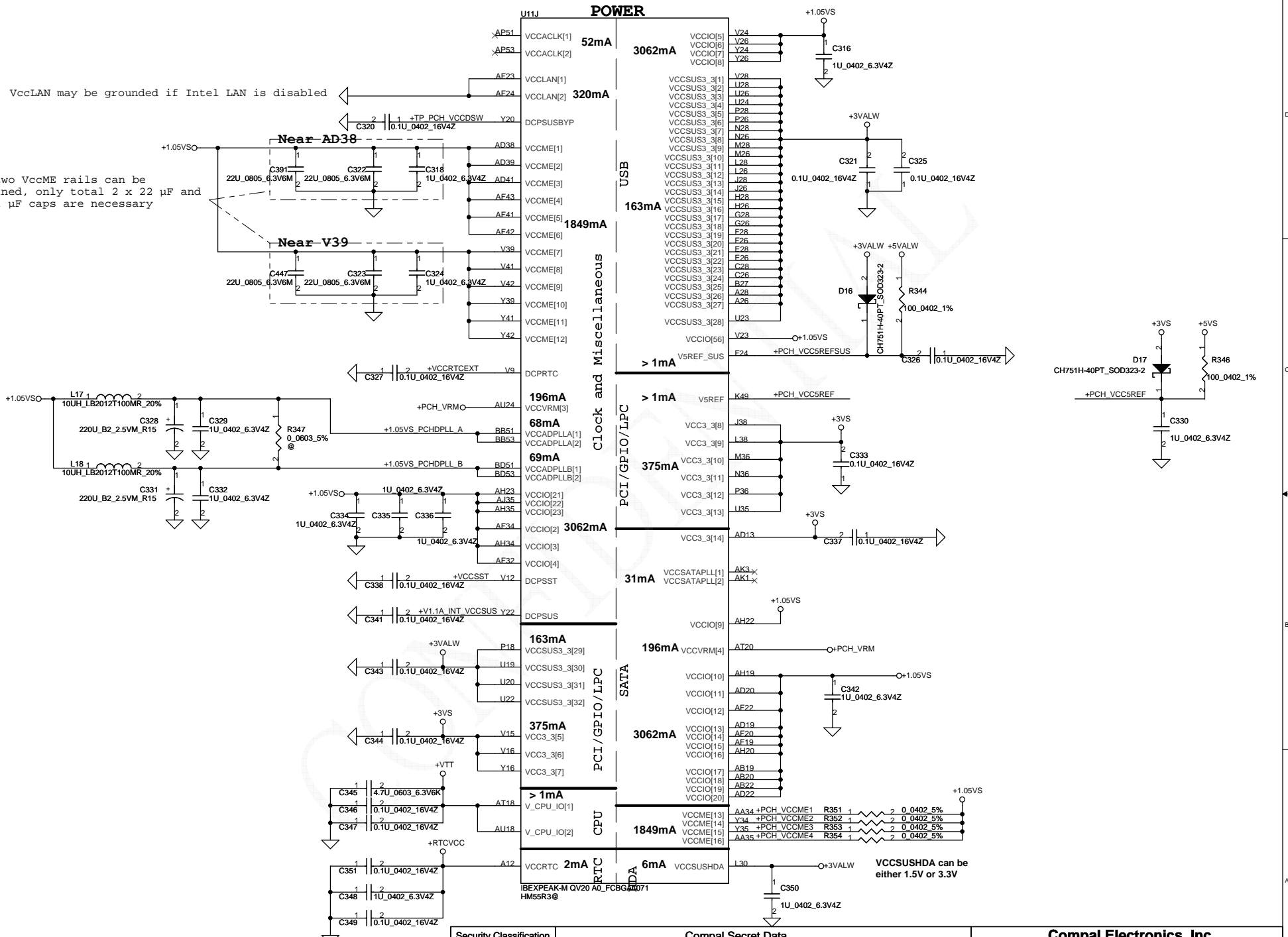
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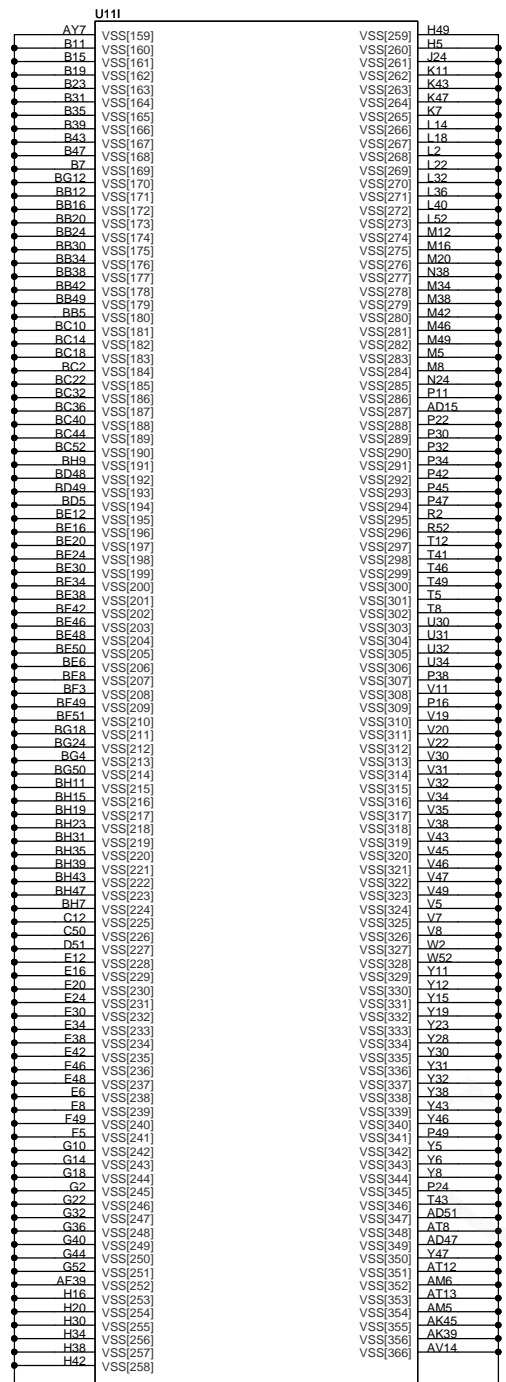
VccLAN may be grounded if Intel LAN is disabled

If two VccME rails can be combined, only total 2 x 22 µF and 2 x 1 µF caps are necessary

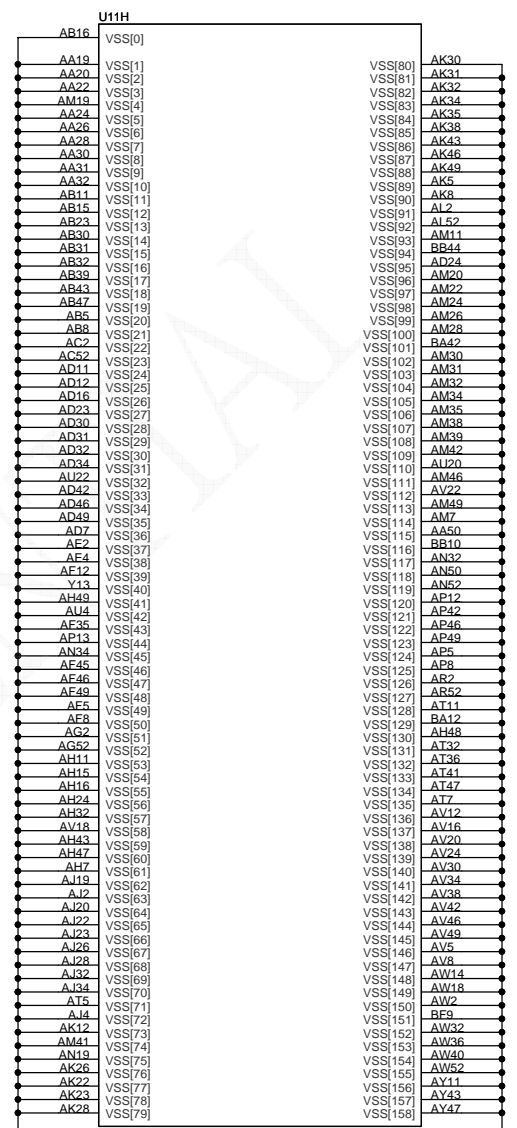


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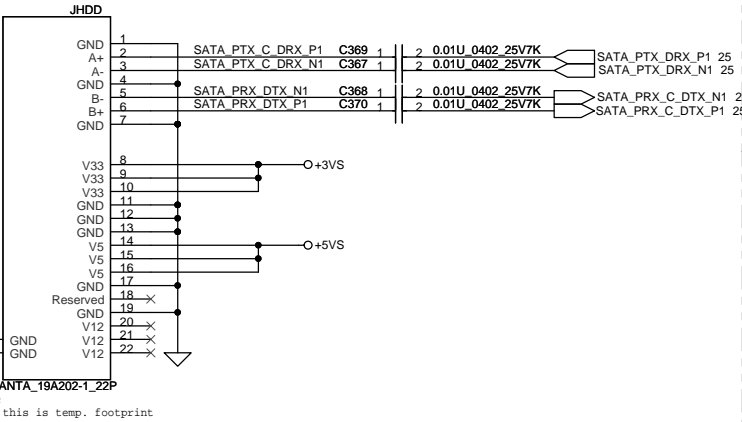
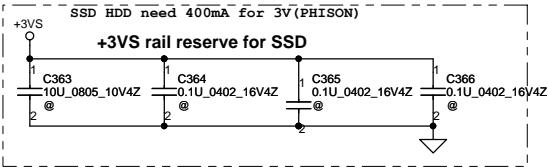
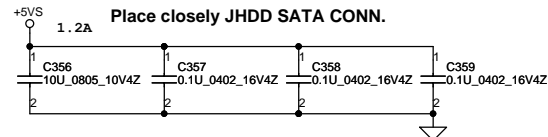
IBEXPEAK-M QV20 A0_FCBGA1071
HM55R3@



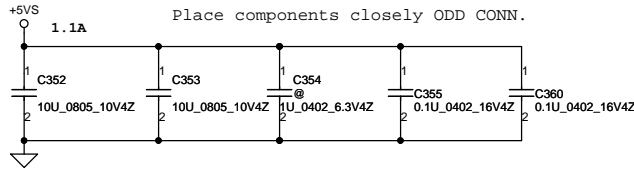
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HM55R3@

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SATA HDD Conn.

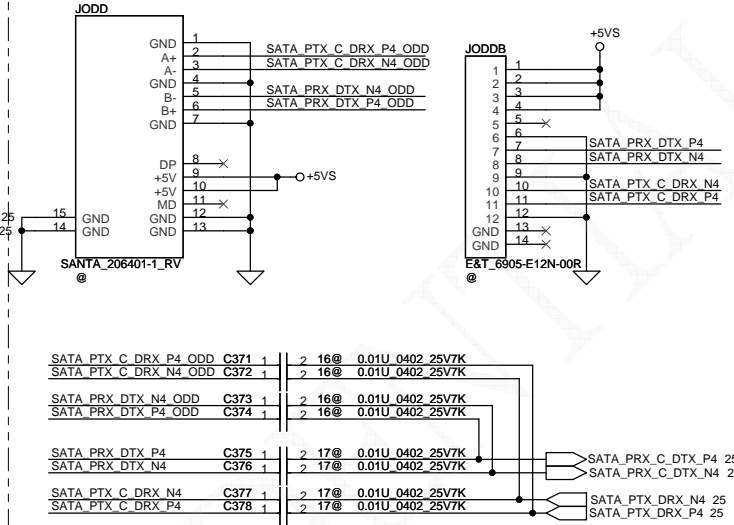


SATA ODD Conn

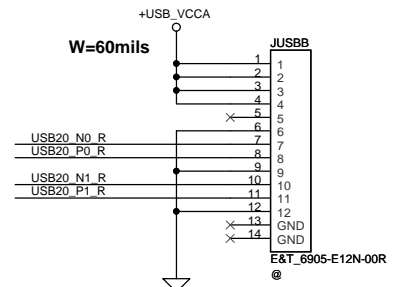
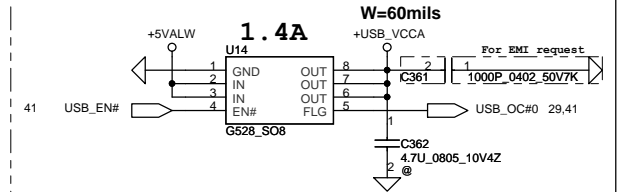


for 16" use

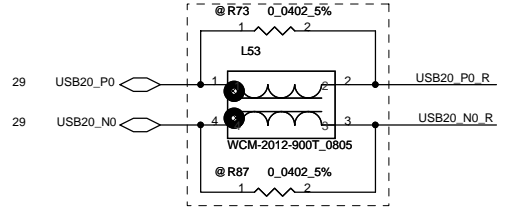
for 17" expansion using



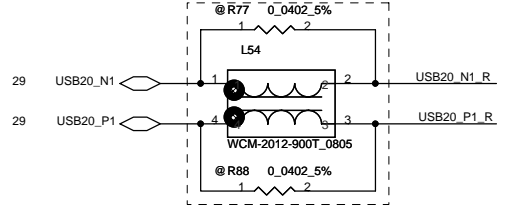
USB Board



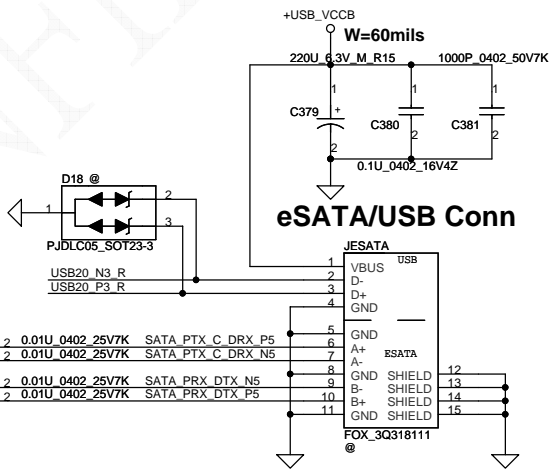
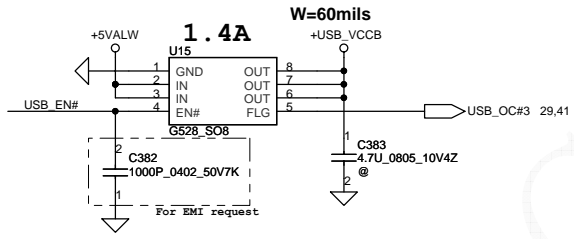
Reserve for EMI request



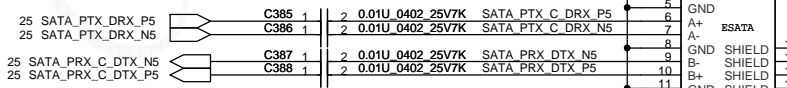
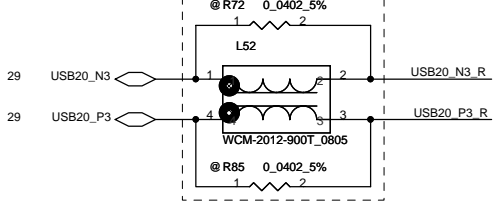
Reserve for EMI request



eSATA/USB

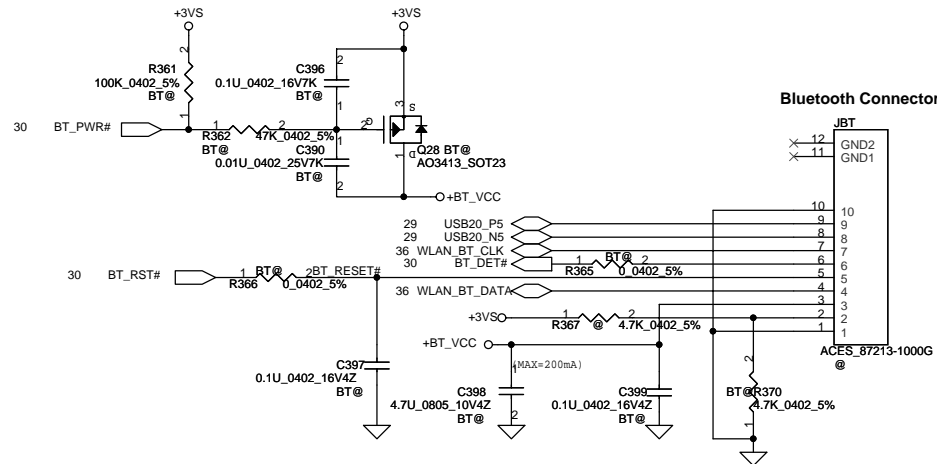


Reserve for EMI request

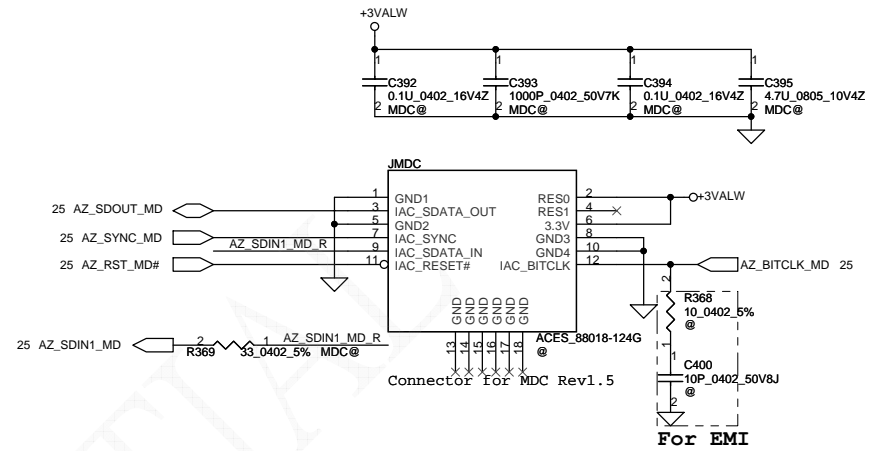


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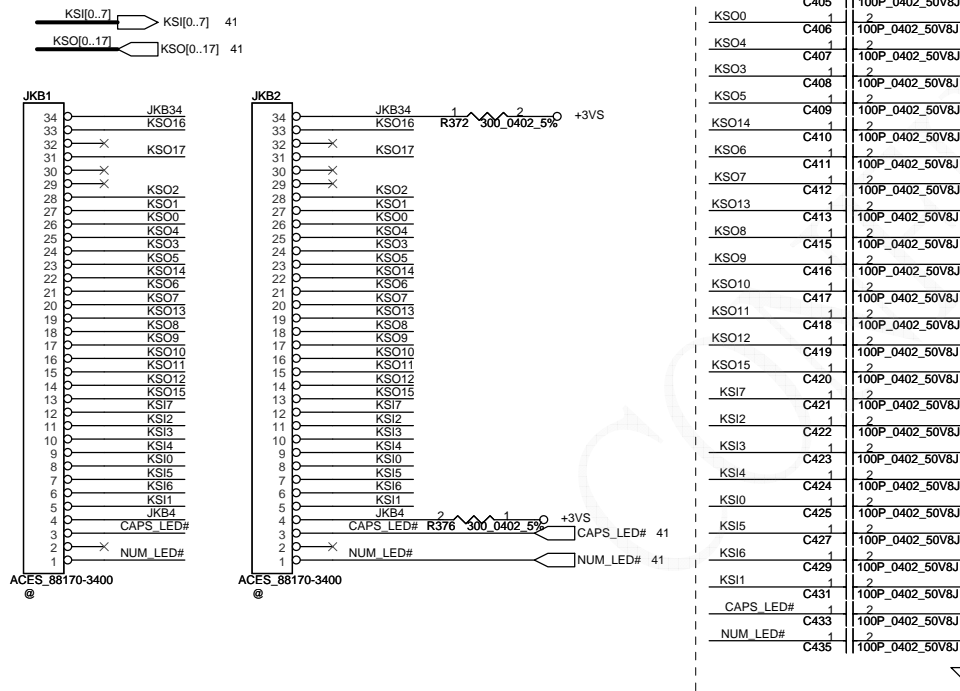
BlueTooth Interface



MDC 1.5 Conn.



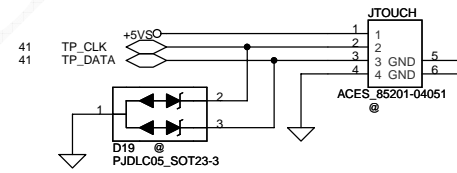
KEYBOARD CONN. for 16" KEYBOARD CONN. for 17"



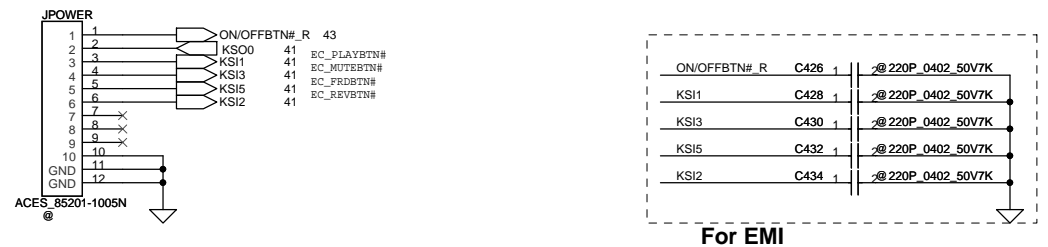
please close to JKBI

KSO16	1	2
KSO17	C401	100P_0402_50V8J
KSO2	C402	100P_0402_50V8J
KSO1	C403	100P_0402_50V8J
KSO0	C404	100P_0402_50V8J
KSO4	C405	100P_0402_50V8J
KSO3	C406	100P_0402_50V8J
KSO5	C407	100P_0402_50V8J
KSO6	C408	100P_0402_50V8J
KSO14	C409	100P_0402_50V8J
KSO7	C410	100P_0402_50V8J
KSO8	C411	100P_0402_50V8J
KSO13	C412	100P_0402_50V8J
KSO9	C413	100P_0402_50V8J
KSO10	C414	100P_0402_50V8J
KSO11	C415	100P_0402_50V8J
KSO12	C416	100P_0402_50V8J
KSO15	C417	100P_0402_50V8J
KSO15	C418	100P_0402_50V8J
KSO15	C419	100P_0402_50V8J
KSO15	C420	100P_0402_50V8J
KSI7	C421	100P_0402_50V8J
KSI2	C422	100P_0402_50V8J
KSI3	C423	100P_0402_50V8J
KSI4	C424	100P_0402_50V8J
KSI0	C425	100P_0402_50V8J
KSI5	C426	100P_0402_50V8J
KSI6	C427	100P_0402_50V8J
KSI6	C428	100P_0402_50V8J
KSI6	C429	100P_0402_50V8J
KSI1	C430	100P_0402_50V8J
CAPS_LED#	C431	100P_0402_50V8J
CAPS_LED#	C432	100P_0402_50V8J
NUM_LED#	C433	100P_0402_50V8J
NUM_LED#	C434	100P_0402_50V8J
NUM_LED#	C435	100P_0402_50V8J

Touch/B Connector

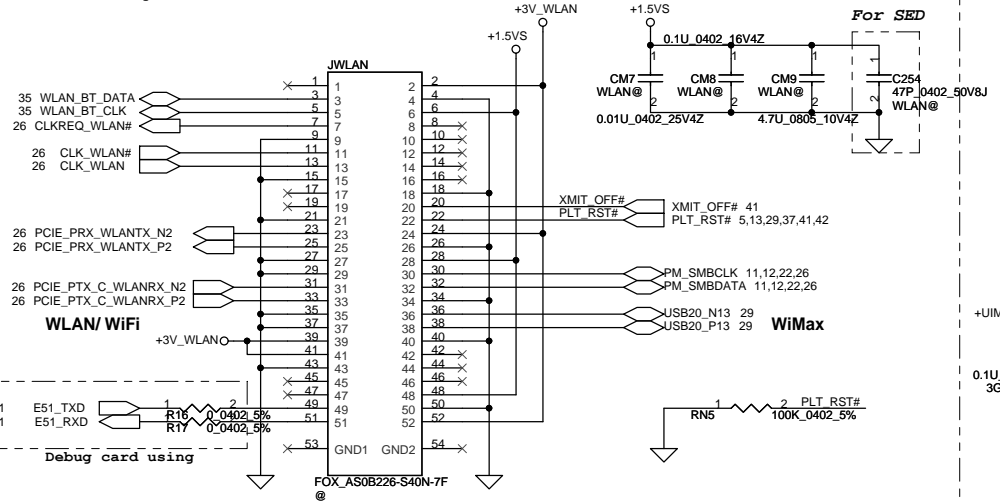
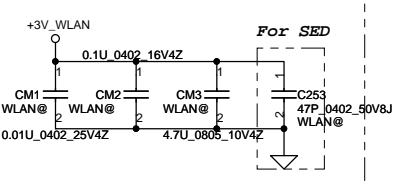
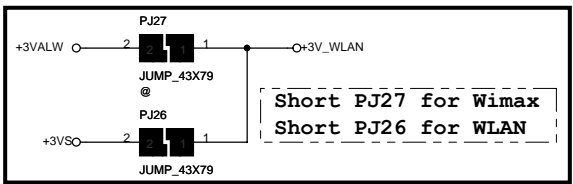


SW/B Connector

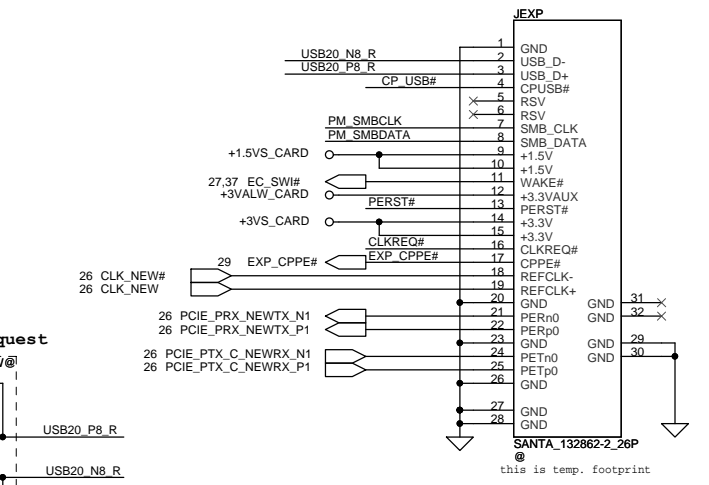
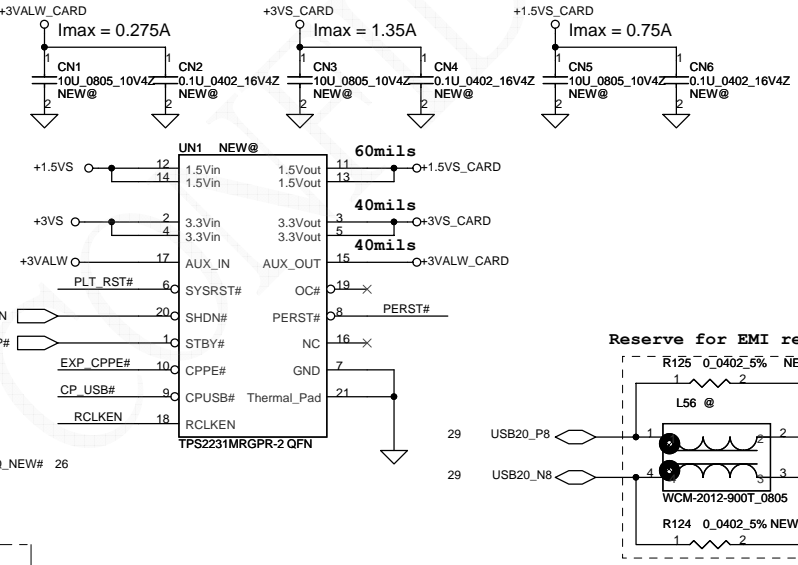
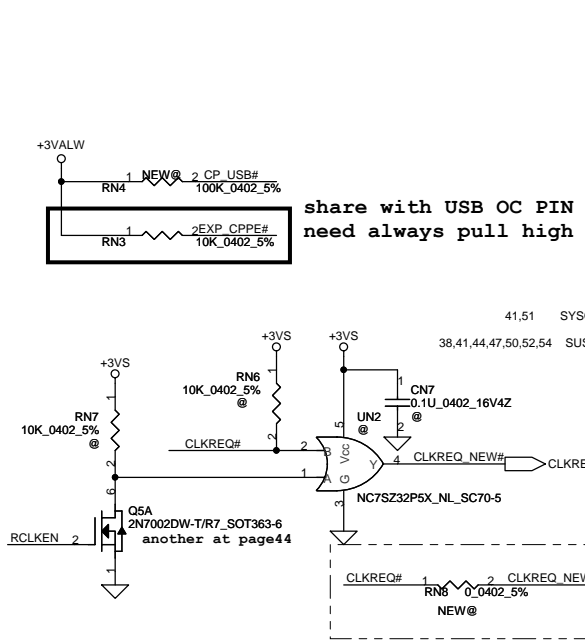
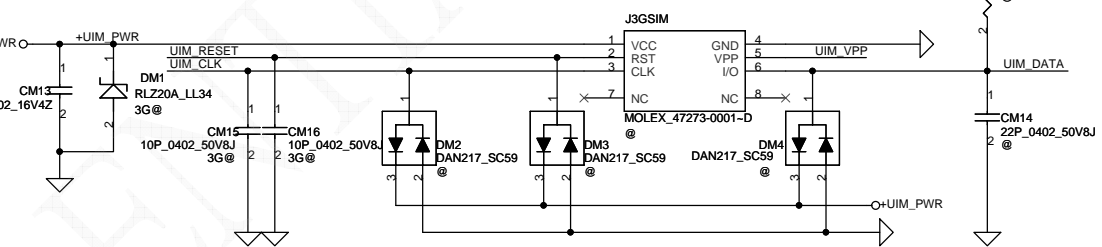
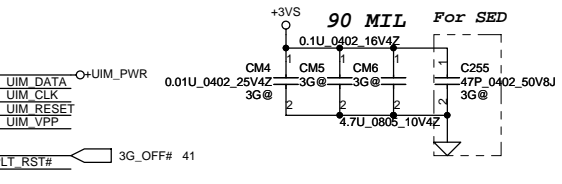
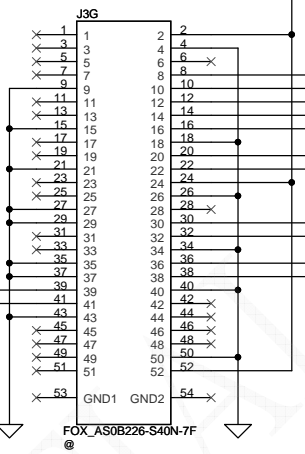


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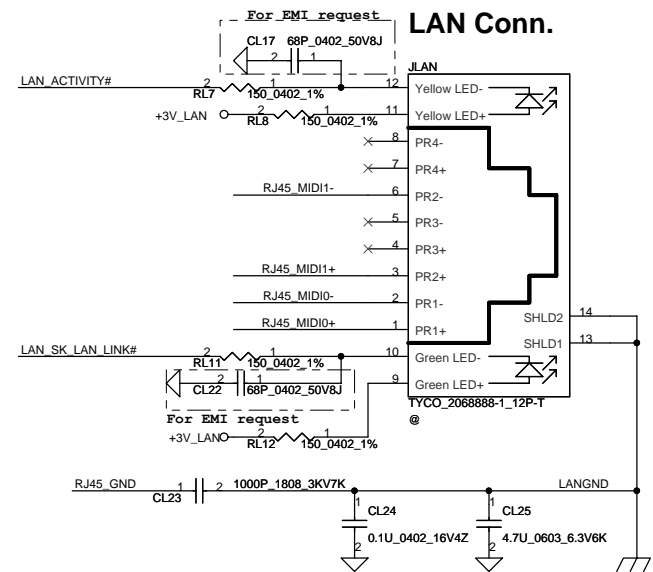
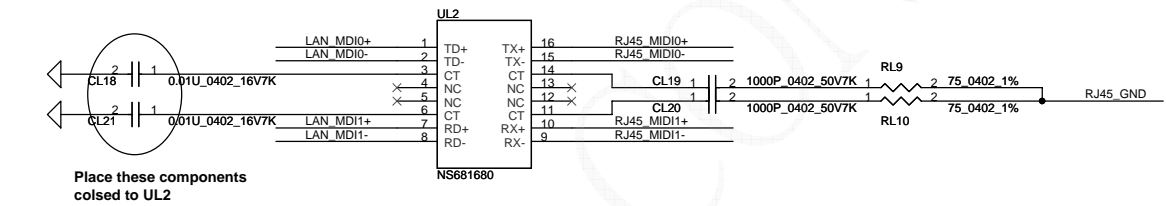
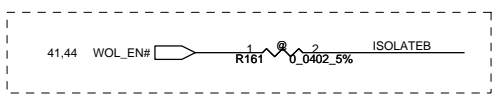
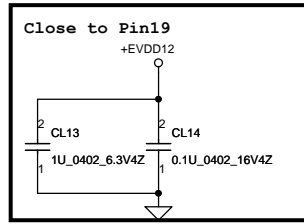
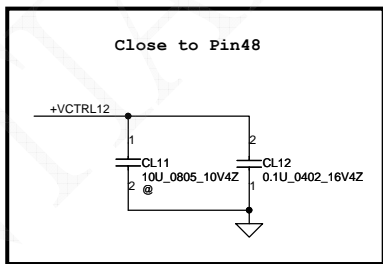
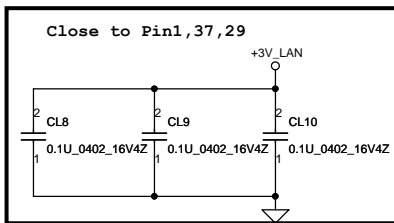
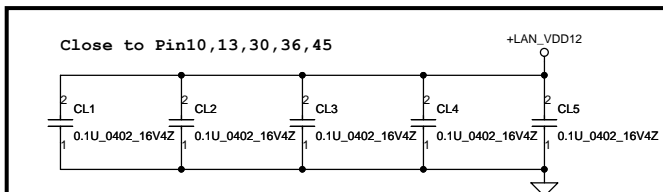
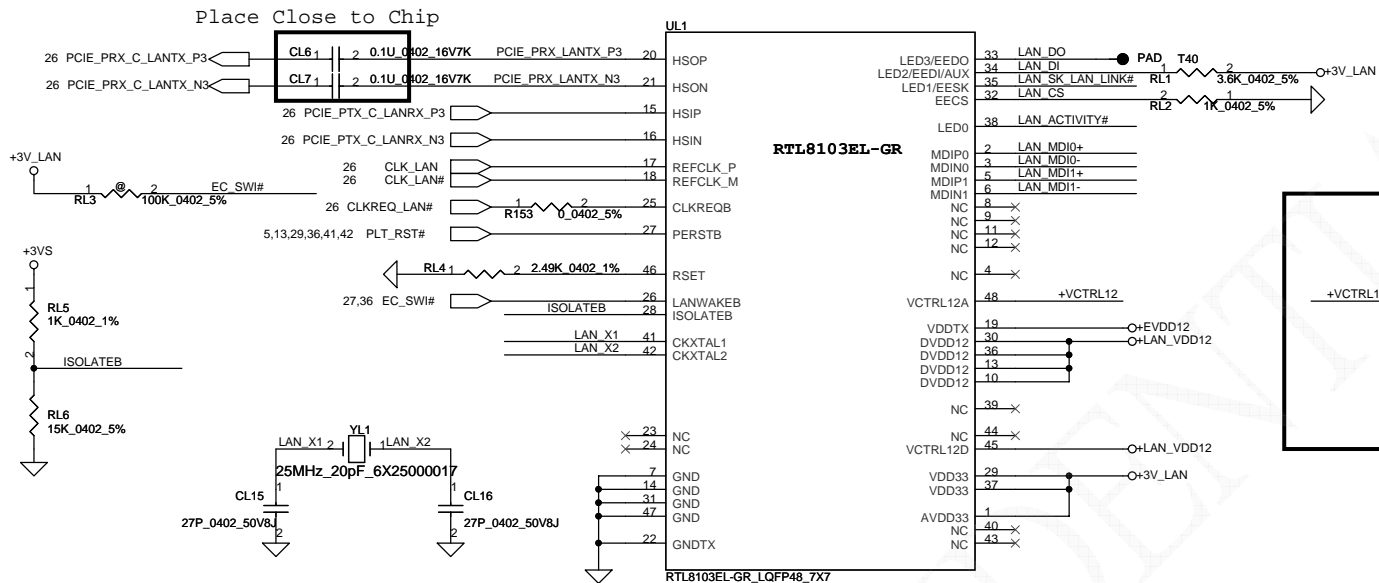
PCIe Mini Card-WLAN/WiMax



PCIe Mini Card-3G

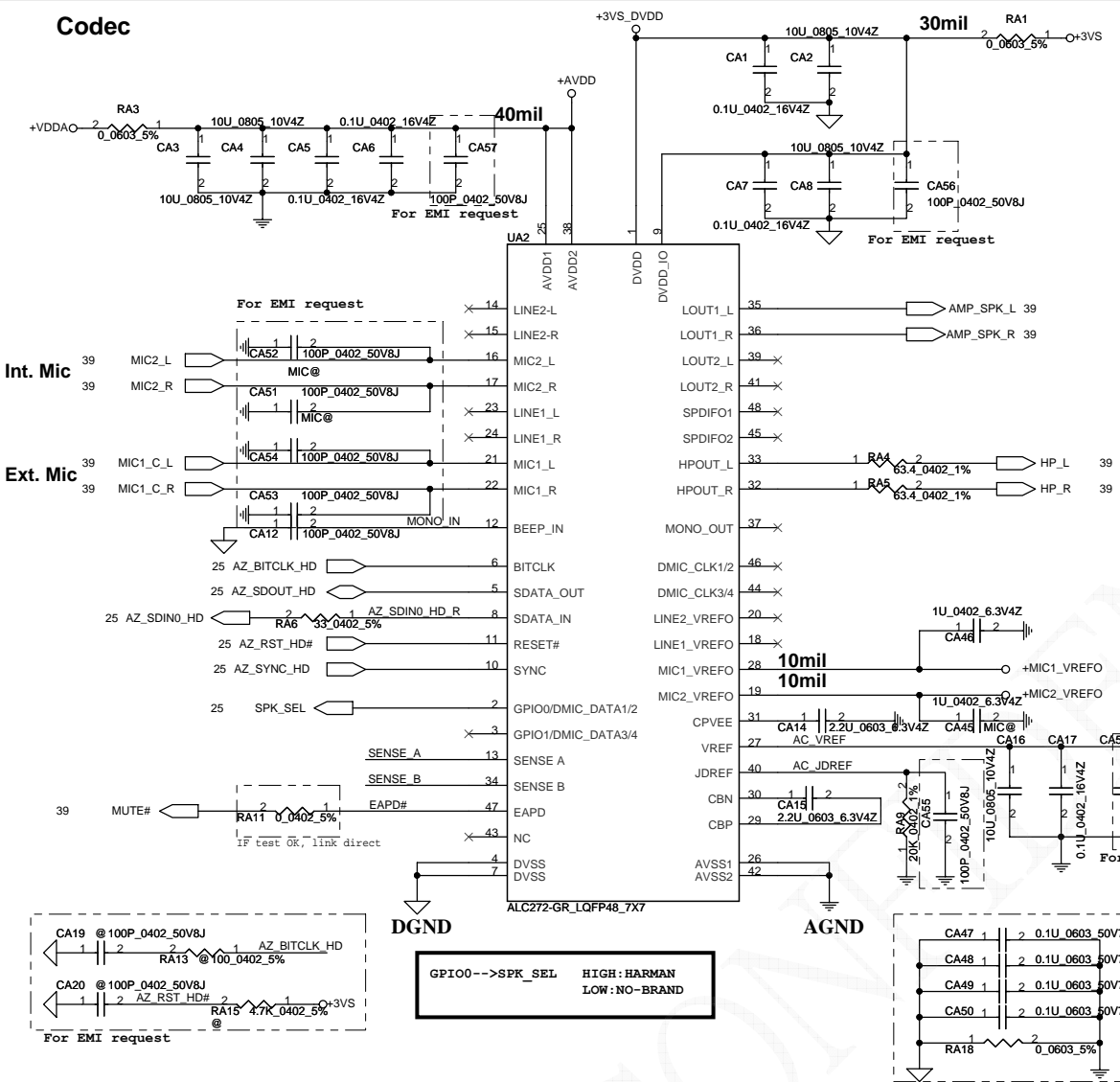


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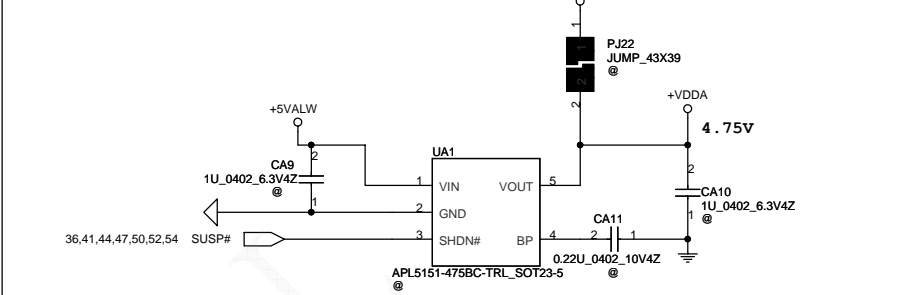


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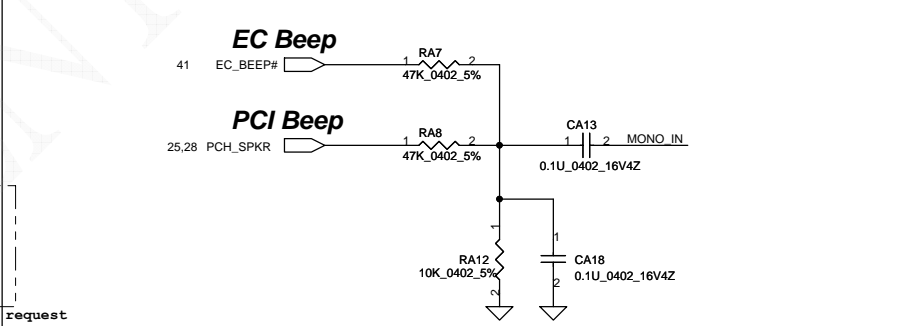
Codec



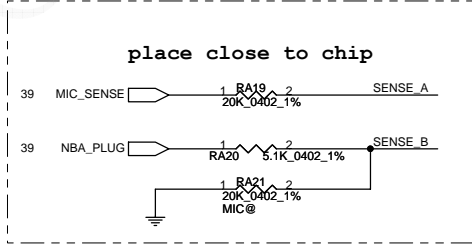
Audio regulator



Beep sound

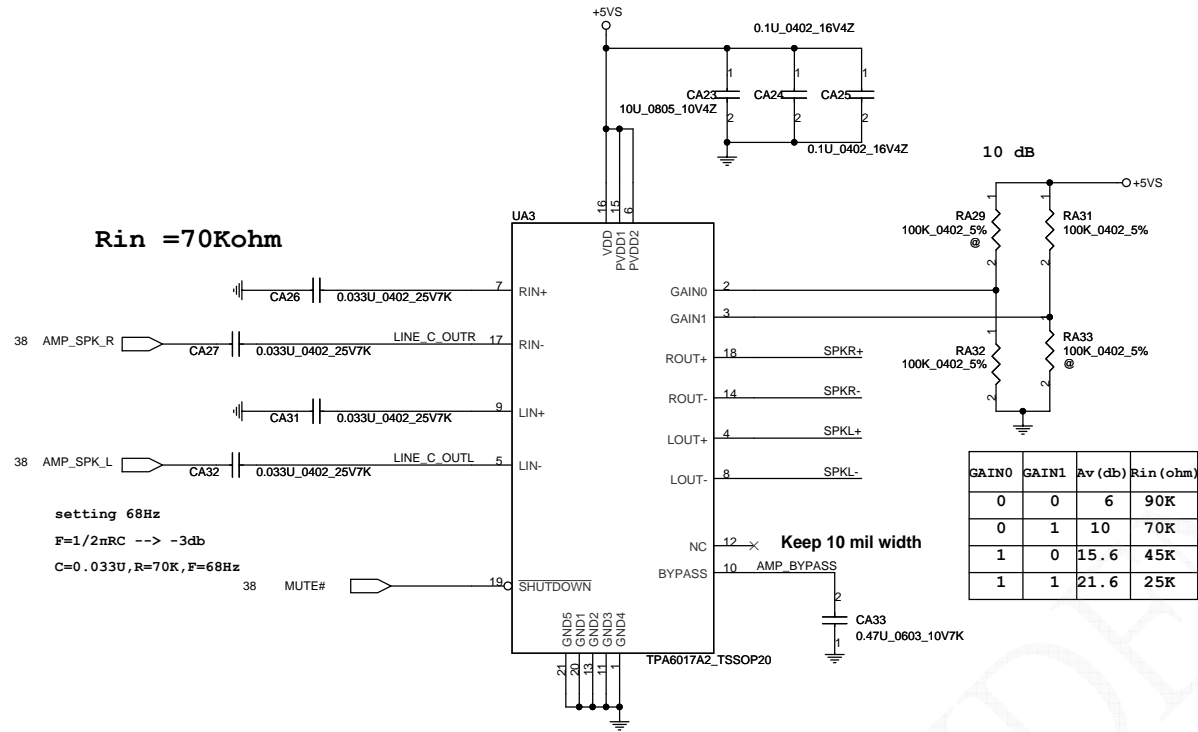


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out

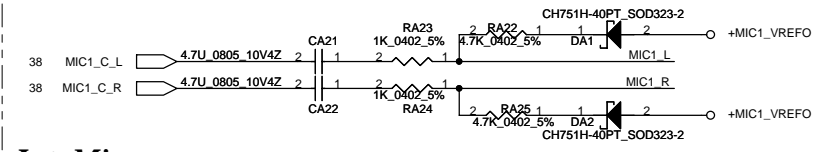


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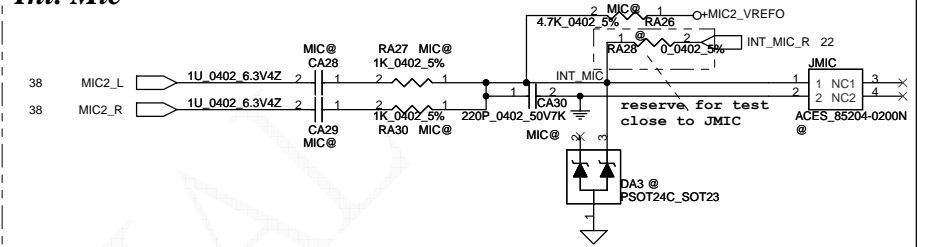
TPA6017 Medium Range Amplifier



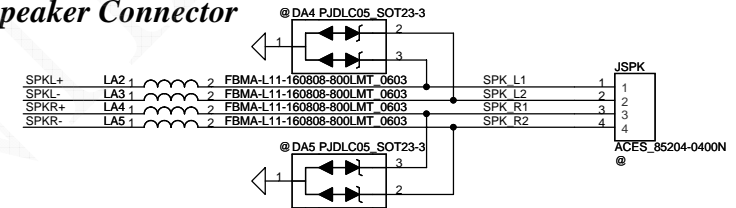
Ext. Mic



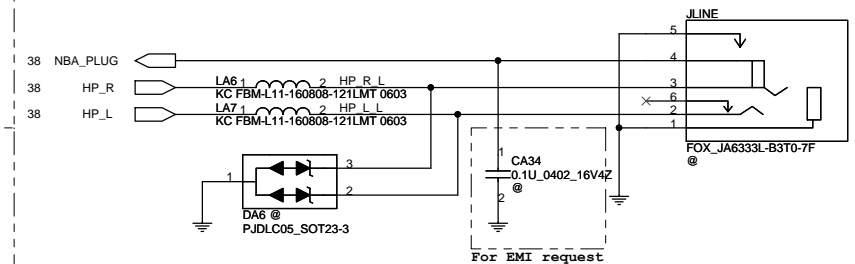
Int. Mic



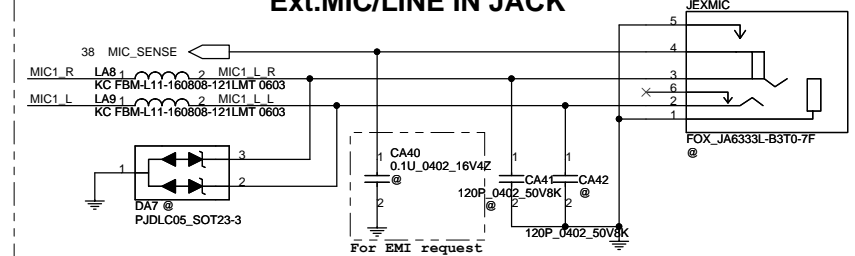
Speaker Connector



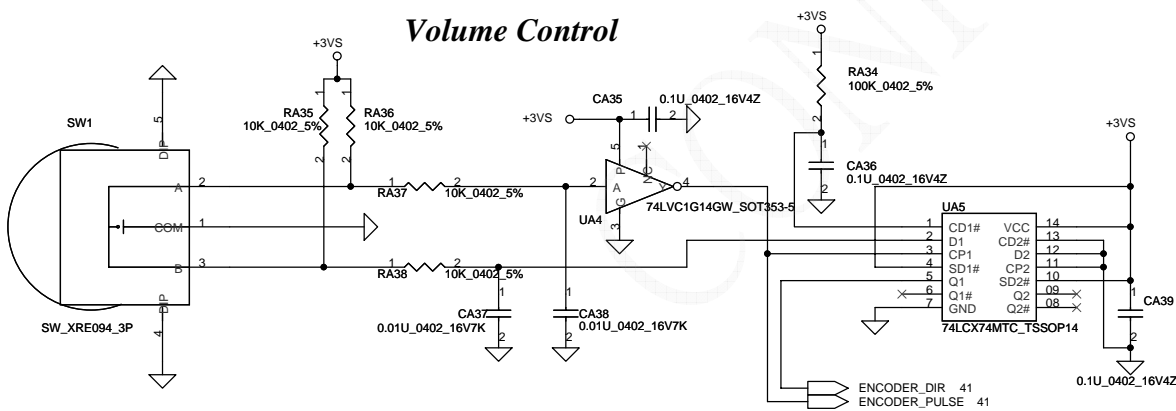
HeadPhone/LINE Out JACK



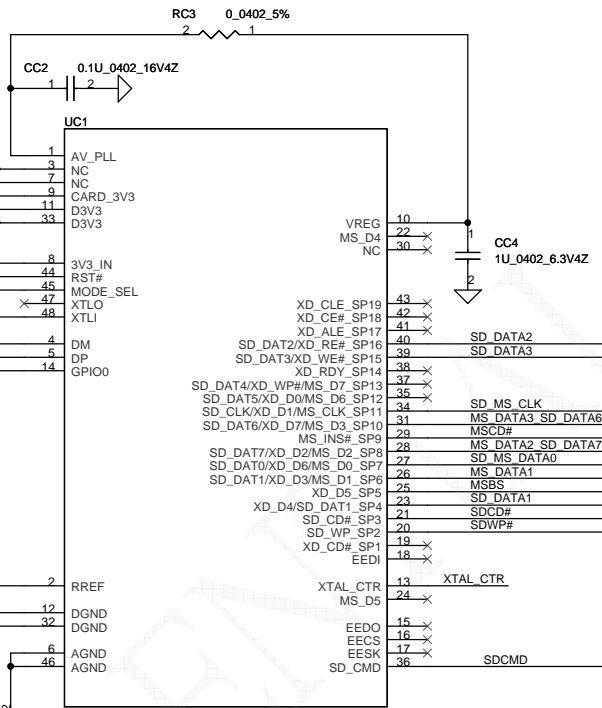
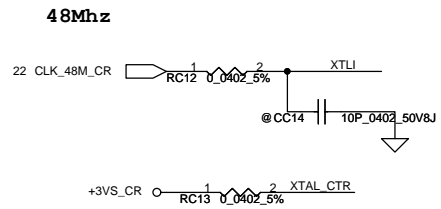
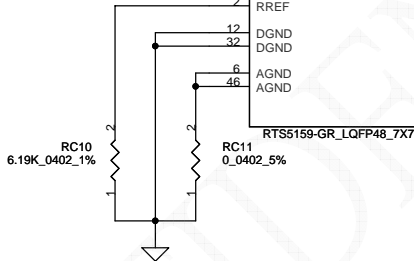
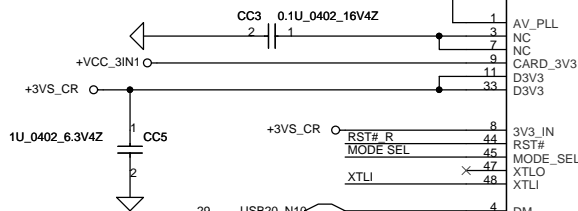
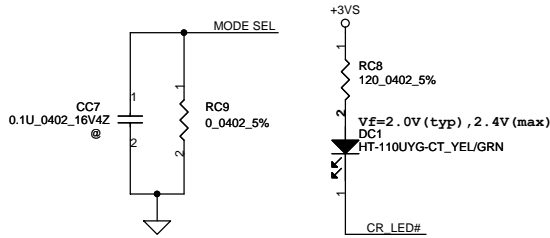
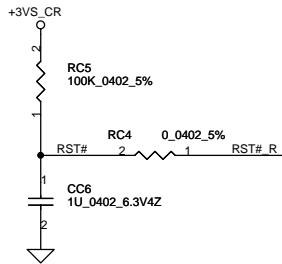
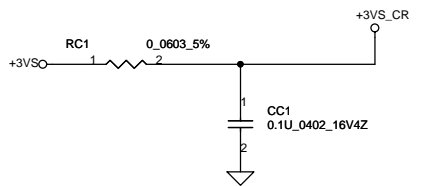
Ext.MIC/LINE IN JACK



Volume Control

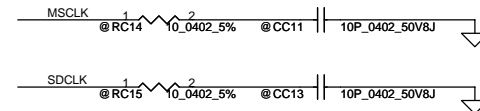
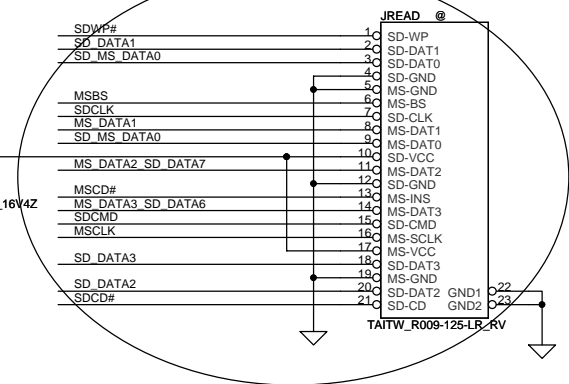


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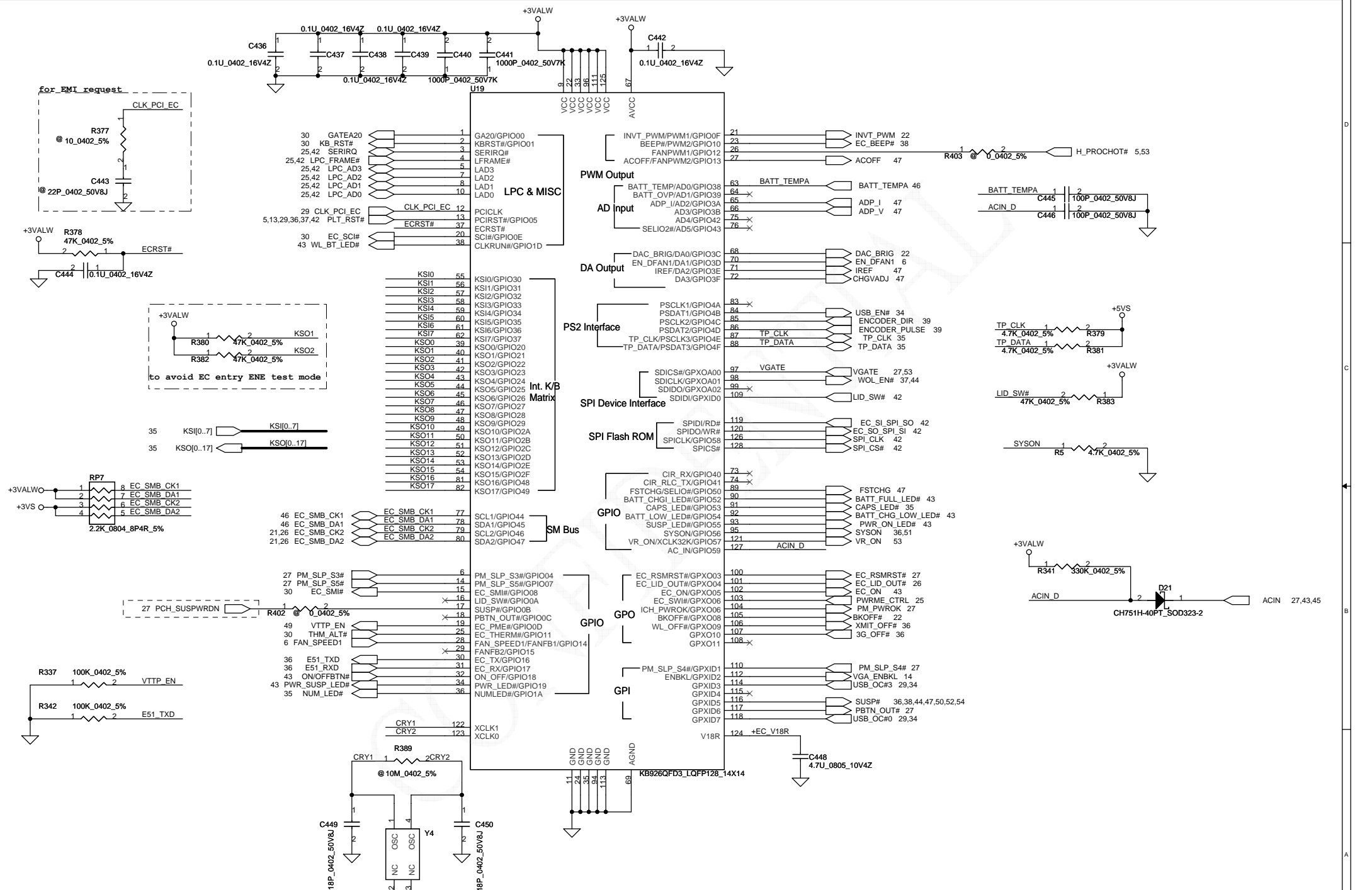
3 in 1 Card Reader

confirm all pin define with connector spec.



R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

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Compal Electronics, Inc.

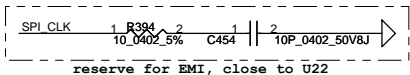
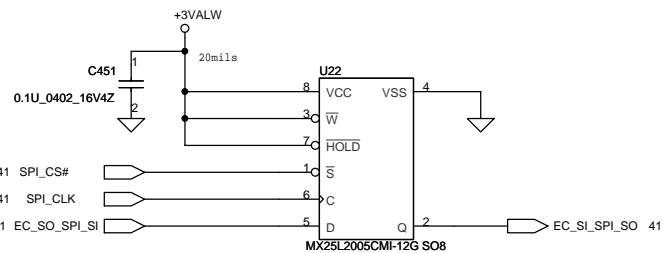
Schematic, LA5322P M/B

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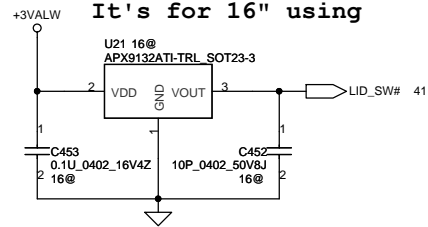
SPI Flash (256KB)

Socket: SP07000F500 & SP07000H900

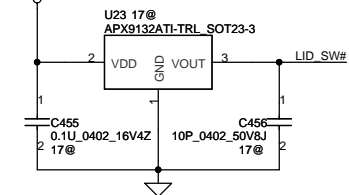


Lid SW

It's for 16" using

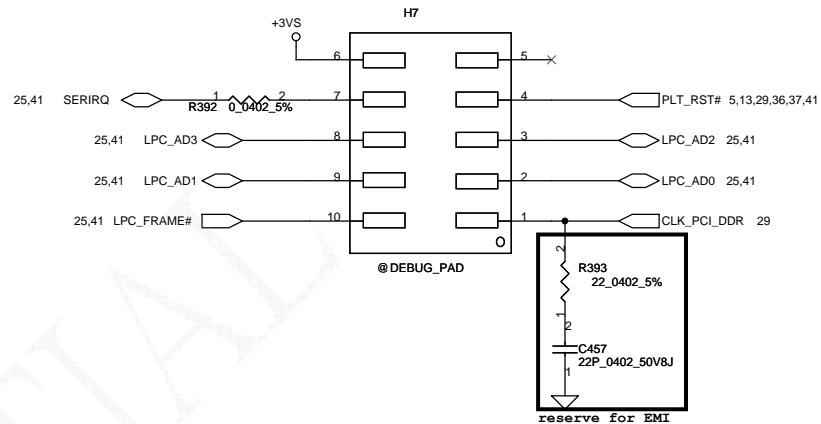


It's for 17" using



LPC Debug Port

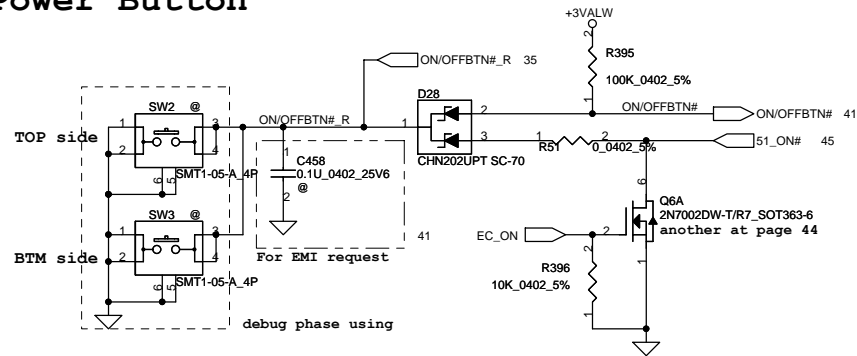
Please place the PAD under DDR DIMM.



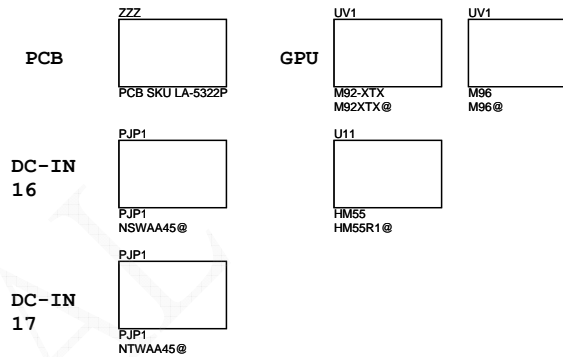
CONFIDENTIAL

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Power Button

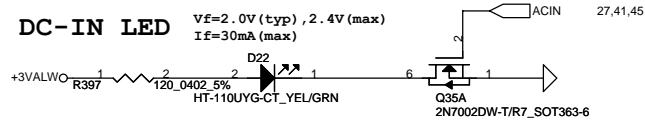


ISPD

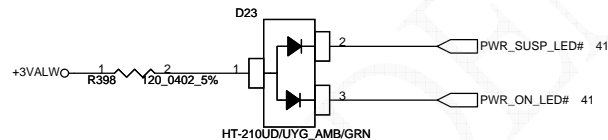


DC-IN LED

$V_f = 2.0V$ (typ), $2.4V$ (max)
 $I_f = 30mA$ (max)

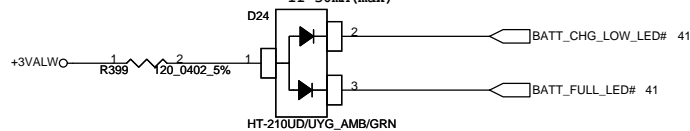


POWER/SUSPEND LED

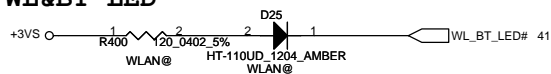


BATT CHARGE/FULL LED

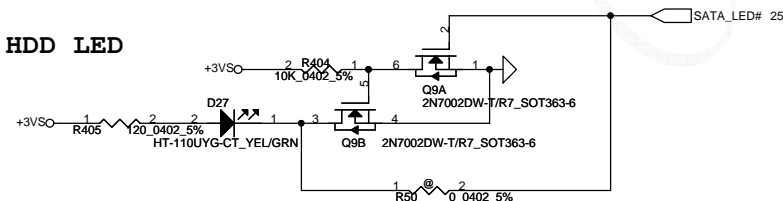
$V_f = 1.9V$ (typ), $2.4V$ (max) for amber
 $V_f = 2.0V$ (typ), $2.4V$ (max) for green
 $I_f = 30mA$ (max)



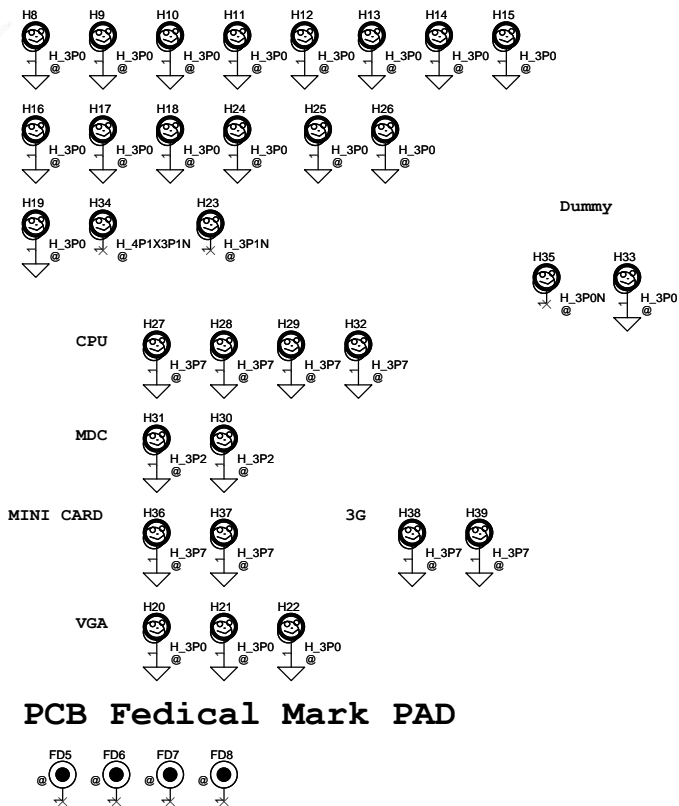
WL&BT LED



HDD LED

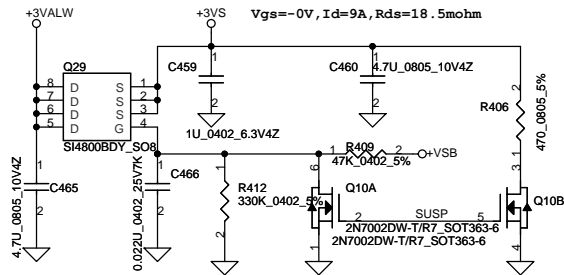


Screw Hole

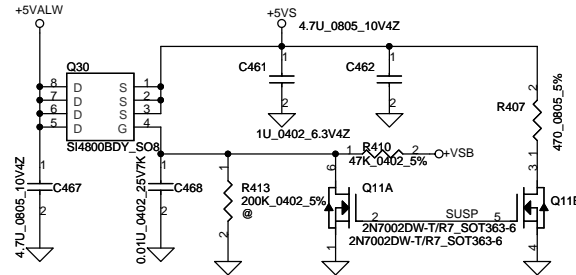


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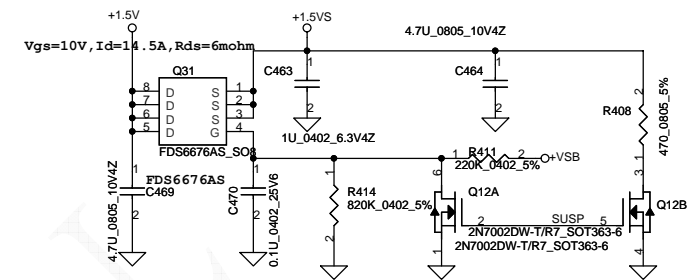
+3VALW TO +3VS



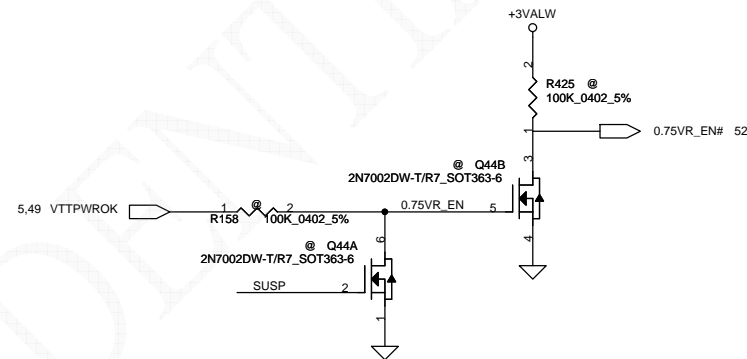
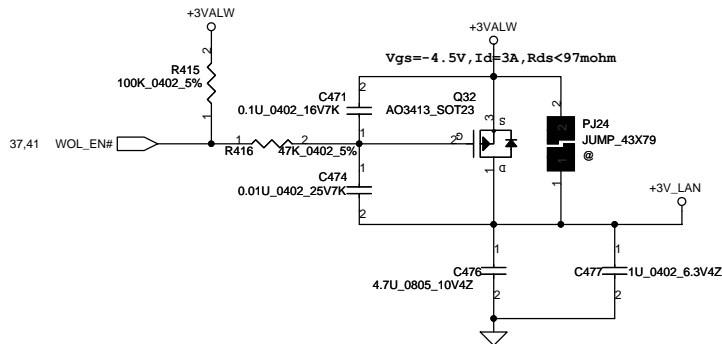
+5VALW TO +5VS



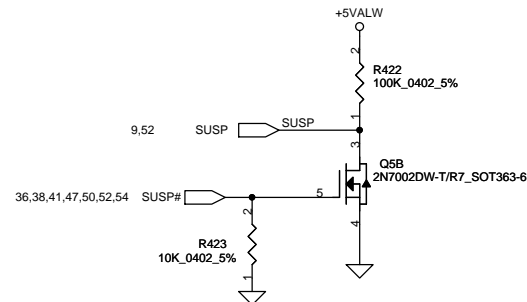
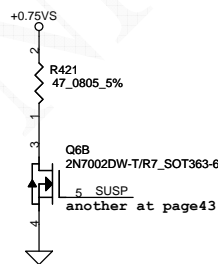
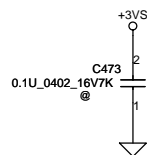
+1.5V to +1.5VS



+3VALW TO +3V_LAN

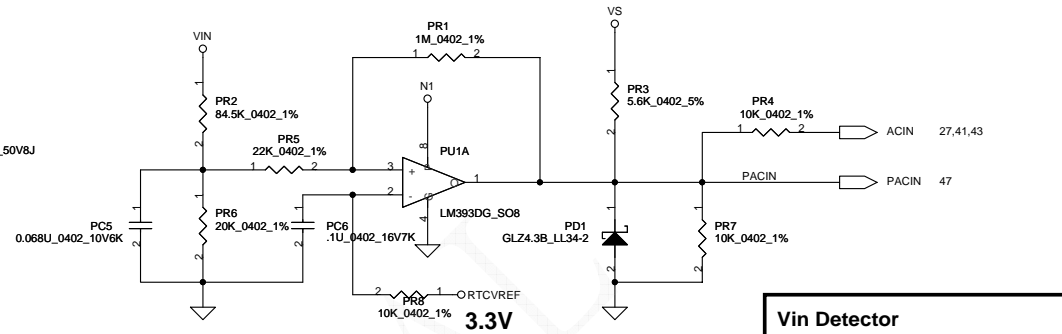
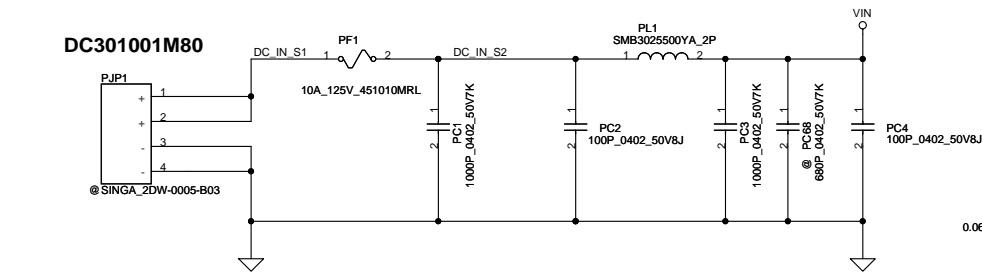


Reserve for EMI request

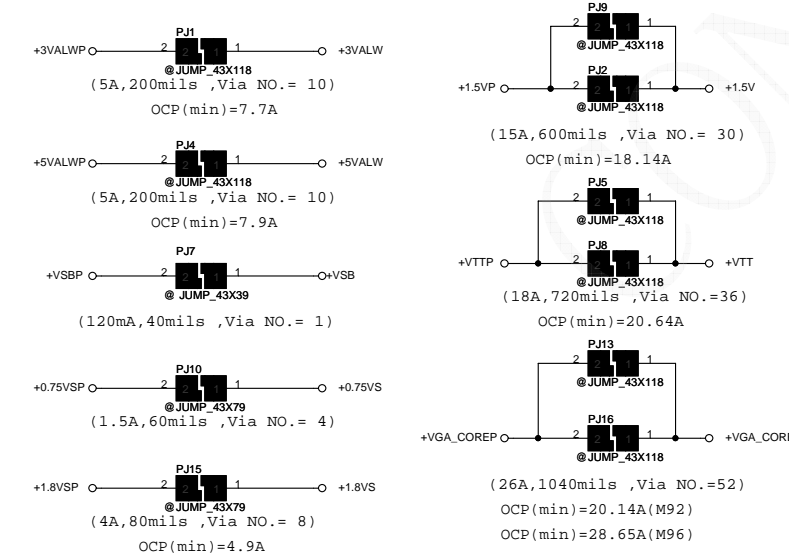
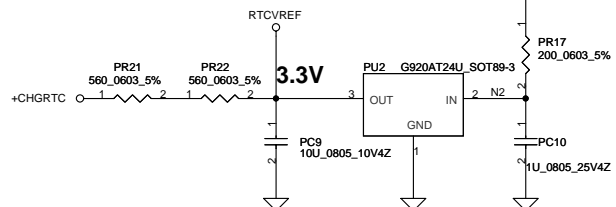
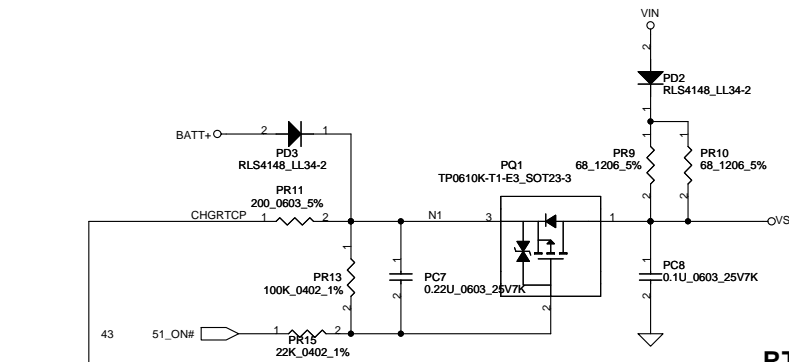


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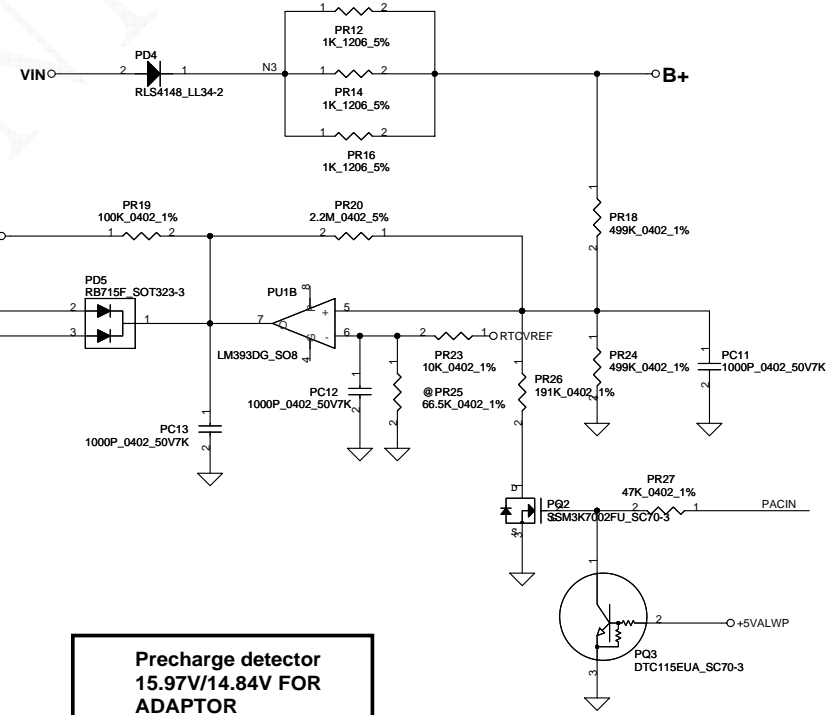
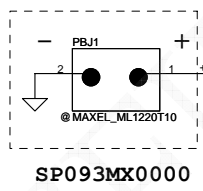
DC301001M80



Vin Detector
 High 18.384 17.901 17.430
 Low 17.728 17.257 16.976



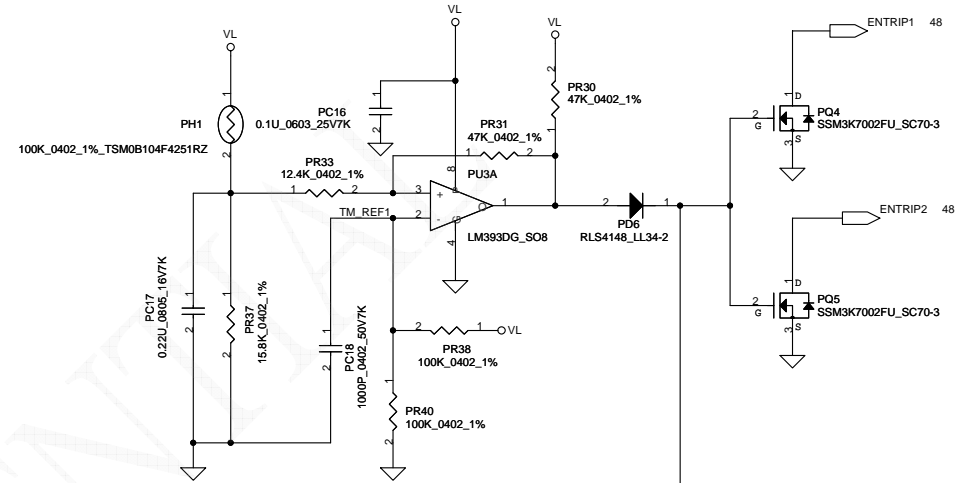
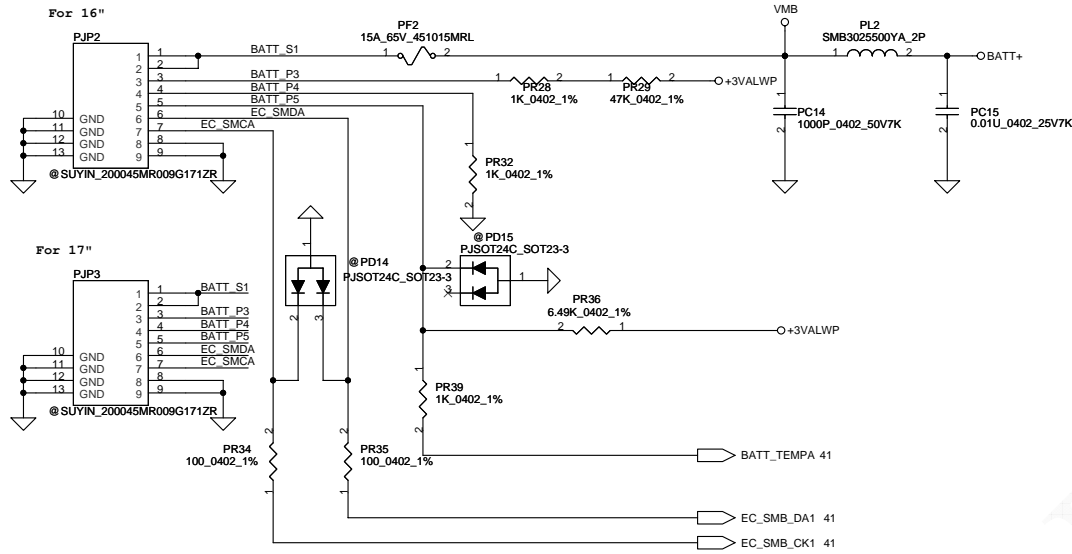
RTC Battery



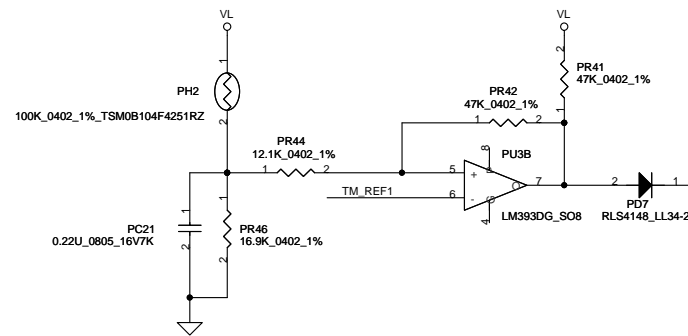
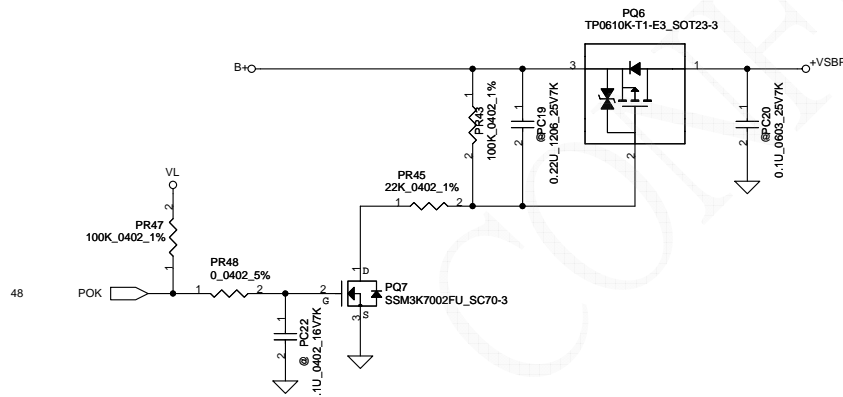
Precharge detector
 15.97V/14.84V FOR ADAPTOR

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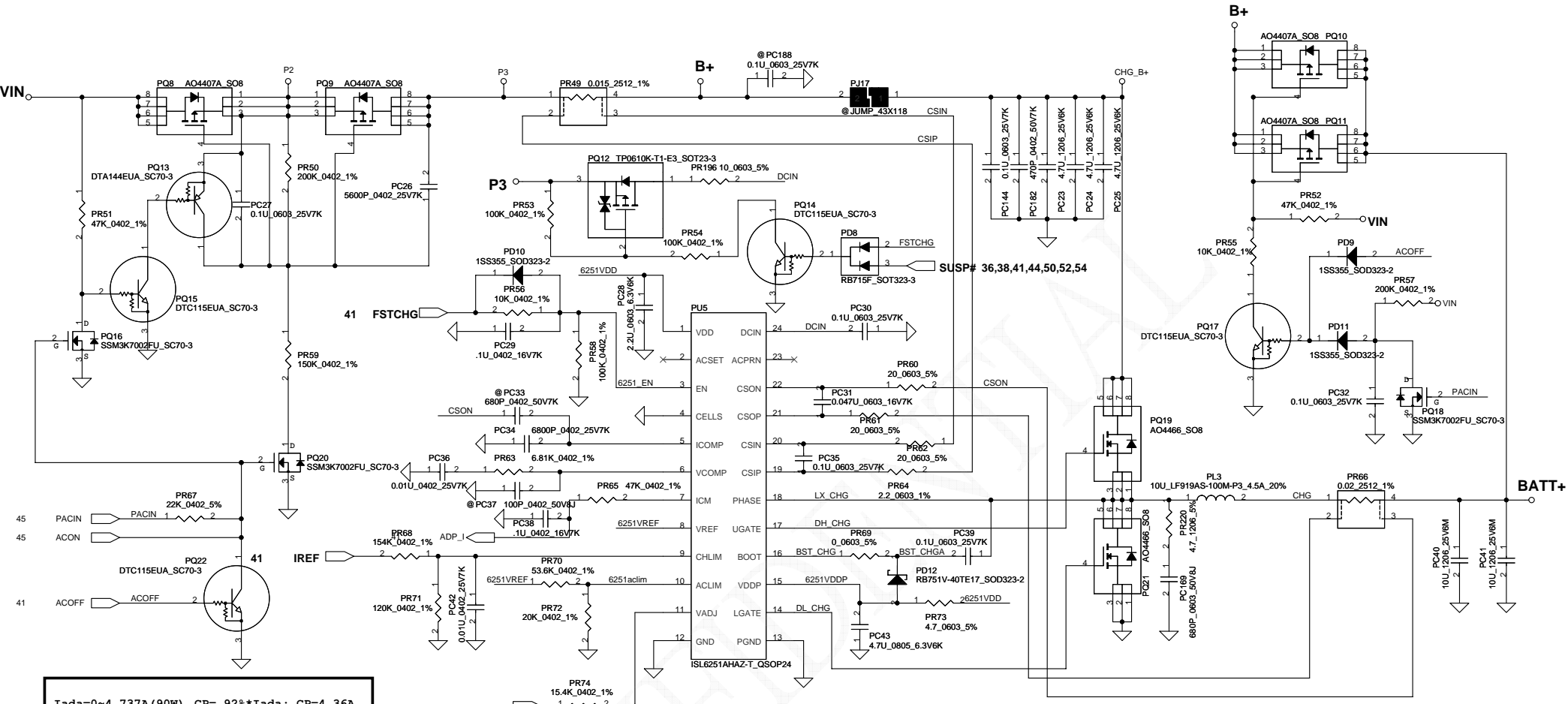
PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 90 degree C
 Recovery at 55 degree C



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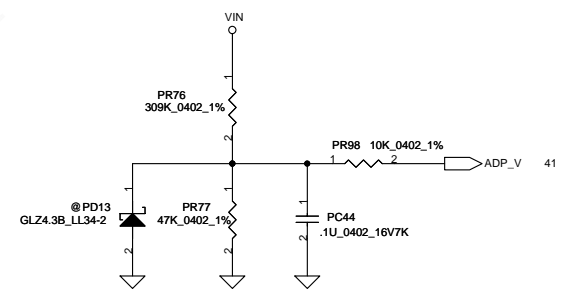
$I_{ada} = 0 \sim 4.737A (90W)$ $CP = 92\% * I_{ada}$; $CP = 4.36A$
 $I_{ada} = 0 \sim 3.42A (65W)$ $CP = 92\% * I_{ada}$; $CP = 3.147A$

CP mode
 $V_{ac1im} = 0.736V (90W)$ $PR70 = 53.6k$ $PR49 = 0.015$
 $V_{ac1im} = 1.08V (65W)$ $PR70 = 75k$ $PR49 = 0.02$

$CC = 0.25A \sim 3A$
 $I_{REF} = 1.016 * I_{charge}$
 $I_{REF} = 0.254V \sim 3.048V$
 V_{CHLIM} need over 95mV

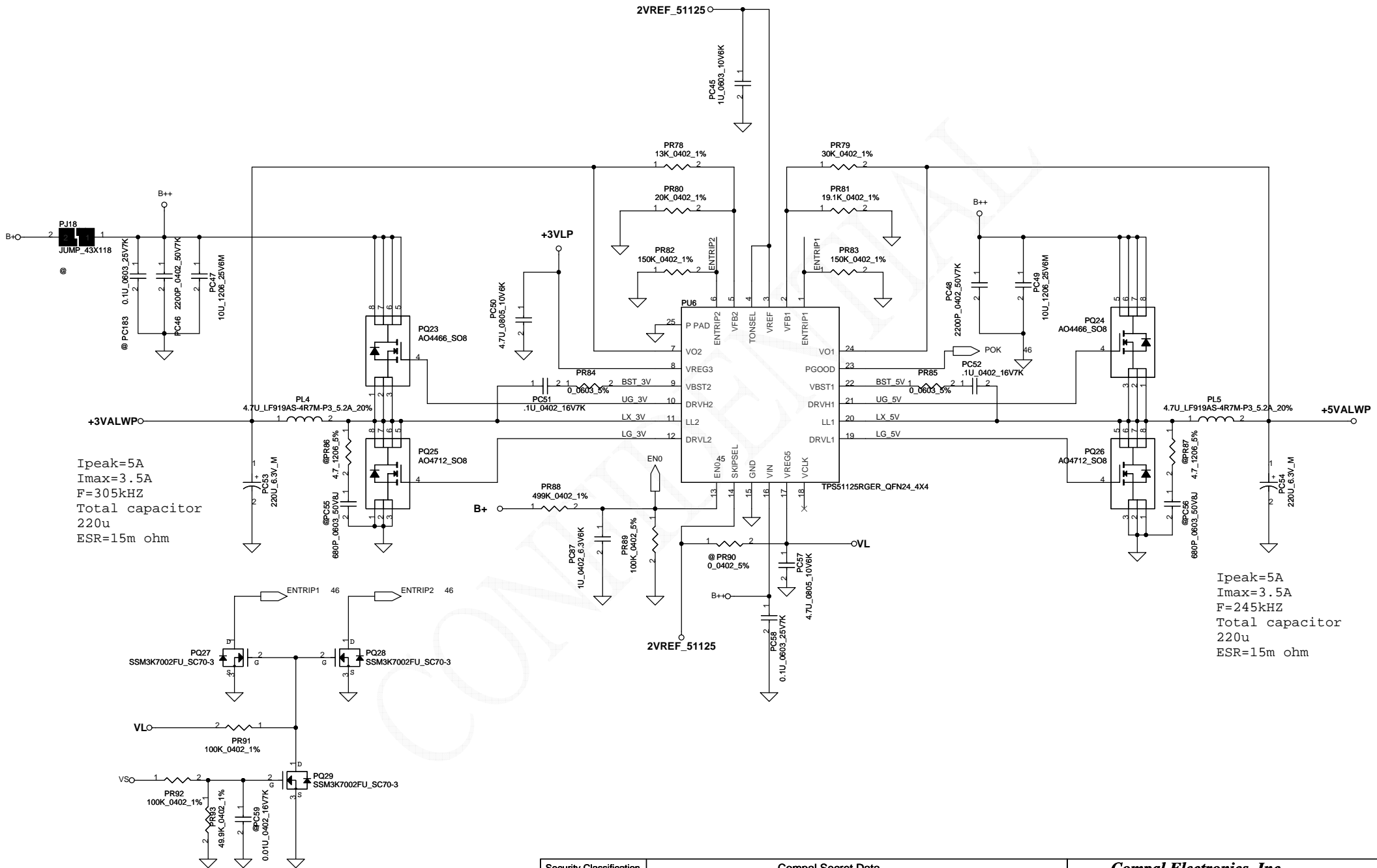
$CHGVADJ = (V_{cell} - 4) / 0.10627$	
V_{cell}	$CHGVADJ$
4V	0V
4.2V	1.882V
4.35V	3.2935V

CELLS	VDD	GND	Float
CELL number	4	3	2



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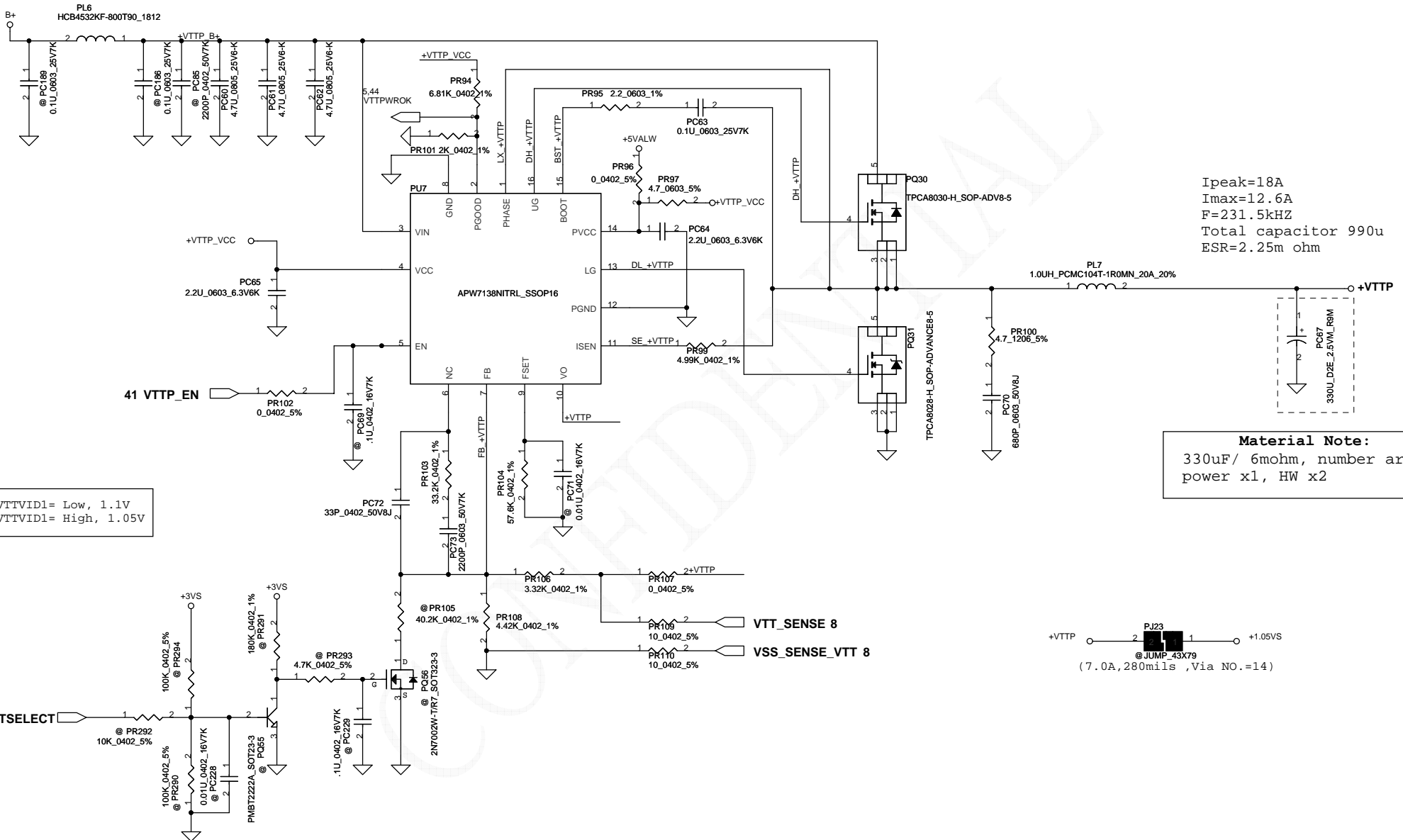
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Ipeak=5A
 Imax=3.5A
 F=305kHz
 Total capacitor
 220u
 ESR=15m ohm

Ipeak=5A
 Imax=3.5A
 F=245kHz
 Total capacitor
 220u
 ESR=15m ohm

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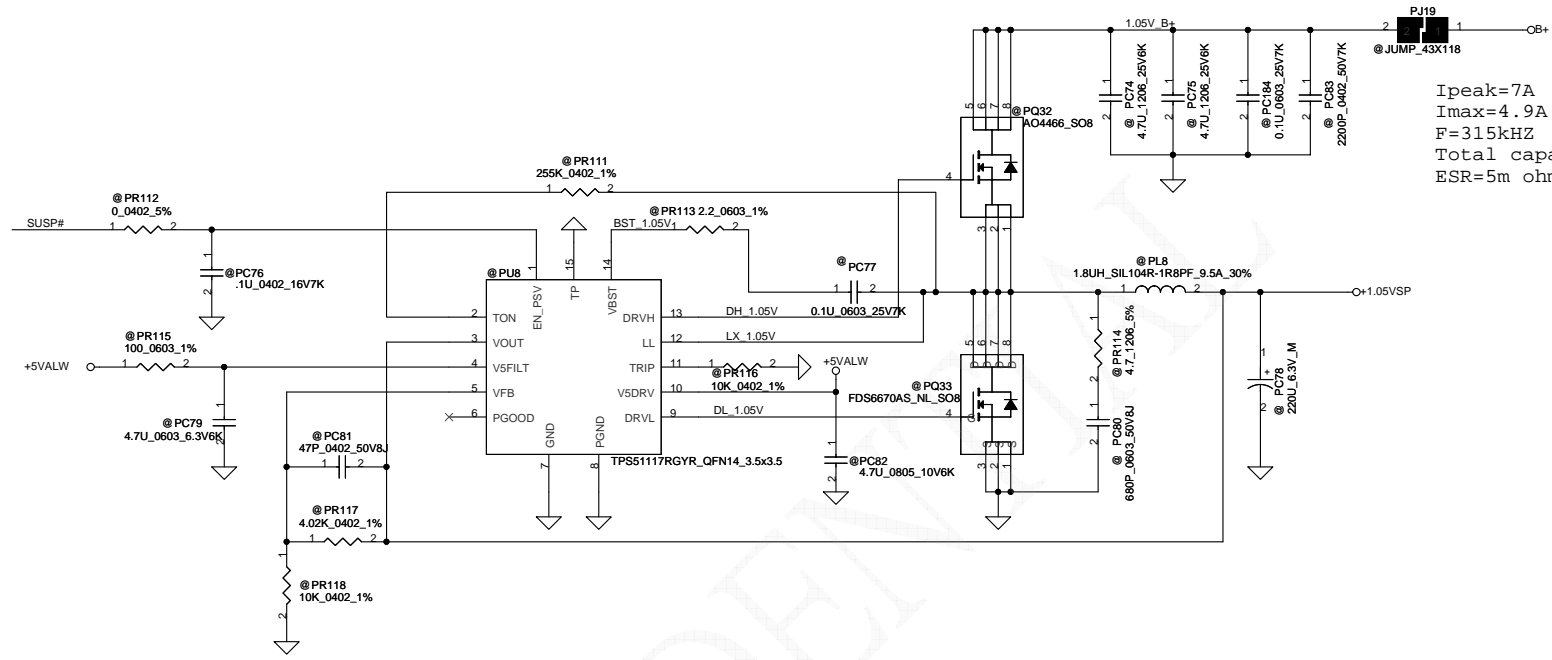
H_VTTVID1= Low, 1.1V
H_VTTVID1= High, 1.05V

I_{peak}=18A
I_{max}=12.6A
F=231.5kHz
Total capacitor 990u
ESR=2.25m ohm

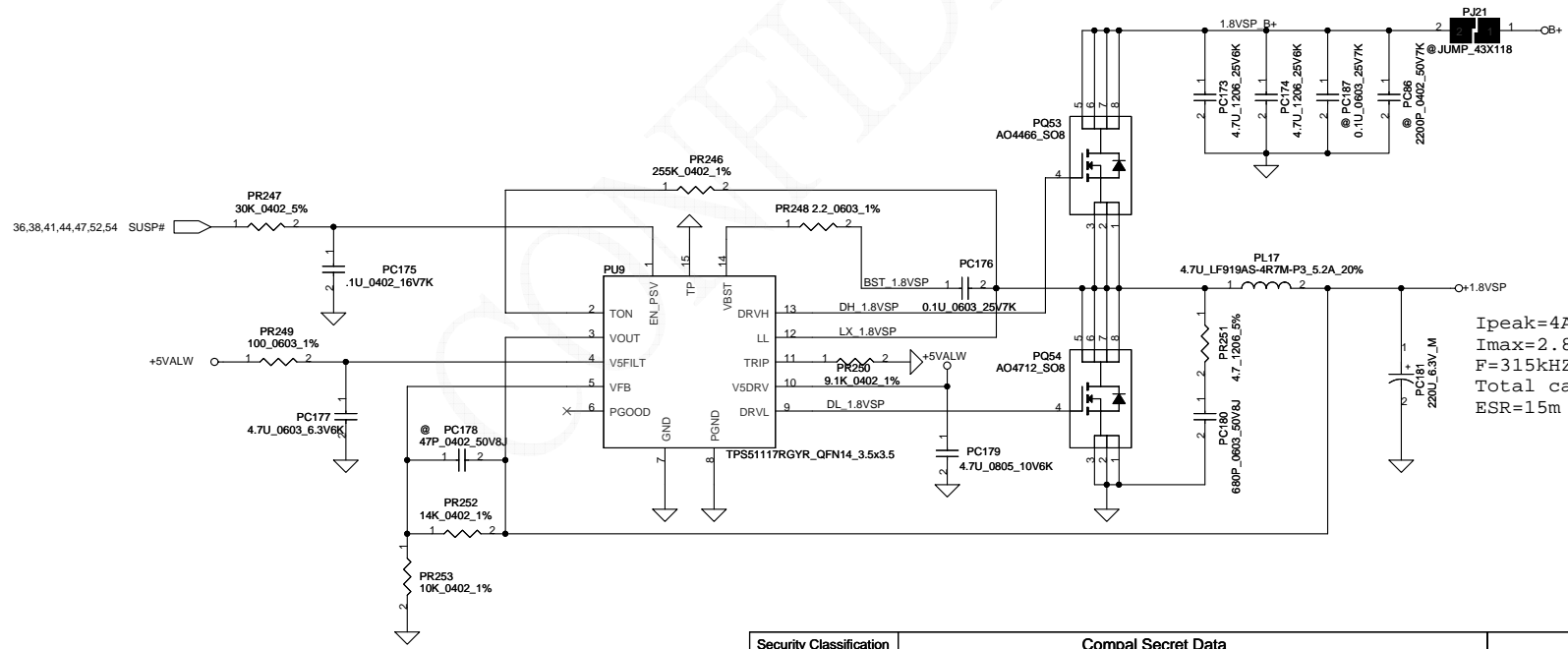
Material Note:
330uF/ 6mohm, number are 3,
power x1, HW x2

+VTTTP — PJ23 — +1.05VS
@ JUMP_43X79
(7.0A, 280mils, Via NO.=14)

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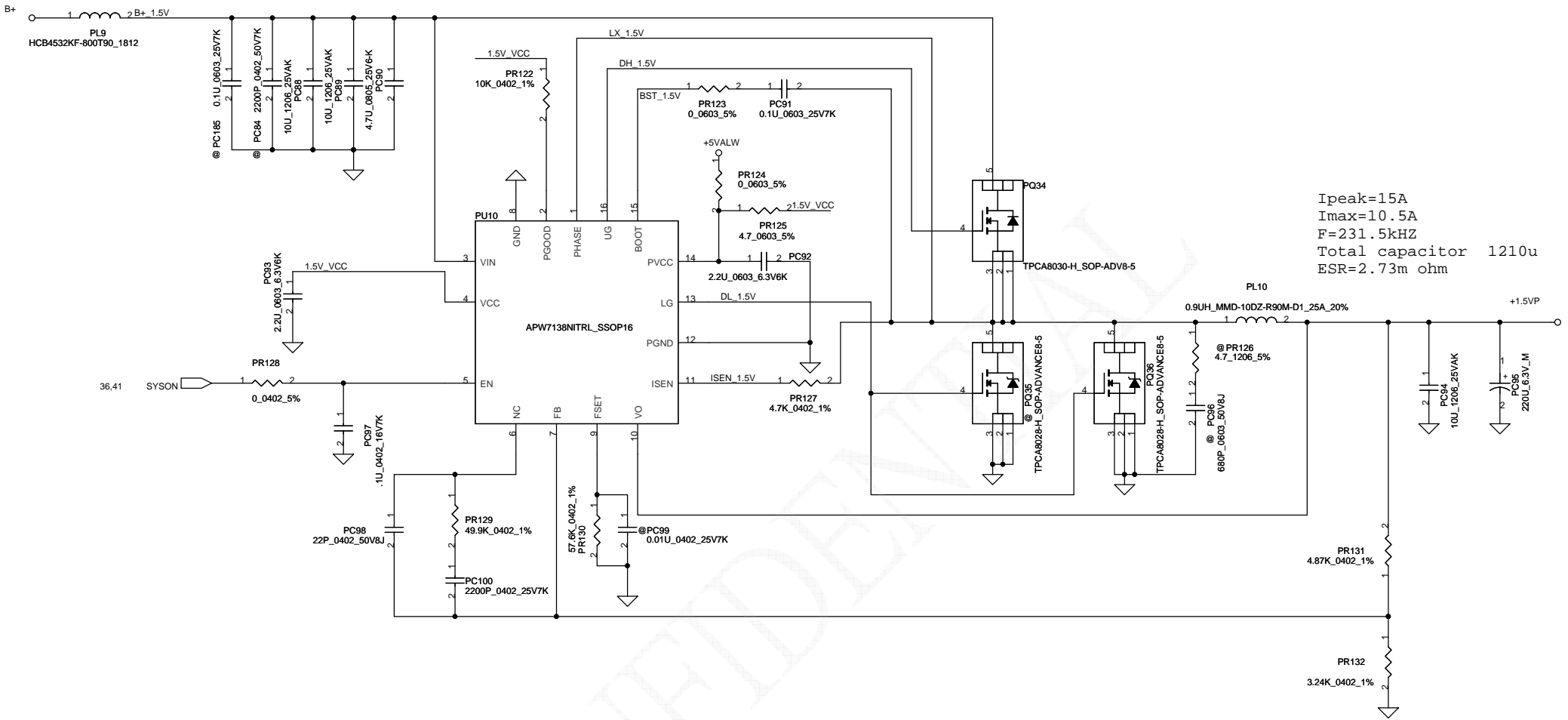


I_{peak}=7A
 I_{max}=4.9A
 F=315kHz
 Total capacitor 660u
 ESR=5m ohm



I_{peak}=4A
 I_{max}=2.8A
 F=315kHz
 Total capacitor 220u
 ESR=15m ohm

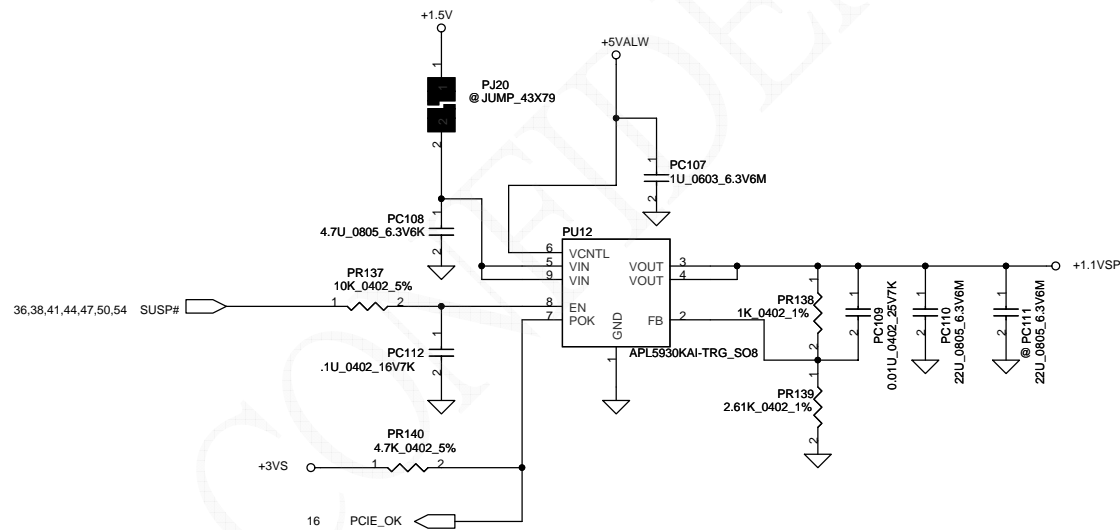
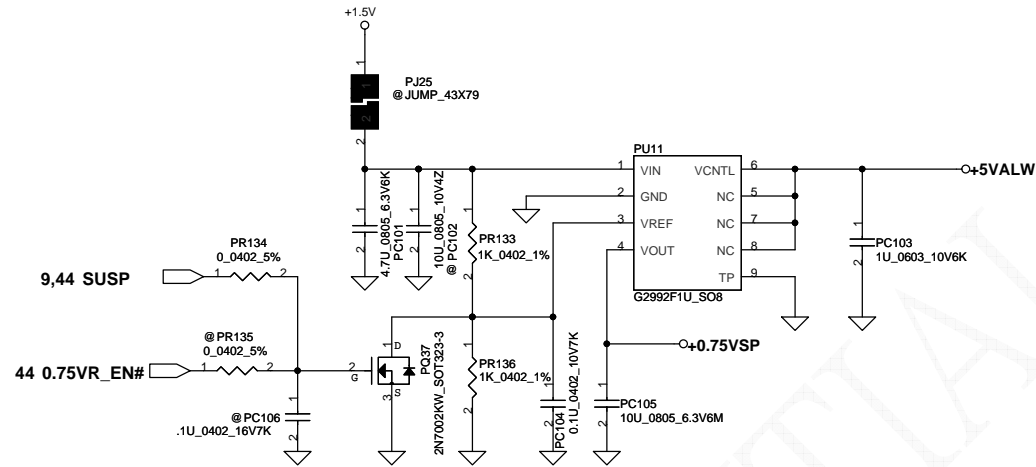
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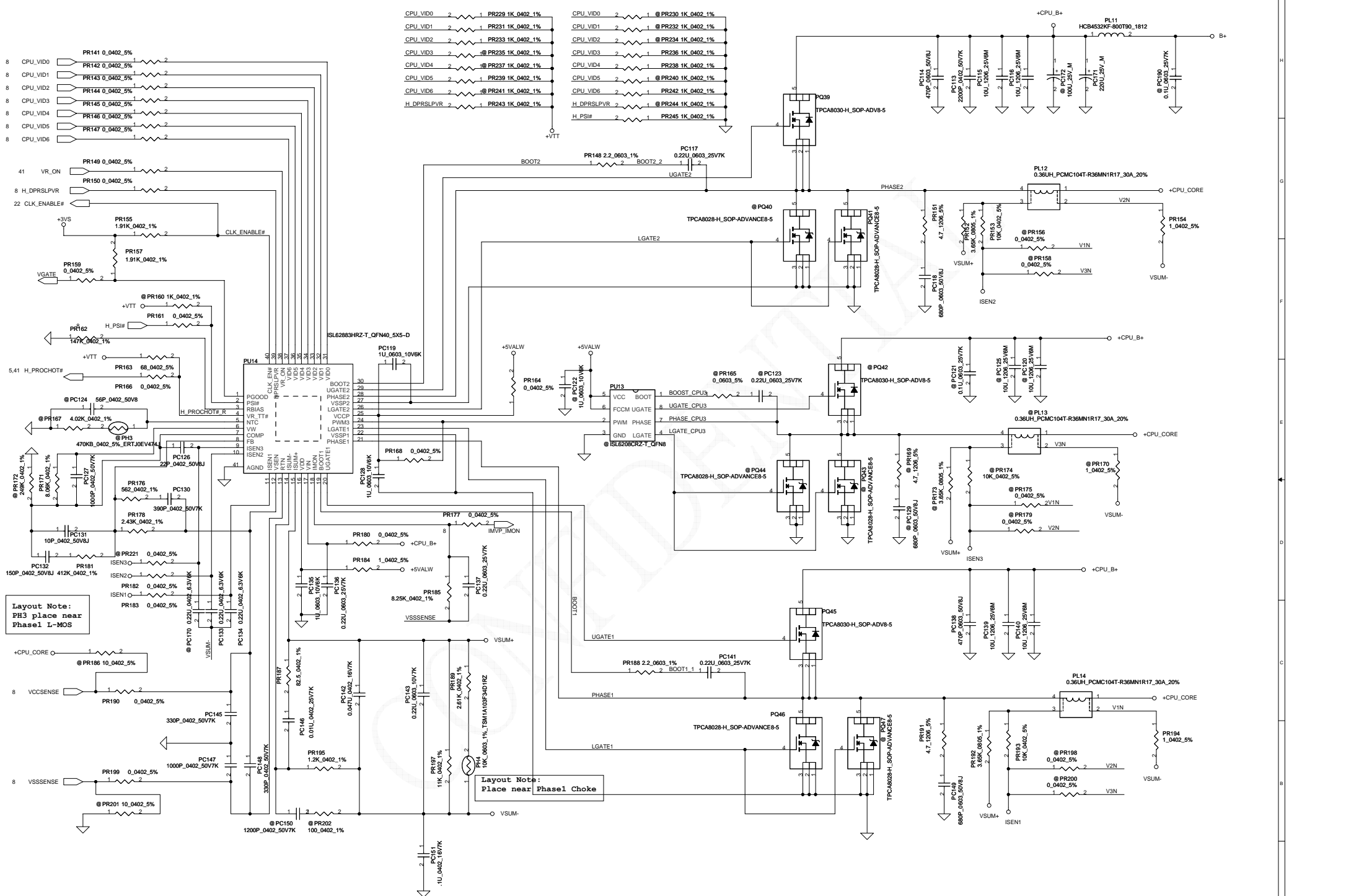
$I_{peak}=15A$
 $I_{max}=10.5A$
 $F=231.5kHz$
 Total capacitor 1210u
 $ESR=2.73m\ ohm$

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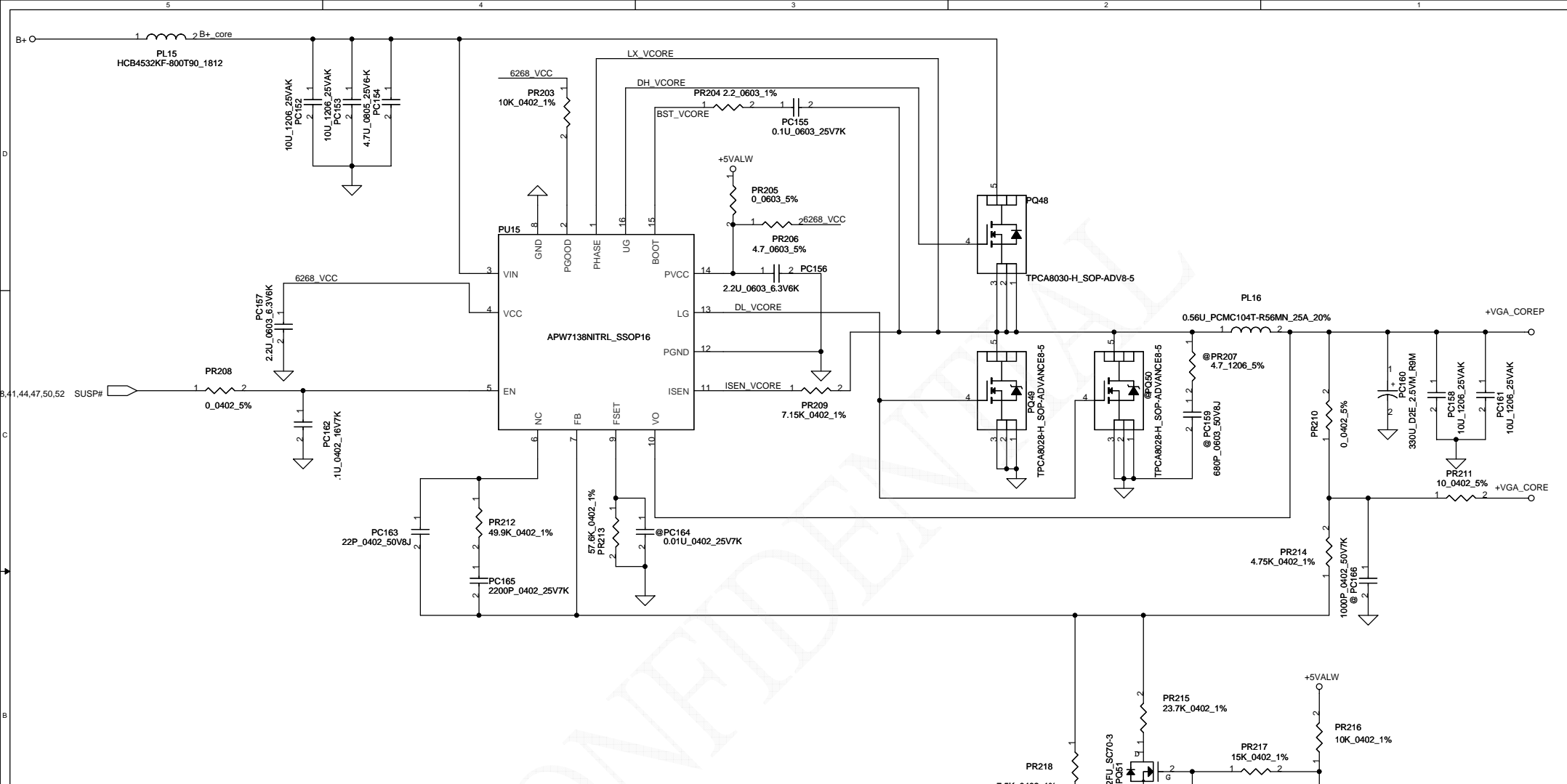
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Layout Note:
PH3 place near
Phase L-MOS

Layout Note:
Place near
Phase Choke

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$VFB(0.6) = V_{out} * R_{bottom} / (R_{top} + R_{bottom})$

$FSW = 1 / (75E-12 * 57.6K) = 231.48KHz$

	M96	M92
VGA_PWSELECT	Core Voltage Level	Core Voltage Level
High	0.98 V	0.98 V
Low	1.1 V	1.2 V
resistor setting	PR214 = 4.75K PR218 = 7.5K PR215 = 23.7K	PR214 = 4.75K PR218 = 7.5K PR215 = 13K

M96	M92
Imax=18.23A Ipeak=26.05A IoCP=28.65A	Imax=12.81A Ipeak=18.30A IoCP=20.14A
PR209=7.15K PQ50=unpop	PR209=5.36K PQ50=unpop

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PIR (Product Improve Record)

NSWAA LA-5322P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
3/25		31, 32	DEL L14, C302, L15, C312, L16, C314, C315, L19, C339, C340	DG1.5: these pins have internal VRM

NSWAA LA-5322P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
6/29		11	Add R92, R93	To support M1 mode
6/29		27	Change R324 from 10K to 330K	To solve ACIN LED issue
7/02		30	Change BT_PWR# from GPIO0 to GPIO34, add VGA_HDMI_HPD on GPIO0.	For common design with NSKAA
7/02		35	DEL JCAM (R431, R432, C403, R371, R373, R374, R375, L20)	CAM cable combine with LVDS
7/02		22	DEL R387	Remove +5VALW power to camera
7/02		40	DEL YC1, CC10, CC12	Remove 12MHz crystal to cardreader
7/02		40	DEL RC2	Remove +3VALW to cardreader
7/02		15-18	Add LV31, CV253, CV236, CV270, LV35, LV36, CV303, CV304, CV305, CV306, CV307, CV308, LV34, RV157, RV156, RV24, RV56, RV59, RV60, RV126, RV127	Reserve for support Park/Madsion
7/03		22	Add R120, R401	Reserve +1.5VS to clk gen for low power clk gen test
7/03		22, 30	Add R154	Reserve LVDS_SEL on PCH GPIO45
7/03		30, 41	Connect PCH GPIO33 to EC pin 103 as PWRME_CTRL Change 3G_OFF# from EC pin 103 to pin 107	To reflash ME BIOS
7/17		43	Add R50 on SATA_LED#	Reserve for cost down plan
7/17		29	DEL R277, D12, Connect USB_OC#3_D to USB_OC#3	
7/17		27, 41, 43	DEL R384, D14. Add R331	Modify ACIN circuit
7/17		22, 43	Change Q7, Q34 to Dual Q35	For cost down
7/20		5, 9, 11, 30, 44	Add Q41, R19, R123, R22, D54, U10, R33, R52, Q33, R424, R417, C179, Q46, C472, R417, R418, C205, C186, C185, C180, PJ30, PJ31, R80, Q44, R425, R158, Q39, Q40, R94, R95, R122, R121 Add RST_GATE on PCH GPIO46	Reserve S3 power reduction circuit
7/27		41	Add R5	To solve SYSON glitch issue
7/27		30, 41	Connect PCH GPIO49 to EC pin25 as THM_ALT#	Reserve for test
7/27		8, 9, 11, 16, 20	Add C144, C159, C218, C216, C217, CV309, CV310, CV311, CV312	For cost down
7/30		9, 44	Add C160, C256, C257, C258, C473, C475	For EMI request
7/30		25, 42	Change U13 to 8MB, U22 to 1MB	For SW and EC request

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PIR (Product Improve Record)

**NSWAA LA-5322P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 0.4**

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
8/19		14,22	Add R159,R160 for VGA BKL control	Reserve for deep green test
9/1			Change +3VL to +3VALW, DEL PJ12	.
9/1		25,42	Change EC ROM to 256KB and PCH ROM to 4MB	For PVT test
9/1		34	Add L52,R72,R85,L53,R73,R87,L54,R77,R88	For EMI request
9/9		37	Connect WOL_EN# to LAN IC	For PVT test

**NSWAA LA-5322P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.4 TO 1.0**

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
9/30		25	Change C287,C290 from 18p to 15p	To fine tune RTC timing
9/30		5	Change R22 from 10k to 1k	Modify S3 circuit
10/28		5	Reserve C301,C384,C389	Reserve for S3 power saving circuit

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NO DATE PAGE MODIFICATION LIST PURPOSE

EVT	P47-PWR_CHARGER	Change PR65 100 to 47k	For CPU throttling setting (2009/05/20)
EVT	P48-PWR_3VALWP/5VALWP	Change PR81 19.6k to 19.1k	modify +5VALWP voltage to 5.14V (2009/05/20)
EVT	P49-PWR_+1.1V_VTTP	Add PR290 100K, PR291 180K, PR292 10K, PR293 4.7K, PR294 100K, PC228 0.01U, PC229 0.1U, PQ55,PQ56	Add switching circuit for H_VTTSELECT function (2009/05/20)
EVT	P49-PWR_+1.1V_VTTP	Change PR94 10K to 3.4K Add PR101 1K	Set VTTPWROK voltage level to 1.1V (2009/05/20)
EVT	P53-PWR_CPU_CORE	Remove PR186,PR201 10 Ohm	Modify CPU_CORE circuit (2009/05/27)
EVT	P46-PWR_BATTERY CONN / OTP	Change PH1,PH2 0603 sizt to 0402 size	For cost down (2009/05/27)
EVT	P50-PWR_1.05VSP/1.8VSP	Change PR115,PR249 4220hm to 100 Ohm Change PC79,PC177 1U to 4.7U	avoid 2nd source RT8209B can no power on (2009/06/05)
EVT	P52-PWR_0.75VSP/1.1VSP	Change PUI2 APL5913 to APL5930	For cost down (2009/06/05)
EVT	P45-PWR_DCIN/DECTOR	Remove DC301000F00	Remove DC IN JACK((2009/06/05))
EVT	P54-PWR_VGA_COREP	Change PR210 10 Ohm to 0 Ohm Change PR211 0 Ohm to 10 Ohm	Change VGA_CORE sense from HW terminal to PWR (2009/06/05)
EVT	P54-PWR_VGA_COREP	Change PL16 0.36U to 0.56U	Change CPU_CORE CHOKE to 0.56U(2009/06/05)
EVT	P50-PWR_1.05VSP/1.8VSP	Change PR116 14.7k to 10k Change PR250 15.4k to 9.1k	Set 1.05V OCP to 8.54A(2009/06/05) Set 1.8V OCP to 4.93A(2009/06/05)
EVT	P51-PWR_1.5VP	Change PR127 7.15k to 2.1k	Set 1.5V OCP to 17A(2009/06/05)
EVT	P49-PWR_+VTTP	Change PR99 5.9k to 2.43k	Change VTT OCP to 19.7A(2009/06/05)
DVT	P50-PWR_1.05VSP/1.8VSP	Add PC175 0.1U Change PR247 0 to 30k	For power sequence(2009/07/07)
DVT	P49-PWR_+VTTP	Change PR99 2.43k to 4.99k	Set OCP(2009/07/07)
DVT	P51-PWR_1.5VP	Change PR127 2.1k to 4.7k	Set OCP(2009/07/07)
DVT	P45-PWR_CPU_CORE	PC133, PC134 SE083224Z80 to SE124224K80	PC133, PC134 tolerance Y5V to X5R(2009/0/07)
DVT	P50-PWR_1.05VSP/1.8VSP	Change PC79, PC177 SE00000MAN0 to SE107475K80	Change part number(2009/07/07)
DVT	P41-PWR_3VALWP/5VALWP	Add PC87 1U_0402_6.3V6K	Avoid pre-charge can not finish(2009/07/07)
DVT	P41-PWR_3VALWP/5VALWP	Add PC45 0.22U to 1U	Prevent +3VALW/+5VALW can't boot up (2009/07/07)
DVT	P45-PWR_CPU_CORE	Change PR229-PR245 and PR160 10k to 1k	Change VID, PSI# and DPRSLPVR select resistor from 10k to 1k (2009/07/17)
DVT	P45-PWR_CPU_CORE	Change PR157 10k to 1.91k	Change PGOOD pull high resistor 10k to 1.91k(2009/07/17)
DVT	P45-PWR_CPU_CORE	Remove PH3, PC124, PR167 Change PC133, PC134, PC170 pin 2 from GND to VSUM- Change PR152, PR192 0402 size to 0805 size	Modify circuit for CPU_CORE(2009/07/17)
DVT	P39-PWR_BATTERY CONN / OTP	Change +3VLP to +3VALWP	Remove +3VLP power rail (2009/07/17)

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Issued Date	2009/01/23	Deciphered Date	2010/01/23		
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
DVT		P47-PWR_CHARGER	Reserve PC188 0.1U	Reserve for EMI solution (2009/07/23)
DVT		P49-PWR_VTTP	Reserve PC189 0.1U	Reserve for EMI solution (2009/07/23)
DVT		P49-PWR_VTTP	Change PR95 0 ohm to 2.2 ohm	Add boot strap resistor (2009/07/23)
DVT		P49-PWR_VTTP	Add PR100 4.7 ohm, PC70 680P	Add snubber (2009/07/23)
DVT		P49-PWR_VTTP	Change PR94 3.4k to 1.5k, PR101 1k to 3k	For HW solution(S3 power reduction) (2009/07/23)
DVT		P49-PWR_VTTP	Add P023	For power test(2009/07/23)
DVT		P52-PWR_0.75VSP/1.1VSP	Add 0.75VSP_EN control signal	For HW solution(S3 power reduction) (2009/07/23)
DVT		P53-PWR_CPU_CORE	Add PR151, PR191 4.7 ohm, PC118, PC149 680P	Add snubber (2009/07/23)
DVT		P53-PWR_CPU_CORE	Change PR148, PR188 0 ohm to 2.2 ohm	Add boot strap resistor (2009/07/23)
DVT		P53-PWR_CPU_CORE	Add PC190 0.1U	Reserve for EMI solution (2009/07/23)
DVT		P45-PWR_CPU_CORE	Remove PQ40, PQ47	For design change(2009/07/28)
DVT		P52-PWR_0.75VSP/1.1VSP	Change PC101 10U to 4.7U	For design change(2009/07/28)
DVT		P52-PWR_0.75VSP/1.1VSP	Change PC106 SE076104KM8 to SE076104K80	Change to COMPAL PN(2009/08/03)
DVT		P45-PWR_CPU_CORE	Change PC151 SE076104KM8 to SE076104K80	Change to COMPAL PN(2009/08/03)
DVT			Change PC53, PC54, PC78, PC95, PC181 SF22001M200 to SF000001H00	SF22001M200 is forbids to use (2009/08/03)
DVT		P45-PWR_CPU_CORE	Change PR195 1.1k to 1.2k	Change Ri for load line (2009/08/03)
DVT		P45-PWR_CPU_CORE	Remove PR202 100 ohm, PC150 1200P	Modify CPU_CORE circuit (2009/08/03)
DVT		P49-PWR_VTTP	Change PU7 ISL6268 to APW7138	For cost down (2009/08/03)
			Remove PC71 0.01U	For APW7138 solution (2009/08/03)
DVT		P51-PWR_1.5VP	Change PU10 ISL6268 to APW7138	For cost down (2009/08/03)
			Remove PC99 0.01U	For APW7138 solution (2009/08/03)
DVT		P54-PWR_VGA_COREP	Change PU15 ISL6268 to APW7138	For cost down (2009/08/03)
			Remove PC164 0.01U	For APW7138 solution (2009/08/03)
DVT		P51-PWR_1.5VP	Change PL9 SM01000DJ00 to SM010018210	Use same PN bead (2009/08/03)
DVT		P53-PWR_CPU_CORE	Change PL11 SM010020720 to SM010018210	Use same PN bead (2009/08/03)
DVT		P54-PWR_VGA_COREP	Change PL15 SM01000DJ00 to SM010018210	Use same PN bead (2009/08/03)
DVT		P39-PWR_BATTERY CONN / OTP	Change PR33 13.7k to 12.4k	Set OTP (2009/08/03)
			Change PR37 15.4k to 15.8k	
DVT		P47-PWR_CHARGER	Add PR220 4.7 ohm, PC169 680P	Add charger snubber(RF solution) (2009/08/03)
			Add PC144 0.1U, PC182 470P	Add charger snubber(RF solution) (2009/08/03)
DVT		P45-PWR_CPU_CORE	Add PC113 2200P, PC114 470P, PC138 470P	RF solution (2009/08/03)
PVT		P42-PWR_VTTP	Change PL7 0.47U to 1U	Design change (2009/09/04)
PVT		P42-PWR_VTTP	Remove PC66, PC68 10U	Design change (2009/09/04)
PVT		P47-PWR_CHARGER	Change PR70 8.25k to 53.6k, PR72 26.7k to 20k	Set 90W CP (2009/09/04)
PVT		P45-PWR_DCIN/DECTOR	Add PC68 680P	For EMI solution (2009/09/14)
PVT		P46-PWR_BATTERY CONN / OTP	Add PD14, PD15	Reserve for EMI(ESD diode) (2009/09/14)
PVT		P42-PWR_VTTP	Remove PR290, PR291, PR292, PR293, PR105, PC228, PC229, PQ55, PQ56	Remove VTTP voltage switch circuit(arrandale only) (2009/09/14)
PVT		P47-PWR_CHARGER	Change PR64 PN SD013220B80 to SD014220B80	Use same PN (2009/09/14)
PVT		P49-PWR_VTTP	Change PR95 PN SD013220B80 to SD014220B80	Use same PN (2009/09/14)
PVT		P50-PWR_1.05VSP/1.8VSP	Change PR113, PR248 0 ohm to 2.2 ohm	Add boot trap resistor (2009/09/14)
			Add PR114, PR251 4.7 ohm, PC80, PC180 680P	Add snubber (2009/09/14)
PVT		P45-PWR_CPU_CORE	Change PR148, PR188 PN SD013220B80 to SD014220B80	Use same PN (2009/09/14)
PVT		P54-PWR_VGA_COREP	Change PR204 PN SD013220B80 to SD014220B80	Use same PN (2009/09/14)
PVT		P50-PWR_1.05VSP/1.8VSP	Change PR117 8.25k to 4.02k	Avoid FB trace noise (2009/09/18)
			Change PR118, PR253 20.5k to 10k	
			Change PR252 28.7k to 14k	
PREMP		P45-PWR_DCIN/DECTOR	Change PC7 SE041224K80 to SE000005Z80	Change CAP size from 1206 to 0603 (2009/10/09)
PREMP		P46-PWR_BATTERY CONN / OTP	Change PR44 13.7k to 12.1k	Modify OTP setting (2009/10/09)
PREMP		P44-PWR_CPU_CORE	Change PL12, PL14 SH000005680 to SH12036BM00	Use 5% tolerance DCR choke (2009/10/09)
PREMP		P51-PWR_1.5VP	Change PR131 4.75k to 4.87k	Adjust voltage divided resistor (2009/10/27)
PREMP		P49-PWR_VTTP	Change PR94 1.5k to 39.2k	Adjust VTTPWROK voltage 3.3V to 1.05V (2009/10/27)
			Change PR101 3k to 10.5k	
PREMP		P50-PWR_1.05VSP/1.8VSP	Remove 1.05V component	Cost down (2009/11/3)
MP		P49-PWR_VTTP	Change PR94 39.2k to 6.81k	Modify resistor for VTTPWROK voltage (2009/11/26)
			PR101 10.5k to 2k	

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Issued Date	2008/10/23	Deciphered Date		
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