QFKAA

Yosemite 10F

LA-8392P REV 1.0 Schematic

Intel Processor(Ivy Bridge / Sandy Bridge)
PCH(Panther Point)
2012-02-06 Rev 1.0

Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

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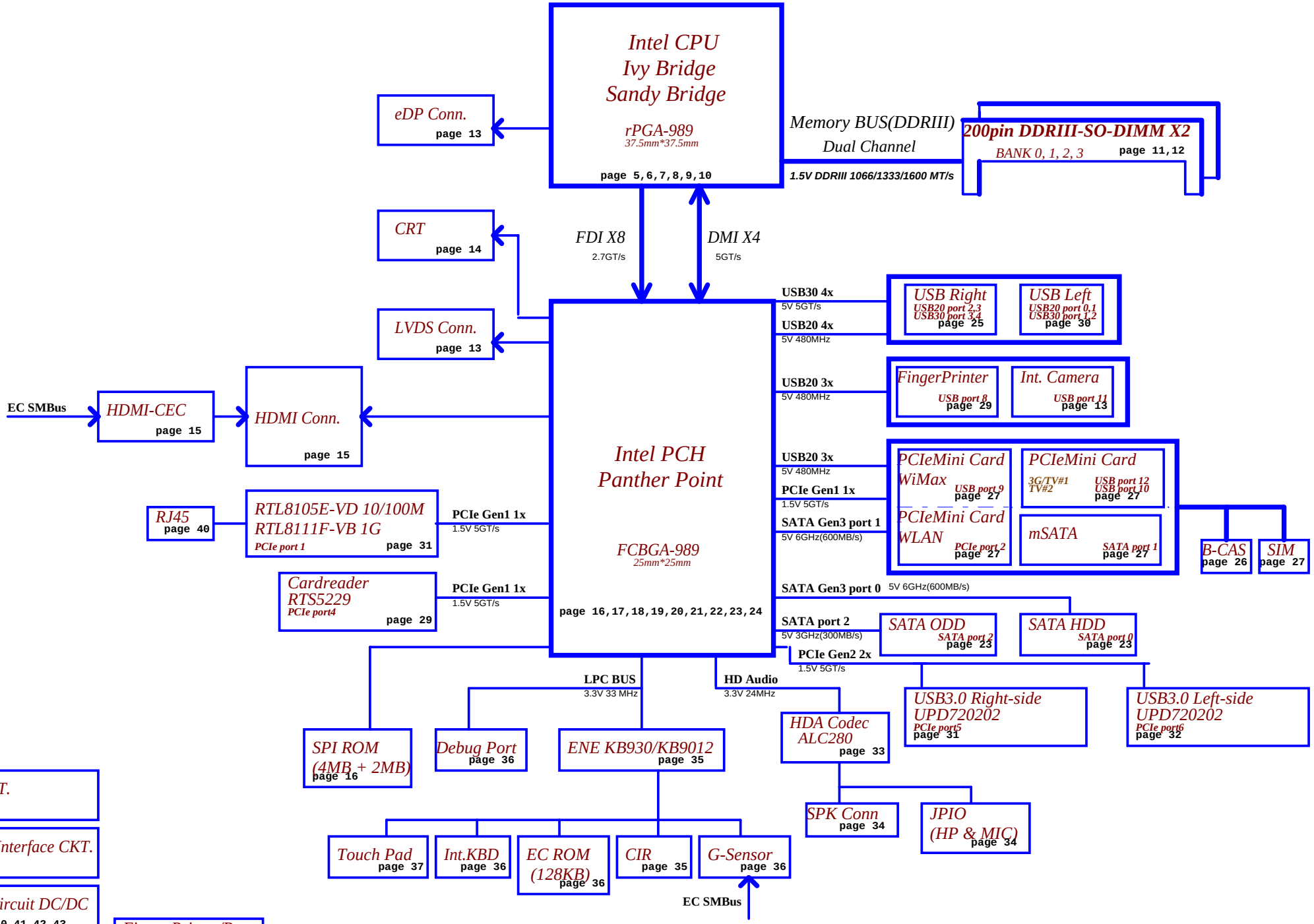
Title: *SCHEMATICS, MB A8392*

Size	Document Number	Rev
B	4019HF	B

Date: Thursday, February 16, 2012 | Sheet 1 of 51



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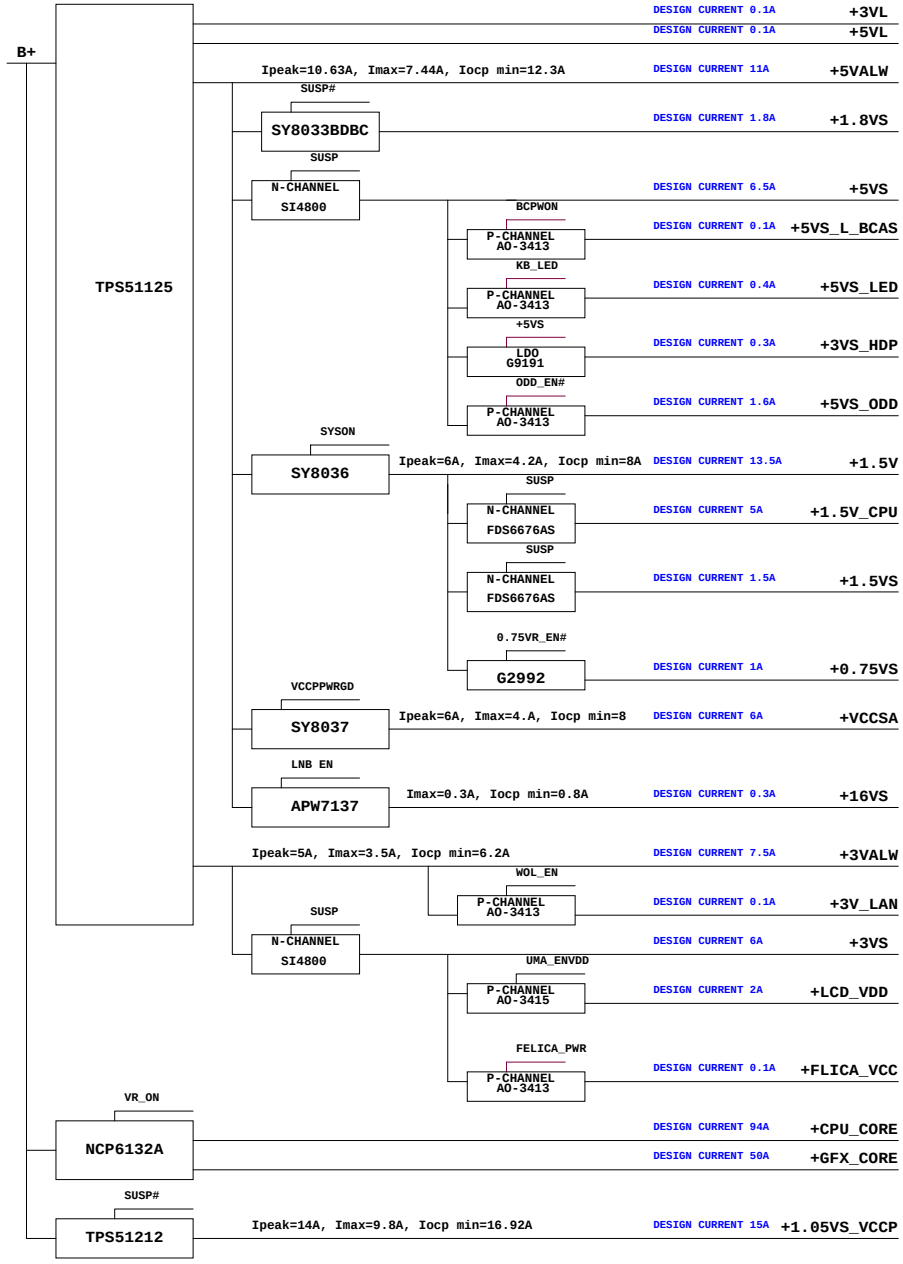
Title	SCHEMATICS, MB A8392		
Size	Document Number 4019HF		Rev B
Date: Thursday, February 16, 2012	Sheet 2 of 51		



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Title: SCHEMATICS, MB A8392

Size: | Document Number: 4019HF | Rev: B

Date: Thursday, February 16, 2012 | Sheet 3 of 51

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

BTO Option Table

Function	HDMI		Internal Display Port		CPU		KB Light
description	HDMI		Internal Display Port		Sandy Bridge	Ivy Bridge	KB Light
explain	HDMI	CEC	LVDS	EDP	Sandy Bridge	Ivy Bridge	KB Light
BTO	HDMI@	CEC@	LVDS@	IEDP@	SANDY@	IVY@	KBL@

Function	MINI PCI-E SLOT					LAN		Fingerprint	CIR
description	SLOT2				SLOT1	LAN		Fingerprint	CIR
explain	3G	TV Tuner	BCAS	mSATA	WIMAX	10/100M	Giga	Fingerprint	CIR
BTO	3G@	TV@	BCAS@	mSATA@	WIMAX@	8105ELDO@	8111FVB@	FP@	CIR@

Function	SPI ROM	Green CLK		G-SENSOR	Sleep&Charge		USB 3.0		Camera & Mic
description	SPI ROM	Green CLK		G-SENSOR	Sleep&Charge		USB 3.0		Camera & Mic
explain	WIN8	Green CLK	NOGCLK	G-SENSOR	14600	14617	Internal	External	Camera & Mic
BTO	WIN8@	271@	NOGCLK@	GSENSOR@	14600@	14617@	IUSB30@	EUSB30@	CAM@

Function	USB Repeater			
description	USB Repeater			
explain	TIUR	PRUR		
BTO	TIUR@	PRUR@		

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b

Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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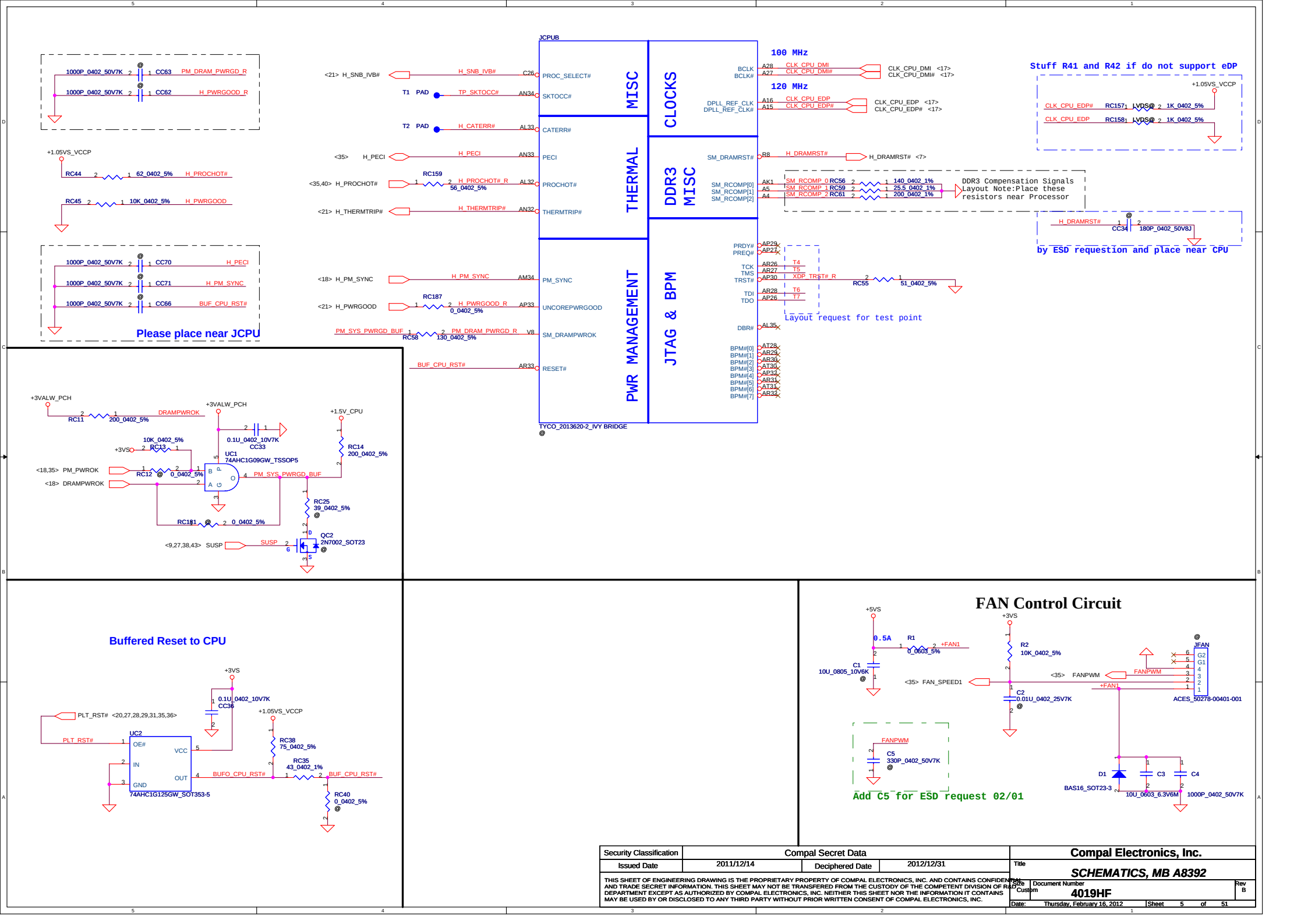
Title: SCHEMATICS, MB A8392

Size: Custom | Document Number: 4019HF | Rev: B

Date: Thursday, February 16, 2012 | Sheet 4 of 51



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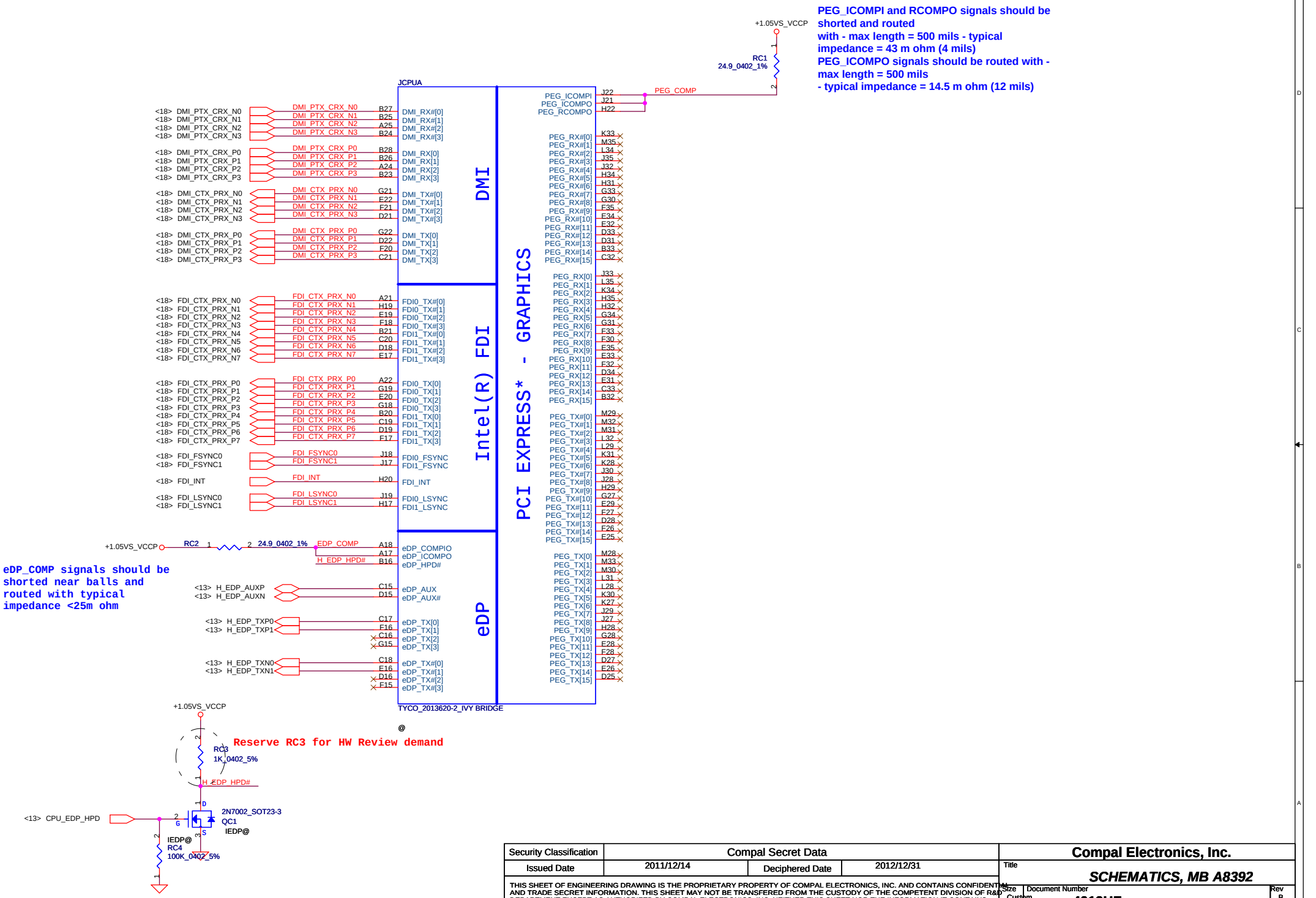
Size: Custom	Document Number: 4019HF		Rev: B
Date: Thursday, February 16, 2012	Sheet 5 of 51		



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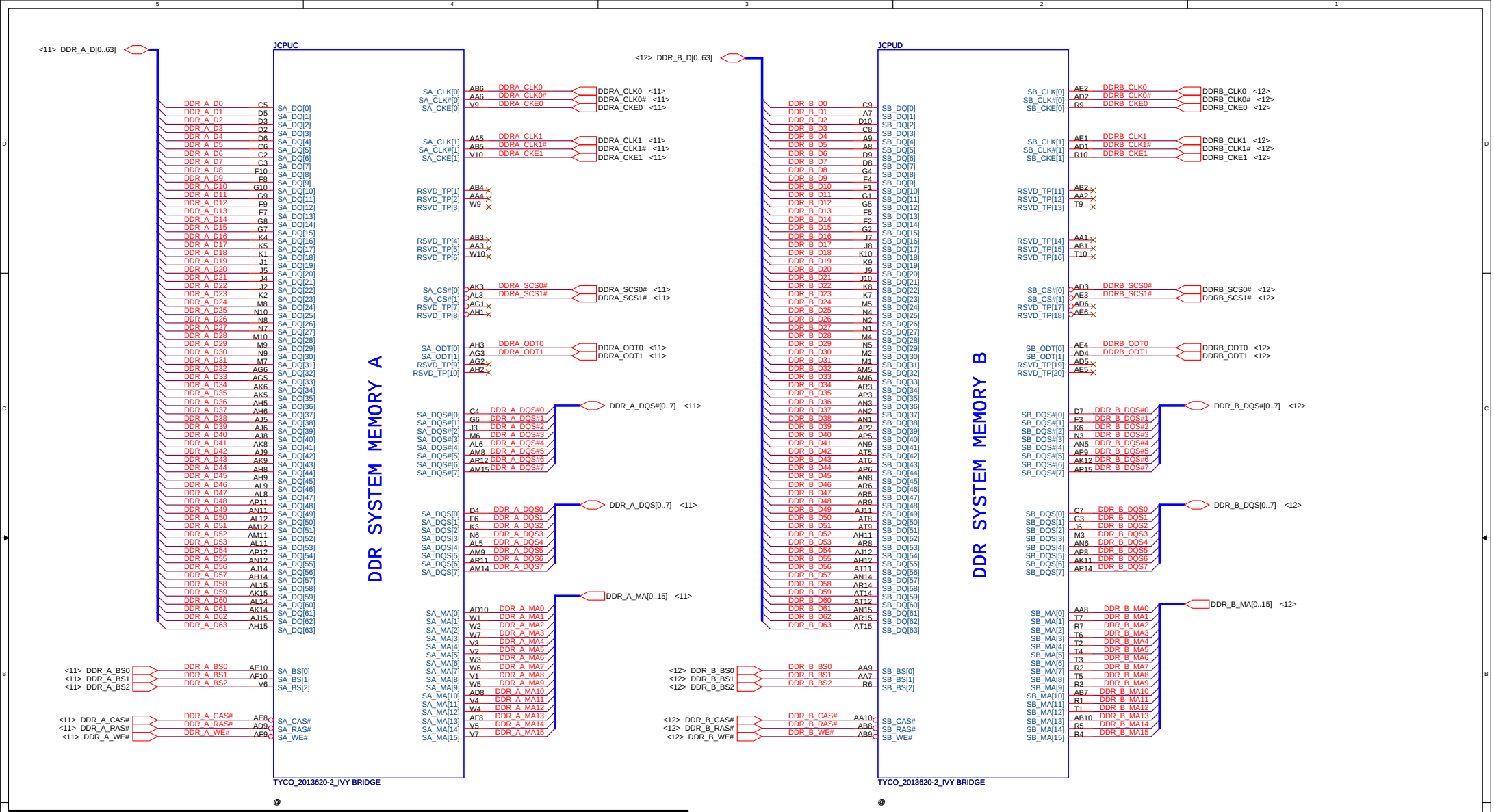
Custom	4019HF	B

Date: Thursday, February 16, 2012 | Sheet 6 of 51



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Compal Electronics, Inc.	
Title	SCHEMATICS, MB A8392
Size: Custom	Document Number: 4019HF
Rev	B
Date: Thursday, February 16, 2012	Sheet 7 of 51

POWER

JCPUF

+CPU_CORE

CORE SUPPLY — 97A

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

PEG AND DDR — 8.5A

+1.05VS_VCCP

VCCIO1	AH13
VCCIO2	AH10
VCCIO3	AG10
VCCIO4	AC10
VCCIO5	Y10
VCCIO6	U10
VCCIO7	P10
VCCIO8	L10
VCCIO9	J14
VCCIO10	J13
VCCIO11	J12
VCCIO12	J11
VCCIO13	H14
VCCIO14	H12
VCCIO15	H11
VCCIO16	G14
VCCIO17	G13
VCCIO18	G12
VCCIO19	F14
VCCIO20	F13
VCCIO21	F12
VCCIO22	F11
VCCIO23	E14
VCCIO24	E12
VCCIO25	E11
VCCIO26	D14
VCCIO27	D13
VCCIO28	D12
VCCIO29	D11
VCCIO30	C14
VCCIO31	C13
VCCIO32	C12
VCCIO33	C11
VCCIO34	B14
VCCIO35	B12
VCCIO36	A14
VCCIO37	A13
VCCIO38	A12
VCCIO39	A11
VCCIO40	J23

SVID

+1.05VS_VCCP

0.1U_0402_10V7K
CC50 @
RC91 130_0402_5%

+1.05VS_VCCP

0.1U_0402_10V7K
CC49 @
RC89 75_0402_5%

VIDALERT#	AJ29	H_CPU_SVIDALRT#	RC90 43_0402_1%	VR_SVID_ALRT# <46>
VIDSCLK	AJ30	H_CPU_SVIDCLK	RC88 0_0402_5%	VR_SVID_CLK <46>
VIDSOUT	AJ28	H_CPU_SVIDDAT	RC92 0_0402_5%	VR_SVID_DAT <46>

Pull high resistor on VR side

SENSE LINES

+CPU_CORE

RC93 100_0402_1%

Close to CPU

VCC_SENSE	AJ35	VCCSENSE_R	RC94 0_0402_5%	VCCSENSE <46>
VSS_SENSE	AJ34	VSSSENSE_R	RC95 0_0402_5%	VSSSENSE <46>

VCCIO_SENSE	B10	VCCIO_SENSE	VCCIO_SENSE <44>
VSS_SENSE_VCCIO	A10		

RC97 100_0402_1%

RC96 10_0402_1%

RC98 10_0402_1%

+1.05VS_VCCP

Close to CPU

@TYCO_2013620-2_IVY BRIDGE

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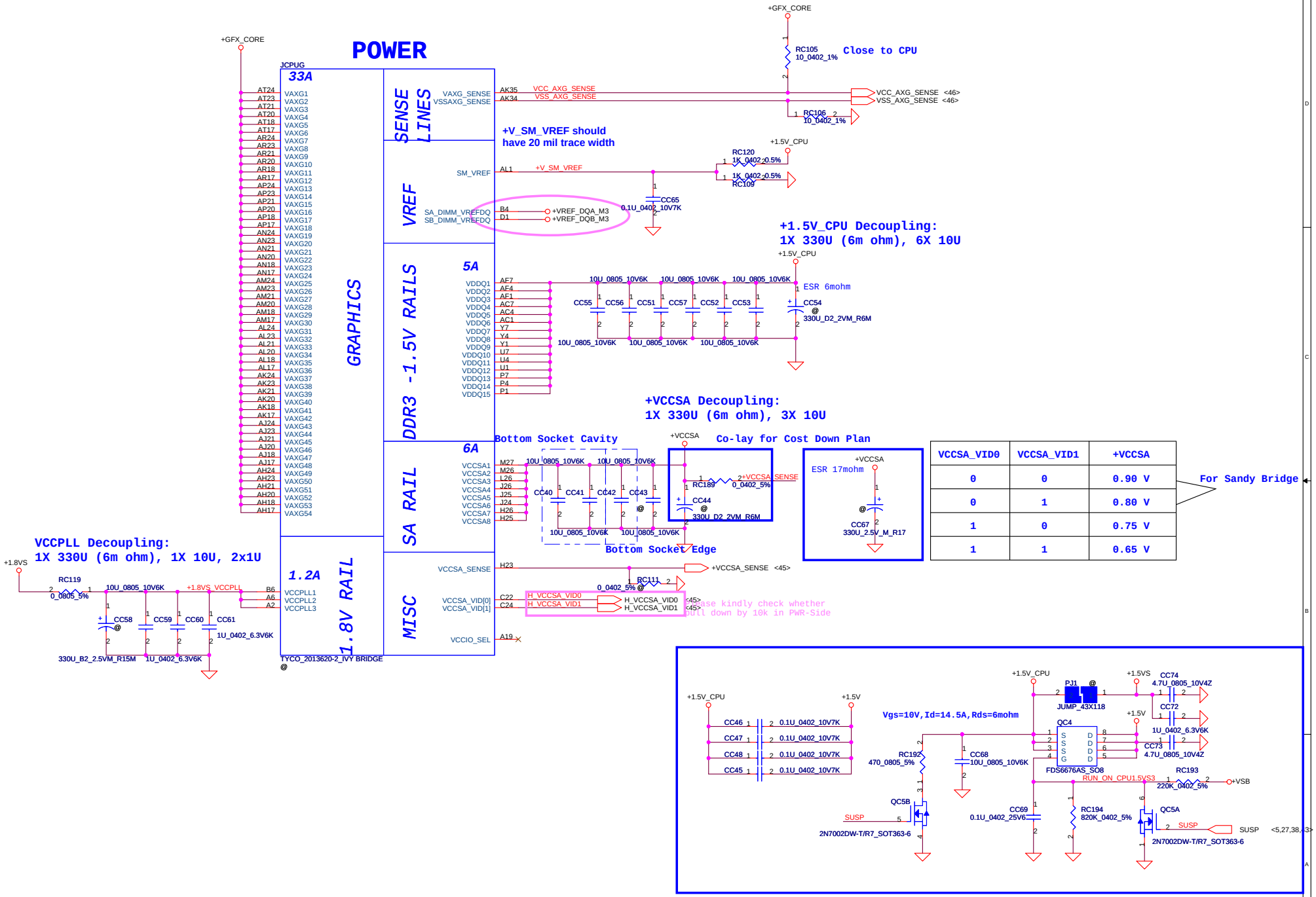
Size: Custom | Document Number: 4019HF | Rev: B

Date: Thursday, February 16, 2012 | Sheet 8 of 51

POWER



VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.75 V
1	1	0.65 V

For Sandy Bridge

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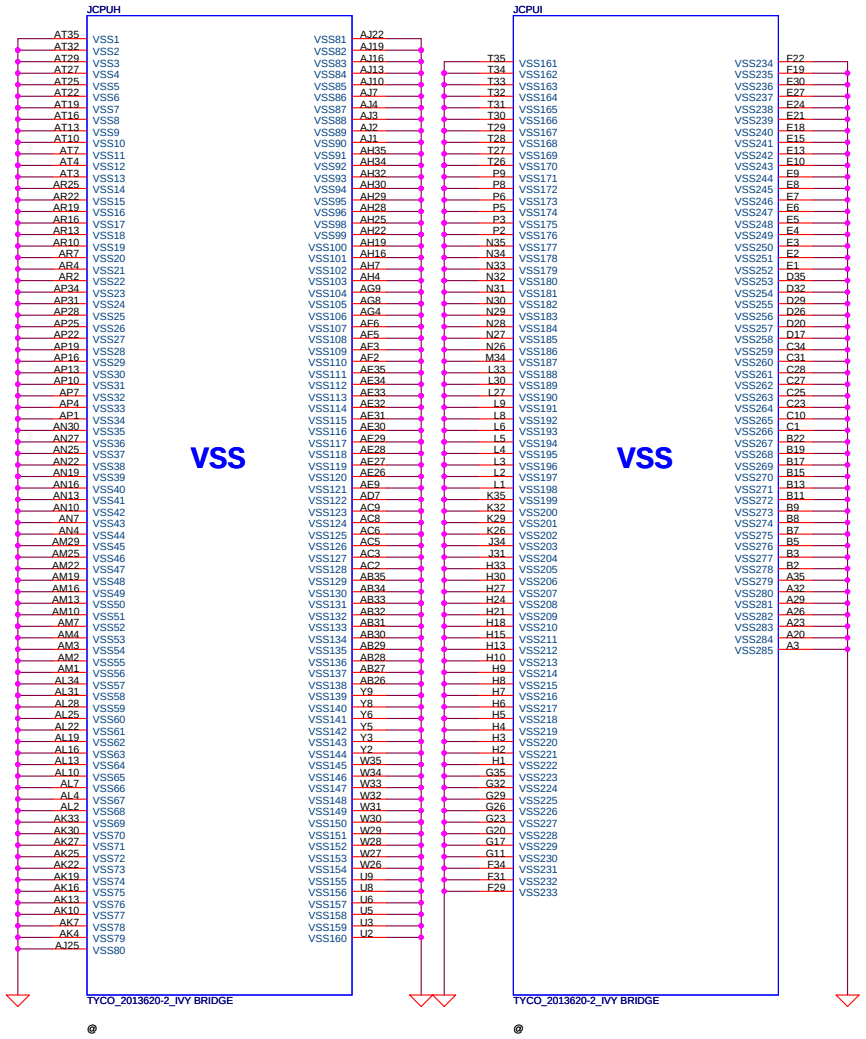
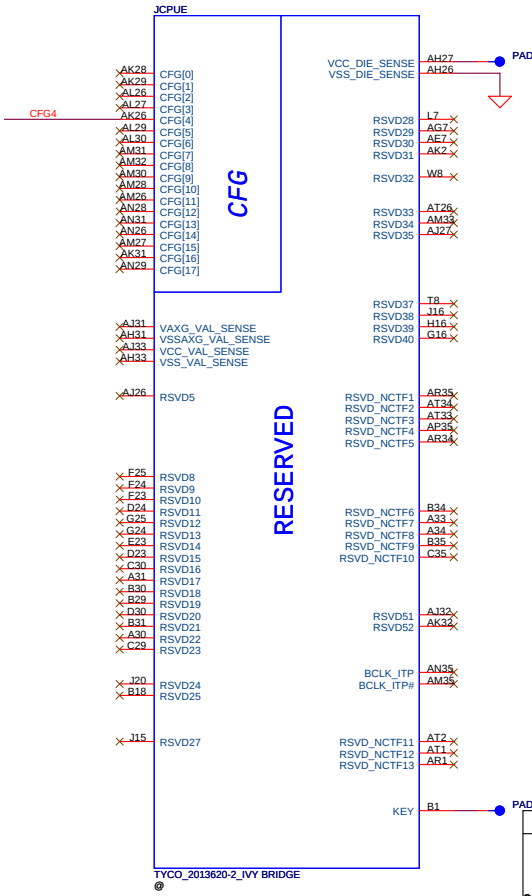
Title	SCHEMATICS, MB A8392
Size: Custom	Document Number: 4019HF
Rev: B	
Date: Thursday, February 16, 2012	Sheet 9 of 51

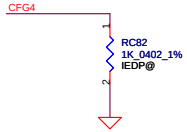
CFG Straps for Processor

(CFG[17:0] internal pull high to VCCIO)





PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Embedded Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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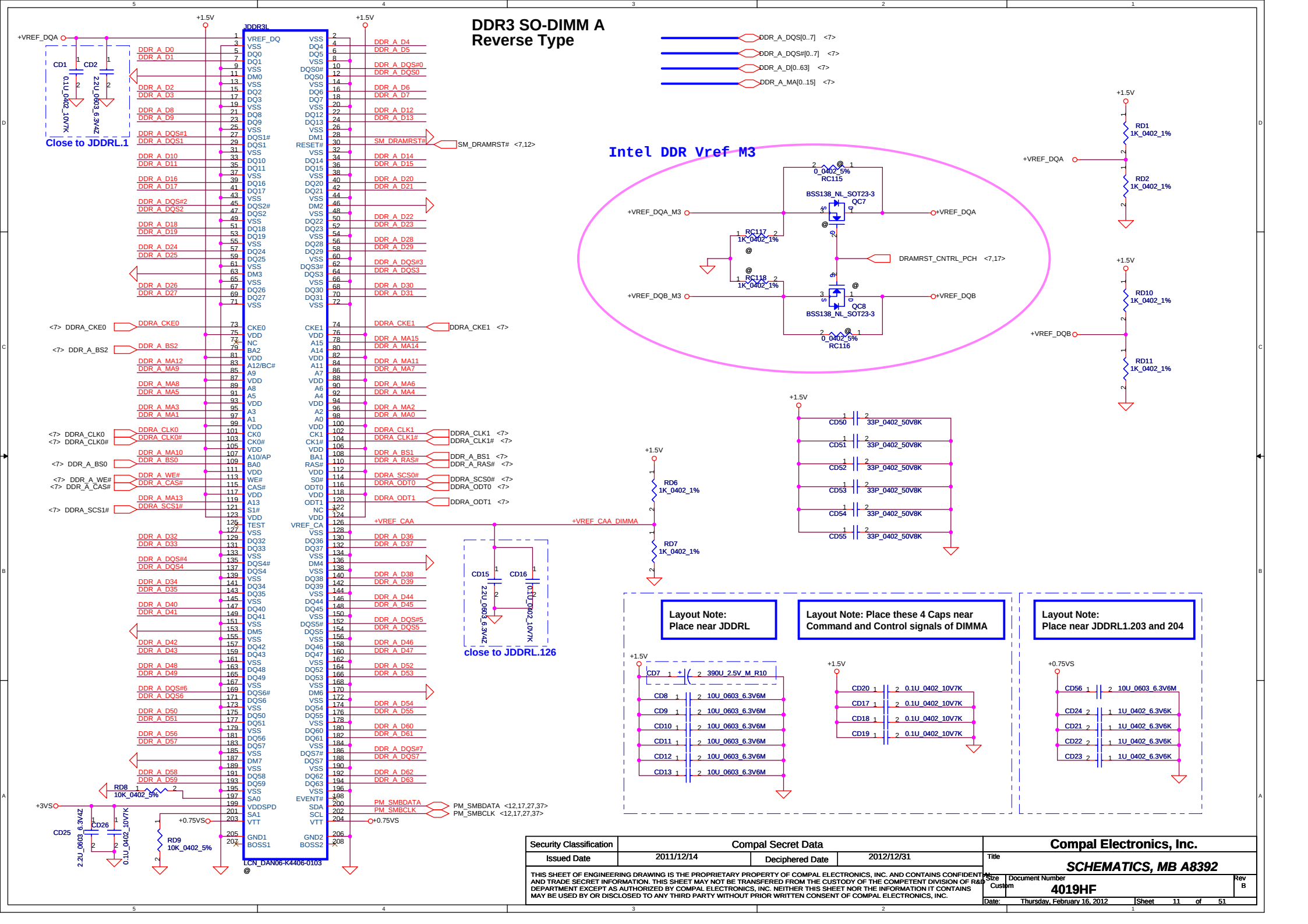
Title: ***SCHEMATICS, MB A8392***

Size	Document Number	Rev
Custom	4019HF	B

Date: Thursday, February 16, 2012 | Sheet 10 of 51

DDR3 SO-DIMM A
Reverse Type



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Title: ***SCHEMATICS, MB A8392***

Size	Document Number	Rev
Custom	4019HF	B

Date: Thursday, February 16, 2012 | Sheet 11 of 51

Reverse Type
DDR3 SO-DIMM B

JDDR3H

DDR_B_DQS#[0..7] <7>
DDR_B_DQS[0..7] <7>
DDR_B_D[0..63] <7>
DDR_B_MA[0..15] <7>

Close to JDDRH.1

Close to JDDRH.126

FOX_AS0A626-UASN-7F_204P

Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

Layout Note:
Place near JDDRH.203 and 204

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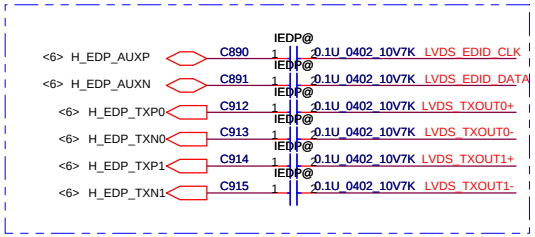
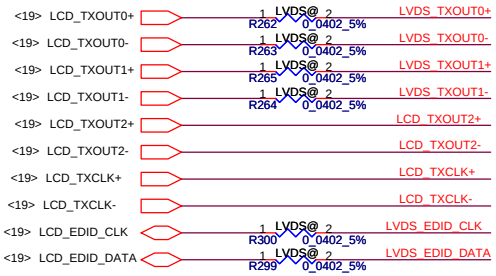
Title: SCHEMATICS, MB A8392

Size: Custom | Document Number: 4019HF | Rev: B

Date: Thursday, February 16, 2012 | Sheet 12 of 51

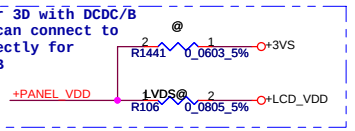
OPT for 2D HD eDP Panel

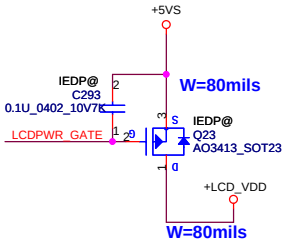




LCD/PANEL BD. Conn.

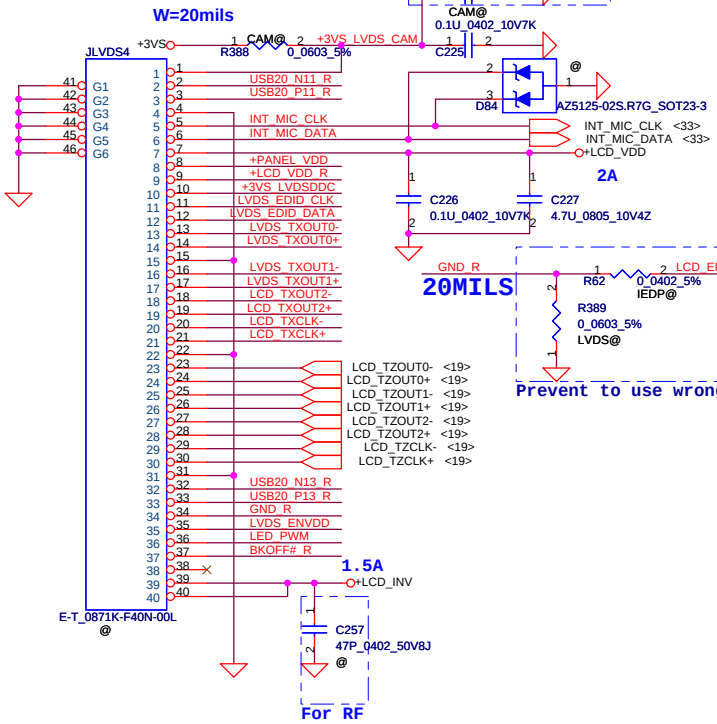
only need for 3D with DCDC/B ,JLVDS Pin8 can connect to +LCV_VDD directly for 3D w/o DCDC/B





For RF @ C256 47P_0402_50V8J

W=20mils

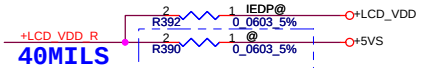


1.5A +LCD_INV C257 47P_0402_50V8J @ For RF

GND_R 20MILS R62 0_0402_5% LCD_ENVDD_R IEDP@ R389 0_0603_5% LVDS@

Prevent to use wrong interface panel.

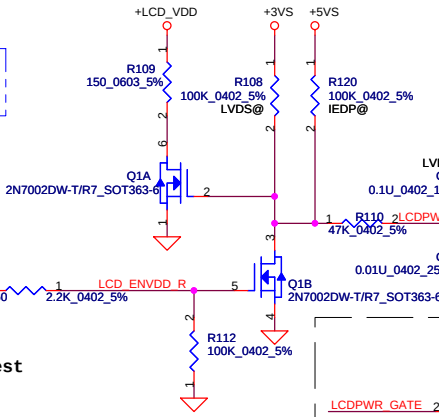
+LCD_VDD_R 40MILS

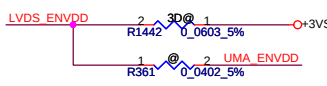


For LVDS 3D only

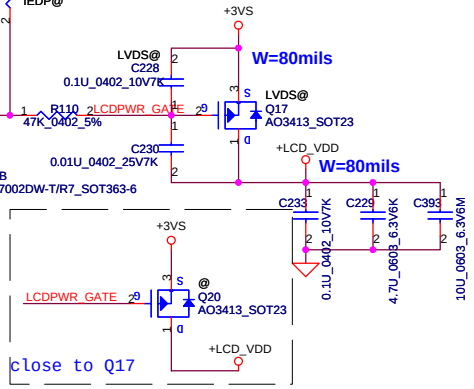
For RF @ C258 47P_0402_50V8J +LCD_VDD

reserve for 3D w/o DCDC/B

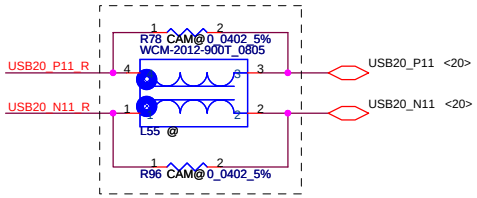




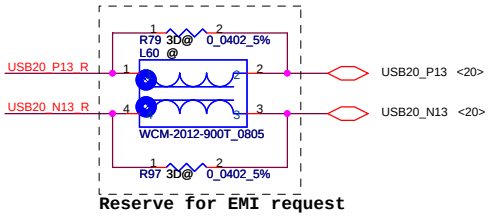
for 3D with DCDC/B



Reserve for EMI request

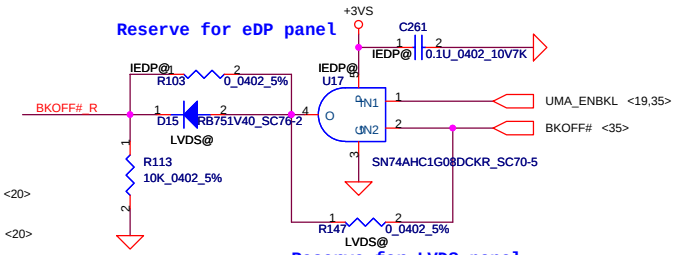


USB for Glasses free 3D



Reserve for EMI request

Reserve for eDP panel

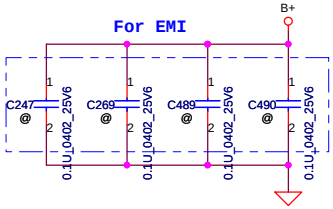


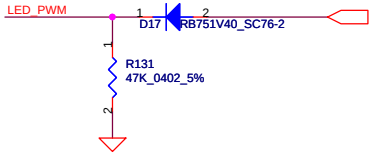
Reserve for LVDS panel

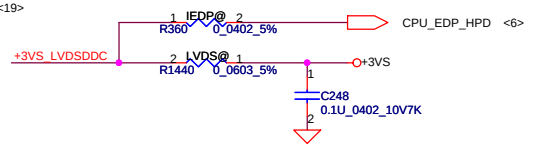
1.5A +LCD_INV L2 FBMA-L11-201209-221LMA30T_0805 F3 3A_32V_S1206-F-3.0A B+ C234 68P_0402_50V8J C235 0.1U_0402_25V6

Add F3 to prevent burn on PVT

For EMI







LVDS & eDP cable pine definition notice.

Prevent to use wrong interface panel.

	LVDS cable MB side Pin 22	eDP cable MB side Pin 22
LVDS	GND	
eDP		NC

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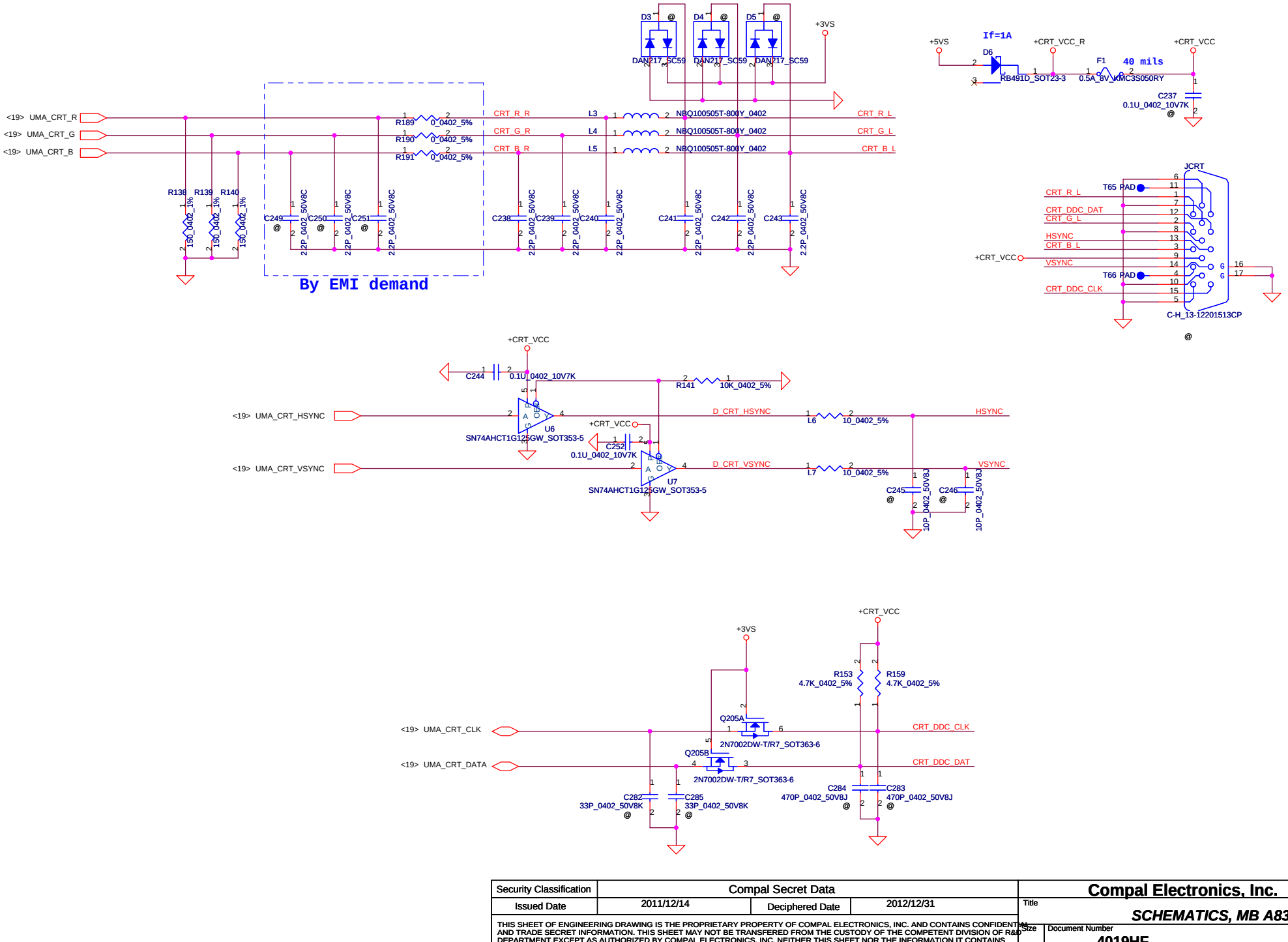
Size: Custom	Document Number: 4019HF
Rev	B
Date: Thursday, February 16, 2012	Sheet 13 of 51

CRT CONNECTOR



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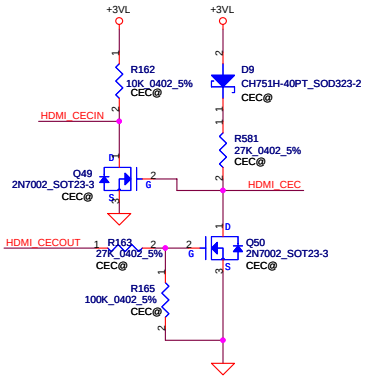
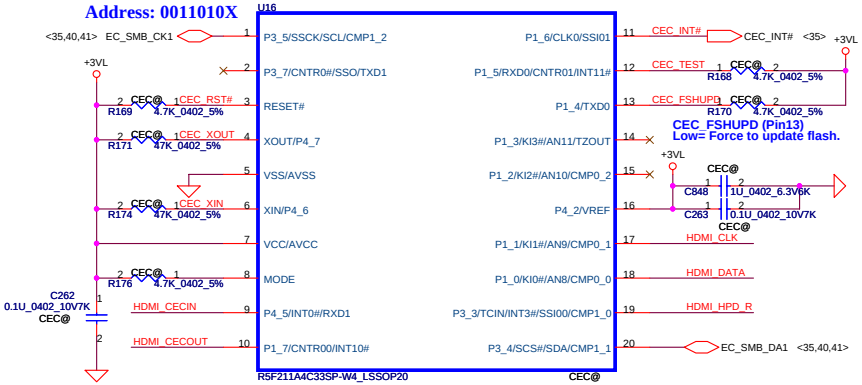
Title: ***SCHEMATICS, MB A8392***

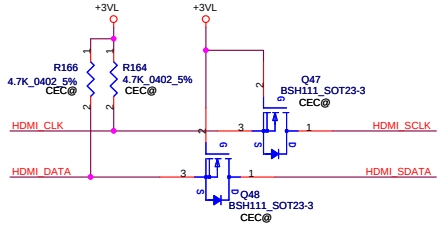
Size	Document Number	Rev
	4019HF	B

Date: Thursday, February 16, 2012 Sheet 14 of 51

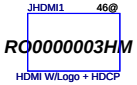
HDMI CEC Controller



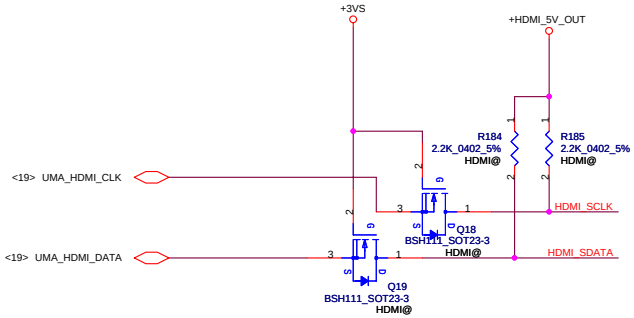


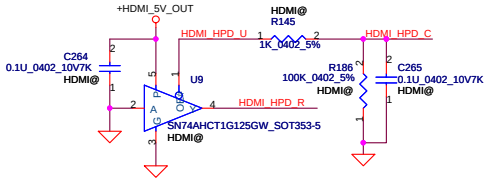


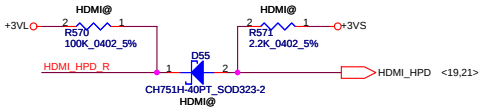
HDMI Royalty

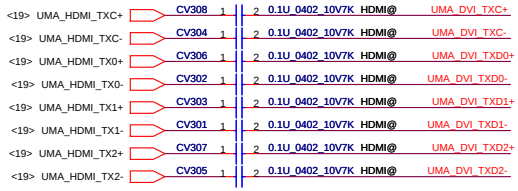


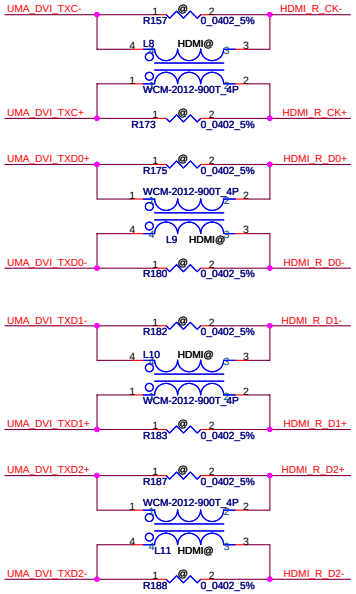
HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM

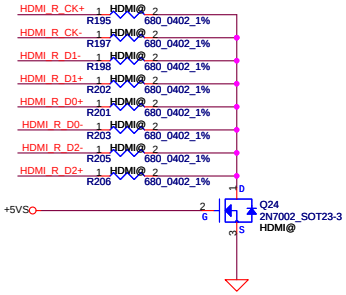


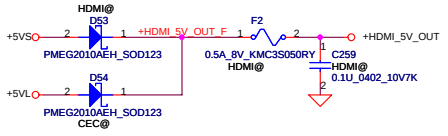




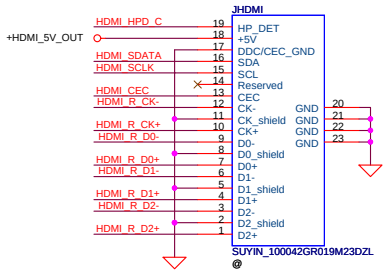








HDMI Connector



Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.	
Title	SCHEMATICS, MB A8392
Size	Document Number: 4019HF — Rev: B
Date: Thursday, February 16, 2012	Sheet 15 of 51

CMOS Setting, near DDR Door

iME Setting.

Integrated SUS 1.05V VRM Enable	
PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)

PCH_SPK
High = Enabled (No Reboot)
Low = Disabled (Default)

HDA_SDO
ME debug mode,
this signal has a weak internal pull down
*Low = Disable (default)
High = Enable (flash descriptor security overide)

HDA_SYNC
*This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
Need to pull high for Huron River platform

8/30 Change PWRME_CTRL# to HDA_SDO by PCH EDS

Placement near to YH1

SPI ROM for BIOS & ME (4MByte)

4MB ROM P/N:
SA00003K800
SA00004LI00

Socket: SP07000F500/SP07000H900
Please place U13 & U4 close to U2 PCH,
please place RH66, RH67, RH68 near UH3
Please place RH267 near RH66, Please place RH271 near RH67,
Please place RH269 near RH68.

SPI ROM for Win8 (2MByte)

2MB ROM P/N:
SA000041N00
SA00003FO10

If use GCLK, please delet DH1

BOOT BIOS Strap Bit 0

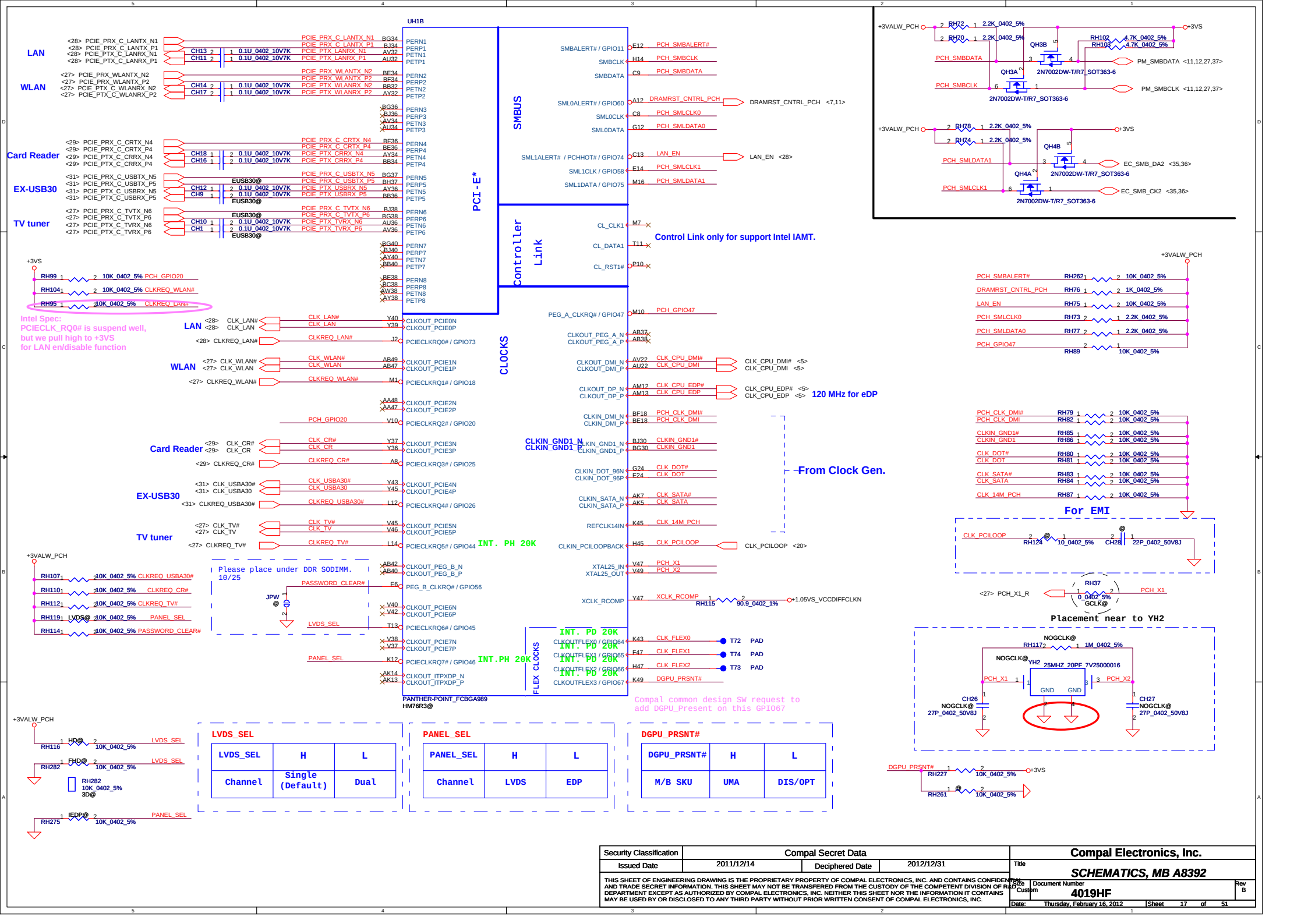
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: SCHEMATICS, MB A8392

Size: Custom | Document Number: 4019HF | Rev: B

Date: Thursday, February 16, 2012 | Sheet 16 of 51

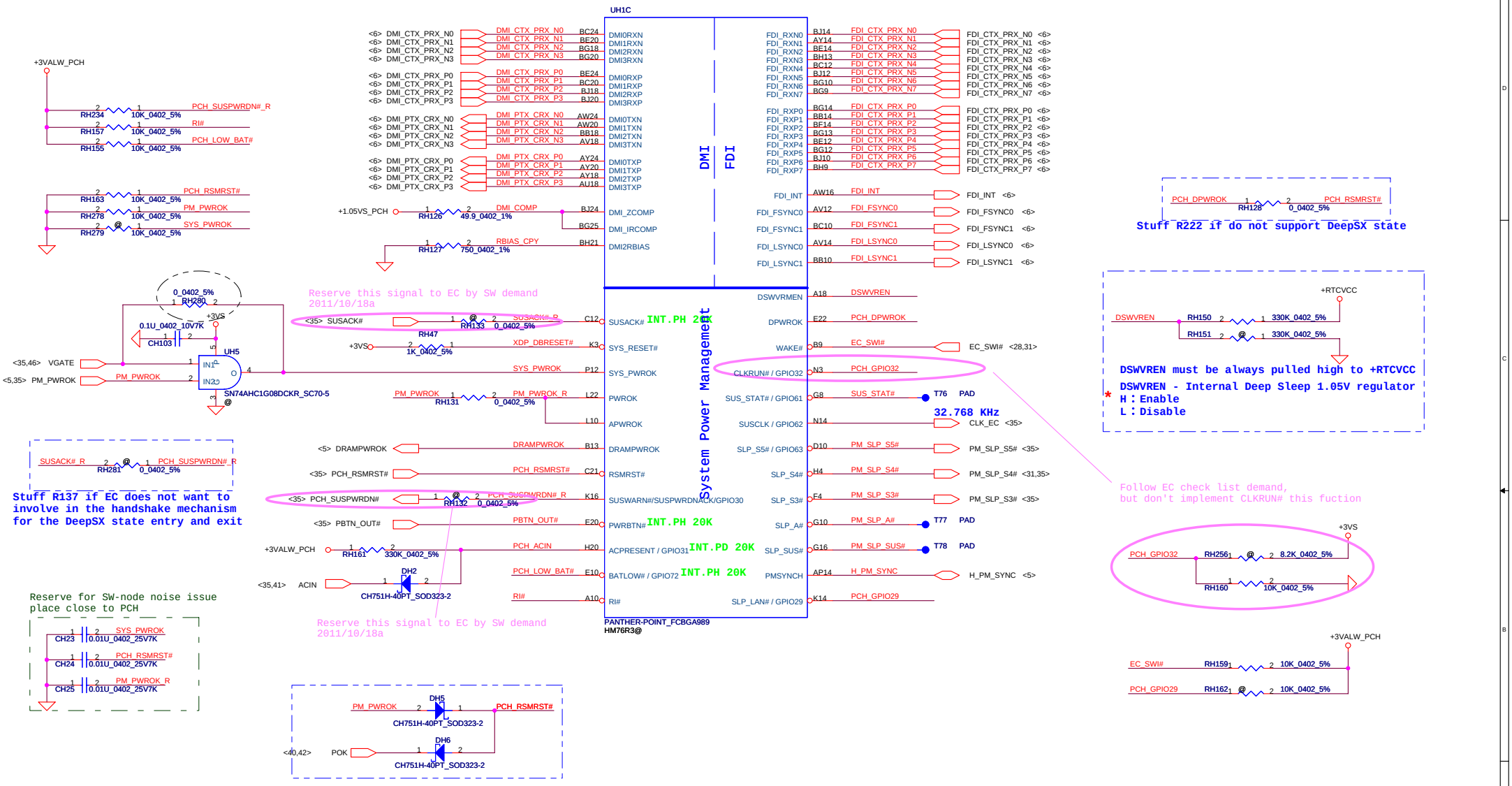


LVDS_SEL	H	L
Channel	Single (Default)	Dual

PANEL_SEL	H	L
Channel	LVDS	EDP

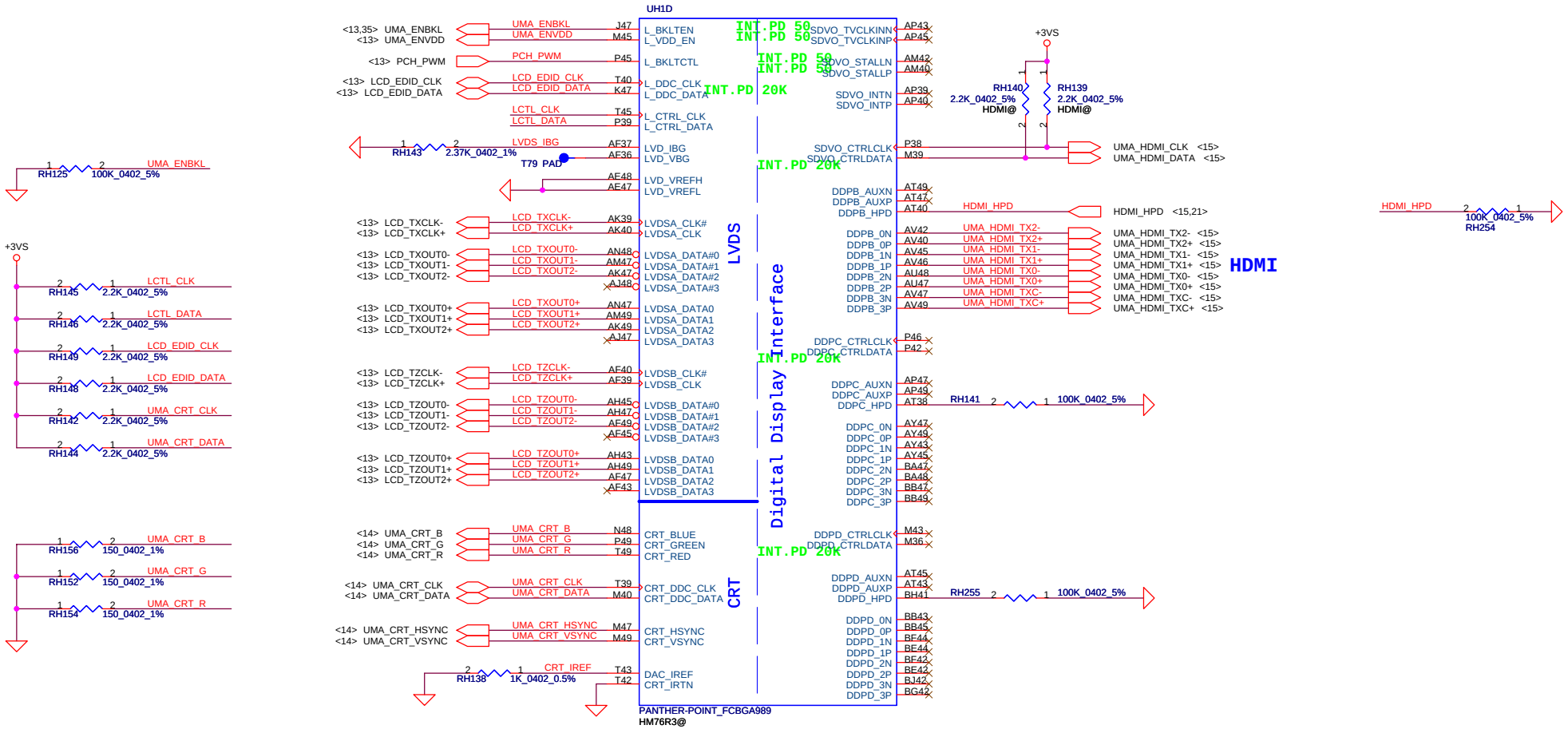
DGPU_PRSNT#	H	L
M/B SKU	UMA	DIS/OPT

Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31



Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	SCHEMATICS, MB A8392		
Size: Custom	Document Number: 4019HF		Rev: B
Date: Thursday, February 16, 2012	Sheet 18 of 51		



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Issued Date	2011/12/14	Deciphered Date	2012/12/31

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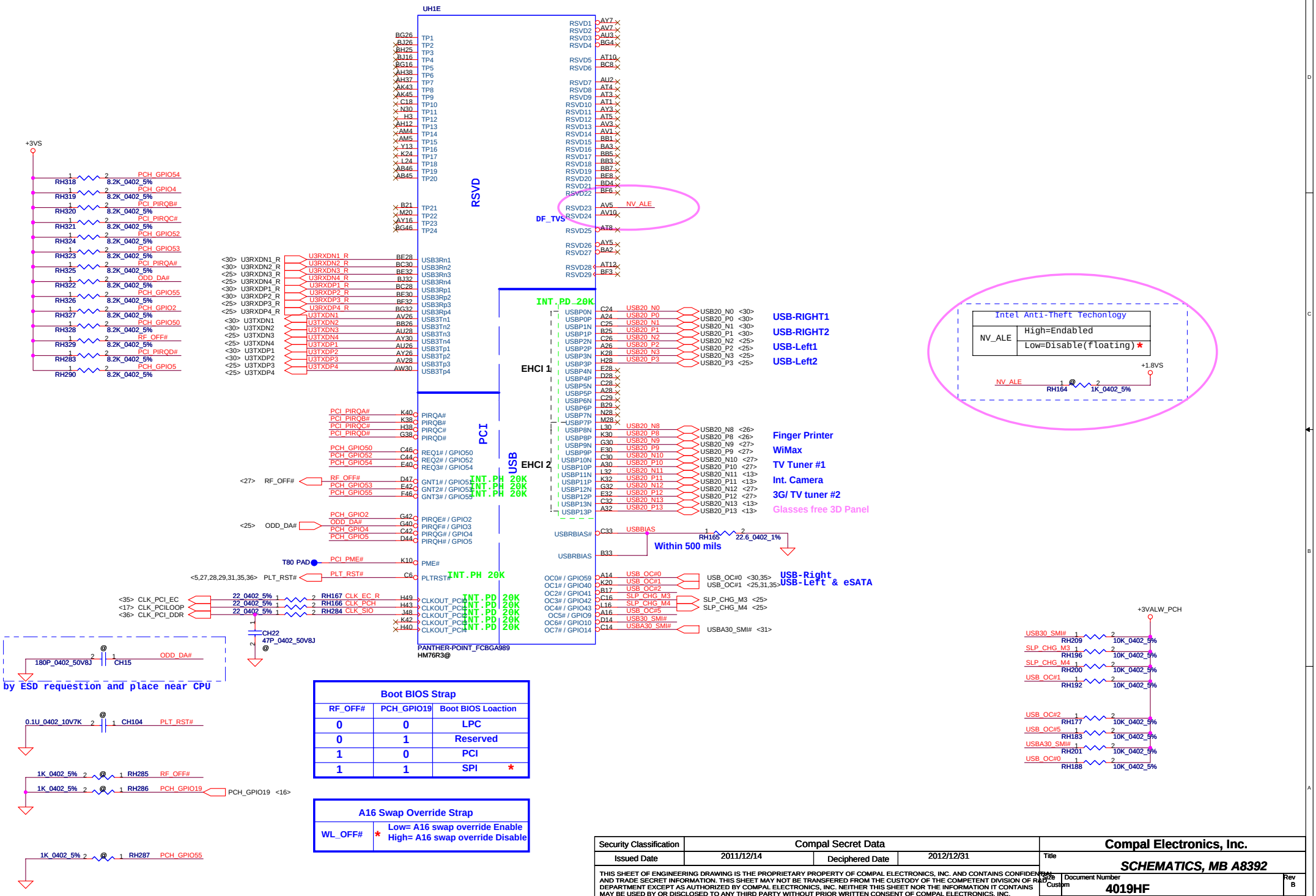
Title: ***SCHEMATICS, MB A8392***

Size	Document Number	Rev
Custom	4019HF	B

Date: Thursday, February 16, 2012 | Sheet 19 of 51



Boot BIOS Strap		
RF_OFF#	PCH_GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

A16 Swap Override Strap	
WL_OFF#	* Low= A16 swap override Enable High= A16 swap override Disable

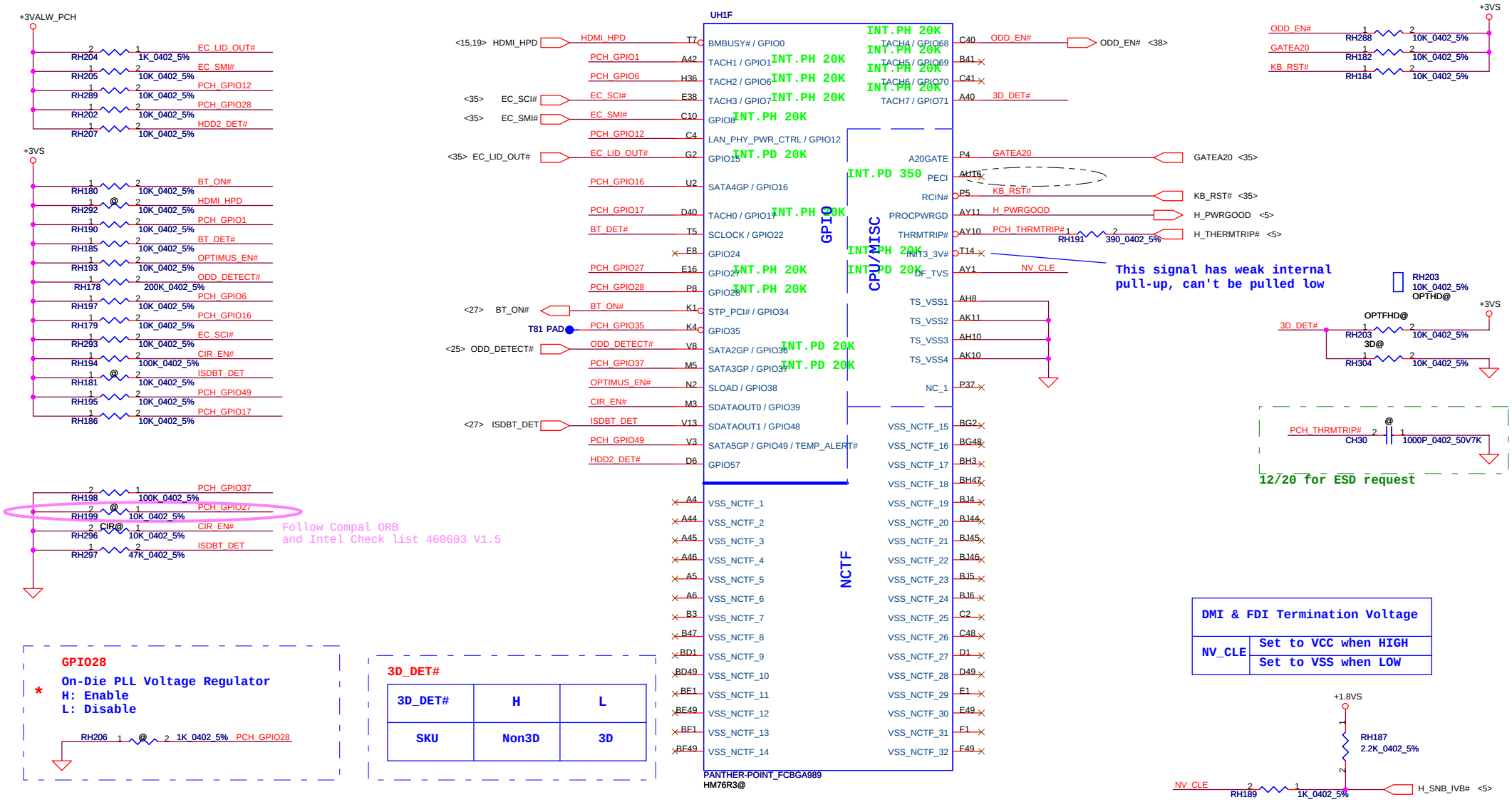
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: *SCHEMATICS, MB A8392*

Size: Custom | Document Number: 4019HF | Rev: B

Date: Thursday, February 16, 2012 | Sheet 20 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

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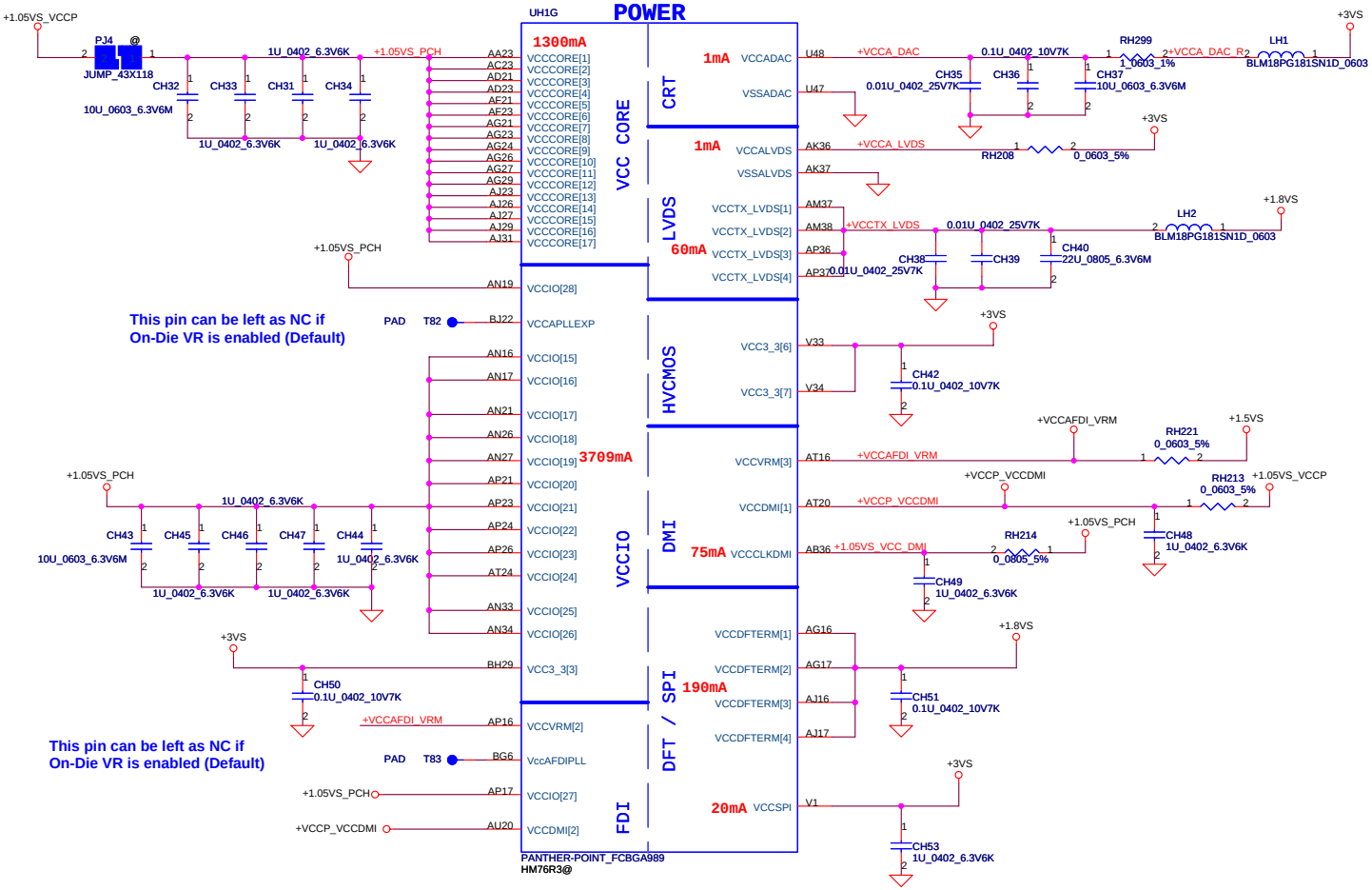
Title	SCHEMATICS, MB A8392		
Size: Custom	Document Number: 4019HF		Rev: B
Date: Thursday, February 16, 2012	Sheet 21 of 51		

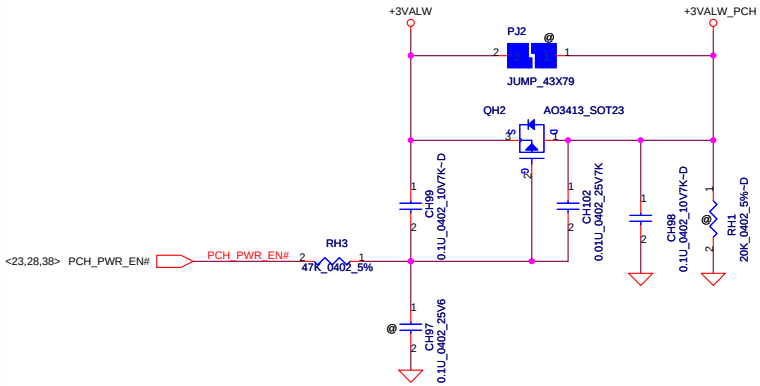


PCH Power Rail Table
Refer to PCH EDS R1.0

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

+3VALW to +3V_PCH

Vgs=-4.5V,Id=3A,Rds<97mohm



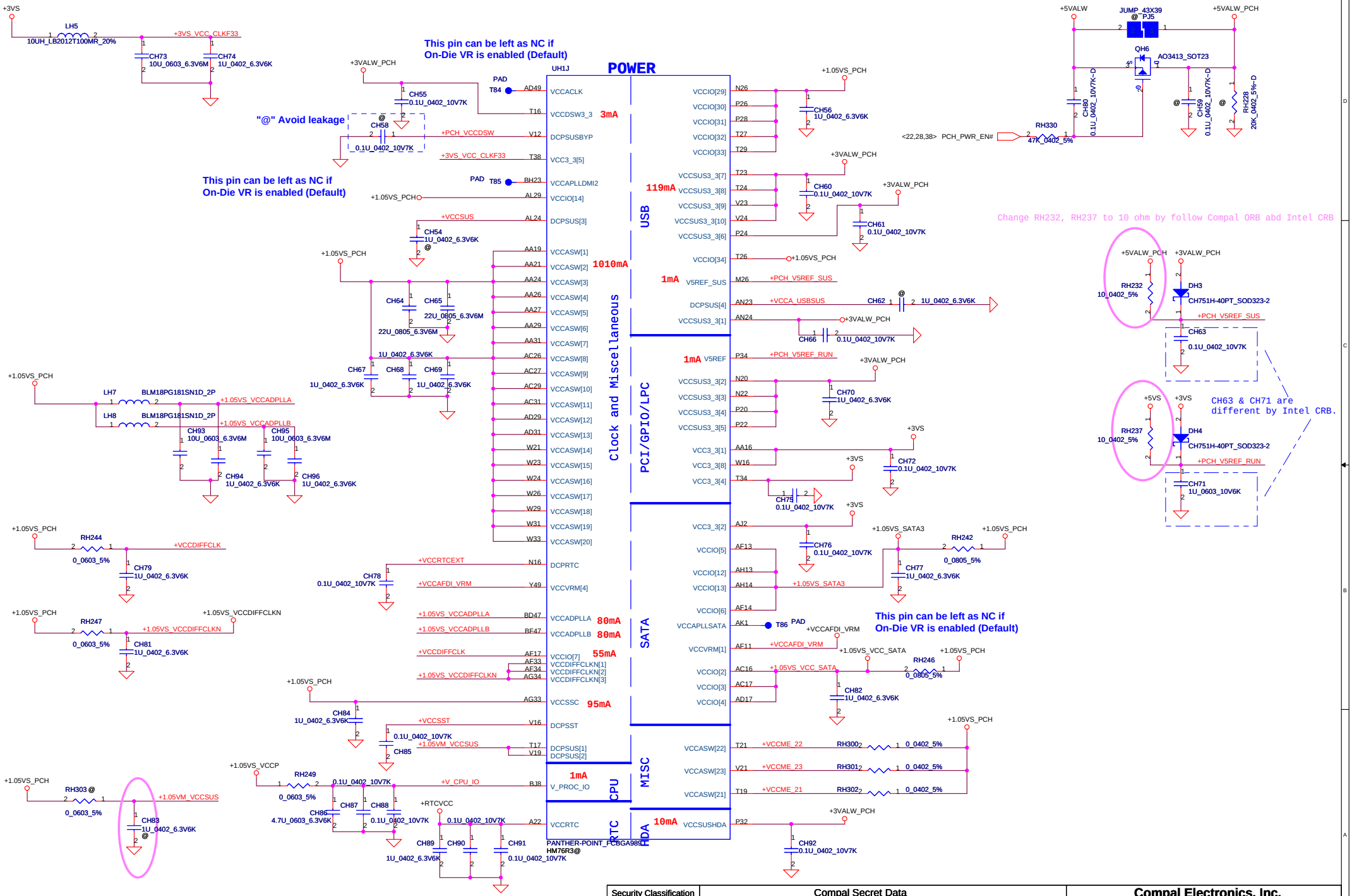
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: *SCHEMATICS, MB A8392*

Size: Custom | Document Number: 4019HF | Rev: B

Date: Thursday, February 16, 2012 | Sheet 22 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

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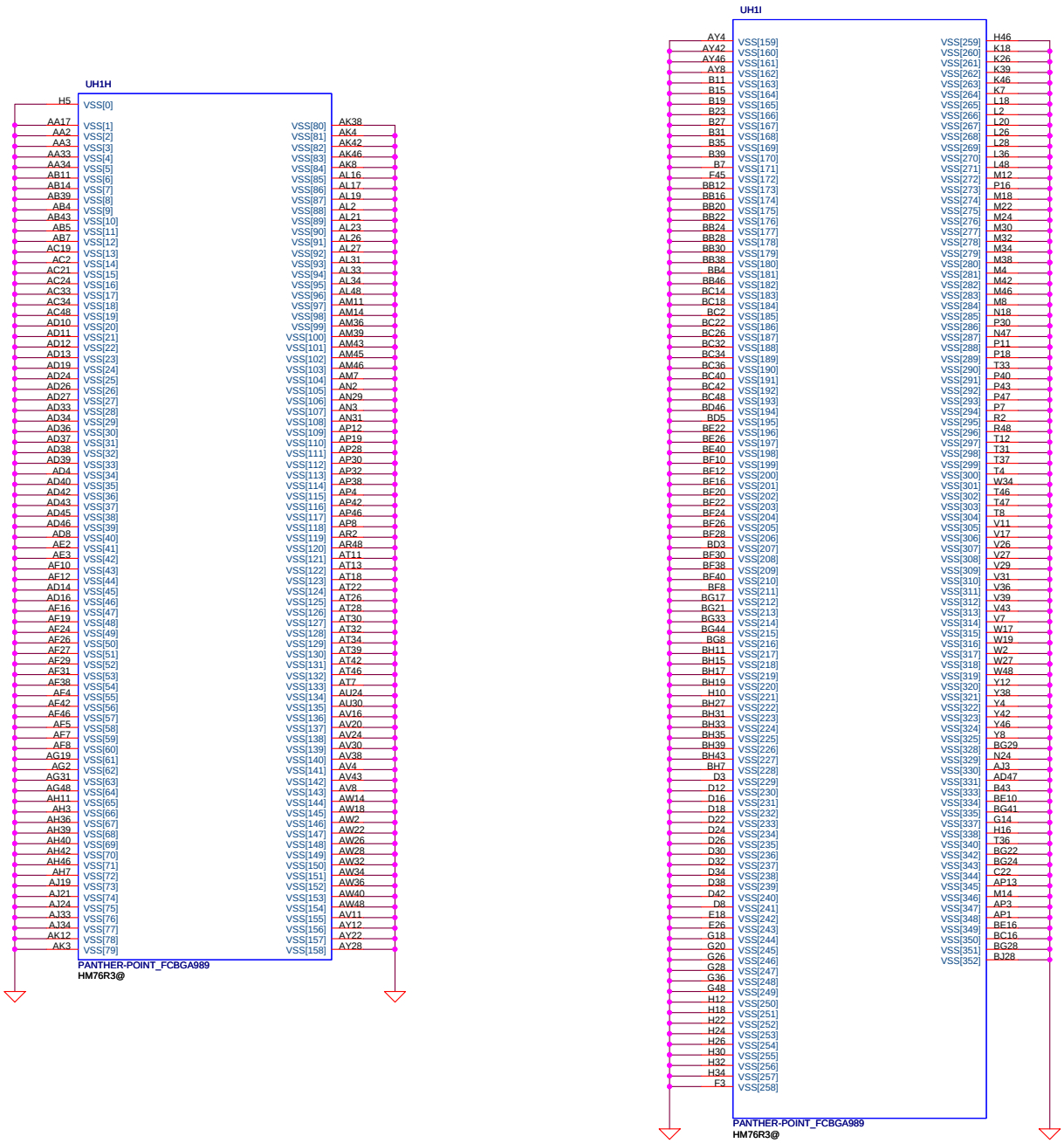
Title	SCHEMATICS, MB A8392
Size: Custom	Document Number: 4019HF
Rev: B	
Date: Thursday, February 16, 2012	Sheet 23 of 51



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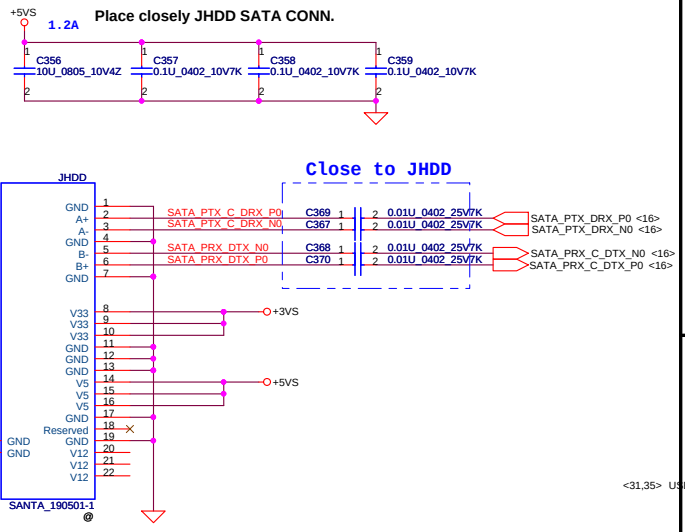
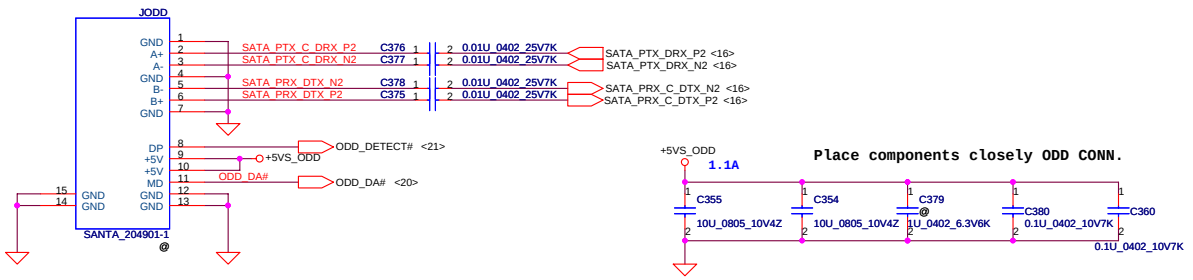
Issued Date	2011/12/14	Deciphered Date 2012/12/31	Title: SCHEMATICS, MB A8392
			Size: Custom; Document Number: 4019HF; Rev: B
			Date: Thursday, February 16, 2012; Sheet 24 of 51

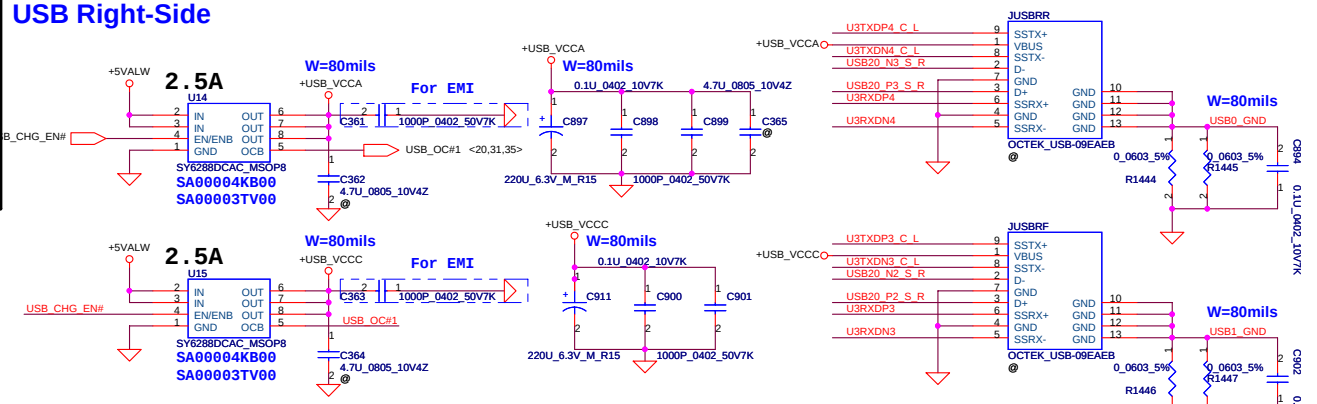
SATA HDD Conn.



SATA ODD Conn

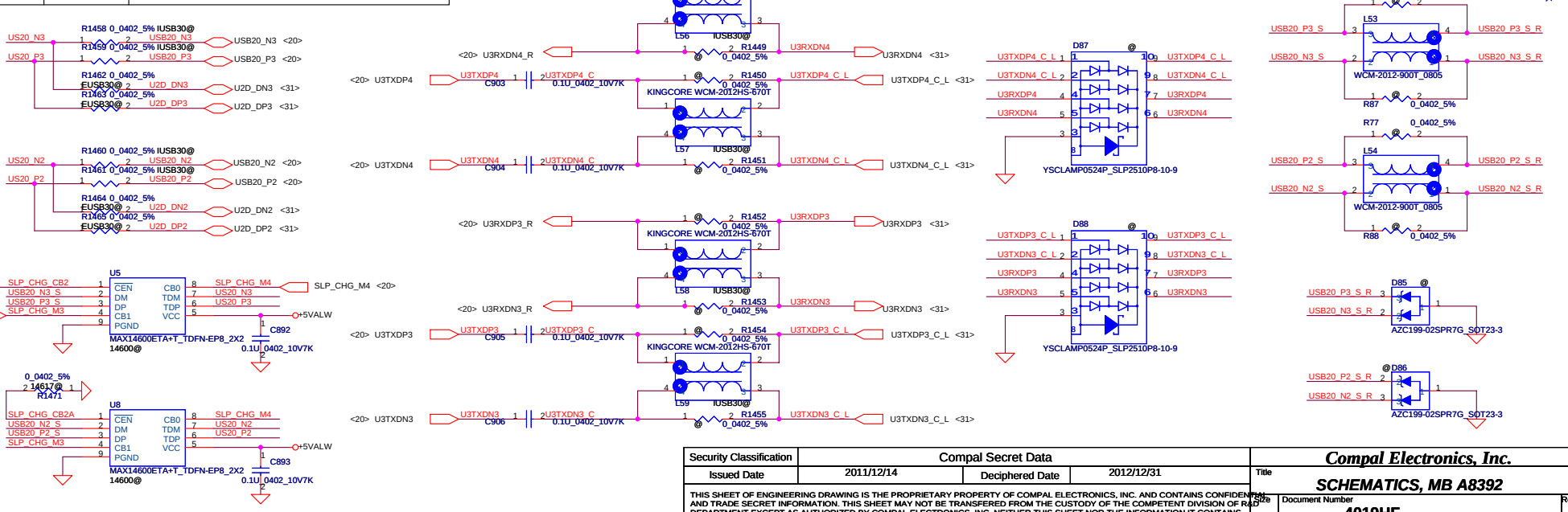


USB Right-Side



USB Sleep & Charge Auto-Mode/Mode3

MAX14600 & MAX14617			
CB0 SLP_CHG_M4	CB1 SLP_CHG_M3	CB2 (14617 only)	STATUS
0	0	0	AUTO MODE
0	1	0	Force Dedicated charger mode (MODE3)
1	0	0	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM
1	1	0	Pass-Through (USB) Mode with CDP Emulation: Auto Connect DP/DM to TDP/TDM depending on CDP status
X	X	1	Force Apple 2A Charger Mode: Apple 2A resistor dividers



Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

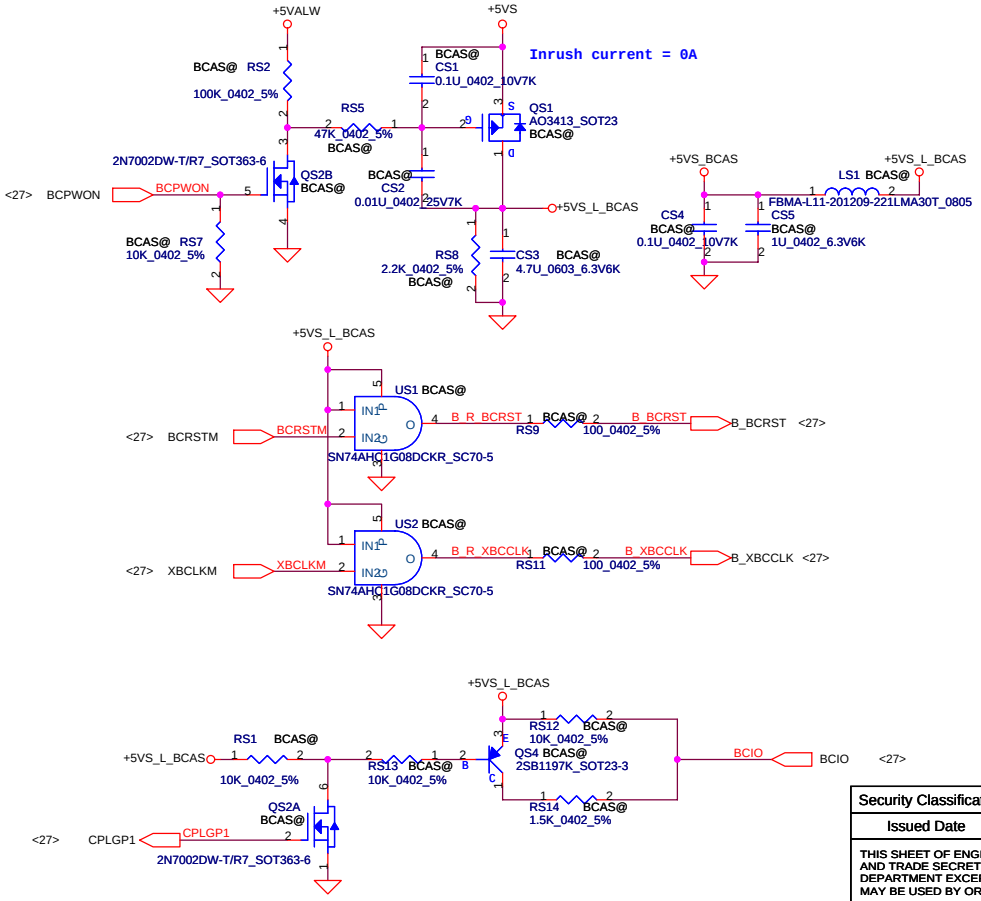
Title: SCHEMATICS, MB A8392

Size | Document Number: 4019HF | Rev: B

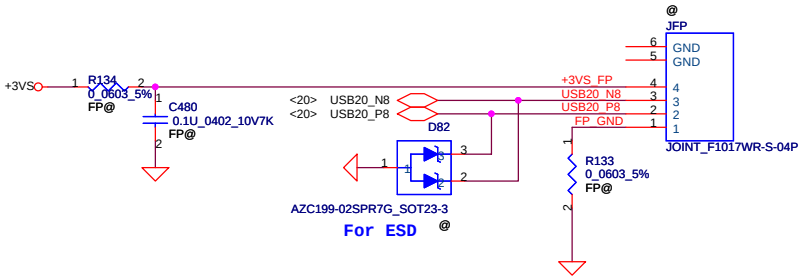
Date: Thursday, February 16, 2012 | Sheet 25 of 51

Screw cap for ESD request

B-CAS Circuit



Finger printer



Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: SCHEMATICS, MB A8392

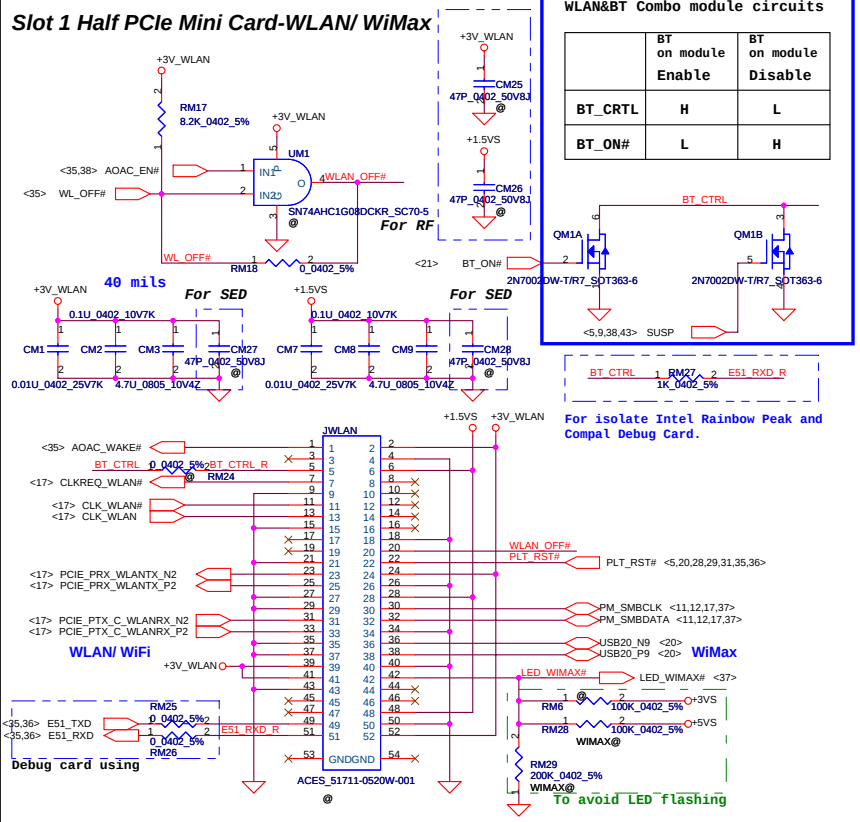
Size | Document Number: 4019HF | Rev: B

Date: Thursday, February 16, 2012 | Sheet 26 of 51

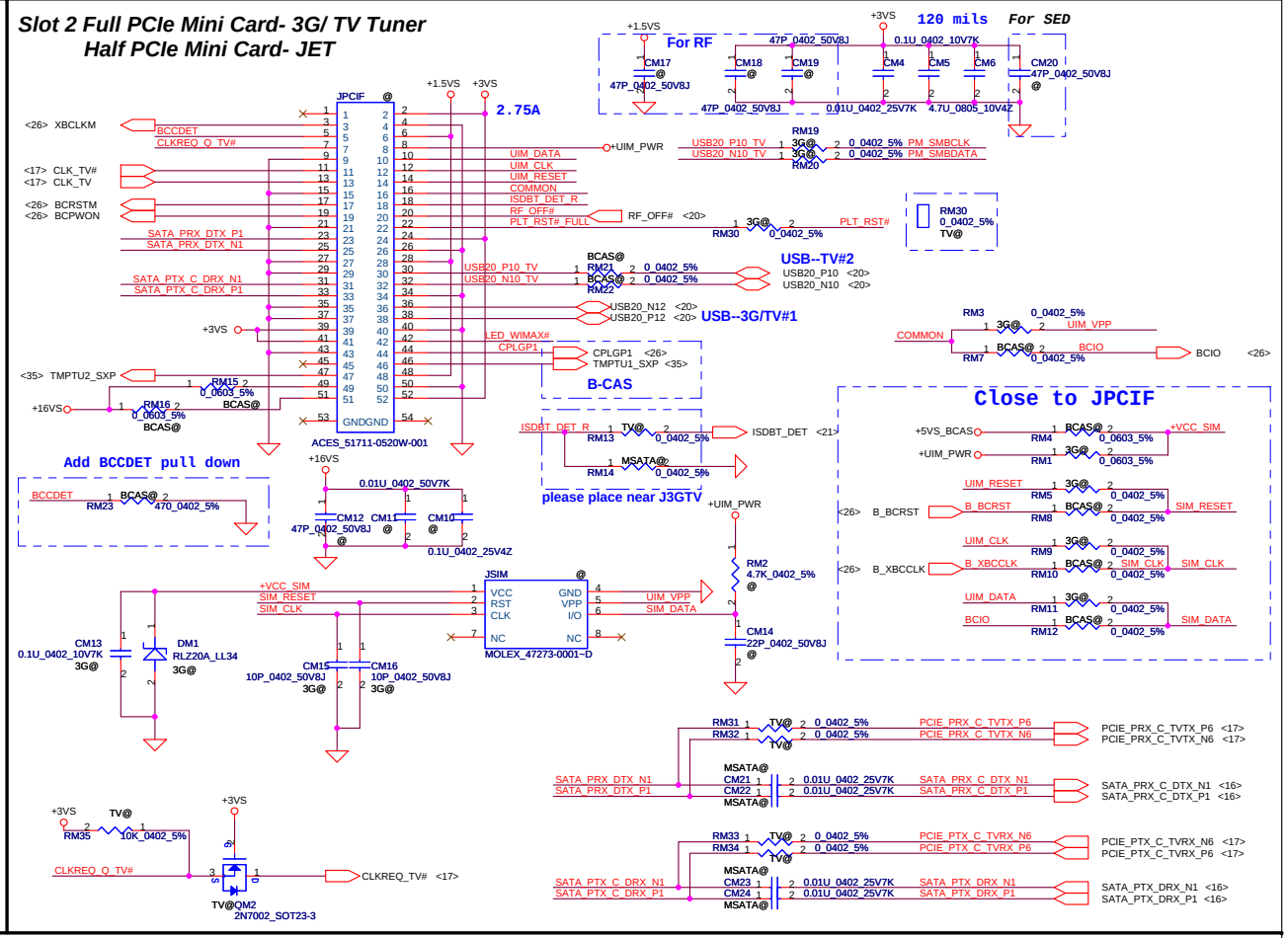
Slot 1 Half PCIe Mini Card-WLAN/ WiMax

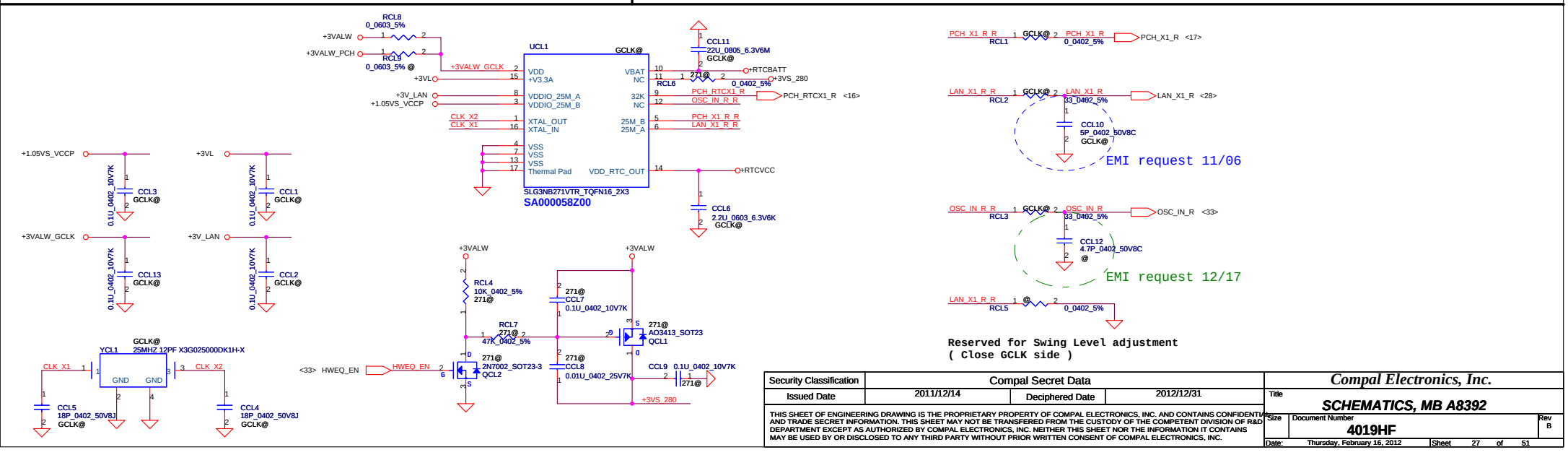
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	H	L
BT_ON#	L	H



Slot 2 Full PCIe Mini Card- 3G/ TV Tuner Half PCIe Mini Card- JET





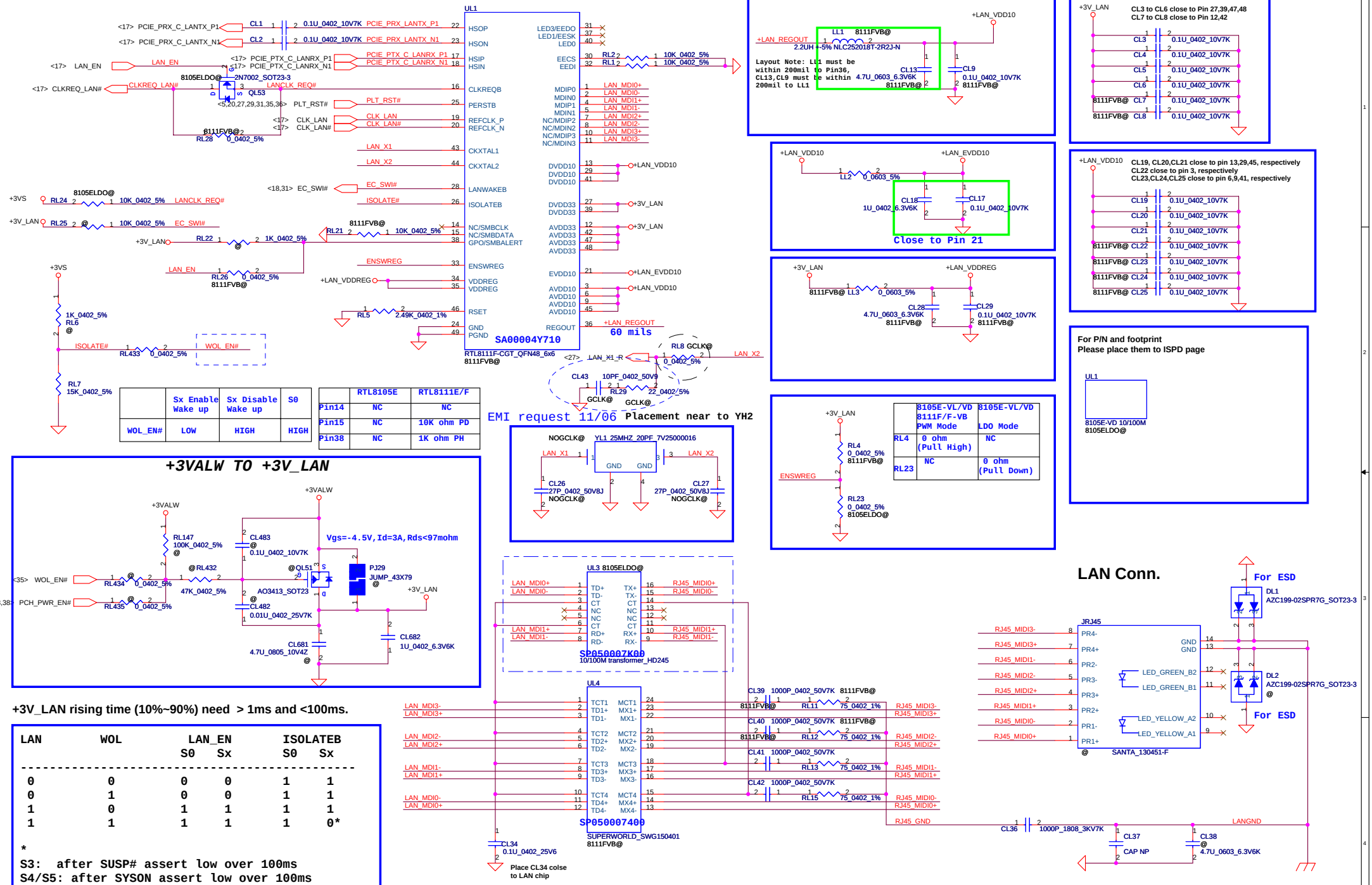
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: SCHEMATICS, MB A8392

Size | Document Number: 4019HF | Rev: B

Date: Thursday, February 16, 2012 | Sheet 27 of 51



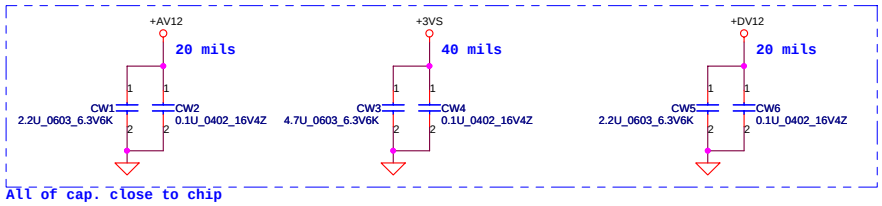
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

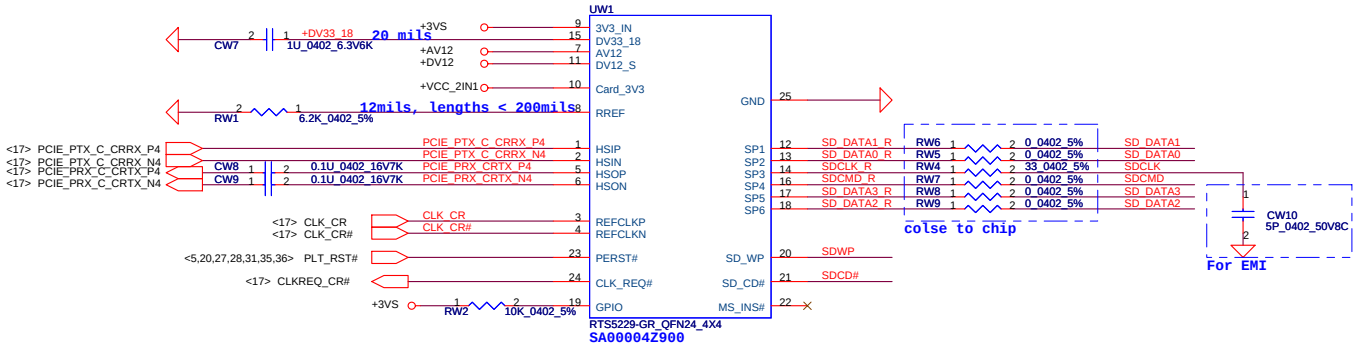
Compal Electronics, Inc.

Title: SCHEMATICS, MB A8392

Size: Custom | Document Number: 4019HF | Rev: B

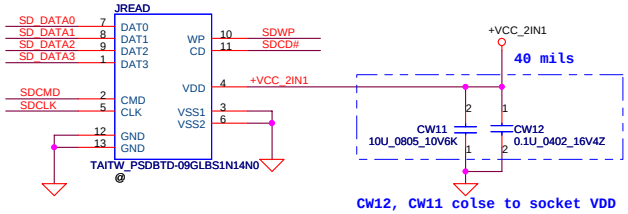
Date: Thursday, February 16, 2012 | Sheet 28 of 51





< 2 in 1 Card Reader >

Connector on bottom side



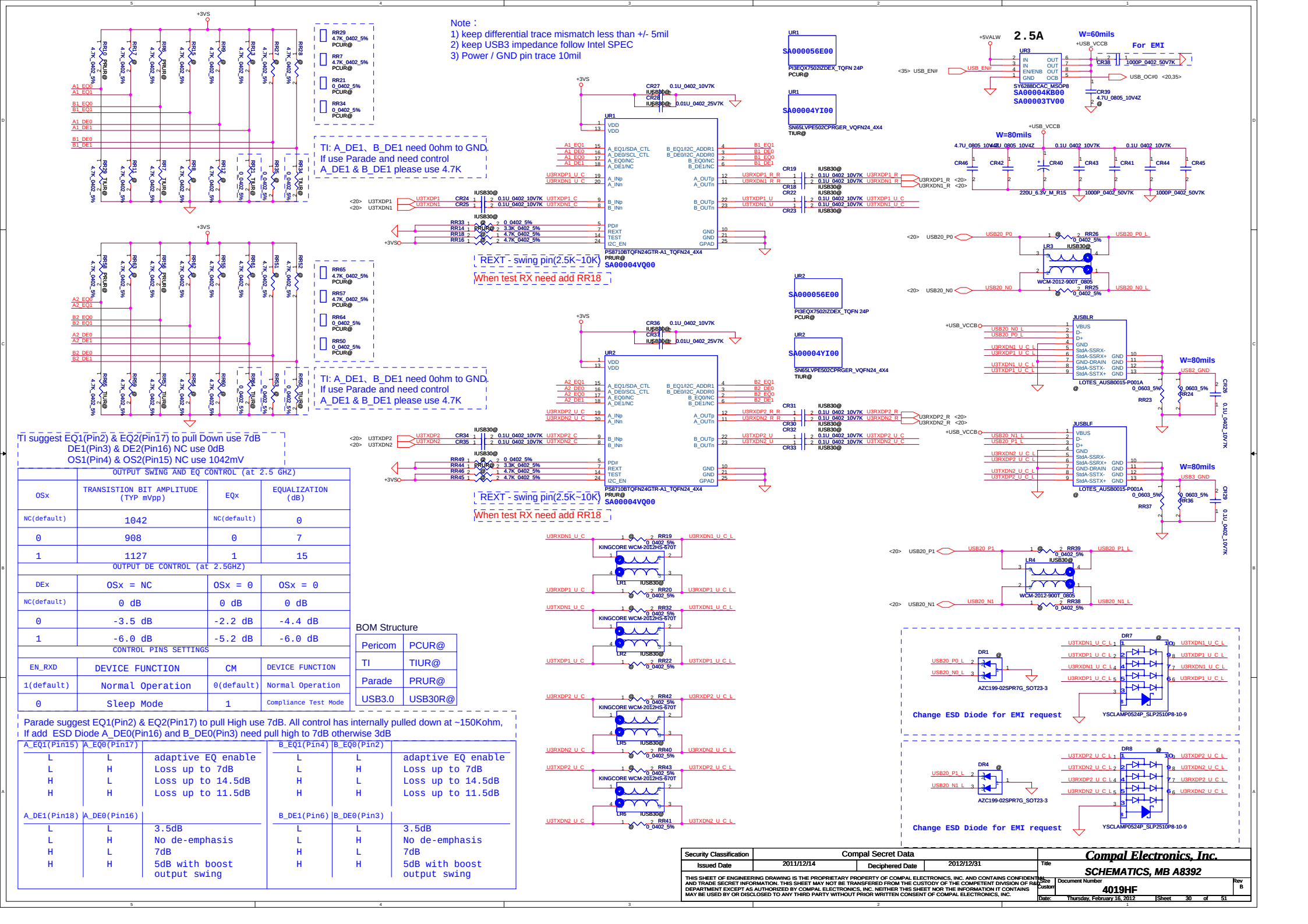
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **SCHEMATICS, MB A8392**

Size: Custom | Document Number: **4019HF** | Rev: B

Date: Thursday, February 16, 2012 | Sheet 29 of 51



OUTPUT SWING AND EQ CONTROL (at 2.5 GHZ)			
OSx	TRANSISTION BIT AMPLITUDE (TYP mVpp)	EQx	EQUALIZATION (dB)
NC(default)	1042	NC(default)	0
0	908	0	7
1	1127	1	15
OUTPUT DE CONTROL (at 2.5GHZ)			
DEx	OSx = NC	OSx = 0	OSx = 0
NC(default)	0 dB	0 dB	0 dB
0	-3.5 dB	-2.2 dB	-4.4 dB
1	-6.0 dB	-5.2 dB	-6.0 dB
CONTROL PINS SETTINGS			
EN_RXD	DEVICE FUNCTION	CM	DEVICE FUNCTION
1(default)	Normal Operation	0(default)	Normal Operation
0	Sleep Mode	1	Compliance Test Mode

BOM Structure

Pericom	PCUR@
TI	TIUR@
Parade	PRUR@
USB3.0	USB30R@

A_EQ1(Pin15)	A_EQ0(Pin17)	
L	L	adaptive EQ enable
L	H	Loss up to 7dB
H	L	Loss up to 14.5dB
H	H	Loss up to 11.5dB

B_EQ1(Pin4)	B_EQ0(Pin2)	
L	L	adaptive EQ enable
L	H	Loss up to 7dB
H	L	Loss up to 14.5dB
H	H	Loss up to 11.5dB

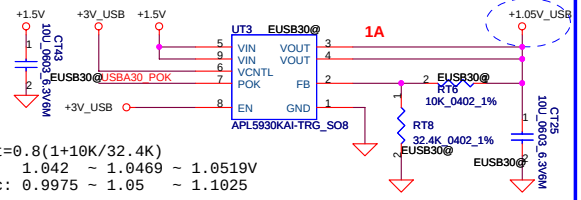
A_DE1(Pin18)	A_DE0(Pin16)	
L	L	3.5dB
L	H	No de-emphasis
H	L	7dB
H	H	5dB with boost output swing

B_DE1(Pin6)	B_DE0(Pin3)	
L	L	3.5dB
L	H	No de-emphasis
H	L	7dB
H	H	5dB with boost output swing

Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

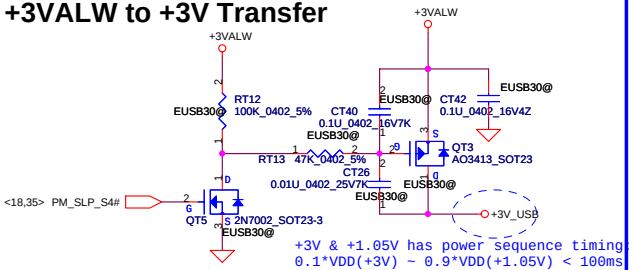
Title	Compal Electronics, Inc.
	SCHEMATICS, MB A8392
Size: Custom	Document Number: 4019HF
Rev: B	
Date: Thursday, February 16, 2012	Sheet 30 of 51

+1.5V to +1.05V Transfer

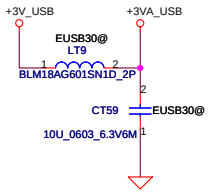


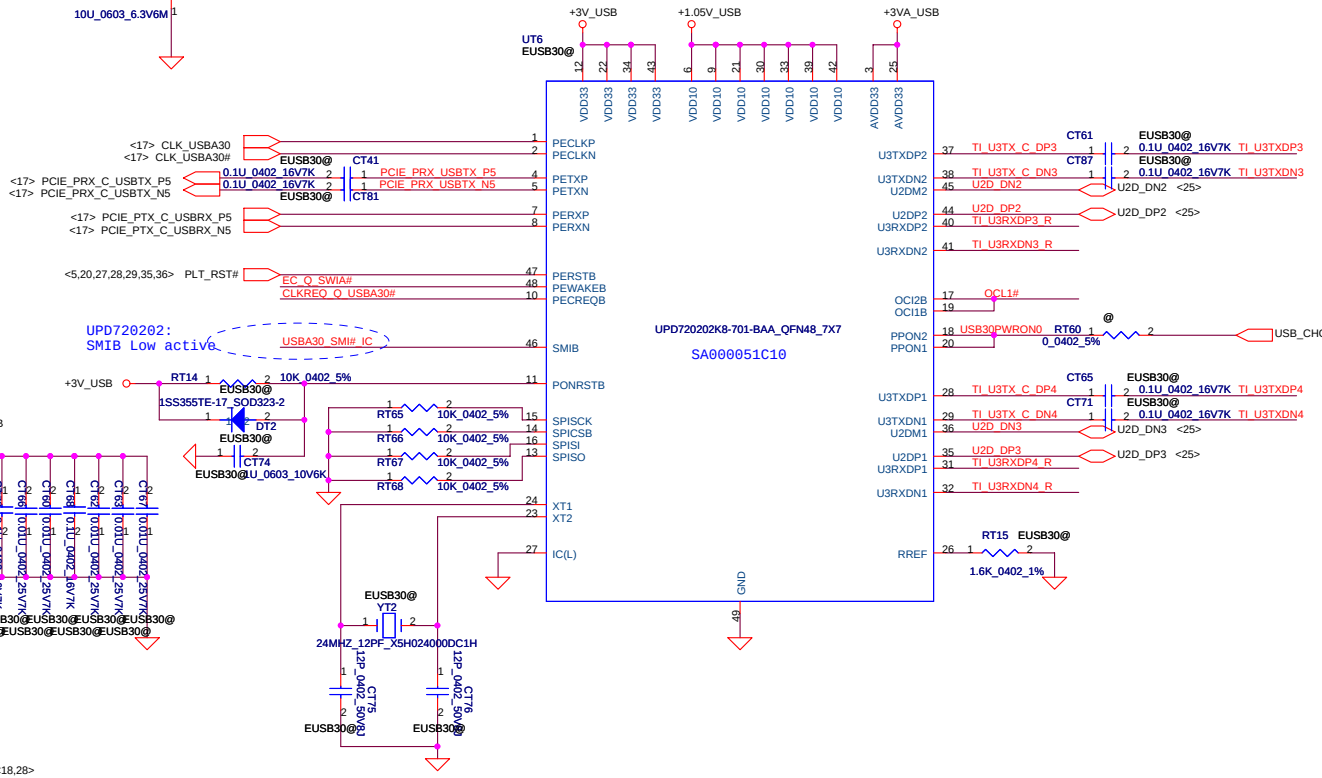
Vout=0.8(1+10K/32.4K)
1.042 ~ 1.0469 ~ 1.0519V
Spec: 0.9975 ~ 1.05 ~ 1.1025

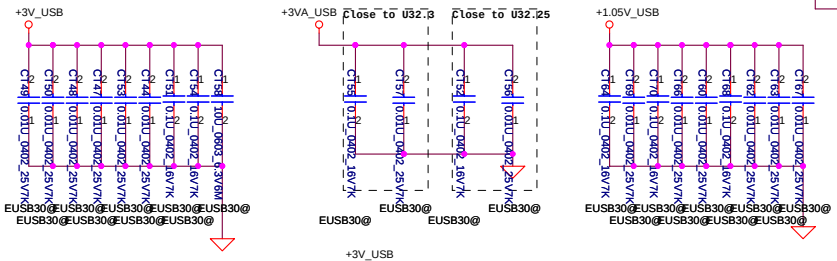
+3VALW to +3V Transfer

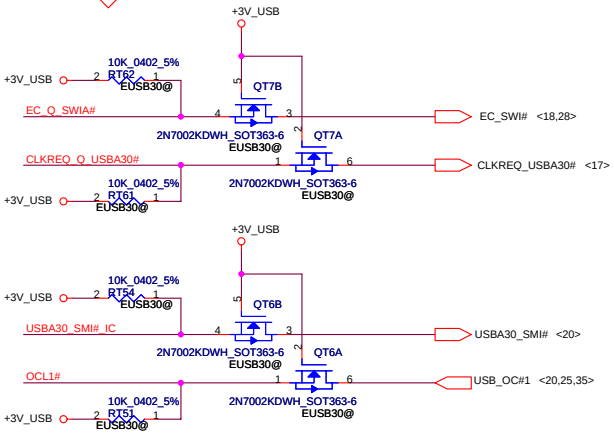


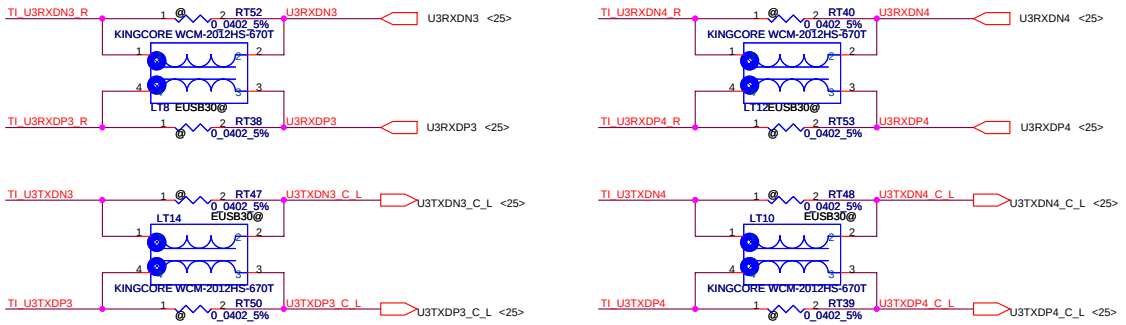
+3V & +1.05V has power sequence timing
0.1*VDD(+3V) ~ 0.9*VDD(+1.05V) < 100ms











Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: ***SCHEMATICS, MB A8392***

Size	Document Number	Rev
Custom	4019HF	B

Date: Thursday, February 16, 2012 | Sheet 31 of 51

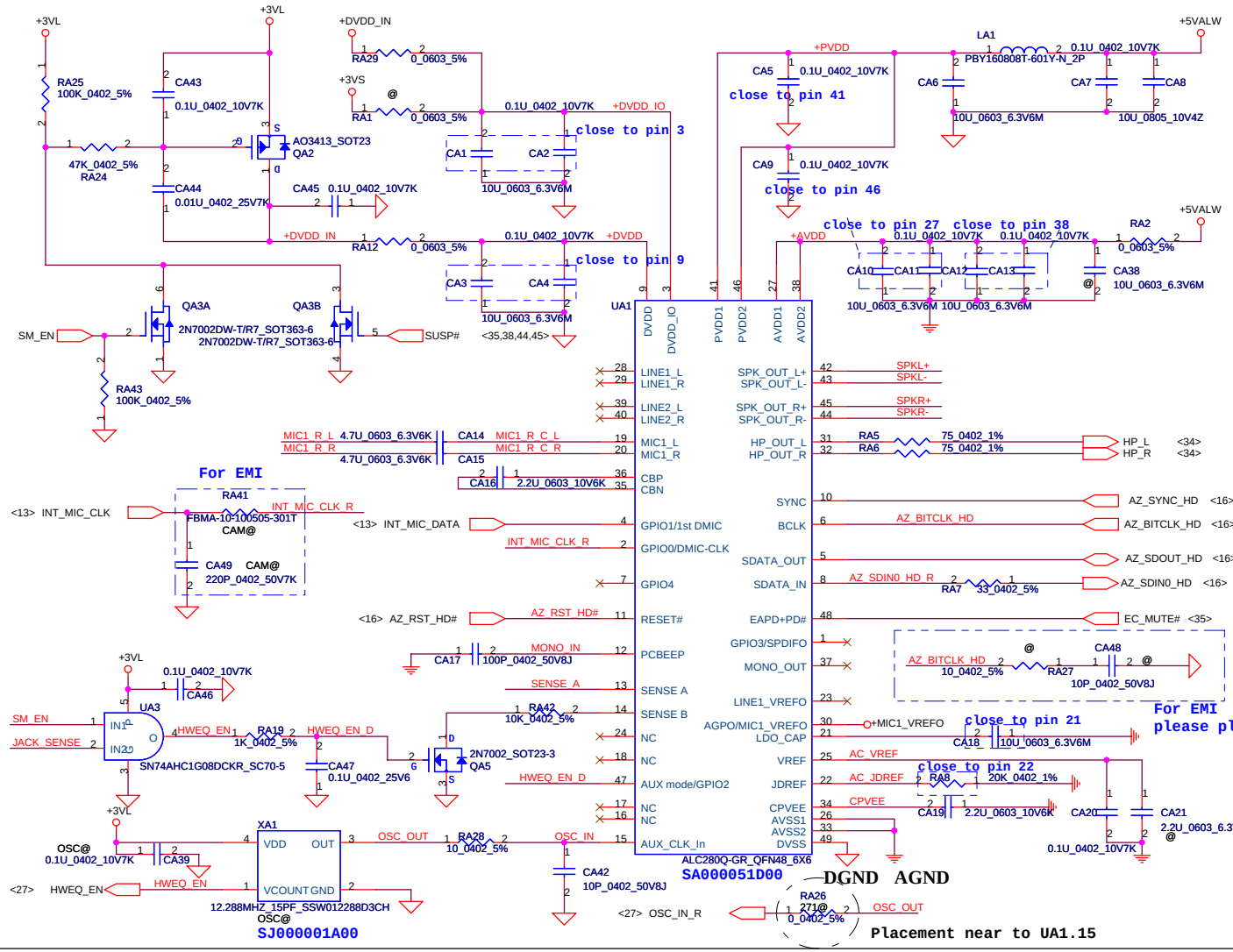
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

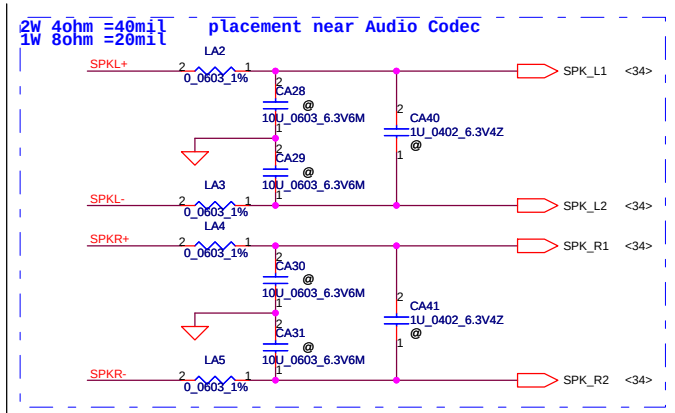
Compal Electronics, Inc.

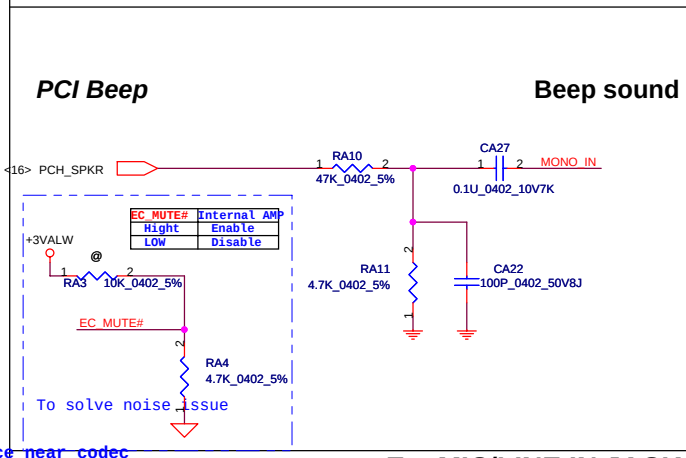
Title: ***SCHEMATICS, MB A8392***

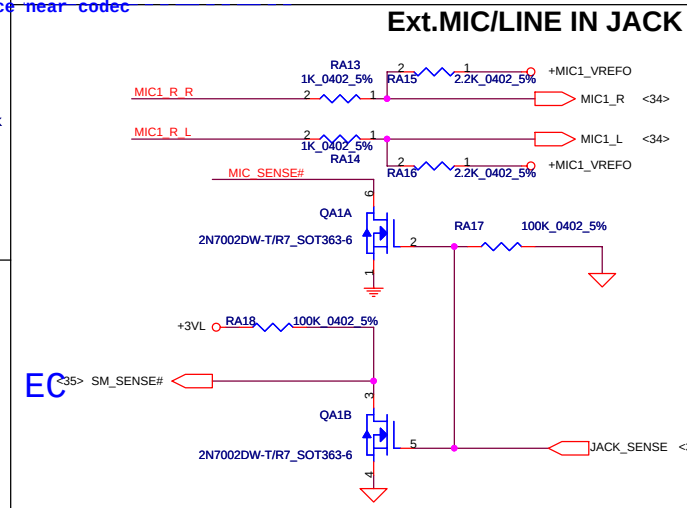
Size	Document Number	Rev
Custom	4019HF	B

Date: Thursday, February 16, 2012 Sheet 32 of 51

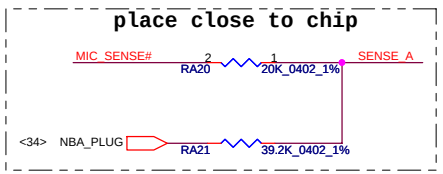


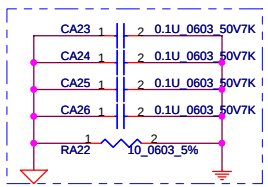






Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 31, 32)	Headphone out
	20K	PORT-B (PIN 19, 20)	Ext. MIC
	10K	PORT-C (PIN 28, 29)	
	5.1K	PORT-E	
SENSE B	39.2K		
	20K		
	10K		

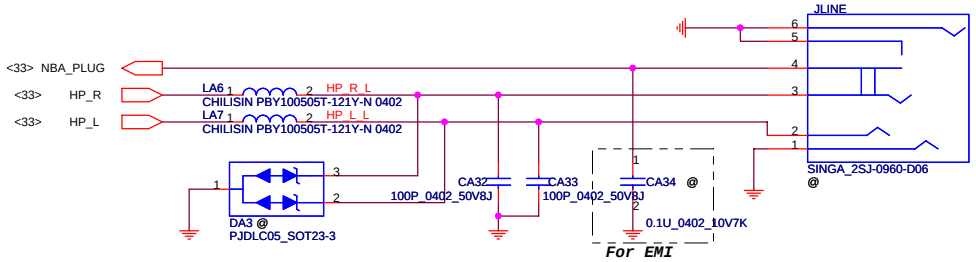




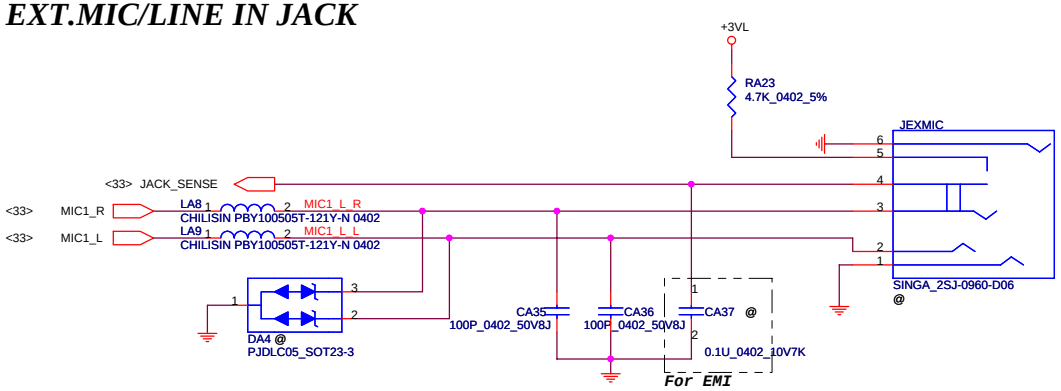
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	SCHEMATICS, MB A8392		
Size	Document Number	4019HF	Rev B
Date: Thursday, February 16, 2012	Sheet 33 of 51		

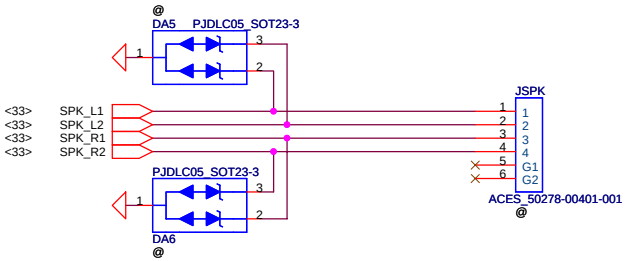
HeadPhone/LINE OUT JACK



EXT.MIC/LINE IN JACK



SPK CONN.



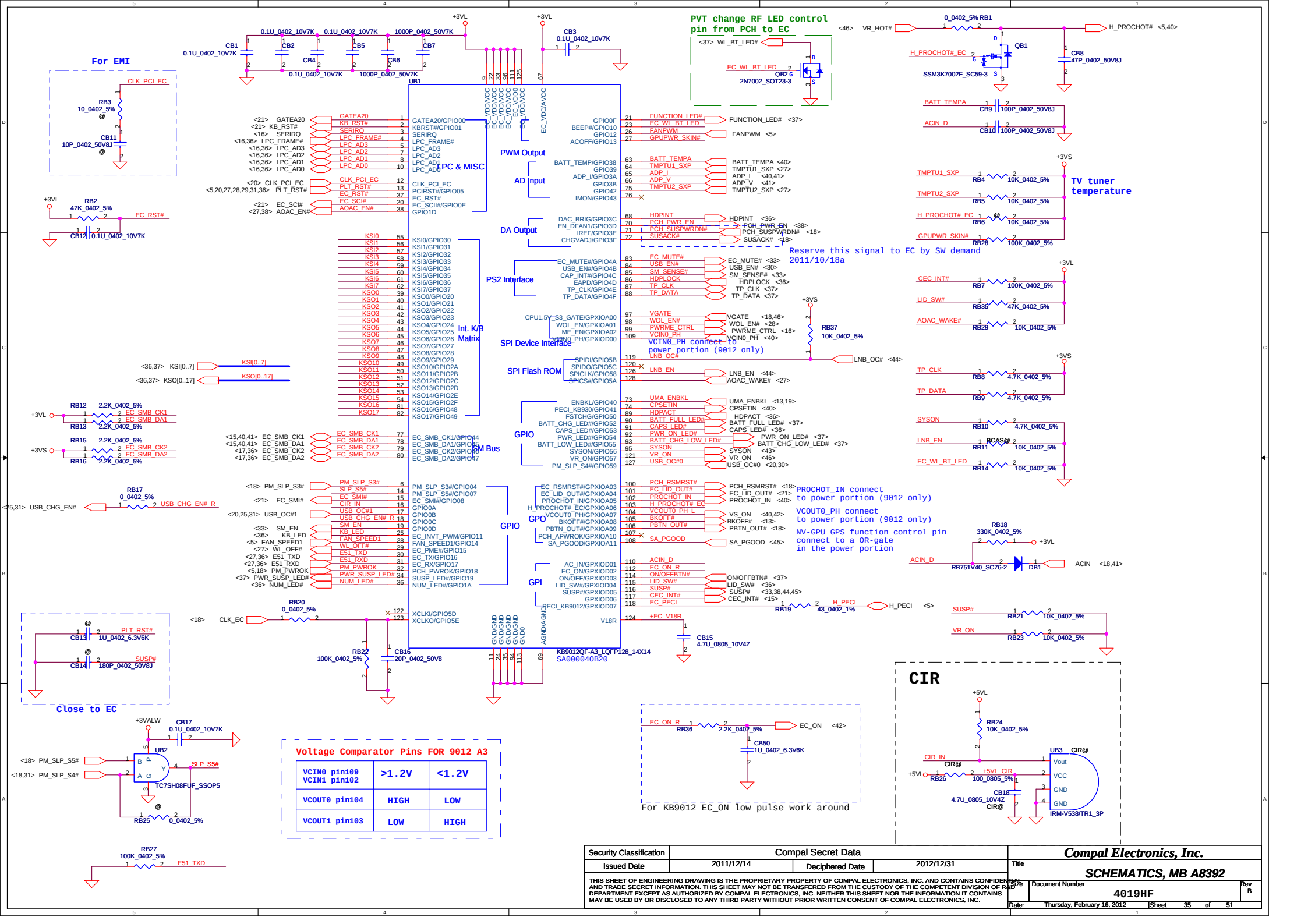
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: SCHEMATICS, MB A8392

Size	Document Number	Rev
	4019HF	B

Date: Thursday, February 16, 2012 Sheet 34 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

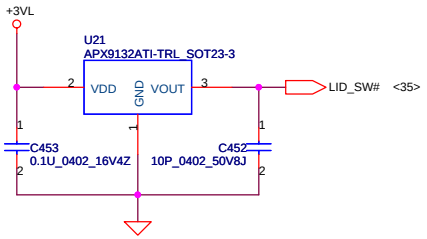
Title: **SCHEMATICS, MB A8392**

Size	Document Number	Rev
	4019HF	B

Date: Thursday, February 16, 2012 | Sheet 35 of 51

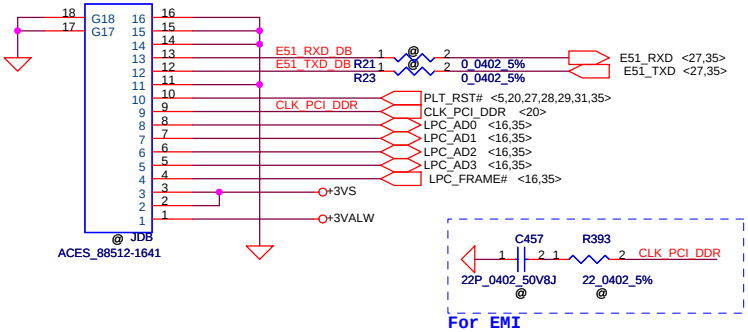
SPI Flash (128KB)

Lid SW

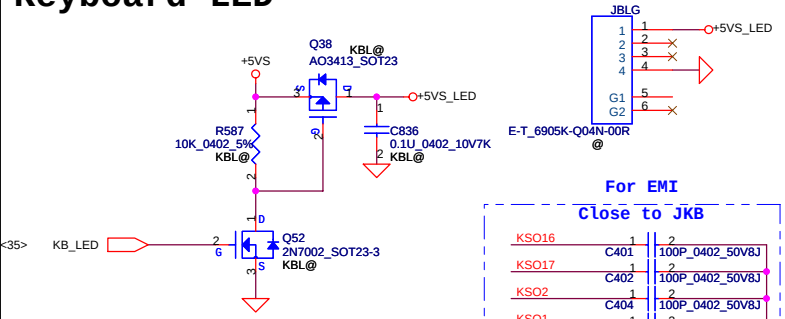


LPC Debug Port

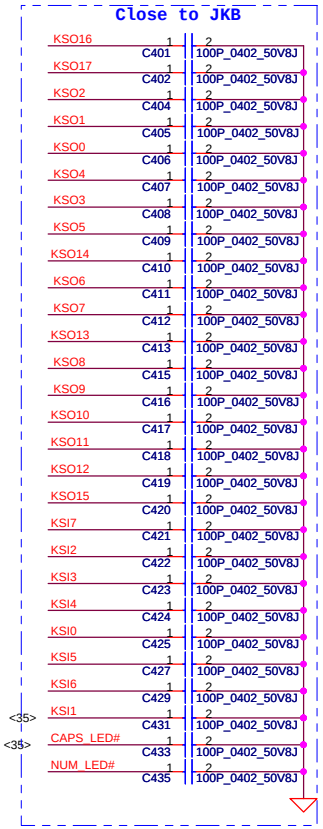
Place the JDB under DDR DIMM.



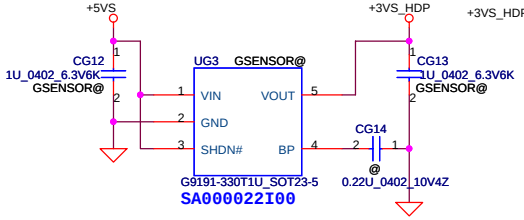
Keyboard LED

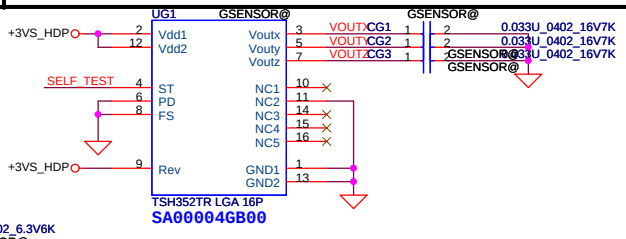


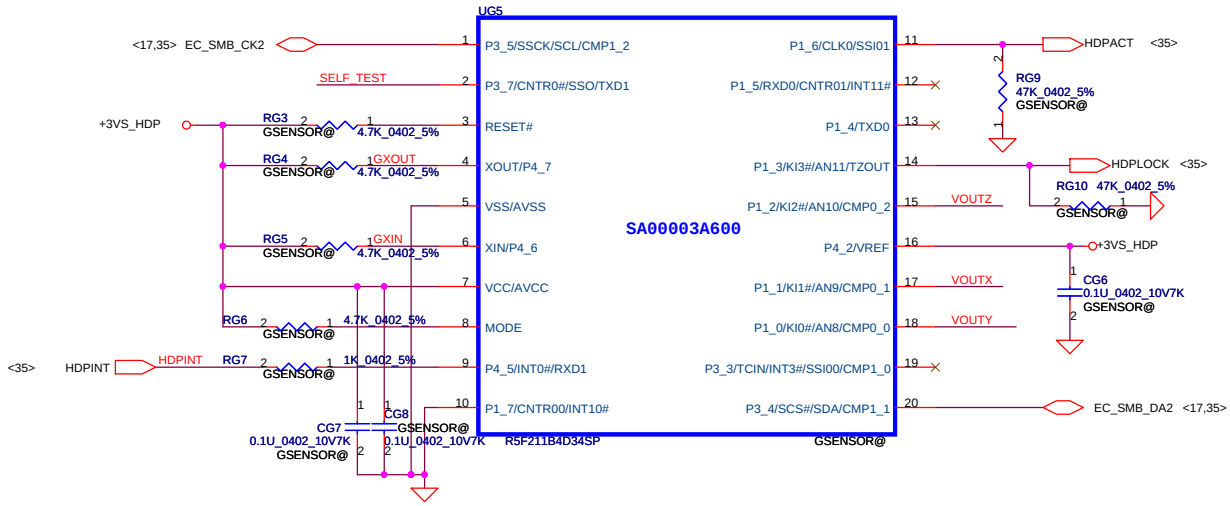
KEYBOARD CONN.



G-Sensor







Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

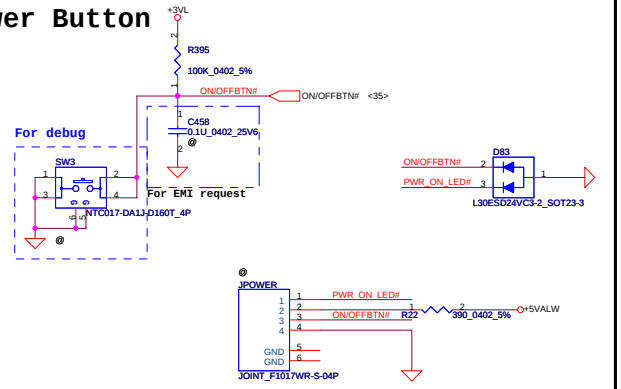
Compal Electronics, Inc.

Title: SCHEMATICS, MB A8392

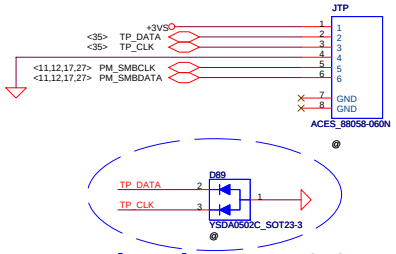
Size | Document Number: 4019HF | Rev: B

Date: Thursday, February 16, 2012 | Sheet 36 of 51

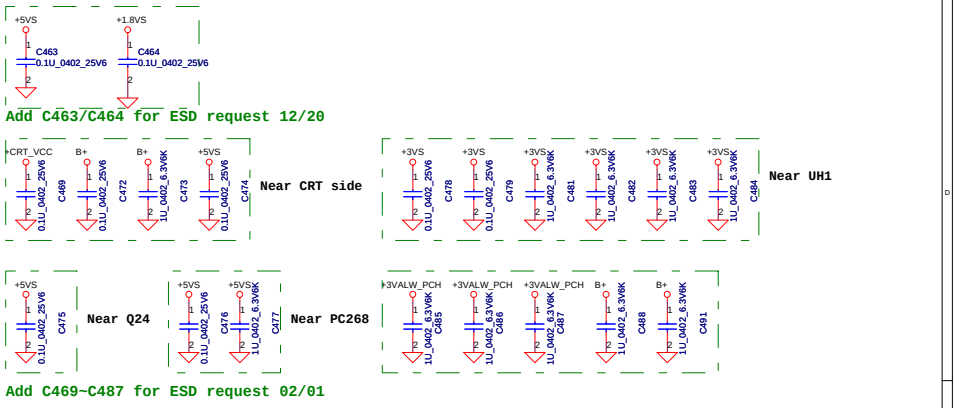
Power Button



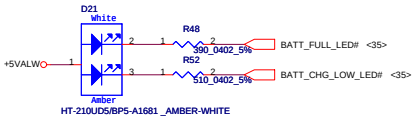
Touchpad Connector



please place near JFUNCTION



BATT CHARGE /FULL LED & AC IN

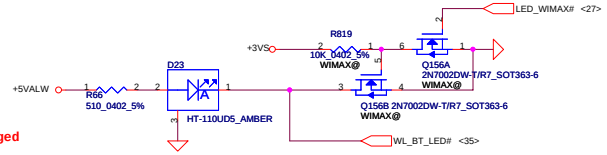


White LED bright when AC-adaptor is plugged and a Battery is full charged

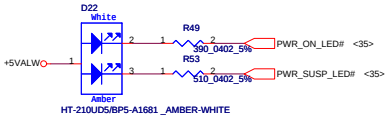
Amber LED bright when charging battery from AC-adaptor

Amber LED blink during Critical Low battery

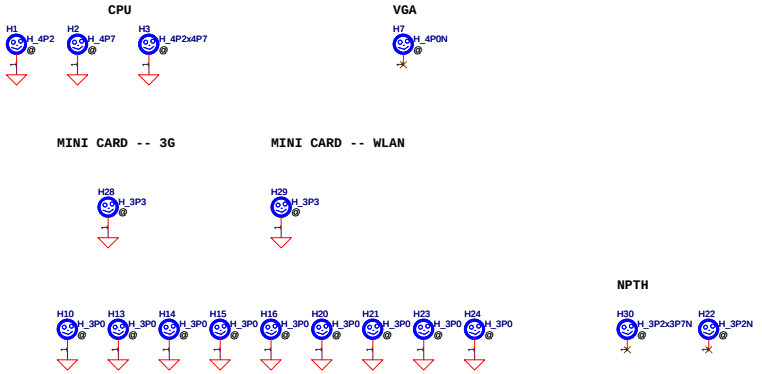
WiMAX LED



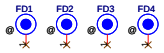
POWER LED



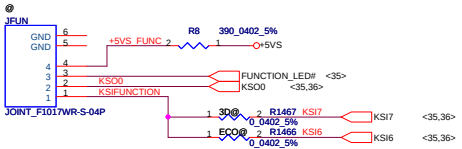
Screw Hole



PCB Fedical Mark PAD

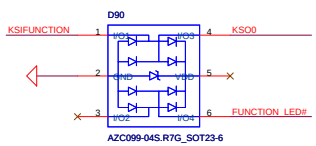


FUNCTION/B Connector



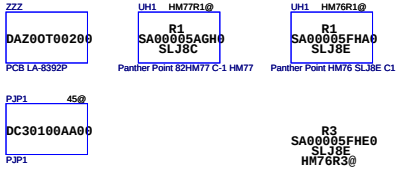
Green LED SC500009S00 VF=2.8V~3.15V, Isink<15mA

White LED SC500004W00 VF=2.75V~3.15V, Isink<15mA



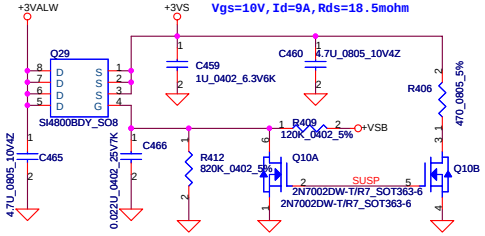
please place near JFUNCTION

ISPD

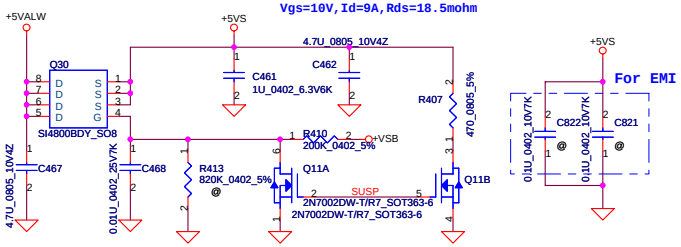


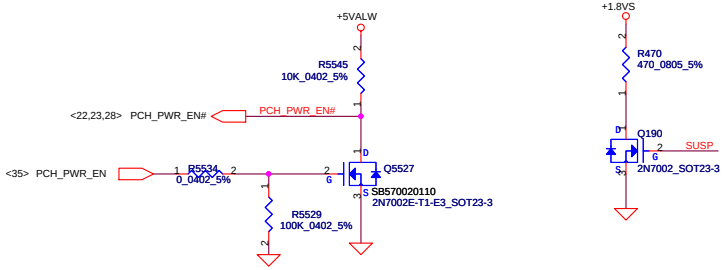
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/12/14	Deciphered Date	2012/12/31
			Title: SCHEMATICS, MB A8392
			Size: Document Number: 4019HF Rev: B
			Date: Thursday, February 16, 2012 Sheet 37 of 51

+3VALW TO +3VS



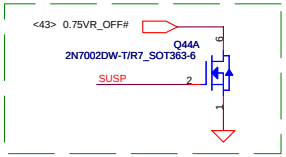
+5VALW TO +5VS



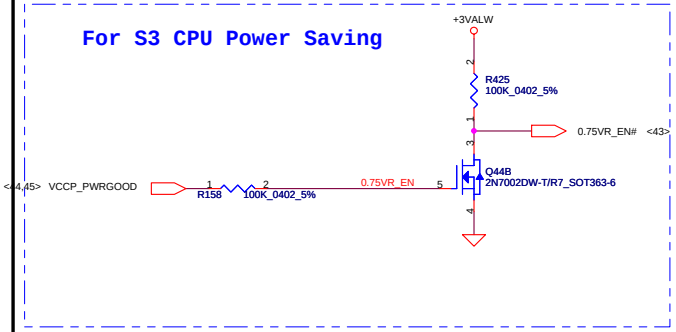


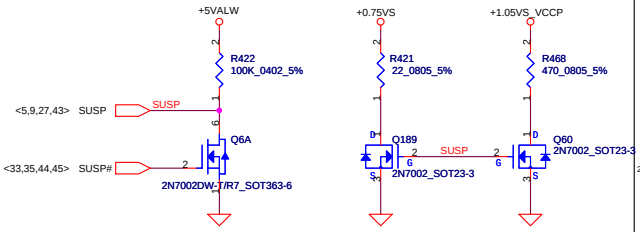
Un-used Dual MOS

Add Q41 for S3 resume problem 12/14



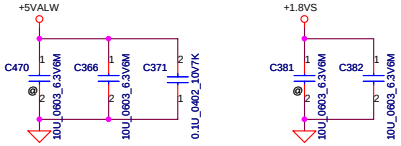
For S3 CPU Power Saving



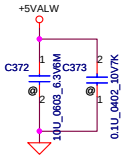


For filter noise

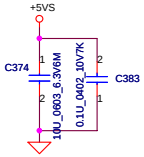
Reserve for SW-node noise
place at noise source



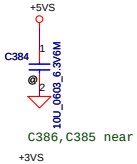
C372,C373 near to PQ352



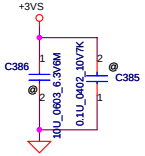
C374,C383 near to
PQ402 and place on TOP



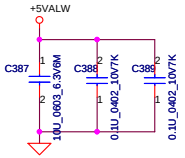
C384 near to RW2



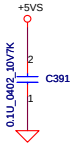
C386,C385 near to PC364



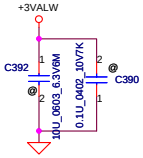
C389 near to Q49
C387,C388 near to D84



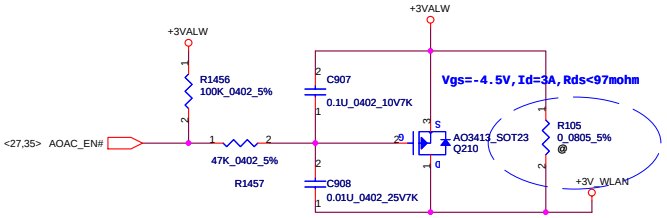
C391 near to CH93



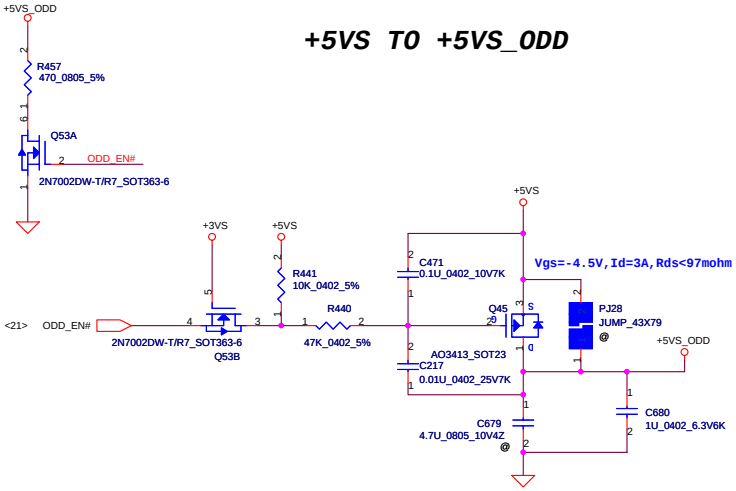
C392,C390 near to PL332



+3VALW TO +3V_WLAN for AOAC and WOWL



+5VS TO +5VS_ODD



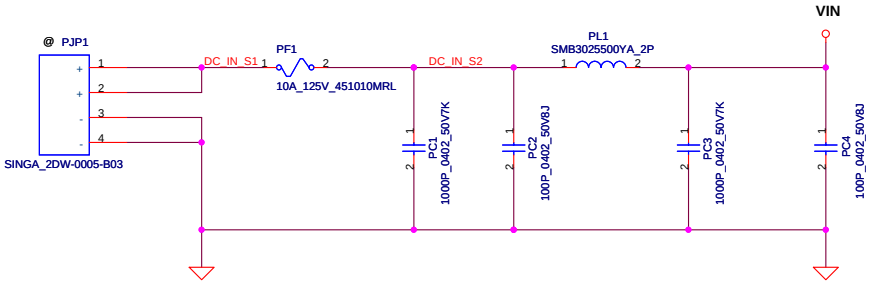
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

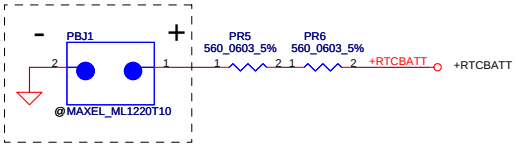
Title: SCHEMATICS, MB A8392

Size	Document Number	Rev
	4019HF	B

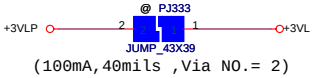
Date: Thursday, February 16, 2012 Sheet 38 of 51



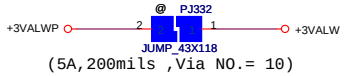
RTC Battery



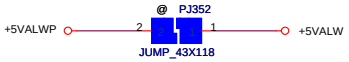
SP093MX0000



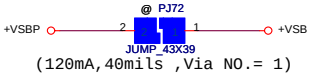
(100mA,40mils ,Via NO.= 2)



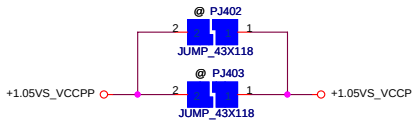
(5A,200mils ,Via NO.= 10)
OCP=6.2A



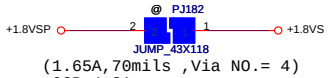
(10.63A,425mils ,Via NO.= 20)
OCP=12.3A



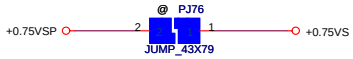
(120mA,40mils ,Via NO.= 1)



(14A,560mils ,Via NO.=28)
OCP=16.92A



(1.65A,70mils ,Via NO.= 4)
OCP=4.2A



(0.5A,40mils ,Via NO.= 1)

(6A, 240mils ,Via NO.= 12)
OCP=9.5A

ACIN

Precharge detector	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: ***SCHEMATICS, MB A8392***

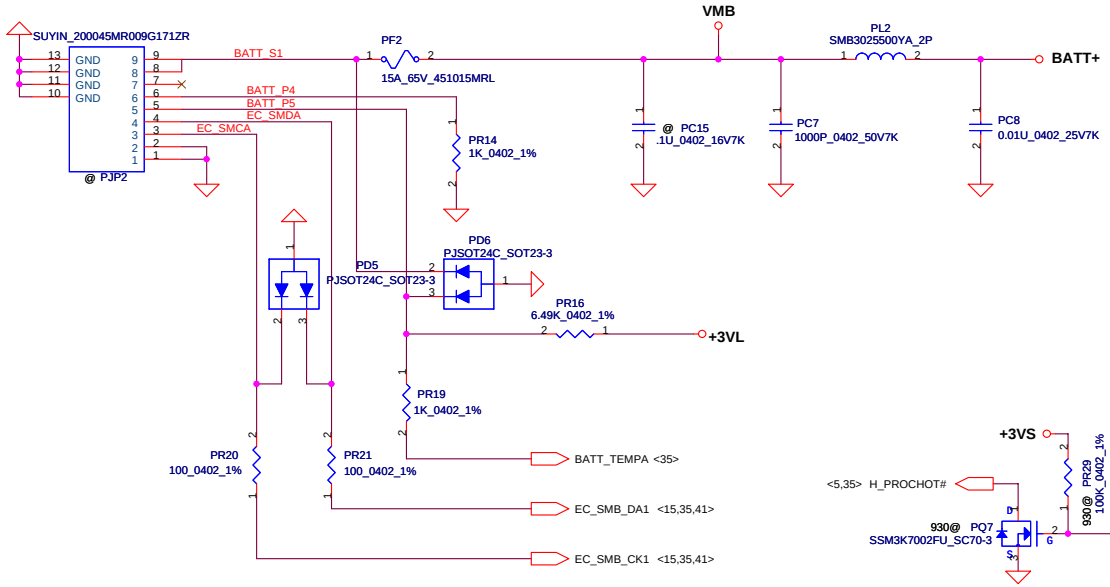
Size: | Document Number: **4019HF** | Rev: B

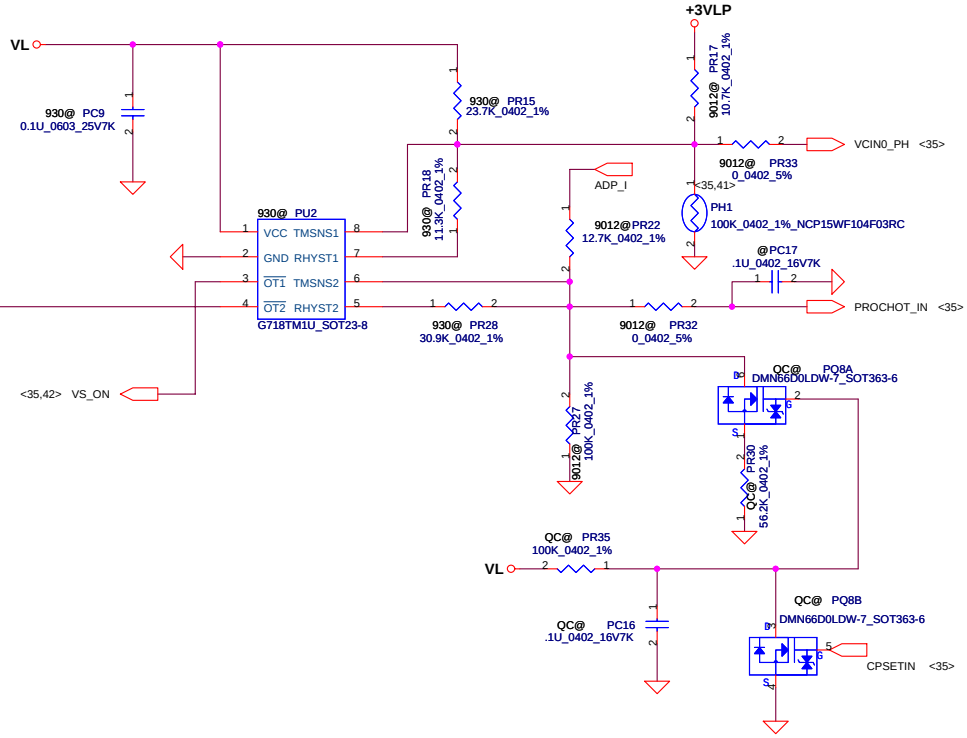
Date: Thursday, February 16, 2012 | Sheet 39 of 51

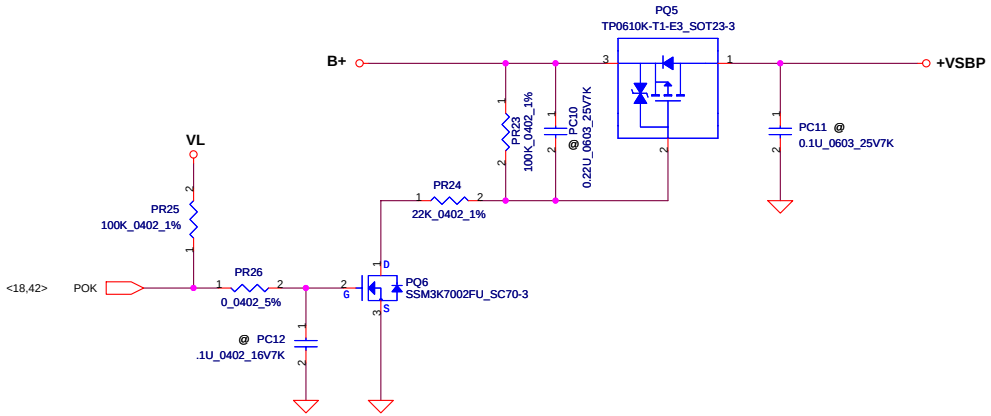
PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 56 degree C

Rset = 3 * Rtmh
Rhyst = (Rset* Rtml) / (3*Rtml - Rset)

Rtmh at 90C = 7.87K, Rtml at 56C = 26.1K
Rset = 3 * 7.87K = 23.61K ==> 23.7K
Rhyst = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K ==> 11.3K







Adaptor protection

Adaptor	Throttling point	ADP_I	Recovery point	ADP_I
90W	113.5W	1.783V	86.4W	1.357V
65W	71.8W	1.504V	62.5W	1.308V

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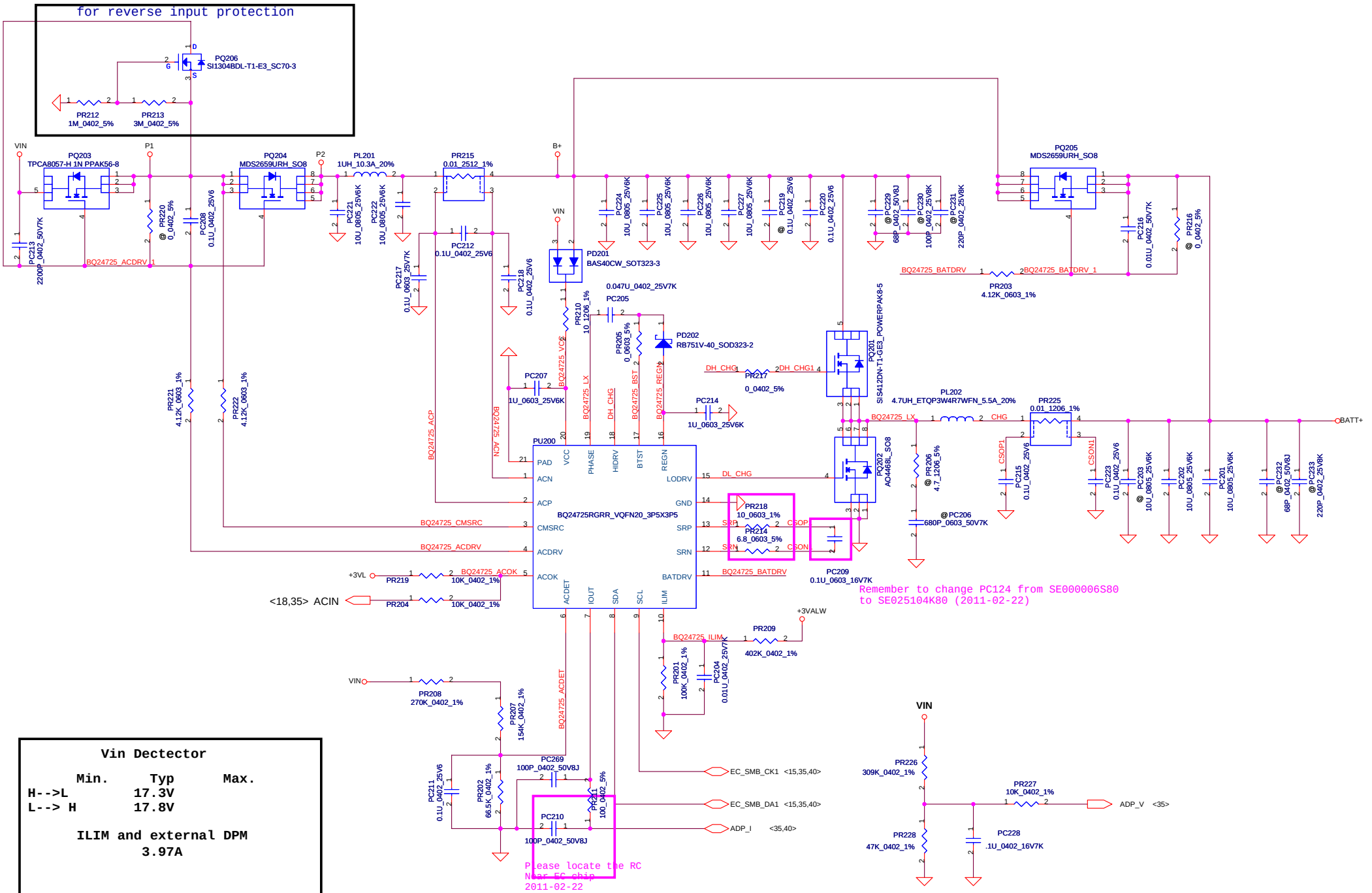
Title: SCHEMATICS, MB A8392

Size | Document Number: 4019HF | Rev: B

Date: Thursday, February 16, 2012 | Sheet 40 of 51



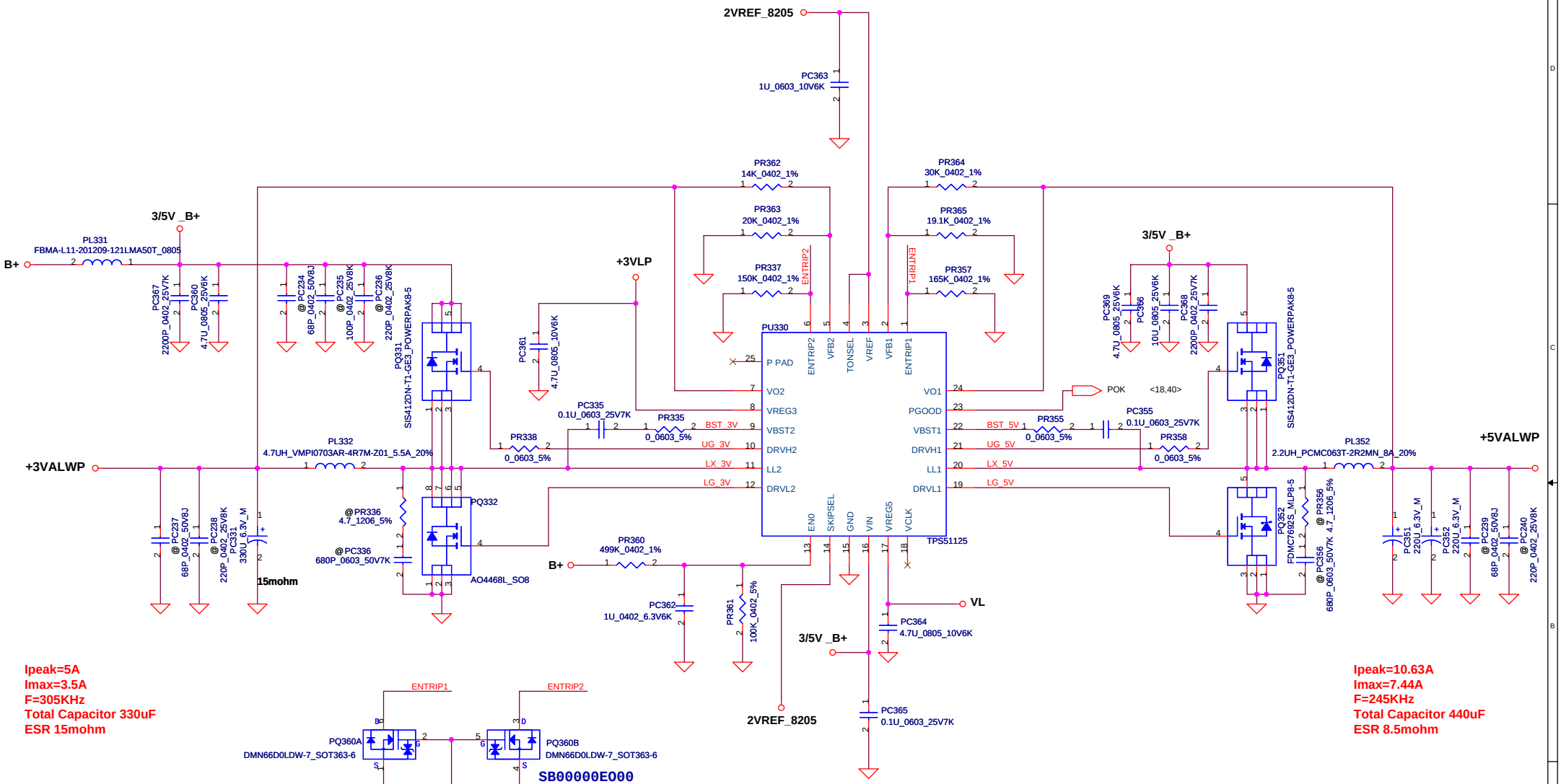
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: SCHEMATICS, MB A8392

Size: Document Number: 4019HF Rev: B

Date: Thursday, February 16, 2012 Sheet 41 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: SCHEMATICS, MB A8392

Size | Document Number: 4019HF | Rev: B

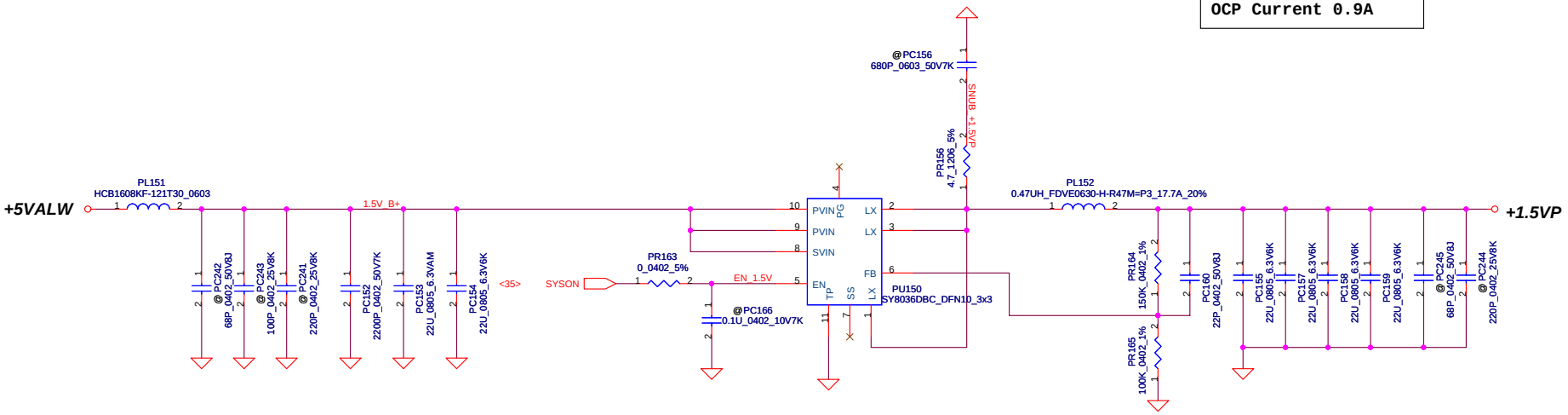
Date: Thursday, February 16, 2012 | Sheet 42 of 51

HW side:
C106 330uF 17m
C218 390uF 10m
VGA@ CV122 390uF 10m
@ C189 330uF 15m

UMA
Ipeak=8.5A
Imax=5.95A
Rtrip=5.9K, OCP=11.338A
F=315KHz
Total Capacitor 1050uF,
ESR 4.43mohm

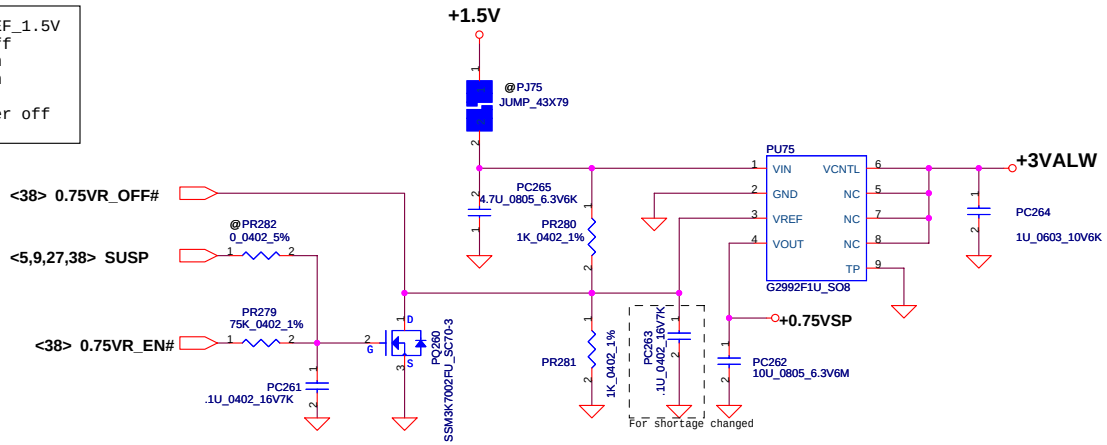
DIS
Ipeak=20A
Imax=14A
Rtrip=14K, OCP=24.136A
F=315KHz
Total Capacitor 1440uF,
ESR 3.07mohm

0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A



Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off



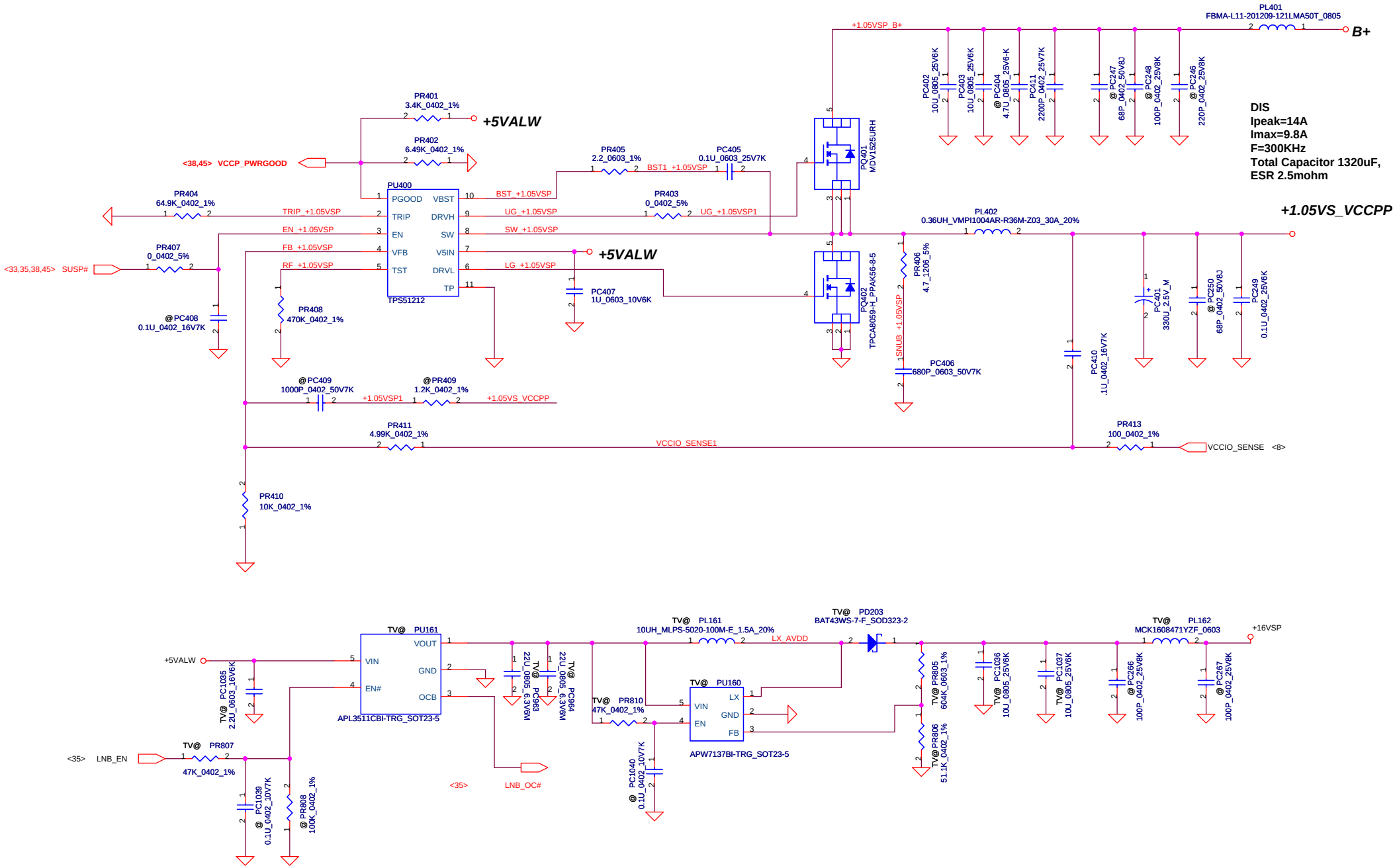
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: SCHEMATICS, MB A8392

Size | Document Number: 4019HF | Rev: B

Date: Thursday, February 16, 2012 | Sheet 43 of 51



Compal Electronics, Inc.

Title: SCHEMATICS, MB A8392

Size: Custom | Document Number: 4019HF | Rev: B

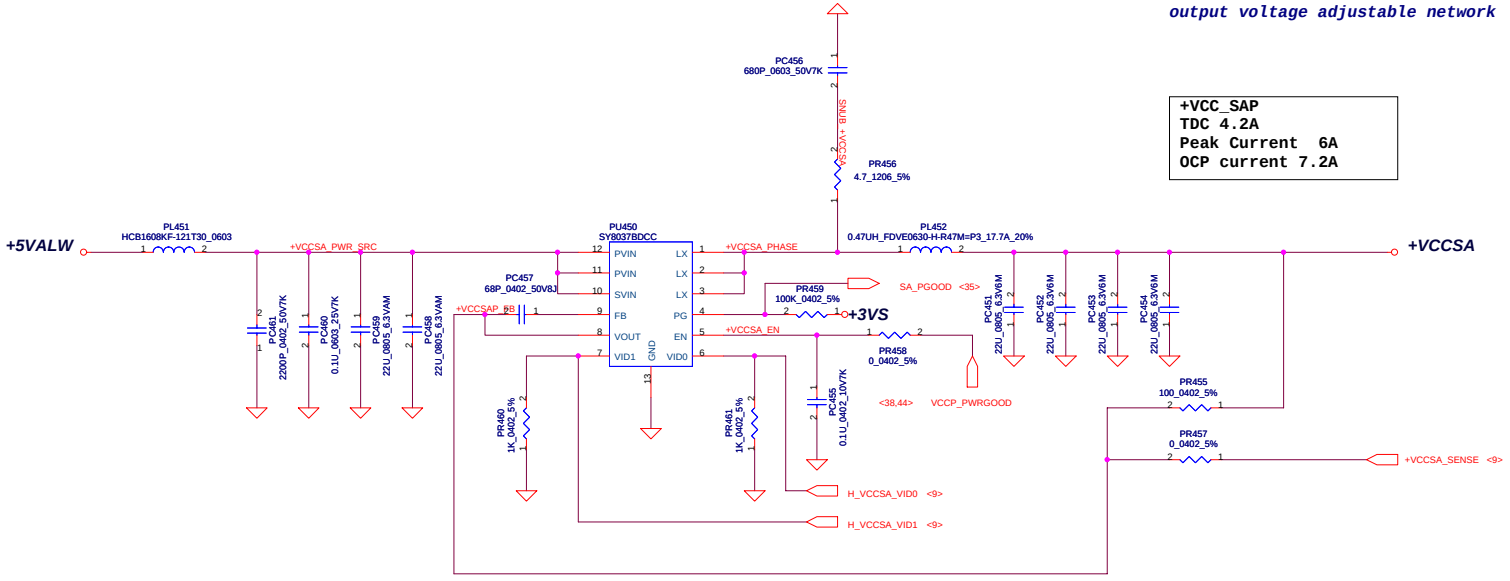
Date: Thursday, February 16, 2012 | Sheet 44 of 51

The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A



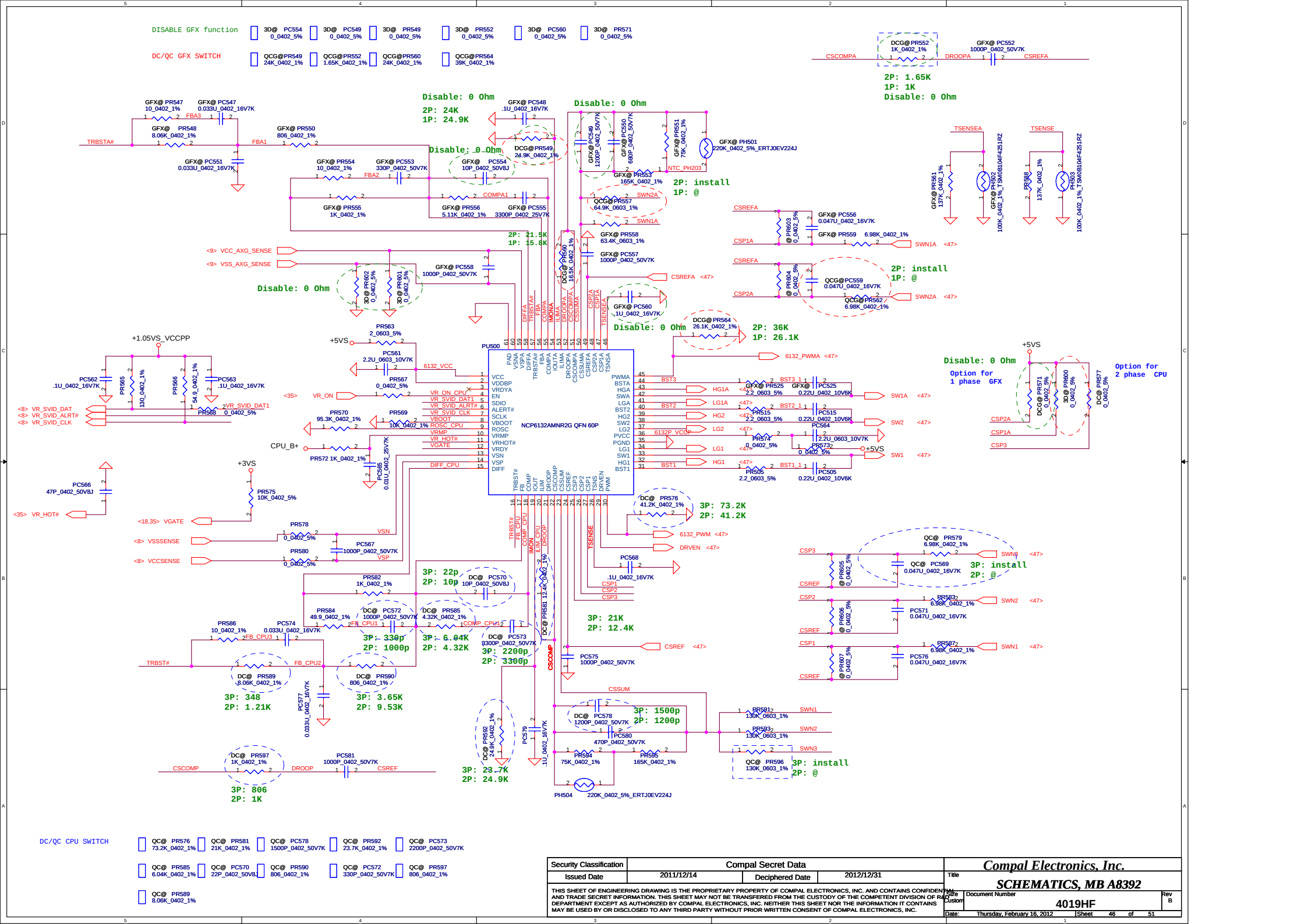
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: SCHEMATICS, MB A8392

Size	Document Number	Rev
C	4019HF	B

Date: Thursday, February 16, 2012 | Sheet 45 of 51

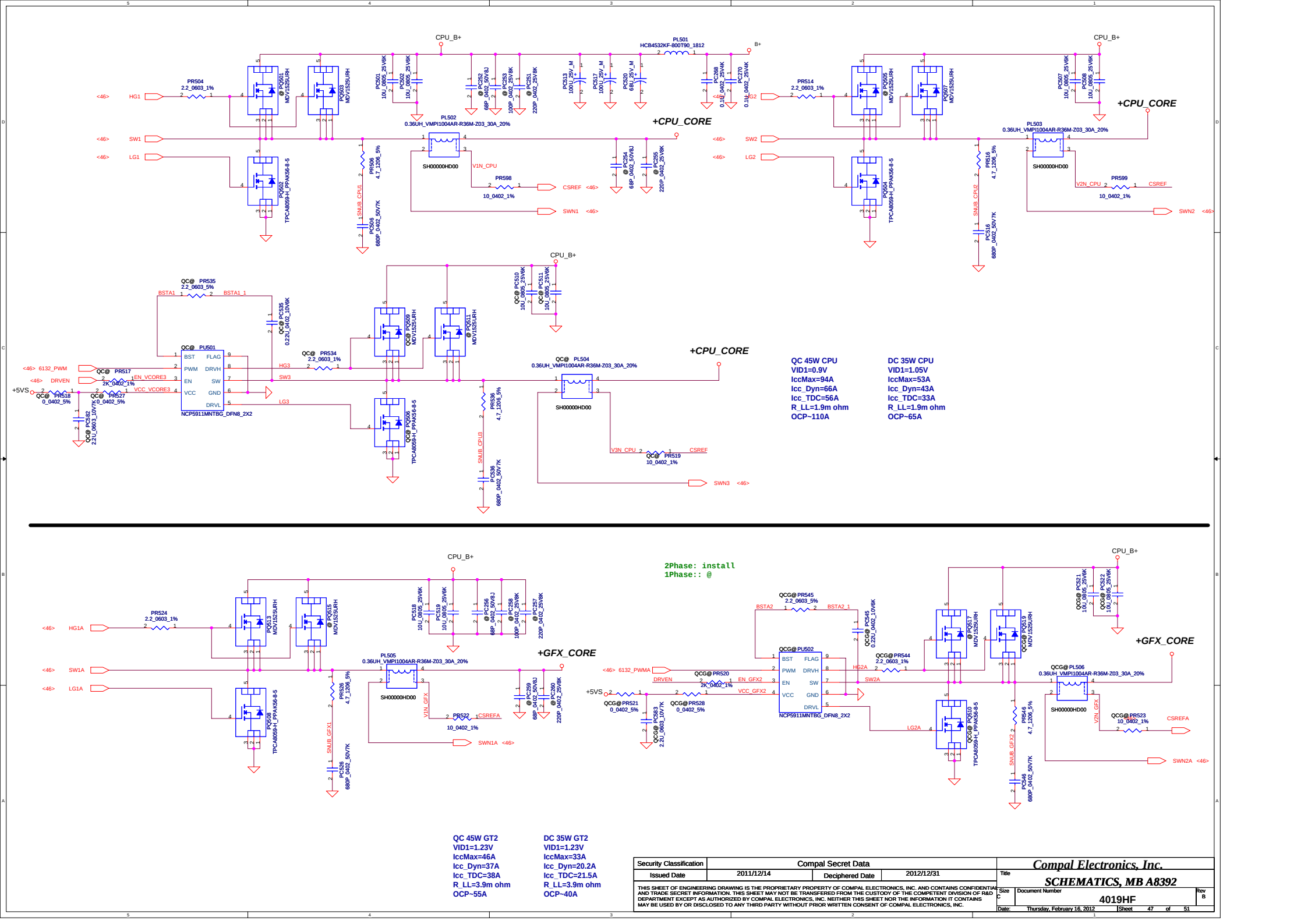


Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: SCHEMATICS, MB A8392

Size: Custom	Document Number: 4019HF	Rev: B
Date: Thursday, February 16, 2012	Sheet 46 of 51	



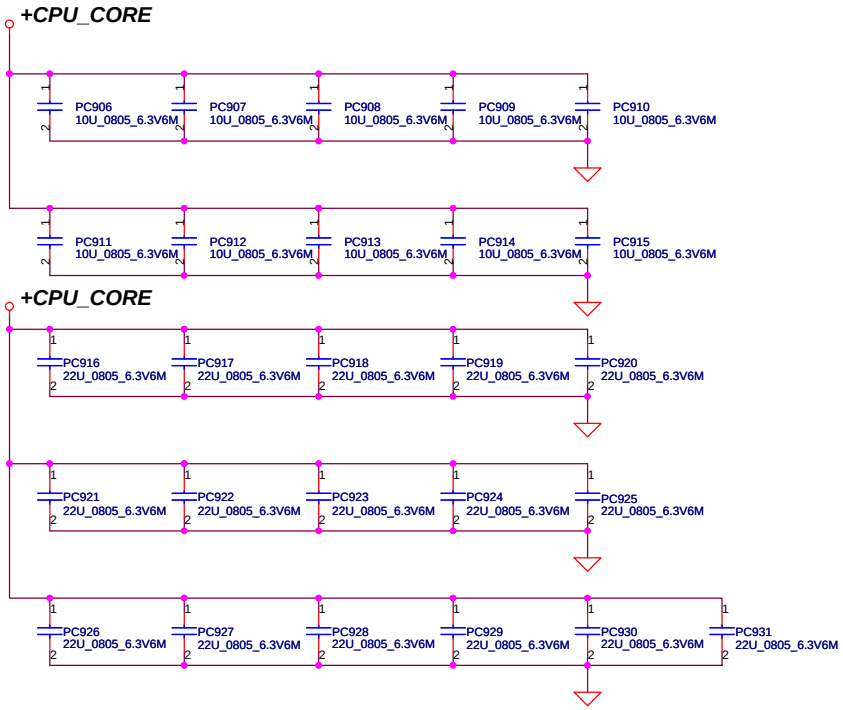
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

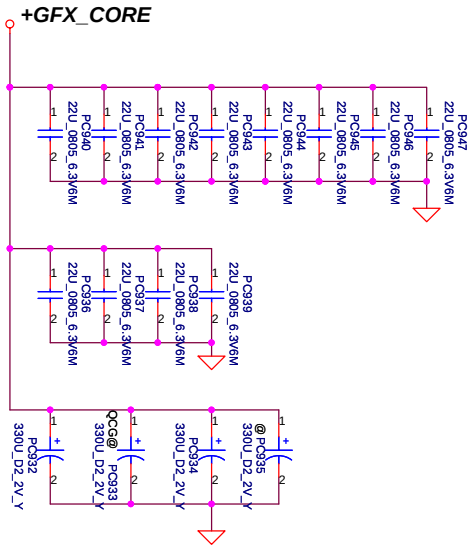
Compal Electronics, Inc.

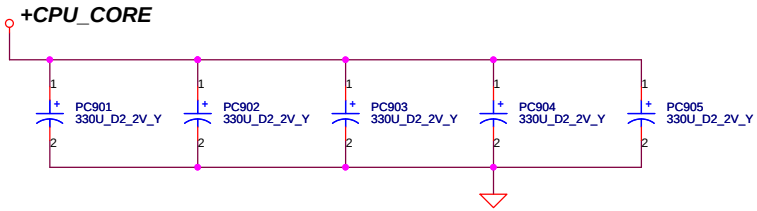
Title: SCHEMATICS, MB A8392

Size	Document Number	Rev
C	4019HF	B

Date: Thursday, February 16, 2012 | Sheet 47 of 51

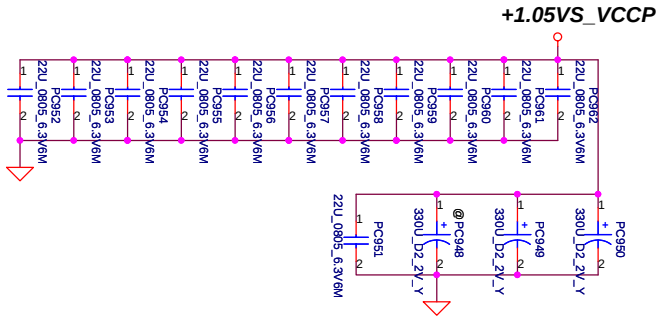






Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: SCHEMATICS, MB A8392

Size | Document Number: 4019HF | Rev: B

Date: Thursday, February 16, 2012 | Sheet 48 of 51

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	2011/09/29	P51-PWR_+3VALWP/+5VALWP	Change PU330 to RT8205L	Change source
2.	2011/09/29	P53-PWR_ +1.05VS_VCCP/+16VSP	Change PU400 to RT8237C	Change source
3.	2011/09/29	P54-PWR_+VCCSAP/1.8VSP	Change PU450 to SY8037B	Change source
4.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change HMOS to MDV1525	Change source
5.	2011/09/29	P53-PWR_ +1.05VS_VCCP/+16VSP	Change HMOS to MDV1525	Change source
6.	2011/09/29	P49-PWR_BATTERY CONN / OTP	Change PD5,PD6 to SCA00001G00	ESD team request
7.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PR589 from 348 to 8.06k	FAE suggestion
8.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PR590 from 3.65k to 806	FAE suggestion
10.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PC574 from 680P to 0.033u	FAE suggestion
11.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PC577 from 4700P to 0.033u	FAE suggestion
12.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PR548 from 1.21k to 8.06k	FAE suggestion
13.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PR550 from 10.7k to 806	FAE suggestion
14.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PC547 from 680P to 0.033u	FAE suggestion
15.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PC551 from 4700P to 0.033u	FAE suggestion
16.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Add snubber and boost resistor	For 3x3 H-MOS solution
17.	2011/09/29	P49-PWR_BATTERY CONN / OTP	Add PR22 30k,PR27 100k, PR32 0 Ohm	For 120W adapter protect(9012)
18.	2011/09/29	P51-PWR_+3VALWP/+5VALWP	Change PC360 to SE000006R80	Change source
19.	2011/09/29	P49-PWR_BATTERY CONN / OTP	Add PR17 14k, PR33 0 Ohm	For CPU temperature protect(9012)
20.	2011/09/29	P51-PWR_+3VALWP/+5VALWP	Add PR373 0 Ohm	For 3/5V always power on(9012)

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Title: ***SCHEMATICS, MB A8392***

Size	Document Number	Rev
Custom	4019HF	B

Date: Thursday, February 16, 2012 | Sheet 49 of 51

HW PIR (Product Improve Record)

QFKAA LA-8392P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2
GERBER-OUT DATE: 2011/11/11

Item	Page	Date	Request	Solution
1)	13	2011/9/29a	by ESD demand	change D84 to SCA00001L00
2)	26	2011/9/29a	by ESD demand	change D82 to SCA00001L00
3)	28	2011/9/29a	by ESD demand	change D92 to SCA00001L00
4)	05	2011/10/05a	follow HW4 check list	reserve decoupling cap CC66, CC71, CC70 for H_PM_SYNC & H_PECI, BUF_CPU_RST#
5)	19	2011/10/05a	by Customer demand	add LVDS dual channel signal
6)	13	2011/10/05a	by Customer demand	add LVDS dual channel signal and 0ohm: R267 R268 R269 R270 R283 R329 R333 R337 (OPTFHD@) and R500 R501 R502 R503 R504 R505 R507 R508 (3D@)
7)	17	2011/10/05a	by Customer demand	change RH116 to HD@ add RH282 FHD@
8)	35	2011/10/18a	discuss with EC	change Function_LED from EC_GPIO4D, PIN86 to EC_GPIO11, PIN25 change HDPLOCK from EC_GPIO11, PIN25 to EC_GPIO4D, PIN86 add GPUPWR_SKIN# on EC_GPIO13, pin27. add RB28 for GPUPWR_SKIN# change HDPACT from EC_GPIO43, PIN76 to EC_GPIO50, PIN89 reserve SUSACK# and PCH_SUSPWRDN# by SW demand
9)	18	2011/10/18a	by SW ME demand.	change PCH_SUSPWRDN_R to PCH_SUSPWRDN#_R add PCH_SUSPWRDN# to EC and RH132 remove T75 change SUSACK# to SUSACK#_R add RH133 and SUSACK# to EC
10)	30	2011/10/31a	by Layout demand	swap LR2, LR1, DR7
11)	32	2011/10/31a	by Layout demand	swap LT3, LT2
12)	20	2011/10/31a	by PWR 16V OC control demand	remove RH1, RH174, and change net-name from LNBPWR_MONITOR to LNB_OC
13)	37	2011/11/1a	new touch pad add new function	add JTP connector Pin 5 (PM_SMBCLK) , Pin6 (PM_SMBDATA)
14)	27	2011/11/1a	TV tuner(BCAS) 16V reserve	add RM15 and RM16 reserve for TV tuner (BCAS)
15)	33	2011/11/1a	avoid SM_EN floating	reserve RA43 for SM_EN 100K pull down reserve
16)	33	2011/11/1a	for vendor request	exchange location of RA28 and CA42
17)	33	2011/11/1a	for vendor request	RA26 pin2 change name from OSC_IN to OSC_OUT
18)	33	2011/11/1a	for vendor request, S&M HP need shut down	delete DA1. add RA19 ,QA5 ,RA42 ,
19)	23	2011/11/1a	for lot6 0.5W power consumption	delete CH57, PJ3 then add PJ5, QH6 ,CH59 , RH228
20)	38	2011/11/2a	for lot6 0.5W power consumption	add R5545, Q5527, R5529, R5534
21)	23	2011/11/2a	for lot6 0.5W power consumption	reserve RH228
22)	37	2011/11/2a	for lot6 0.5W power consumption	change D21 power from +5VL to +5VALW
23)	27	2011/11/6a	by EMI demand	add CCL10
24)	28	2011/11/6a	by EMI demand	add CL43, RL29
25)	29	2011/11/6a	by EMI demand	change RW4 from 0ohm to 33ohm, CW10 from 5pF to 6.8pF
26)	25	2011/11/7a	common with ME define location	change JUSB3RR to JUSBRR, JUSB3RF to JUSBRF
27)	30	2011/11/7a	common with ME define location	change JUSB3LR to JUSBLR, JUSB3LF to JUSBLF
28)	27	2011/11/7a	common with ME define location	change J3GTV to JPCIF
29)	37	2011/11/7a	common with ME define location	change JFUNCTION to JFUN
30)	22	2011/11/7a	for lot6 0.5W power consumption	delete CH105, CH106; add QH2, CH97, CH98, RH1, RH3
31)	35	2011/11/7a	for lot6 0.5W power consumption	add EC pin 70 for PCH_PWR_EN
32)	37	2011/11/7b	by proto plan demand	change PCH version to SA00004NQ90(B0) and BOM option to SA00005AG10(C0)
33)	20	2011/11/7b	by PWR 16V OC control demand	change net name from LNB_OC to LNB_OC#; add RH290 to pull high LNB_OC#
34)	37	2011/11/7b	by Layout team demand	delete H4, H8; modify H7, H22, H30 to NPTH
35)	20	2011/11/9a	EC common core for WL_OFF#	UH1.F46 and RH326 chagne net name from WL_OFF# to PCH_GPIO55
36)	35	2011/11/9a	EC common core for WL_OFF#	change UB1.29 net name from CPSETIN to WL_OFF#
37)	27	2011/11/9a	EC common core for WL_OFF#	add RM17 for WL_OFF# pull high to +3V_WLAN
38)	35	2011/11/9a	EC common core for WL_OFF#	CPSETIN signal change from UB1.29 to UB1.74
39)	35	2011/11/9a	by PWR 16V OC control demand	add RB37 10kohm pull high to +3VS for LNB_OC#
40)	13	2011/11/9d	for dual-channel power support	remove BOM selection IEDP@ for R109, R110, C230, C233, Q1
41)	13	2011/11/9d	for dual-channel power support	change R108, C228, Q17 to LVDS@; change Q1, C230, C233, R109, R110 to always mount
42)	13	2011/11/9d	for dual-channel power support	add R390, R1442, R1441, R106
43)	13	2011/11/9d	for dual-channel power support	change R106 to LVDS@, R1441 to @, R361 to @, R1442 to 3D@, R390 to @
44)	13	2011/11/9d	for 3D panel camera	add R79, R97, L60
45)	13	2011/11/9d	for dual-channel power support	add R361; change R62 from 100 to 0
46)	21	2011/11/9d	for dual-channel power support	add RH304
47)	27	2011/11/14a	for vendor recommand	change YCL1 from SJ10000CU00 to SJ10000EF00, CCL4 and CCL5 from 30pF to 15pF
48)	29	2011/11/15a	by EMI demand	change CW10 from 6.8pF to 5pF
49)	27	2011/11/15d	by EMI demand	change BOM structure of CCL10 from @ to GCLK@
50)	28	2011/11/15d	by EMI demand	change BOM structure of RL29, CL43 from @ to GCLK@

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/12/14	Deciphered Date 2012/12/31	Title: SCHEMATICS, MB A8392

Size: Custom	Document Number: 4019HF		Rev: B
Date: Thursday, February 16, 2012	Sheet 50 of 51		

HW PIR (Product Improve Record)

QFKAA LA-8392P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3
GERBER-OUT DATE: 2011/12/22

Item	Page	Date	Request	Solution
1)	18	2011/11/29a	For DVT hang	Add CH23 CH24 CH25 for SW-node noise.
2)	13	2011/11/29a	For ME request	Change location from JLVDS to JLVDS4
3)	38	2011/11/29a	For noise issue	Add C366, C470 at +5VALW power rail; add C381 at +1.8VS power rail
4)	05	2011/12/07a	For leakage	Change from +3VALW to +3VALW_PCH of UC1
5)	38	2011/12/07a	For design change	Add C382 for +1.8VS
6)	33	2011/12/13a	For Codec leakage	Add RA29 for leakage
7)	18	2011/12/13a	For noise issue	Mount CH23,CH24,CH25.
8)	05	2011/12/13a	For leakage	Change pin5 of UC1 from +3VALW to +3VALW_PCH
9)	15	2011/12/13a	For leakage issue	Change pin5 of U9 from +5VL to +HDMI_5V_OUT
10)	38	2011/12/13a	For noise issue	Add C372,C373,C374,C383,C384,C385,C386,C387,C388,C389,C390,C391,C392
11)	35	2011/12/13a	For design change LNB_EN	Change LNB_EN from PCH to EC
12)	35	2011/12/13a	For design change RF LED	Change RF LED control pin from PCH to EC
13)	38	2011/12/13a	For S3 resume sequence	Add Q41 for S3 sequence
14)	26	2011/12/15a	For ME request	Change JFP/JPOWER/JFUN from zif to non-zif
15)	31	2011/12/15a	For adjust EXT 3.0 sequence	Change +3V to +3V_USB control pin from syson to PM_SLP_S4#
16)	32	2011/12/15a	For adjust EXT 3.0 sequence	Change +3V to +3V_USB control pin from syson to PM_SLP_S4#
17)	13	2011/12/17a	For Prevent LVDS burn issue	Add F3 (Poly fuse to prevent burn issue)
18)	37	2011/12/19a	For ME delete stand-off	Delete H25,H26,H27
19)	37	2011/12/19a	For Wimax flash issue	Change +5VS to +3VS of Wimax LED
20)	37	2011/12/19a	For layout request	Add net name +5VS_FUNC with Function conn power pin
21)	21	2011/12/22a	For ESD request	Reserve CH30(1000P) for PCH_THRMTRIP#
22)	13	2011/12/22a	For ME request	change C381, C382, C470, C366 from 0805 to 0603 size

QFKAA LA-8392P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0
GERBER-OUT DATE: 2012/02/02

Item	Page	Date	Request	Solution
1)	27	2012/01/12a	For GCLK	Add CCL13(0.1u) for +3VALW
2)	27	2012/01/12a	For MSATA pin define.	Add RM30 (MSATA define that Pin22 is reserve, so other function need to add PLT_RST#).
3)	27	2012/01/18a	For GLCK	Change CCL13 from +3VLAW to +3VALW_GCLK
4)	27	2012/01/30a	For TV tuner use PCIE interface	Add RM31~RM35 and QM2
5)	17	2012/01/30a	For TV tuner use PCIE interface	Change PCIE 6 from USB to TV tuner
6)	17	2012/01/30a	For TV tuner use PCIE interface	Change CLK_USB30 to CLK_TV and CLKREQ_USB30# to CLKREQ_TV#
7)	37	2012/01/30a	For MP	Unmount SW3
8)	11	2012/01/30a	For M1 only	Unmount RC117/RC118/QC7/QC8
9)	32	2012/01/30a	For Internal USB30 only	Delete Page 32
10)	37	2012/02/01a	For ESD request	Add C469, C472~C479, C481~C488, C491

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Title: *SCHEMATICS, MB A8392*			
Size: Custom	Document Number: 4019HF		Rev: B
Date: Thursday, February 16, 2012	Sheet 51 of 51		