

HAZ00/HTW01

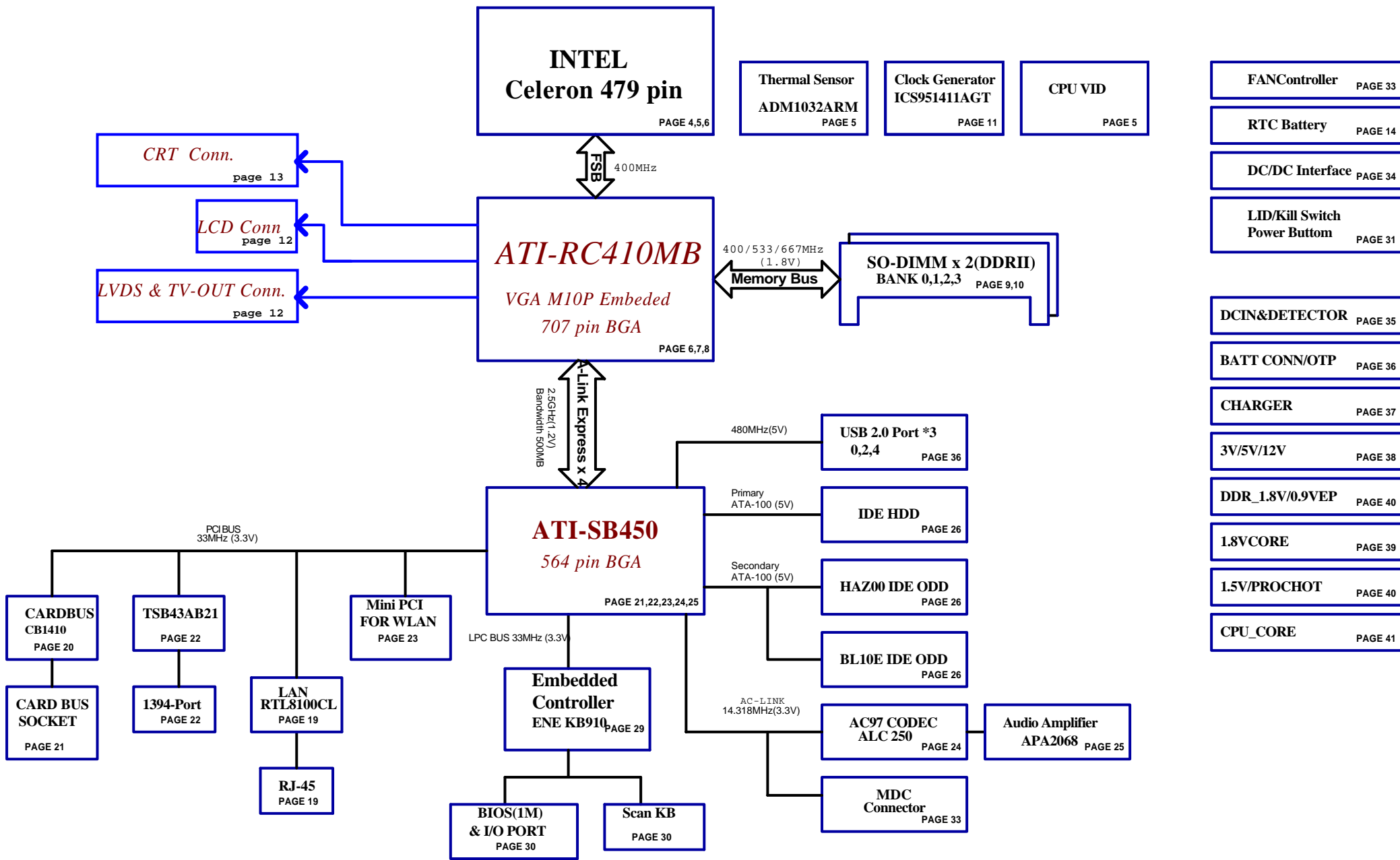
LA-2861 REV 1.0 Schematic

UFC-PGA Dothan/ RC410MD(RC410MB) / SB450

2005-07-11 Rev.1.0

| | | | | | | |
|--|---------------------------|-----------------|------------|--------------------------|----------------------|-----|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | | |
| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 | Title | Black Diagram | |
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| | | | | B | HAZ00/BL10E (LA2861) | 1.0 |
| Date: | Thursday, August 04, 2005 | | | Sheet | 1 of 42 | |

HAZ00 & HTW01 LA-2861 FUNCTION BLOCK DIAGRAM



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| | | | | | |
|---|------------|--------------------|------------|--------------------------|---------------------------|
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| | | | | Rev | 1.0 |

Voltage Rails

| Power Plane | Description | S1 | S3 | S5 |
|-------------|---|----|-----|-----|
| VIN | Adapter power supply (19V) | ON | ON | ON |
| B+ | AC or battery power rail for power circuit. | ON | ON | ON |
| +CPU_CORE | Core voltage for CPU | ON | OFF | OFF |
| +CPUVID | 1.2V switched power rail for CPU AGTL Bus | ON | OFF | OFF |
| +VGA_CORE | 1.0V/1.2V switched power rail for VGA chip | ON | OFF | OFF |
| +1.2VS | 1.2VS for PCI-Express | ON | OFF | OFF |
| +0.9VS | 0.9V switched power rail | ON | OFF | OFF |
| +1.5VS | DOTHAN B | ON | OFF | OFF |
| +1.8VS | 1.8VS switched power rail | ON | OFF | OFF |
| +1.8VALW | 1.8V always on power rail | ON | ON | ON* |
| +1.8V | 1.8V power rail | ON | ON | OFF |
| +3VALW | 3.3V always on power rail | ON | ON | ON* |
| +3VS | 3.3V switched power rail | ON | OFF | OFF |
| +5VALW | 5V always on power rail | ON | ON | ON* |
| +5VS | 5V switched power rail | ON | OFF | OFF |
| +12VALW | 12V always on power rail | ON | ON | ON* |
| +RTCVCC | RTC power | ON | ON | ON |
| | | | | |

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

| Device | IDSEL# | REQ#/GNT# | Interrupts |
|----------------|--------|-----------|-------------|
| TI 1410 | AD20 | 2 | PIRQA/PIRQB |
| LAN | AD22 | 1 | PIRQG |
| Mini-PCI(WLAN) | AD18 | 3 | PIRQF/PIRQG |
| 1394 | AD16 | 0 | PIRQA |

EC SM Bus1 address

| Device | Address | Device | Address |
|---------------|-------------|---------|-------------|
| Smart Battery | 0001 011X b | ADM1032 | 1001 110X b |

EC SM Bus2 address

SB450 SM Bus address

| Device | Address |
|-------------------------------------|---------------|
| Clock Generator (ICS951413BGLFT) | 1101 001Xb |
| DDR DIMM0 | 1010 0100b A4 |
| DDR DIMM1 | 1010 0110b A6 |

| STATE | SIGNAL | SLP_S3# | SLP_S5# | +VALW | +V | +VS | Clock |
|----------------------|--------|---------|---------|-------|-----|-----|-------|
| Full ON | | HIGH | HIGH | ON | ON | ON | ON |
| S1(Power On Suspend) | | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | | LOW | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | | LOW | LOW | ON | OFF | OFF | OFF |

Board ID Table for AD channel

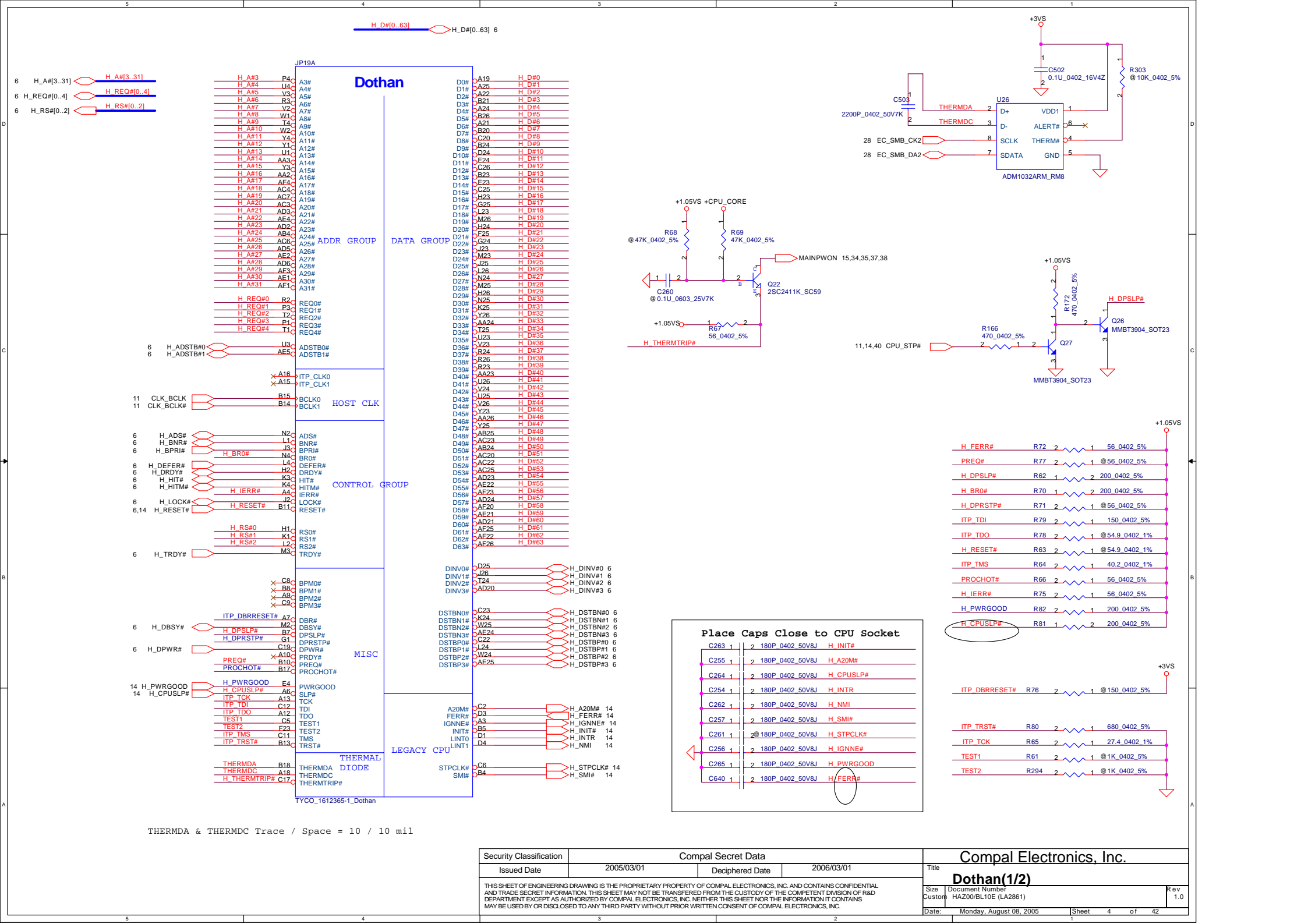
| Vcc | 3.3V +/- 5% | | | |
|----------|-------------|-------------|-------------|-------------|
| Ra | 100K +/- 5% | | | |
| Board ID | Rb | VAD_BID min | VAD_BID typ | VAD_BID max |
| 0 | 0 | 0 V | 0 V | 0 V |
| 1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V |
| 2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V |
| 3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V |
| 4 | 56K +/- 5% | 1.036 V | 1.185 V | 1.264 V |
| 5 | 100K +/- 5% | 1.453 V | 1.650 V | 1.759 V |
| 6 | 200K +/- 5% | 1.935 V | 2.200 V | 2.341 V |
| 7 | NC | 2.500 V | 3.300 V | 3.300 V |

| Board ID | PCB Revision |
|----------|--------------|
| 0 | 0.1, 0.2 |
| 1 | 0.3 |
| 2 | 1.0 |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | |

| SKU ID | SKU Status |
|--------|------------|
| 0 | |
| 1 | |
| 2 | |
| 3 | |
| 4 | |
| 5 | 1 Buttons |
| 6 | |
| 7 | 7 Buttons |

| | HDD Password |
|---|--------------|
| 0 | NO |
| 1 | Yes |

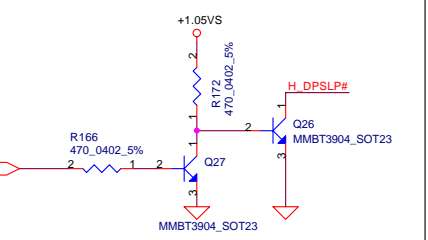
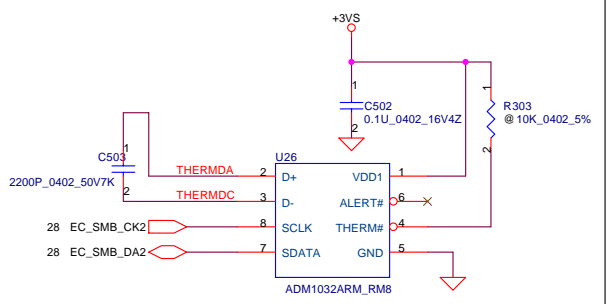
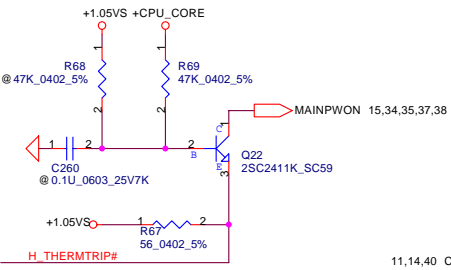
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| Date: | Thursday, August 04, 2005 | Sheet | 3 | of | 42 |



H_D#[0..63] H_D#[0..63] 6

6 H_A#[3..31] H_A#[3..31]
 6 H_REQ#[0..4] H_REQ#[0..4]
 6 H_RS#[0..2] H_RS#[0..2]

| Pin | Signal | Group |
|-------|---------------|---------------|
| P4 | H_A#3 | ADDR GROUP |
| A3# | H_A#4 | ADDR GROUP |
| R3C | H_A#5 | ADDR GROUP |
| A4# | H_A#6 | ADDR GROUP |
| A5# | H_A#7 | ADDR GROUP |
| A6# | H_A#8 | ADDR GROUP |
| W1C | H_A#9 | ADDR GROUP |
| A8# | H_A#10 | ADDR GROUP |
| T4 | H_A#11 | ADDR GROUP |
| A9# | H_A#12 | ADDR GROUP |
| Y4 | H_A#13 | ADDR GROUP |
| A10# | H_A#14 | ADDR GROUP |
| A11# | H_A#15 | ADDR GROUP |
| A12# | H_A#16 | ADDR GROUP |
| A13# | H_A#17 | ADDR GROUP |
| A14# | H_A#18 | ADDR GROUP |
| A15# | H_A#19 | ADDR GROUP |
| A16# | H_A#20 | ADDR GROUP |
| A17# | H_A#21 | ADDR GROUP |
| A18# | H_A#22 | ADDR GROUP |
| A19# | H_A#23 | ADDR GROUP |
| A20# | H_A#24 | ADDR GROUP |
| A21# | H_A#25 | ADDR GROUP |
| A22# | H_A#26 | ADDR GROUP |
| A23# | H_A#27 | ADDR GROUP |
| A24# | H_A#28 | ADDR GROUP |
| A25# | H_A#29 | ADDR GROUP |
| A26# | H_A#30 | ADDR GROUP |
| A27# | H_A#31 | ADDR GROUP |
| A28# | H_A#32 | ADDR GROUP |
| A29# | H_A#33 | ADDR GROUP |
| A30# | H_A#34 | ADDR GROUP |
| A31# | H_A#35 | ADDR GROUP |
| R2C | H_REQ#0 | DATA GROUP |
| REQ0# | H_REQ#1 | DATA GROUP |
| P3C | H_REQ#2 | DATA GROUP |
| T2C | H_REQ#3 | DATA GROUP |
| REQ2# | H_REQ#4 | DATA GROUP |
| P1C | H_REQ#5 | DATA GROUP |
| REQ3# | H_REQ#6 | DATA GROUP |
| T1C | H_REQ#7 | DATA GROUP |
| REQ4# | H_REQ#8 | DATA GROUP |
| U3C | H_ADSTB#0 | CONTROL GROUP |
| AE5C | H_ADSTB#1 | CONTROL GROUP |
| A16 | ITP_CLK0 | CONTROL GROUP |
| A15 | ITP_CLK1 | CONTROL GROUP |
| B15 | BCLK0 | HOST CLK |
| B14 | BCLK1 | HOST CLK |
| N2C | ADS# | CONTROL GROUP |
| L1C | BNR# | CONTROL GROUP |
| J3C | BPR# | CONTROL GROUP |
| N4C | BRO# | CONTROL GROUP |
| H2C | DEFER# | CONTROL GROUP |
| K3C | DRDY# | CONTROL GROUP |
| K4C | HIT# | CONTROL GROUP |
| A4C | H_IERR# | CONTROL GROUP |
| J2C | IERR# | CONTROL GROUP |
| B11C | LOCK# | CONTROL GROUP |
| B11C | H_RESET# | CONTROL GROUP |
| B11C | RESET# | CONTROL GROUP |
| H1C | H_RS#0 | MISC |
| K1C | H_RS#1 | MISC |
| L2C | H_RS#2 | MISC |
| M3C | TRDY# | MISC |
| C8C | BPM#0 | MISC |
| B8C | BPM#1 | MISC |
| A9C | BPM#2 | MISC |
| C9C | BPM#3 | MISC |
| A7C | ITP_DBRRESET# | MISC |
| M2C | DBR# | MISC |
| G1C | H_DPUSLP# | MISC |
| B7C | H_DPRSTP# | MISC |
| C19C | DPRSTP# | MISC |
| C19C | DPWR# | MISC |
| A10C | PRDY# | MISC |
| B10C | PREQ# | MISC |
| B17C | PROCHOT# | MISC |
| E4C | H_PWRGOOD | MISC |
| A6C | H_CPUSLP# | MISC |
| A13C | ITP_TCK | MISC |
| C12C | ITP_TDI | MISC |
| A12C | ITP_TDO | MISC |
| C5C | TEST1 | MISC |
| F23C | TEST2 | MISC |
| C11C | ITP_TMS | MISC |
| B13C | ITP_TRST# | MISC |
| E4C | PWRGOOD | MISC |
| A6C | SLP# | MISC |
| A13C | TCK | MISC |
| C12C | TDI | MISC |
| A12C | TDO | MISC |
| C5C | TEST1 | MISC |
| F23C | TEST2 | MISC |
| C11C | TMS | MISC |
| B13C | TRST# | MISC |
| C2C | A20M# | LEGACY CPU |
| D3C | FERR# | LEGACY CPU |
| B5C | IGNNE# | LEGACY CPU |
| D1C | INIT# | LEGACY CPU |
| LINT0 | LINT0 | LEGACY CPU |
| LINT1 | LINT1 | LEGACY CPU |
| D4C | H_NMI | LEGACY CPU |
| C6C | H_STPCLK# | LEGACY CPU |
| B4C | H_SMI# | LEGACY CPU |
| D25C | H_DINV#0 | LEGACY CPU |
| J26 | H_DINV#1 | LEGACY CPU |
| T24 | H_DINV#2 | LEGACY CPU |
| AD20 | H_DINV#3 | LEGACY CPU |
| D25C | H_DSTB#0 | LEGACY CPU |
| K24 | H_DSTB#1 | LEGACY CPU |
| W25 | H_DSTB#2 | LEGACY CPU |
| D25C | H_DSTB#3 | LEGACY CPU |
| AE24 | H_DSTB#4 | LEGACY CPU |
| C22 | H_DSTB#5 | LEGACY CPU |
| L24 | H_DSTB#6 | LEGACY CPU |
| W24 | H_DSTB#7 | LEGACY CPU |
| W24 | H_DSTB#8 | LEGACY CPU |
| AE25 | H_DSTB#9 | LEGACY CPU |
| AE25 | H_DSTB#10 | LEGACY CPU |
| AE25 | H_DSTB#11 | LEGACY CPU |
| AE25 | H_DSTB#12 | LEGACY CPU |
| AE25 | H_DSTB#13 | LEGACY CPU |
| AE25 | H_DSTB#14 | LEGACY CPU |
| AE25 | H_DSTB#15 | LEGACY CPU |
| AE25 | H_DSTB#16 | LEGACY CPU |
| AE25 | H_DSTB#17 | LEGACY CPU |
| AE25 | H_DSTB#18 | LEGACY CPU |
| AE25 | H_DSTB#19 | LEGACY CPU |
| AE25 | H_DSTB#20 | LEGACY CPU |
| AE25 | H_DSTB#21 | LEGACY CPU |
| AE25 | H_DSTB#22 | LEGACY CPU |
| AE25 | H_DSTB#23 | LEGACY CPU |
| AE25 | H_DSTB#24 | LEGACY CPU |
| AE25 | H_DSTB#25 | LEGACY CPU |
| AE25 | H_DSTB#26 | LEGACY CPU |
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| AE25 | H_DSTB#33 | LEGACY CPU |
| AE25 | H_DSTB#34 | LEGACY CPU |
| AE25 | H_DSTB#35 | LEGACY CPU |
| AE25 | H_DSTB#36 | LEGACY CPU |
| AE25 | H_DSTB#37 | LEGACY CPU |
| AE25 | H_DSTB#38 | LEGACY CPU |
| AE25 | H_DSTB#39 | LEGACY CPU |
| AE25 | H_DSTB#40 | LEGACY CPU |
| AE25 | H_DSTB#41 | LEGACY CPU |
| AE25 | H_DSTB#42 | LEGACY CPU |
| AE25 | H_DSTB#43 | LEGACY CPU |
| AE25 | H_DSTB#44 | LEGACY CPU |
| AE25 | H_DSTB#45 | LEGACY CPU |
| AE25 | H_DSTB#46 | LEGACY CPU |
| AE25 | H_DSTB#47 | LEGACY CPU |
| AE25 | H_DSTB#48 | LEGACY CPU |
| AE25 | H_DSTB#49 | LEGACY CPU |
| AE25 | H_DSTB#50 | LEGACY CPU |
| AE25 | H_DSTB#51 | LEGACY CPU |
| AE25 | H_DSTB#52 | LEGACY CPU |
| AE25 | H_DSTB#53 | LEGACY CPU |
| AE25 | H_DSTB#54 | LEGACY CPU |
| AE25 | H_DSTB#55 | LEGACY CPU |
| AE25 | H_DSTB#56 | LEGACY CPU |
| AE25 | H_DSTB#57 | LEGACY CPU |
| AE25 | H_DSTB#58 | LEGACY CPU |
| AE25 | H_DSTB#59 | LEGACY CPU |
| AE25 | H_DSTB#60 | LEGACY CPU |
| AE25 | H_DSTB#61 | LEGACY CPU |
| AE25 | H_DSTB#62 | LEGACY CPU |
| AE25 | H_DSTB#63 | LEGACY CPU |



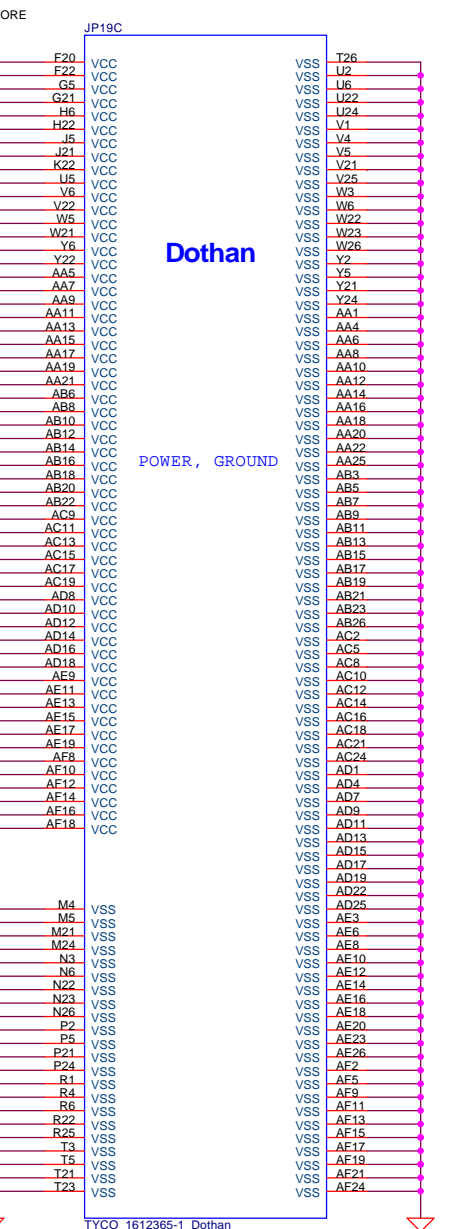
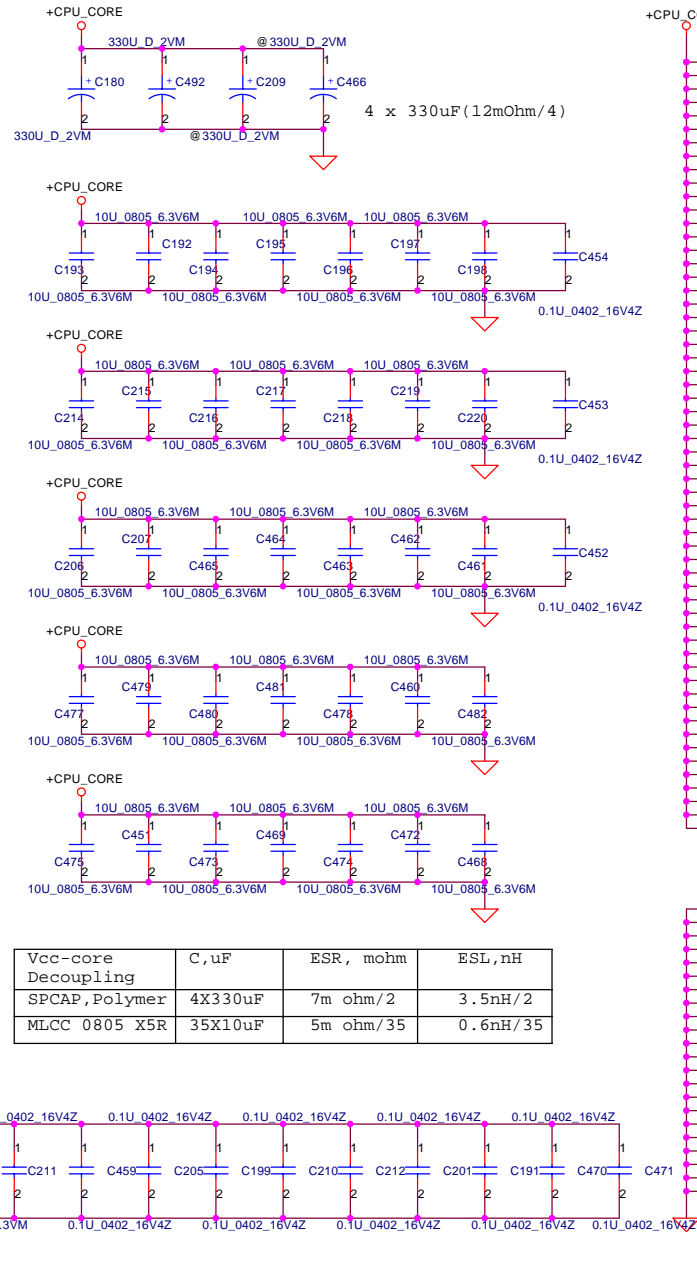
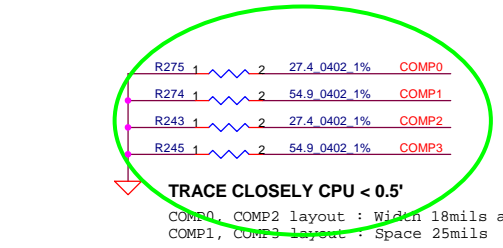
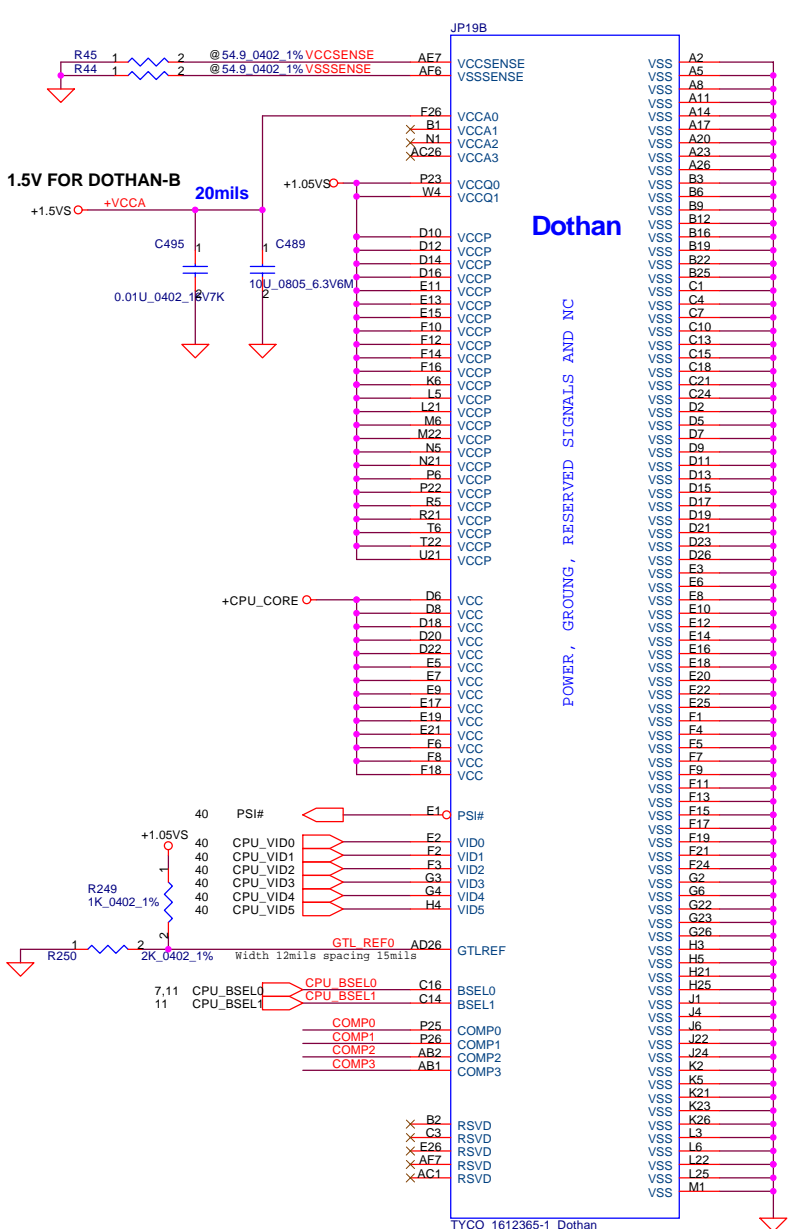
| Signal | Component | Value | Notes |
|---------------|-----------|------------------|-------|
| H_FERR# | R72 | 2 56 0402 5% | |
| PREQ# | R77 | 2 1 56 0402 5% | |
| H_DPUSLP# | R62 | 1 2 200 0402 5% | |
| H_BR0# | R70 | 1 2 200 0402 5% | |
| H_DPRSTP# | R71 | 2 1 56 0402 5% | |
| ITP_TDI | R79 | 2 1 150 0402 5% | |
| ITP_TDO | R78 | 2 1 54.9 0402 1% | |
| H_RESET# | R63 | 2 1 54.9 0402 1% | |
| ITP_TMS | R64 | 2 1 40.2 0402 1% | |
| PROCHOT# | R66 | 2 1 56 0402 5% | |
| H_IERR# | R75 | 2 1 56 0402 5% | |
| H_PWRGOOD | R82 | 2 1 200 0402 5% | |
| H_CPUSLP# | R81 | 1 2 200 0402 5% | |
| ITP_DBRRESET# | R76 | 2 1 150 0402 5% | |
| ITP_TRST# | R80 | 2 1 680 0402 5% | |
| ITP_TCK | R65 | 2 1 27.4 0402 1% | |
| TEST1 | R61 | 2 1 1K 0402 5% | |
| TEST2 | R294 | 2 1 1K 0402 5% | |

Place Caps Close to CPU Socket

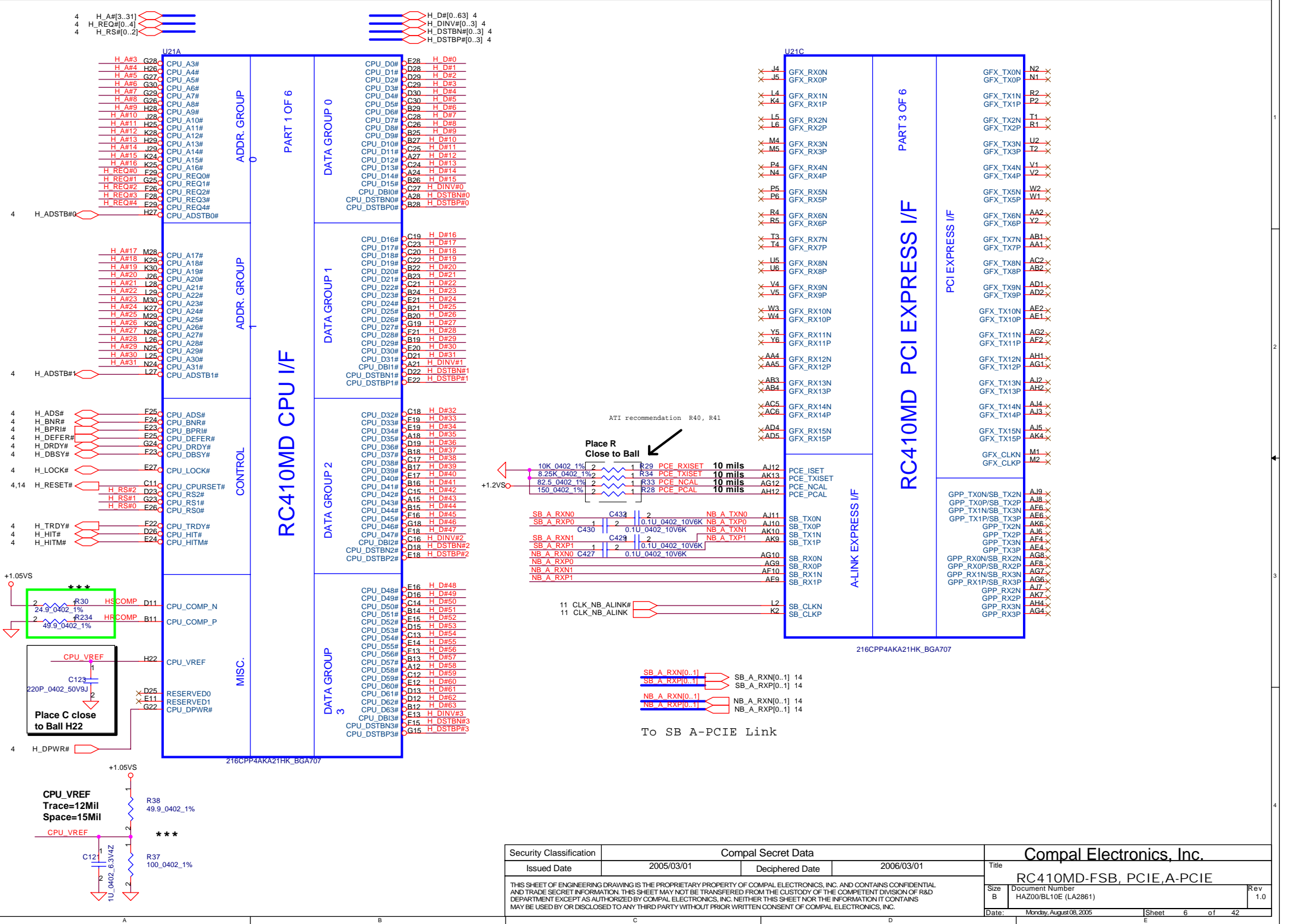
| | | | | |
|------|---|---|-----------------|-----------|
| C263 | 1 | 2 | 180P_0402_50V8J | H_INIT# |
| C255 | 1 | 2 | 180P_0402_50V8J | H_A20M# |
| C264 | 1 | 2 | 180P_0402_50V8J | H_CPUSLP# |
| C254 | 1 | 2 | 180P_0402_50V8J | H_INTR |
| C262 | 1 | 2 | 180P_0402_50V8J | H_NMI |
| C257 | 1 | 2 | 180P_0402_50V8J | H_SMI# |
| C261 | 1 | 2 | 180P_0402_50V8J | H_STPCLK# |
| C256 | 1 | 2 | 180P_0402_50V8J | H_IGNNE# |
| C265 | 1 | 2 | 180P_0402_50V8J | H_PWRGOOD |
| C640 | 1 | 2 | 180P_0402_50V8J | H_FERR# |

THERMDA & THERMDC Trace / Space = 10 / 10 mil

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| | | | Sheet | 5 | of 42 |

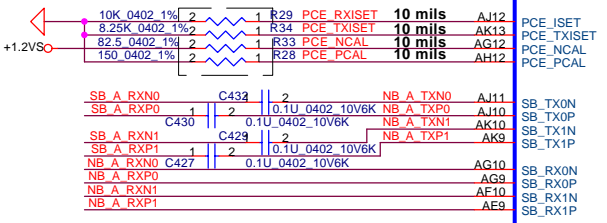


RC410MD CPU I/F

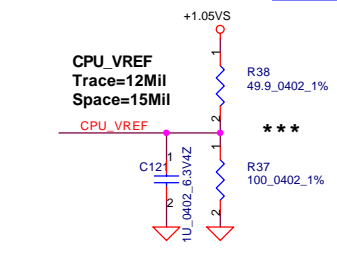
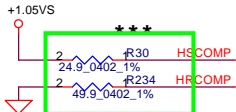
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ATI recommendation R40, R41

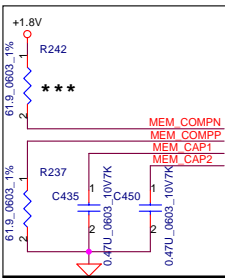
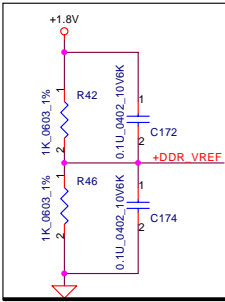
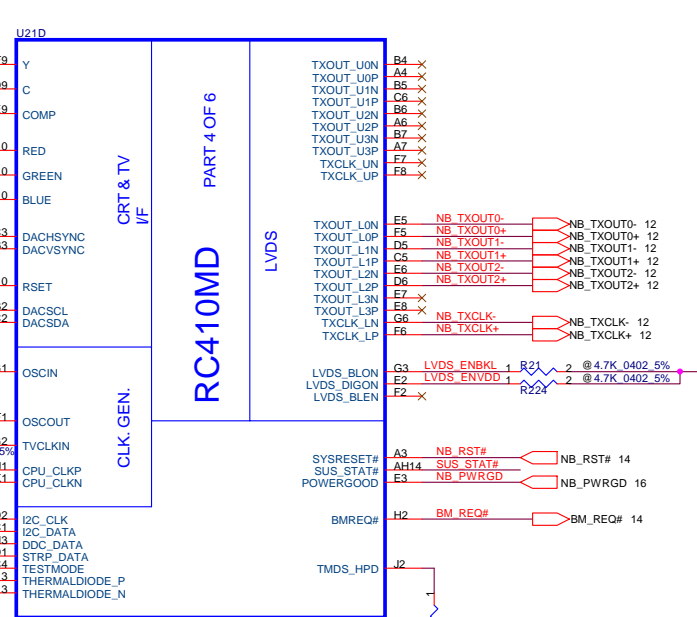
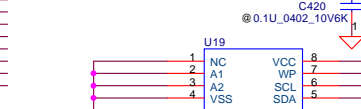
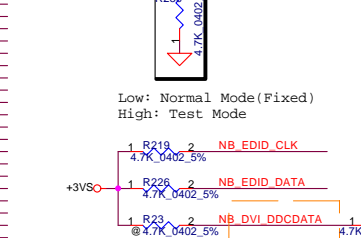
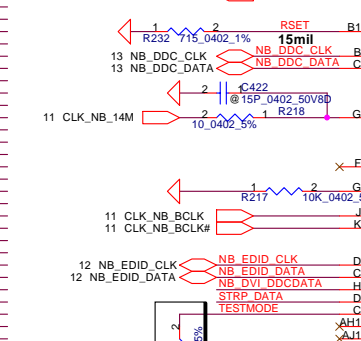
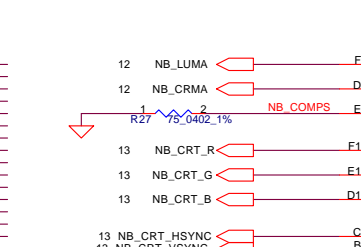
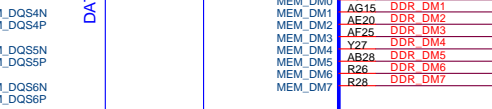
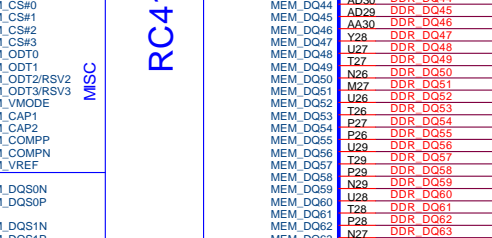
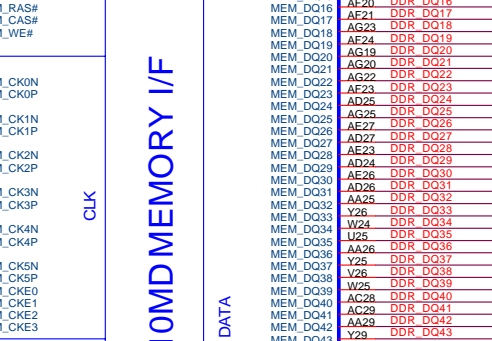
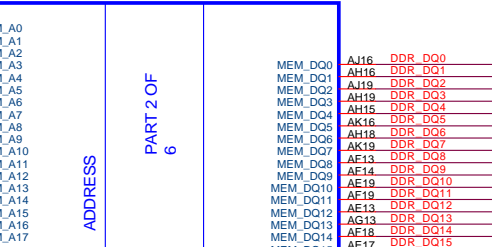
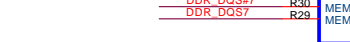
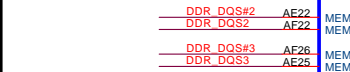
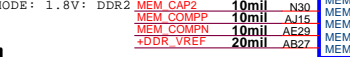
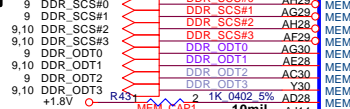
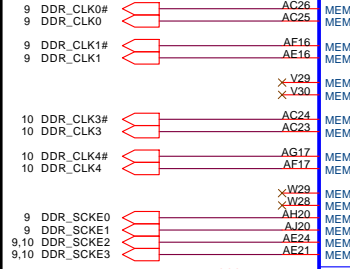
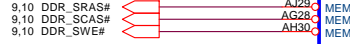
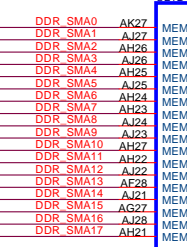
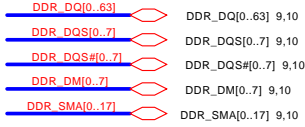
Place R Close to Ball



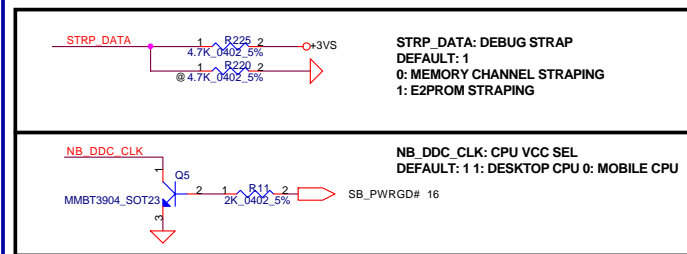
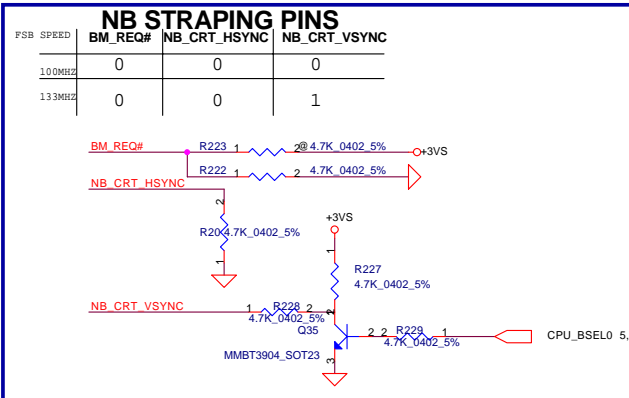
To SB A-PCIE Link



| | | | | | |
|---|-------------------------|--------------------|------------|--------------------------|----|
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| Size | Document Number | | | Rev | |
| B | HA200/BL10E (LA2861) | | | 1.0 | |
| Date: | Monday, August 08, 2005 | Sheet | 6 | of | 42 |

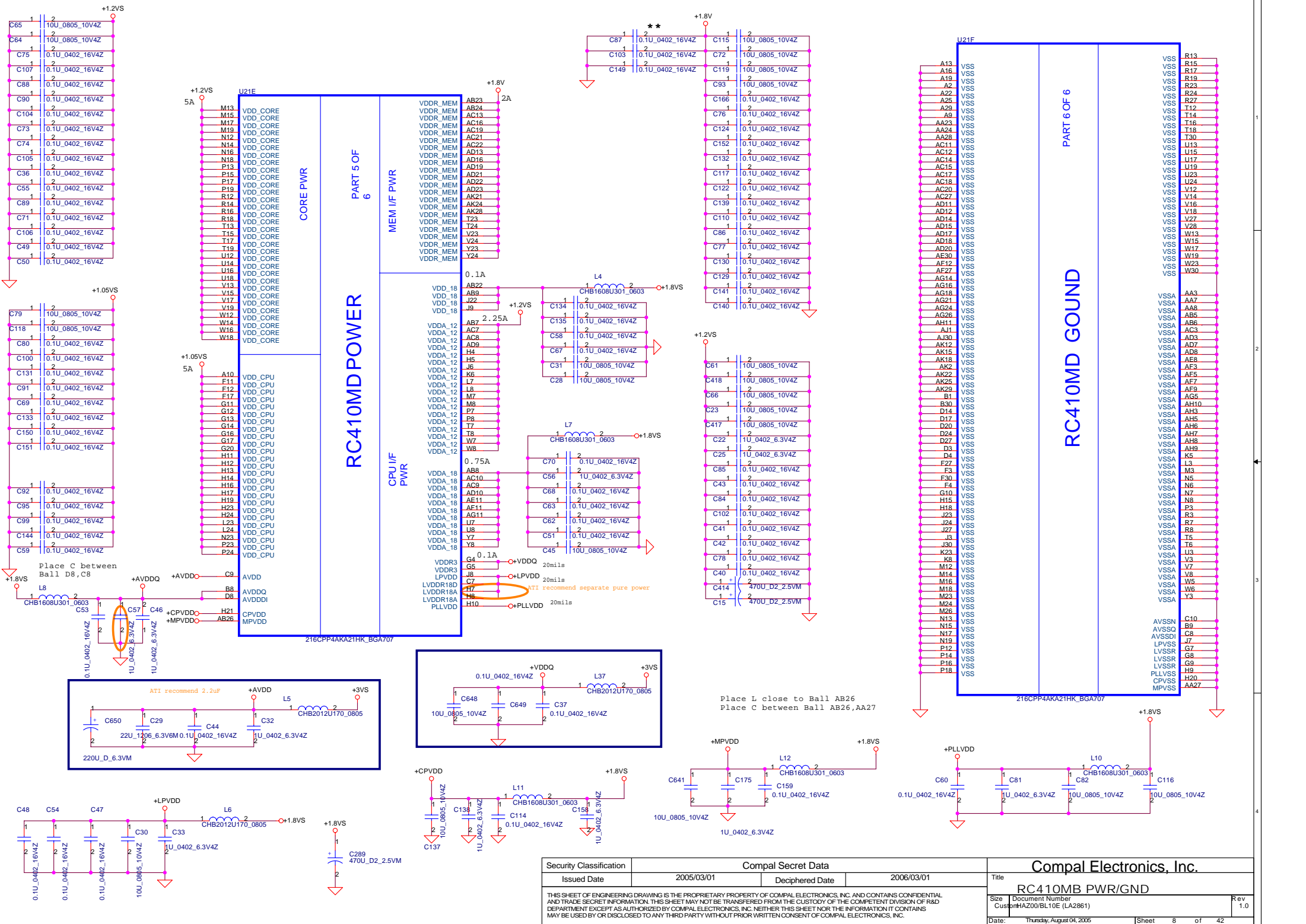


Place these R and C close to relative Ball.



Low: Normal Mode(Fixed)
High: Test Mode

| | | | | |
|---|-------------------------|-----------------|--------------------------|-----------------------|
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| Size | Document Number | Rev | | |
| Custom | HAZ00/BL10E (LA2861) | 1.0 | | |
| Date: | Monday, August 08, 2005 | Sheet | 7 | of 42 |



PART 5 OF 6

RC410MD POWER

CORE PWR

MEM I/F PWR

CPU I/F PWR

PART 6 OF 6

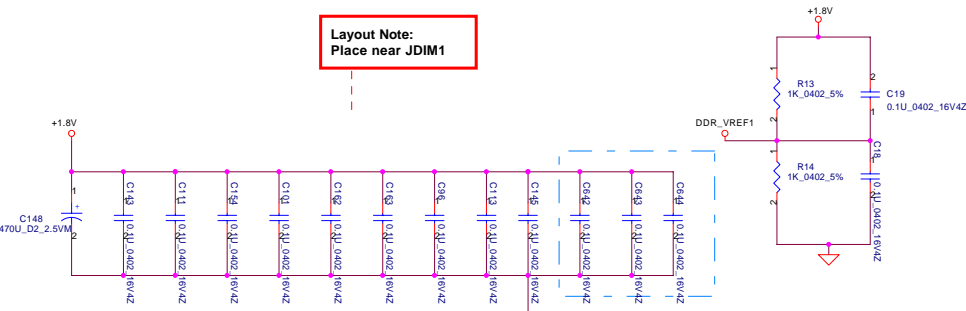
RC410MD GOUND

| | | |
|-------------------------|--------------------|-----------------|
| Security Classification | Compal Secret Data | |
| Issued Date | 2005/03/01 | Deciphered Date |
| | | 2006/03/01 |

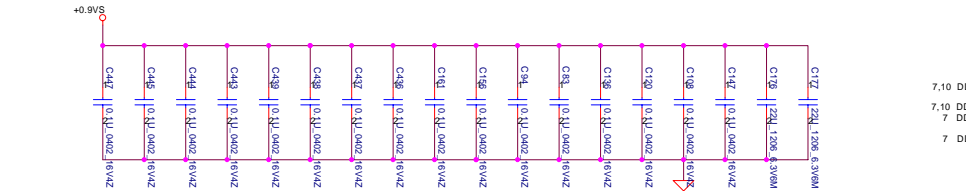
| | | | | | |
|-----------------|----------------------------|-------|--------------------------|----|----|
| Title | | | Compal Electronics, Inc. | | |
| RC410MB PWR/GND | | | Rev 1.0 | | |
| Size | Document Number | | Customer # | | |
| | Cust#HZA200/BL10E (LA2861) | | | | |
| Date: | Thursday, August 04, 2005 | Sheet | 8 | of | 42 |

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Layout Note:
Place near JDIM1

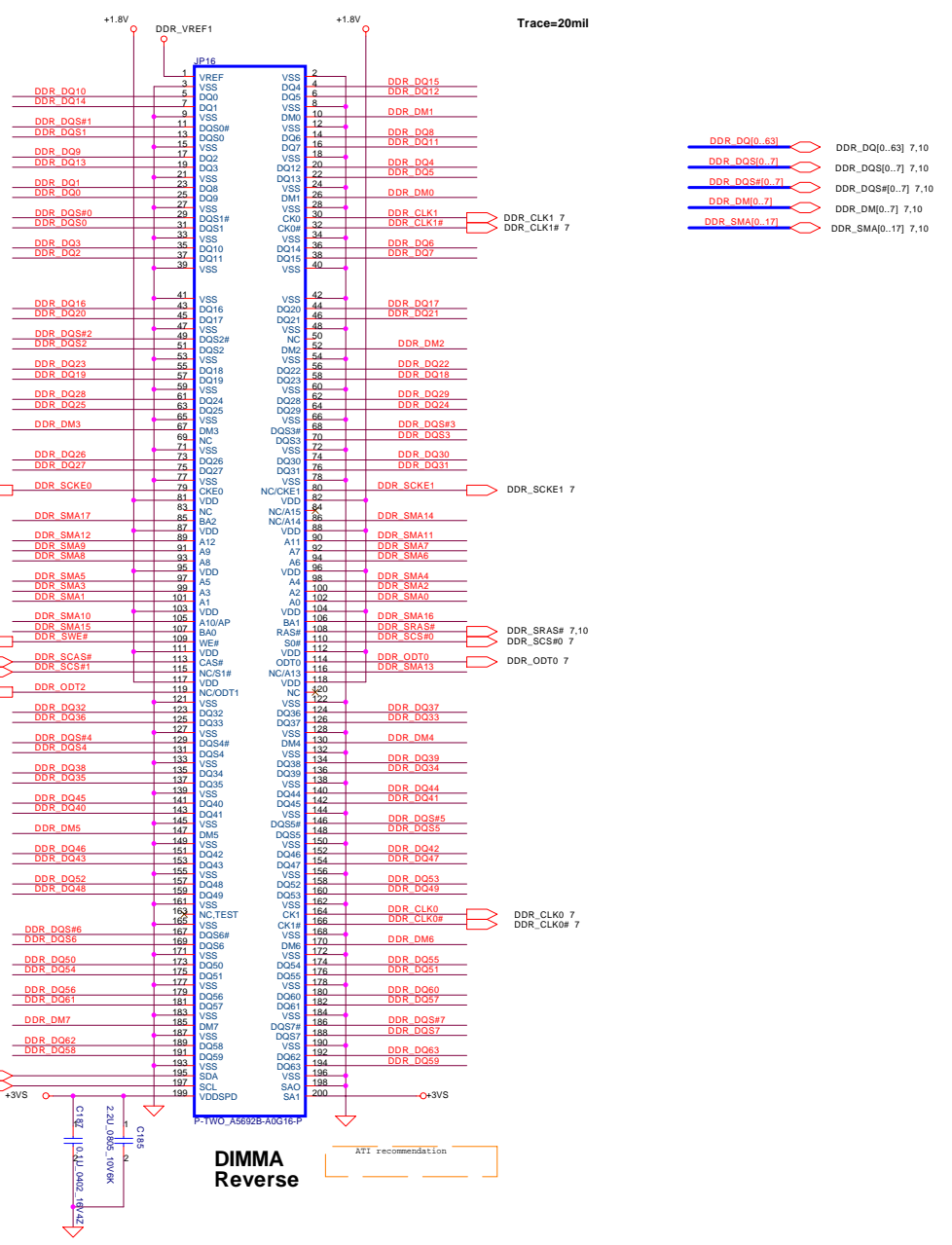
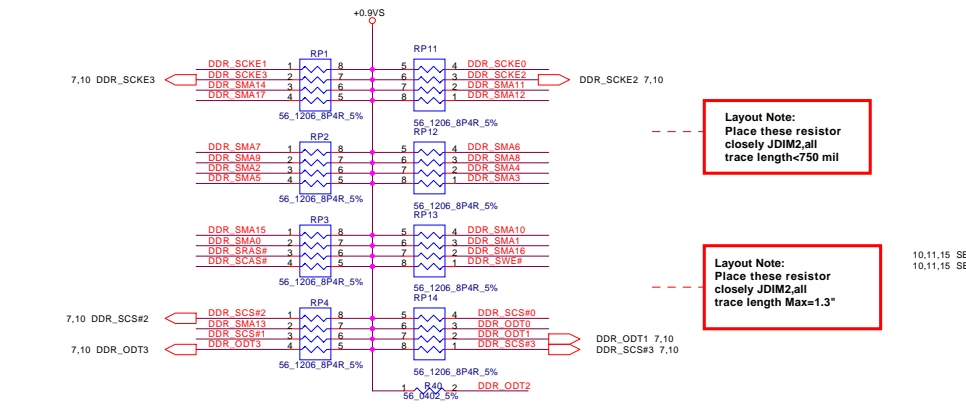


Layout Note:
Place one cap close to every 2 pullup resistors terminated to V_DDR_MCH_REF



Layout Note:
Place these resistor closely JDIM2,all trace length<750 mil

Layout Note:
Place these resistor closely JDIM2,all trace length Max=1.3"

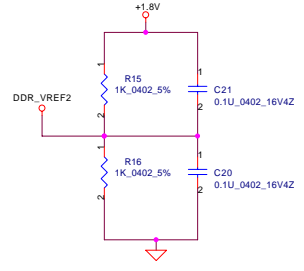
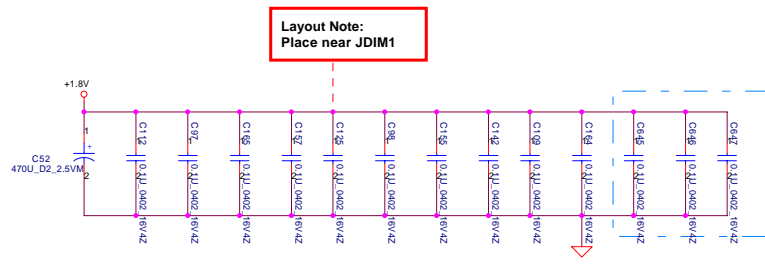
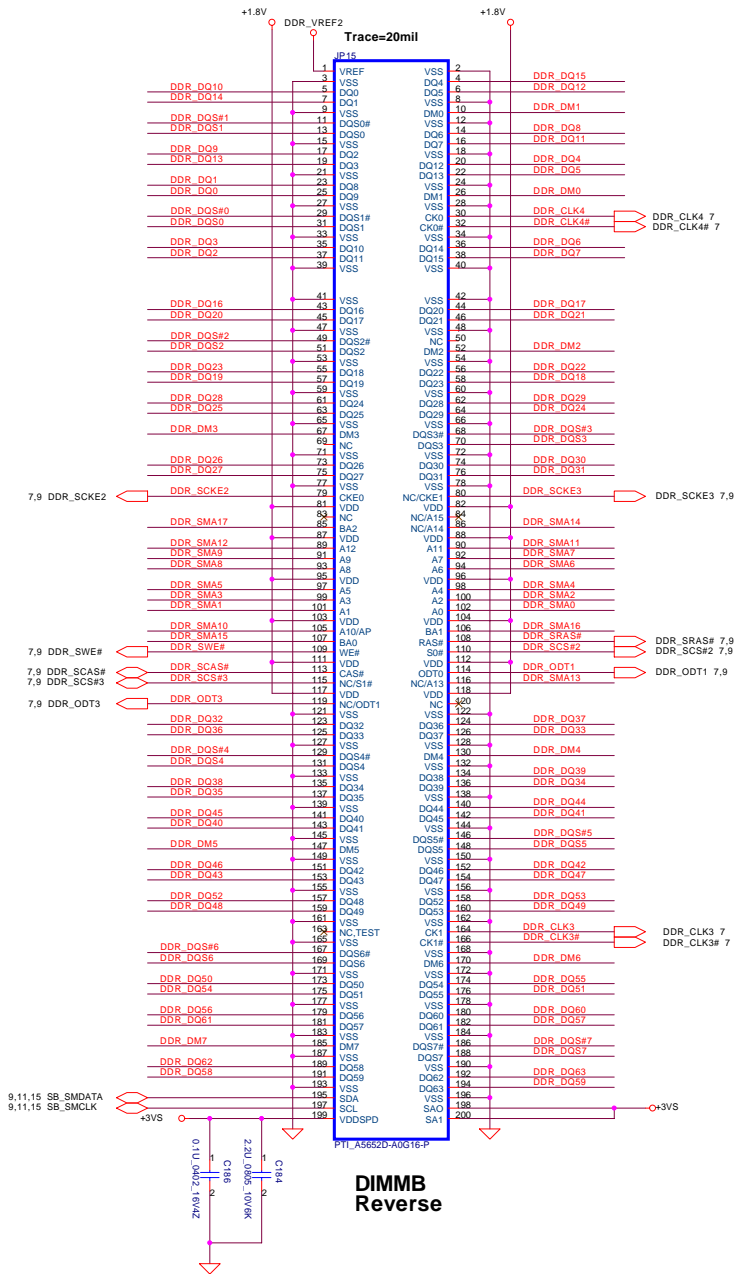


Traces=20mil

DIMMA Reverse

ATI recommendation

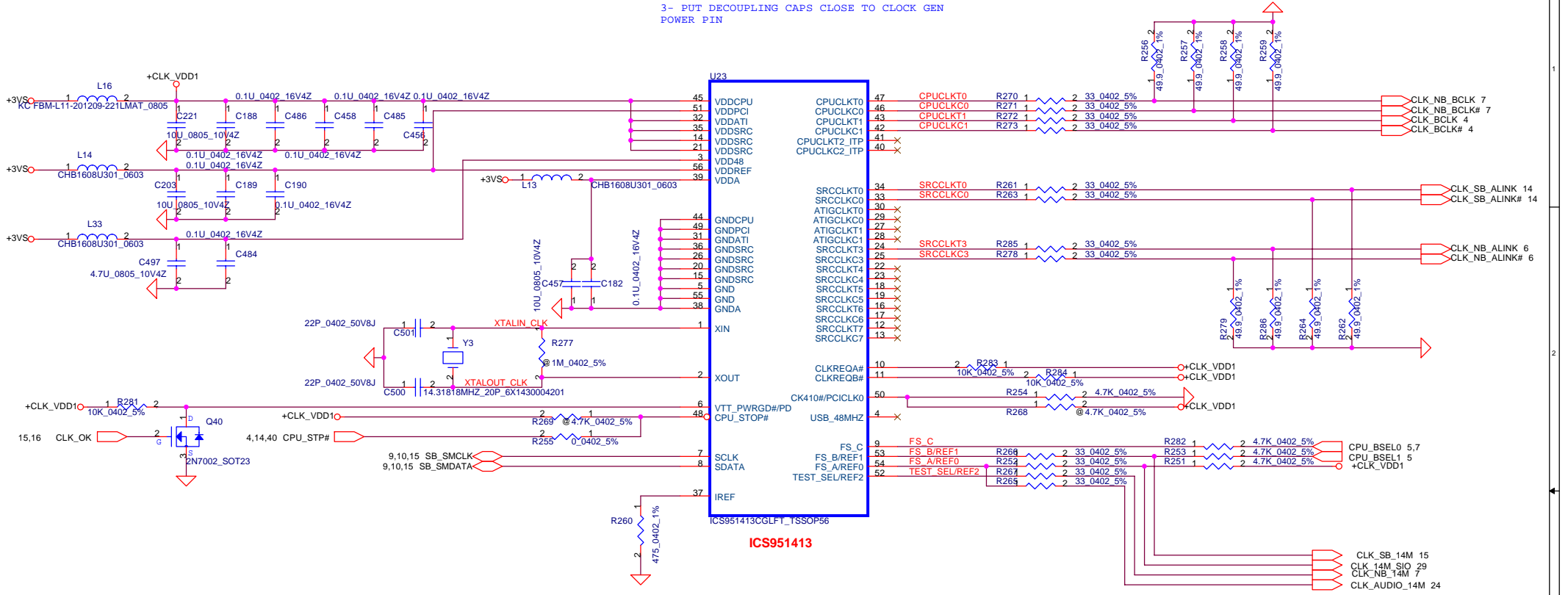
- 7.9 DDR_DQ[0..63] **DDR_DQ[0..63]**
- 7.9 DDR_DQS[0..7] **DDR_DQS[0..7]**
- 7.9 DDR_DQS# [0..7] **DDR_DQS# [0..7]**
- 7.9 DDR_DM[0..7] **DDR_DM[0..7]**
- 7.9 DDR_SMA[0..17] **DDR_SMA[0..17]**



| | | | | |
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| | | | | HAZ00/BL10E (LA2861) |
| Date: | Monday, August 08, 2005 | Sheet | 10 | of 42 |

Clock Generator

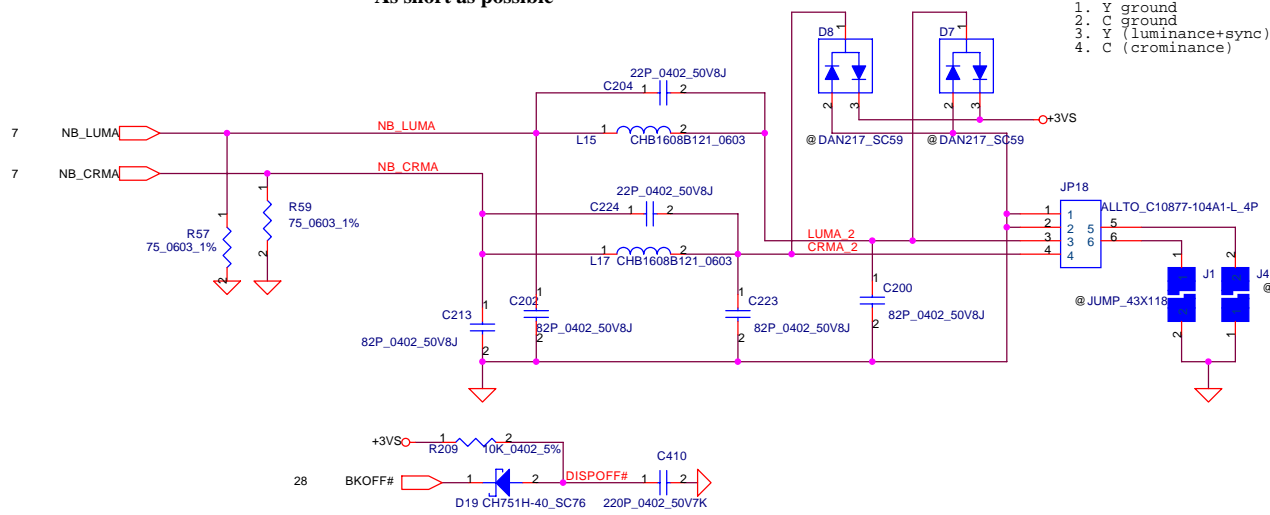
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBCLK/#, ITPCLK/# AND SCR/# ,AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



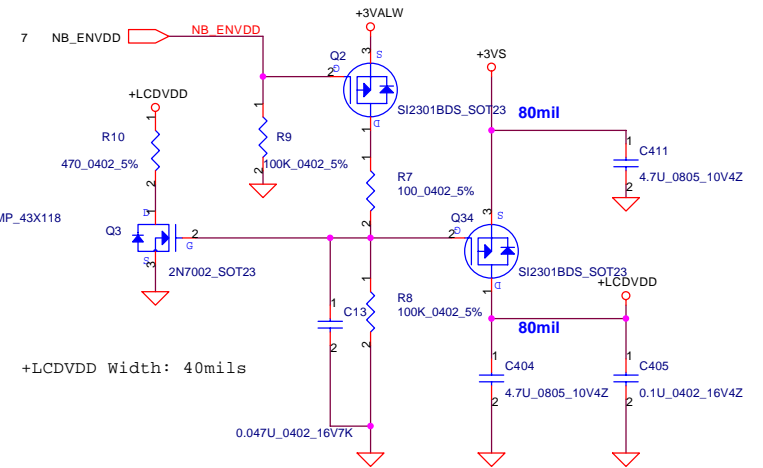
| FS_C | FS_B | FS_A | CPU | SRC | PCI | REF | USB |
|------|------|------|--------|--------|-------|--------|--------|
| 1 | 0 | 1 | 100.00 | 100.00 | 33.33 | 14.318 | 48.000 |
| 0 | 0 | 1 | 133.33 | 100.00 | 33.33 | 14.318 | 48.000 |
| 1 | 1 | 1 | --- | --- | --- | --- | --- |

TV-OUT CONNECTOR

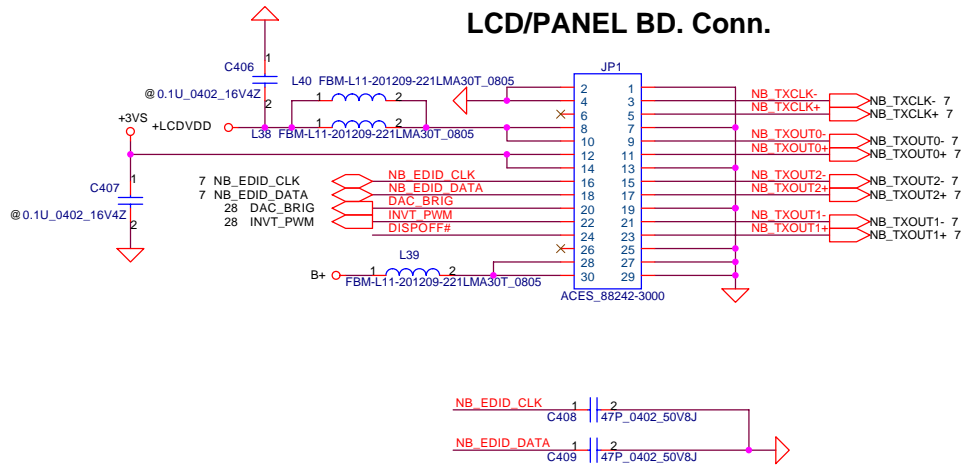
Reduce LUMA_1 and CRMA_1 length
As short as possible



PANEL +LCDVDD CTRL CKT

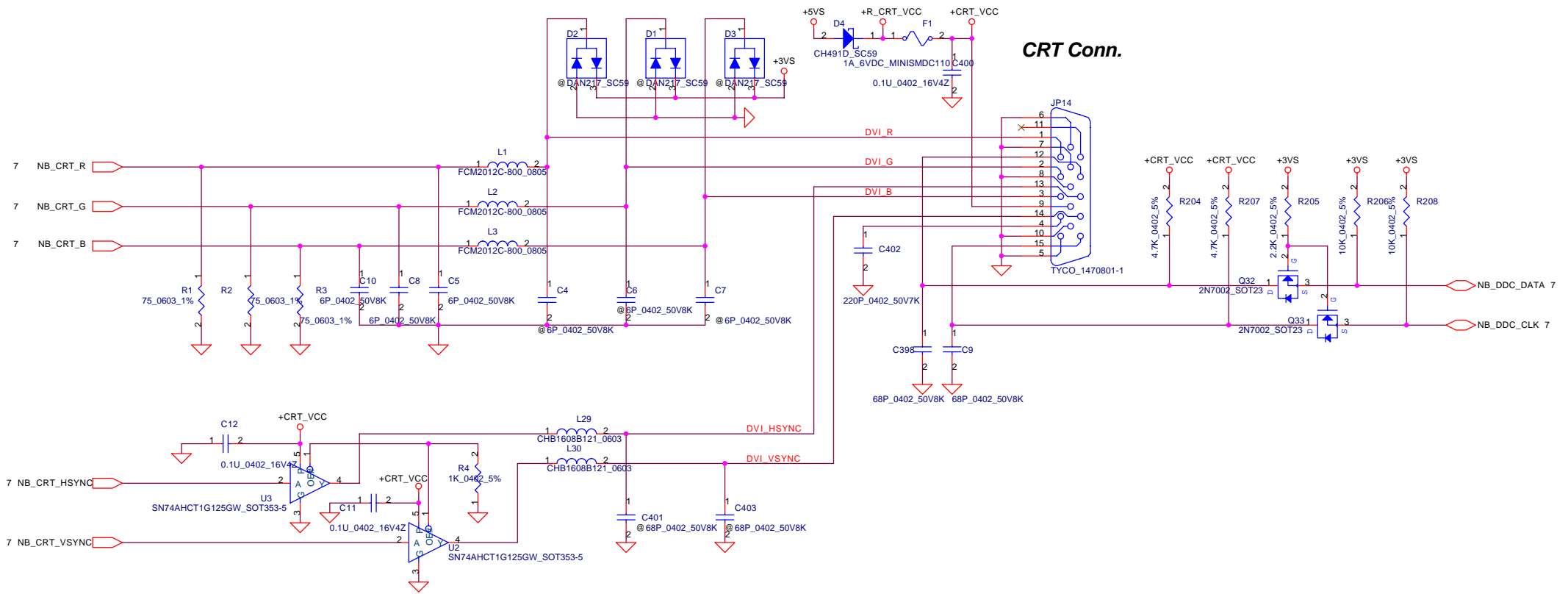


LCD/PANEL BD. Conn.

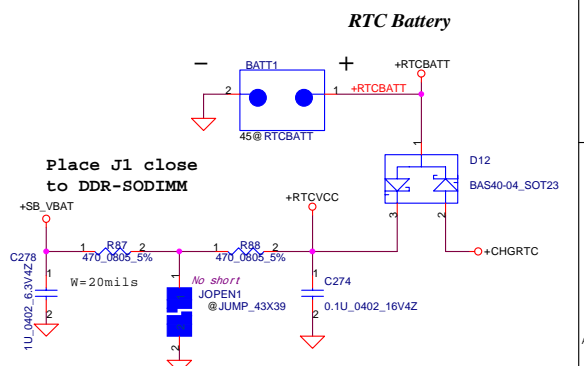
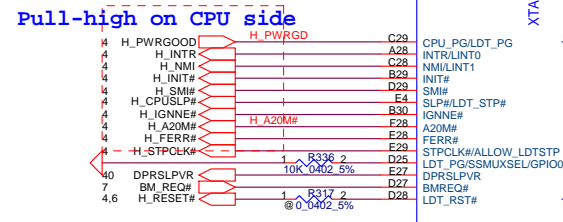
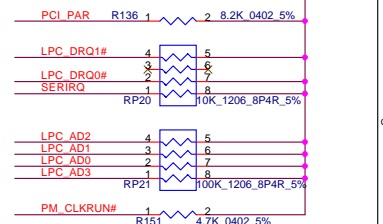
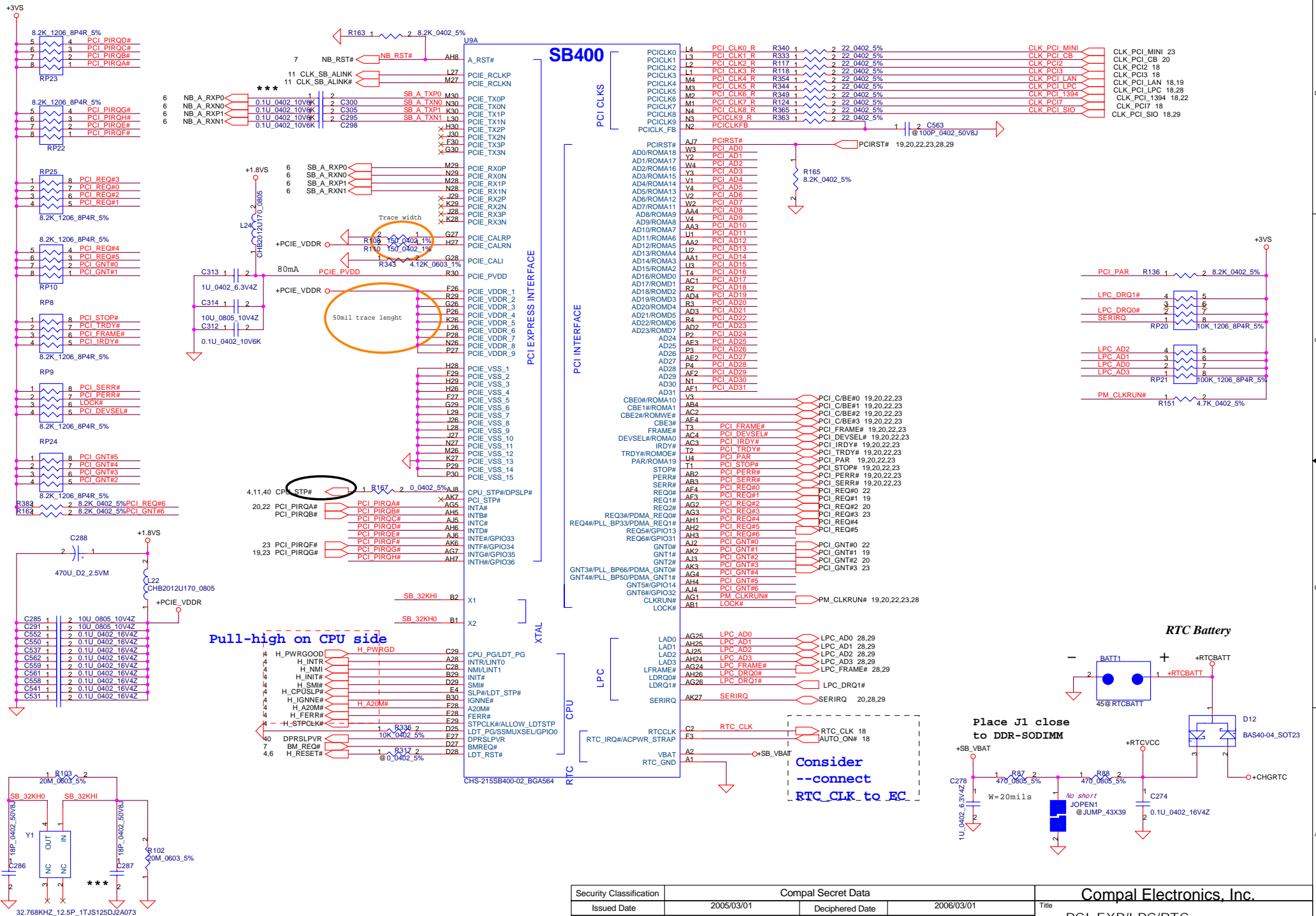


| | | | | | |
|---|-------------------------|--------------------|----------------------|--------------------------|-------|
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| Size | B | Document Number | HA200/BL10E (LA2861) | Rev | 1.0 |
| Date: | Monday, August 08, 2005 | | Sheet | 12 | of 42 |

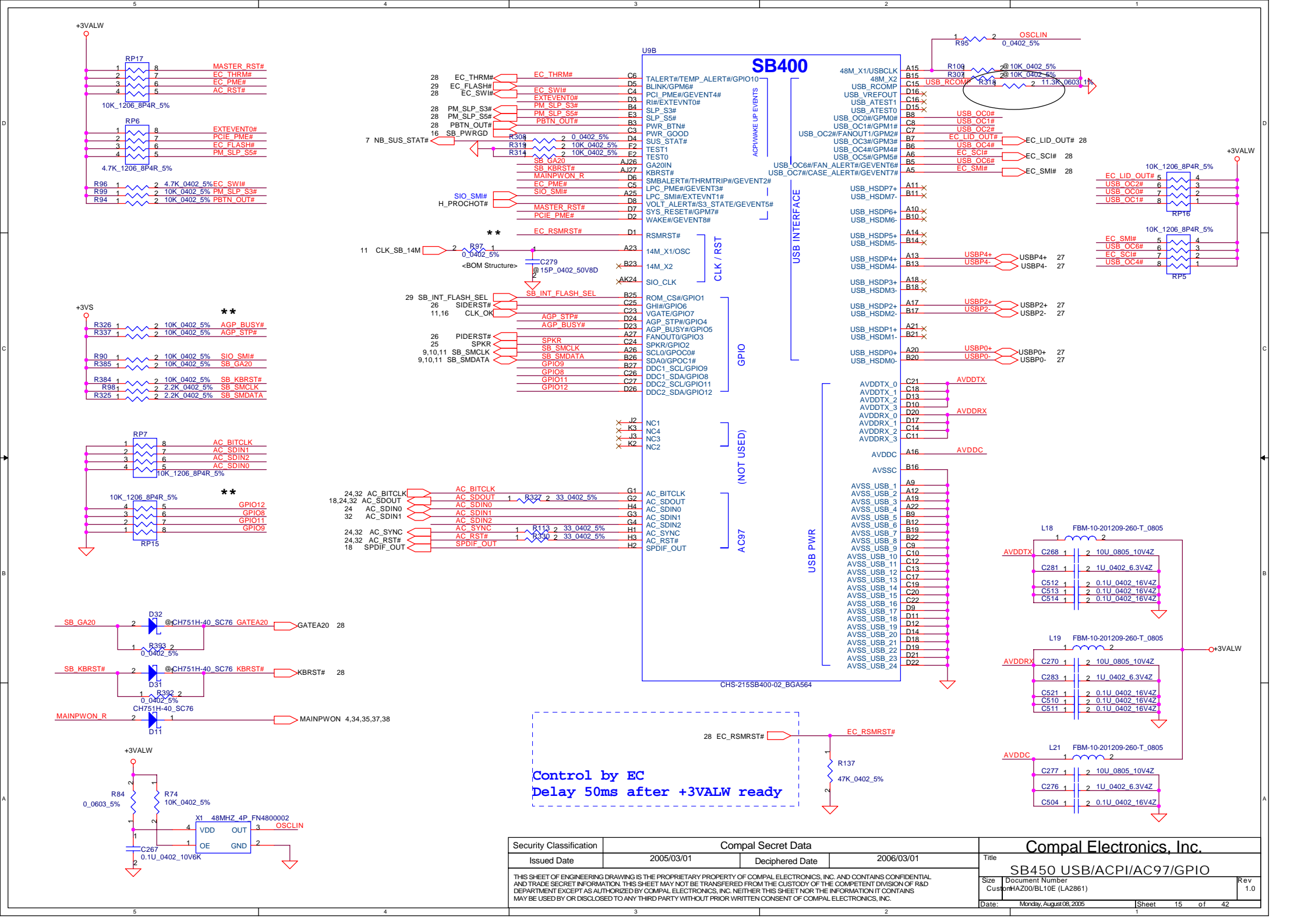
CRT CONNECTOR



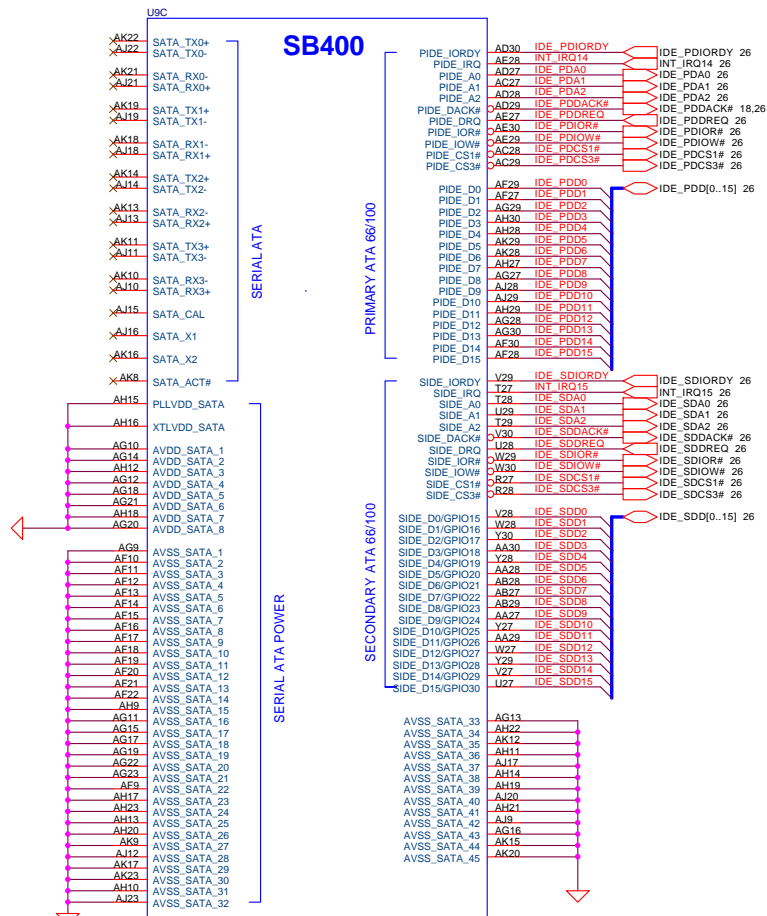
| | | | | | |
|---|---------------------------|--------------------|------------|--------------------------|--|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
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| Size | Document Number | | | Rev | |
| B | HAZ00/BL10E (LA2861) | | | 1.0 | |
| Date: | Thursday, August 04, 2005 | | Sheet | 13 of 42 | |



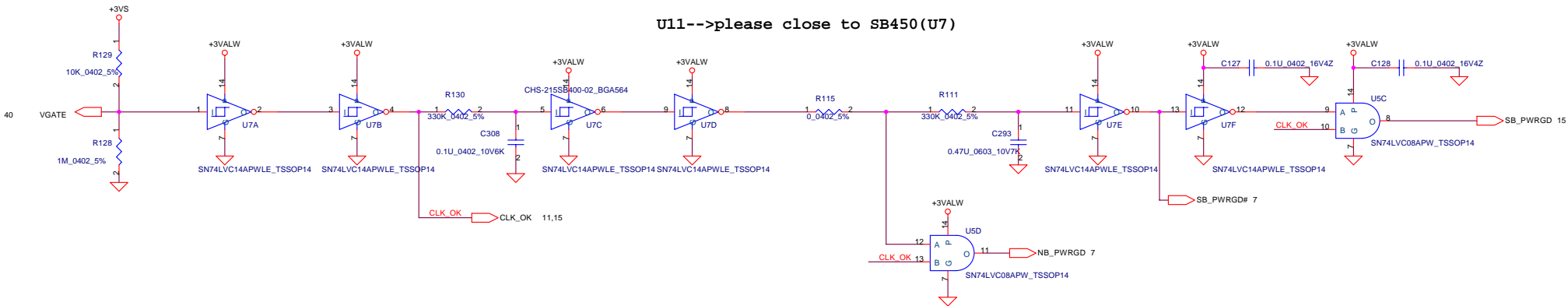
| Security Classification | | Compal Secret Data | | Title | |
|---|--------------------------|--------------------|------------|----------------------|-----------------|
| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 | PCI_EXP/LPC/RTC | |
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| | | | | HAZ00/BL10E (LA2861) | Rev 1.0 |
| Date: | Monrday, August 08, 2005 | Sheet | 14 of 42 | | |



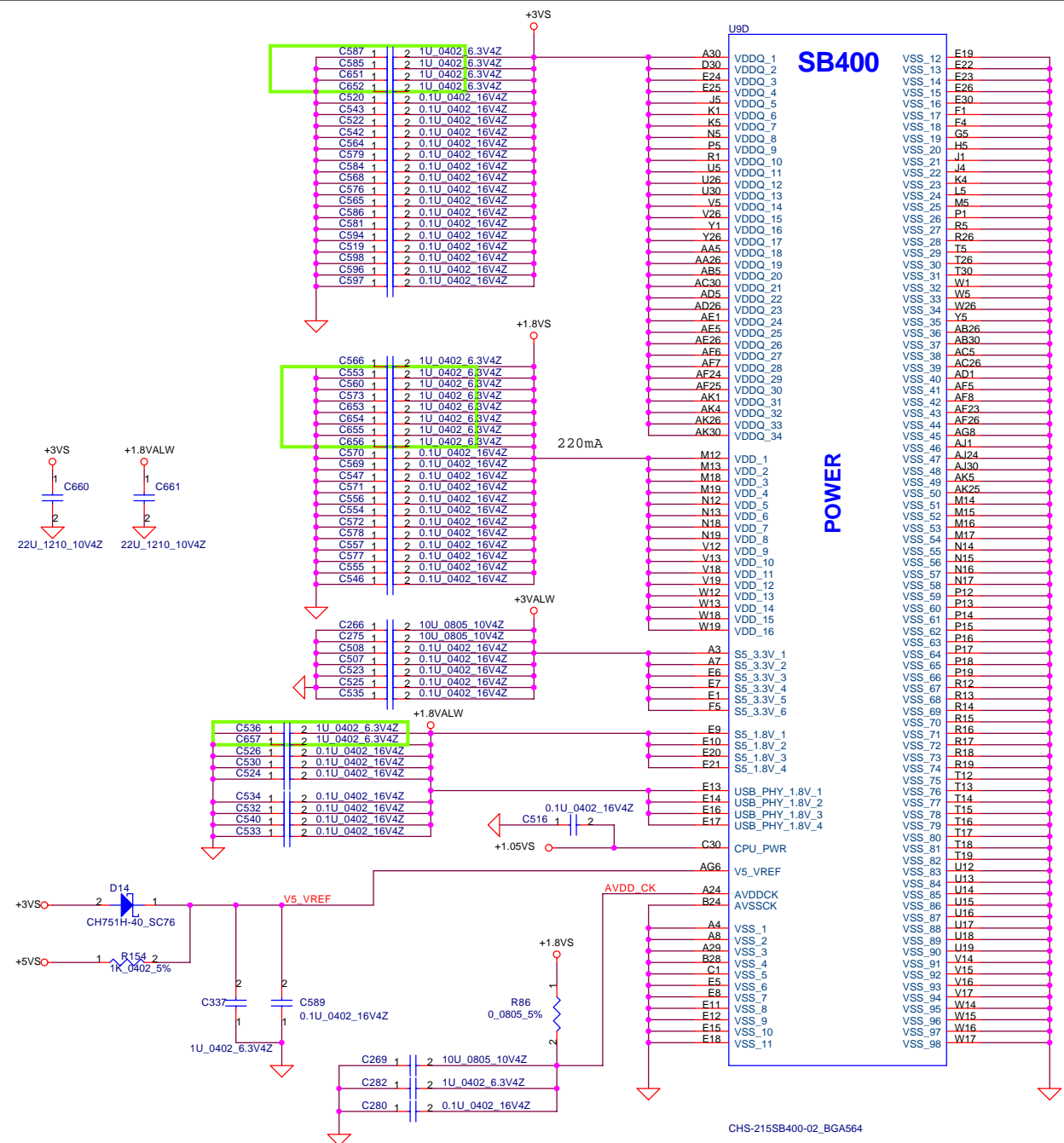
| | | | | | |
|---|-------------------------|----------------------|------------|--------------------------|----|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 | Title | |
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| Size | Document Number | Customer# | | Rev | |
| | | HA200/BL10E (LA2861) | | 1.0 | |
| Date: | Monday, August 08, 2005 | Sheet | 15 | of | 42 |



U11-->please close to SB450(U7)

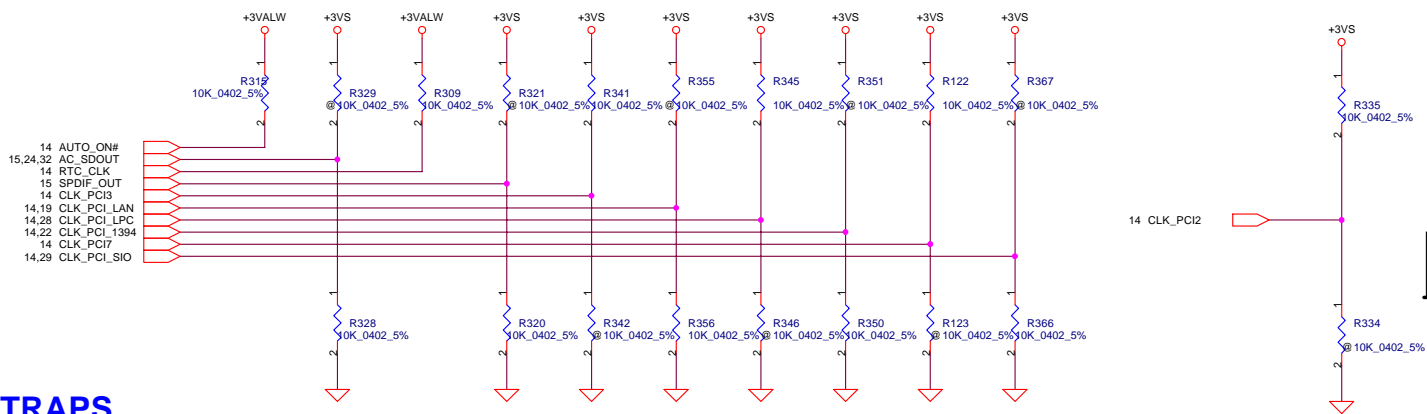


| | | | | |
|---|-------------------------|-----------------|--------------------------|--|
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| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 | Title |
| | | | | SB450 IDE/SATA |
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| Date: | Monday, August 08, 2005 | Sheet | 16 | of 42 |



CHS-215SB400-02_BGA564

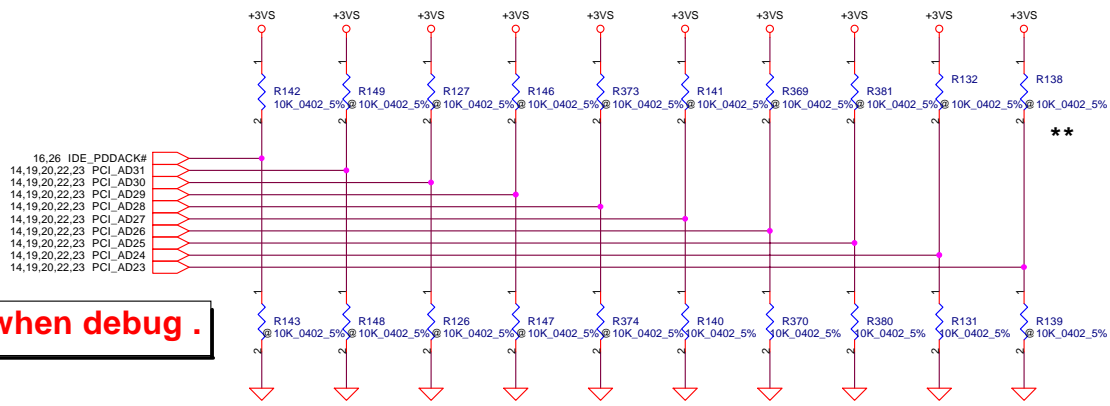
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|---|---------------------------|-----------------|--------------------------|-----------------|
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| Size | Document Number | | | Rev |
| B | HAZ00/BL10E (LA2861) | | | 1.0 |
| Date: | Thursday, August 04, 2005 | Sheet | 17 | of 42 |



REQUIRED STRAPS



| | AUTO_ON# | AC97_SDOUT | RTC_CLK | SPDIF_OUT | CLK_PCI3 | CLK_PCI_LAN | CLK_PCI_LPC | PCI_CLK6 | PCI_CLK7 | PCI_CLK8 | CLK_PCI_MINI2 |
|------------------|--------------------------|--------------------------------|--|-----------------------------------|------------------------------------|---------------------------|----------------------------|-------------------------|--|----------|-------------------------------|
| PULL HIGH | MANUAL PWR ON DEFAULT | USE DEBUG STRAPS DEFAULT | INTERNAL RTC DEFAULT | PU for 48Mhz XTAL mode DEFAULT | USB PHY PWRDOWN DISABLE DEFAULT | Internal PLL DEFAULT | PCIE CM_SET low DEFAULT | CPU I/F = K8 DEFAULT | ROM TYPE H,H = PCI ROM H,L = LPC ROM I | | Clock input buffer DEFAULT |
| PULL LOW | AUTO PWR ON | IGNORE DEBUG STRAPS DEFAULT | EXTERNAL RTC (NOT SUPPORTED W/ IT8712) | 48M OSC mode DEFAULT | USB PHY PWRDOWN ENABLE DEFAULT | External Clock DEFAULT | PCIE CM_SET HIGH | CPU I/F = P4 DEFAULT | L,H = LPC ROM II L,L = FWH ROM | | Crysal Pad |



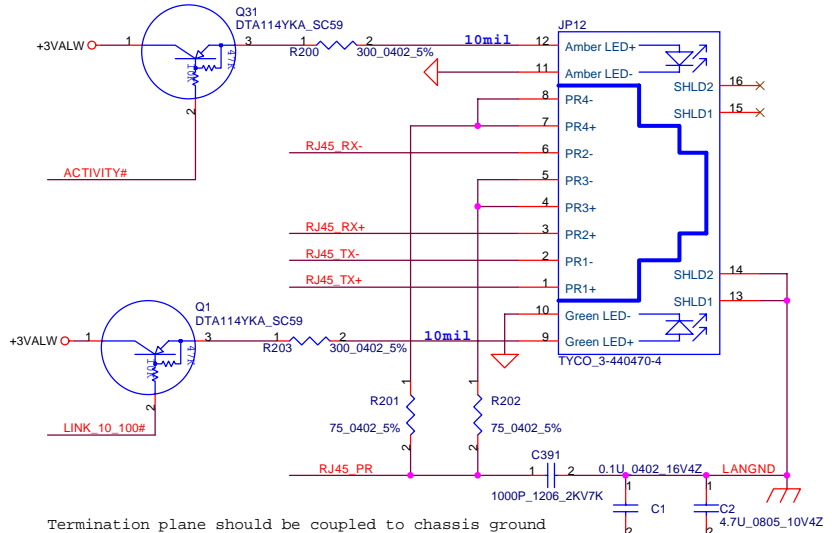
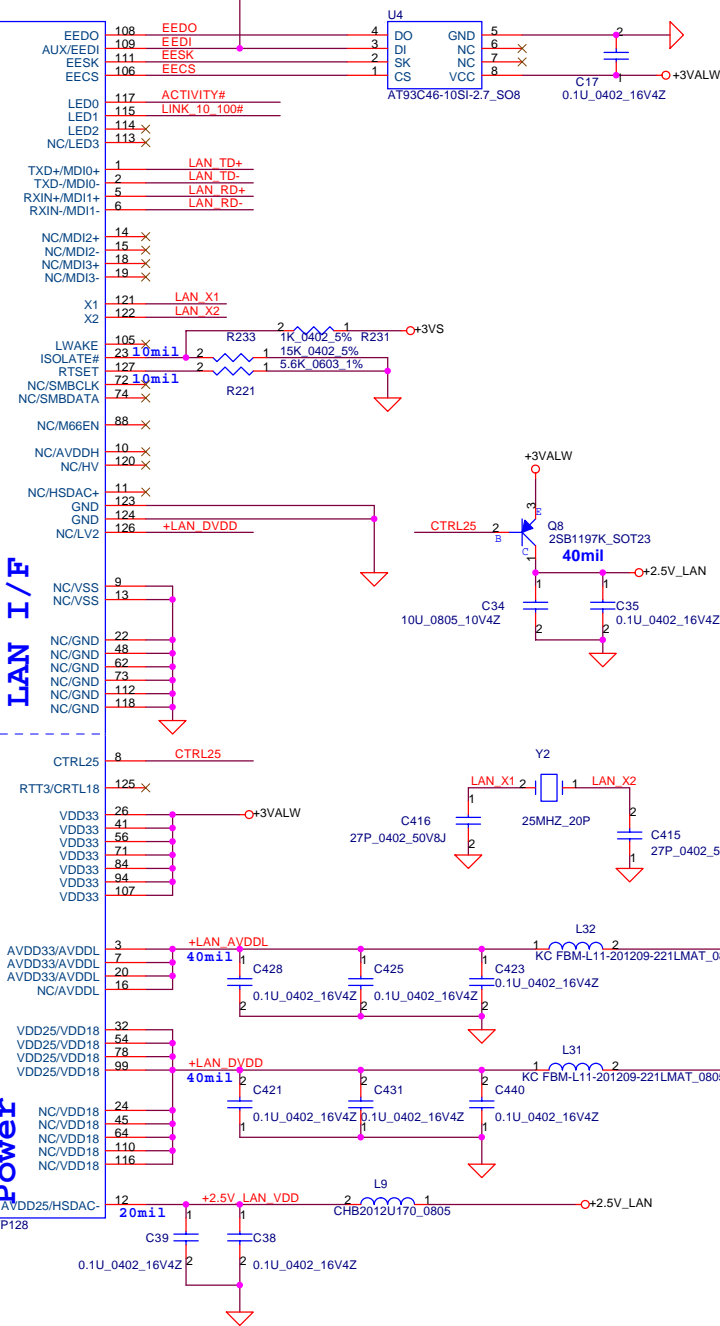
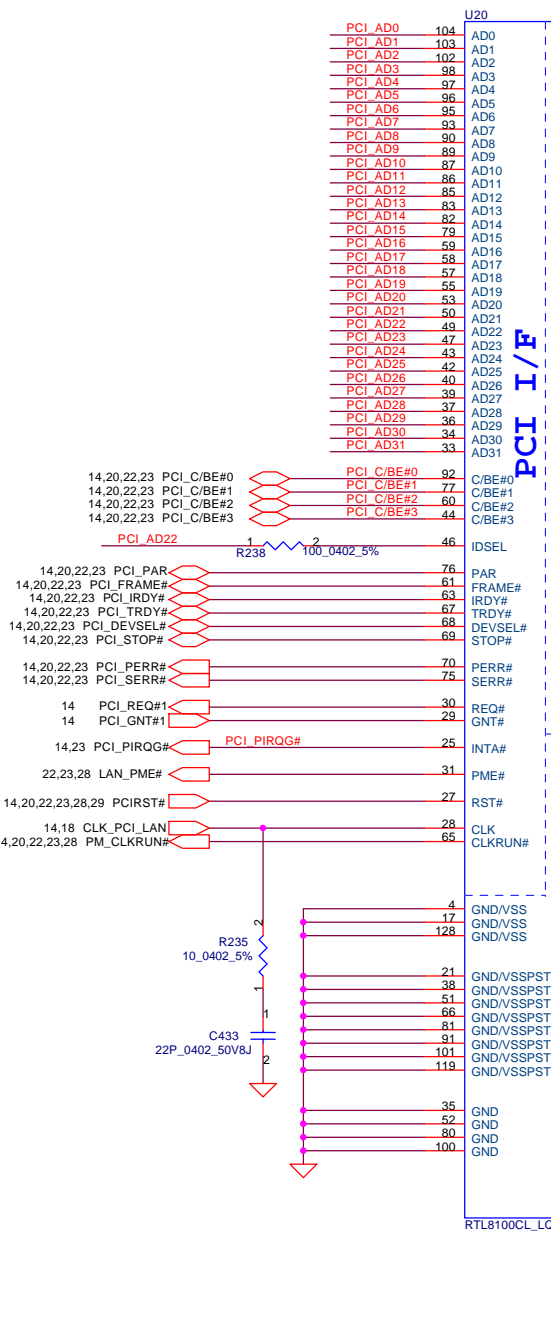
Pop R634 when debug .

DEBUG STRAPS

| | IDE_PDDACK# | PCI_AD31 | PCI_AD30 | PCI_AD29 | PCI_AD28 | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 |
|------------------|---------------------------|----------|----------|----------|----------|------------------------|--------------------------|------------------------|------------------------------------|----------|
| PULL HIGH | USE LONG RESET DEFAULT | Reserved | Reserved | Reserved | Reserved | BYPASS PCI PLL | BYPASS ACPI BCLK | BYPASS IDE PLL | USE EEPROM PCIE STRAPS | Reserved |
| PULL LOW | USE SHORT RESET | | | | | USE PCI PLL DEFAULT | USE ACPI BCLK DEFAULT | USE IDE PLL DEFAULT | USE DEFAULT PCIE STRAPS DEFAULT | |

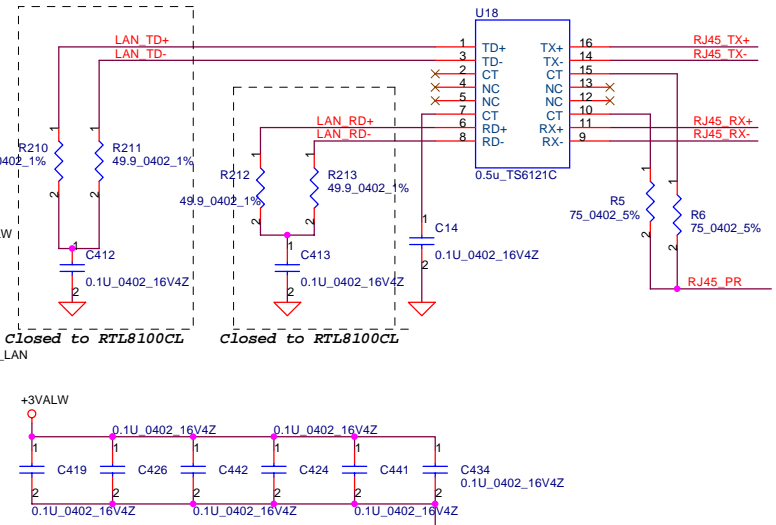
| | | | | | | |
|---|-------------------------|-----------------|------------|---------------|--------------------------|-----|
| Security Classification | Compal Secret Data | | Title | | Compal Electronics, Inc. | |
| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 | HARDWARE TRAP | | |
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| | | | | Customer# | HAZ00/BL10E (LA2861) | 1.0 |
| Date: | Monday, August 08, 2005 | Sheet | 18 | of | 42 | |

14,18,20,22,23 PCI_AD[0..31] PCI_AD[0..31]

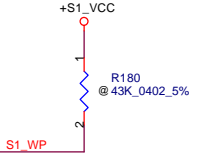
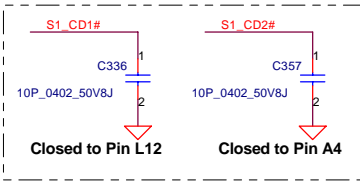
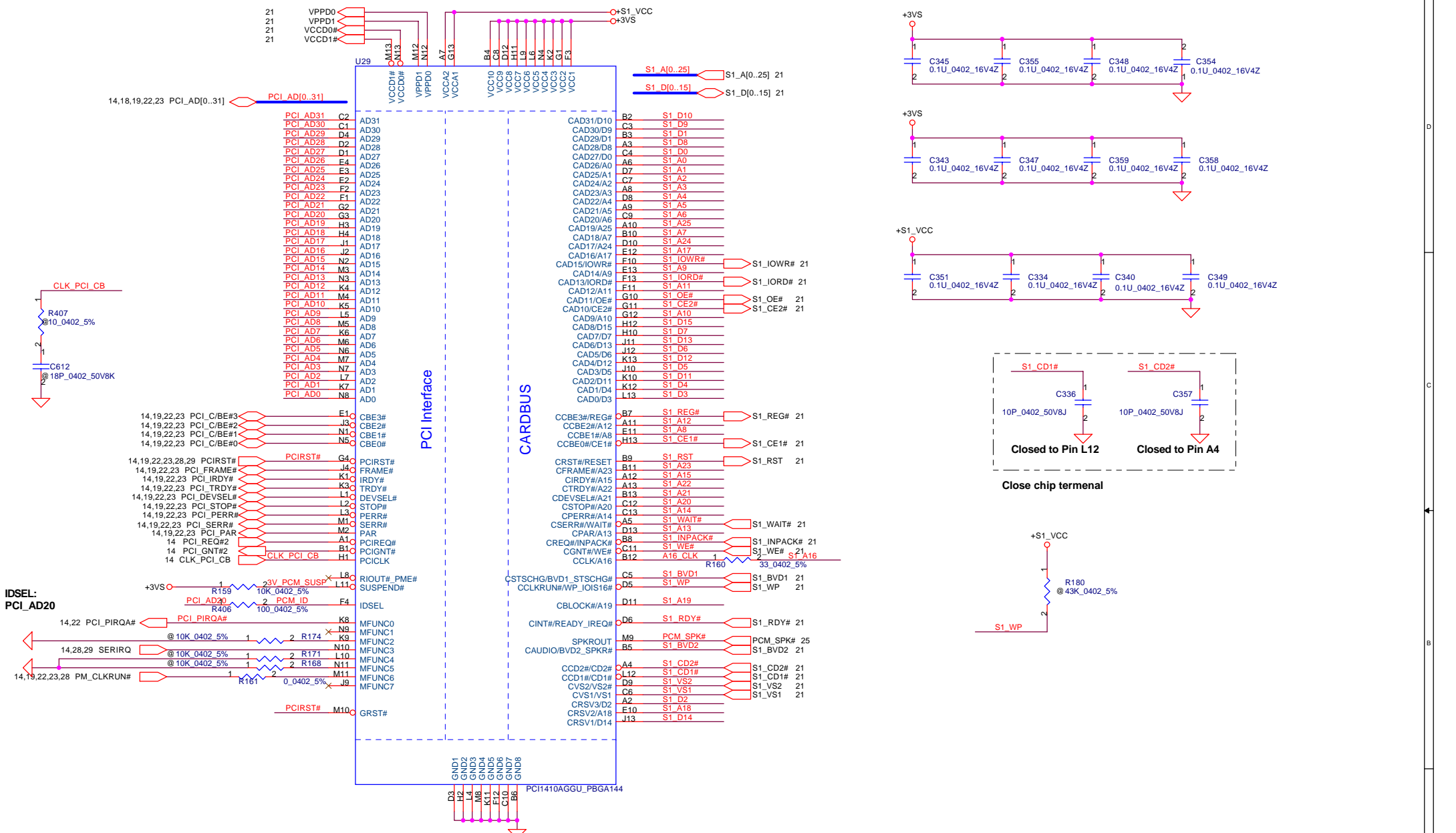


Termination plane should be coupled to chassis ground

Layout Note TS6121 pls close to conn.

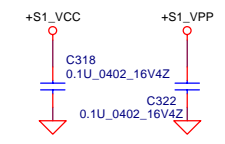
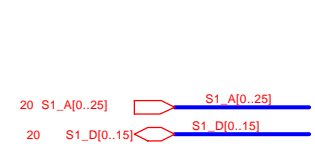
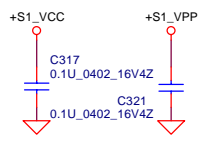
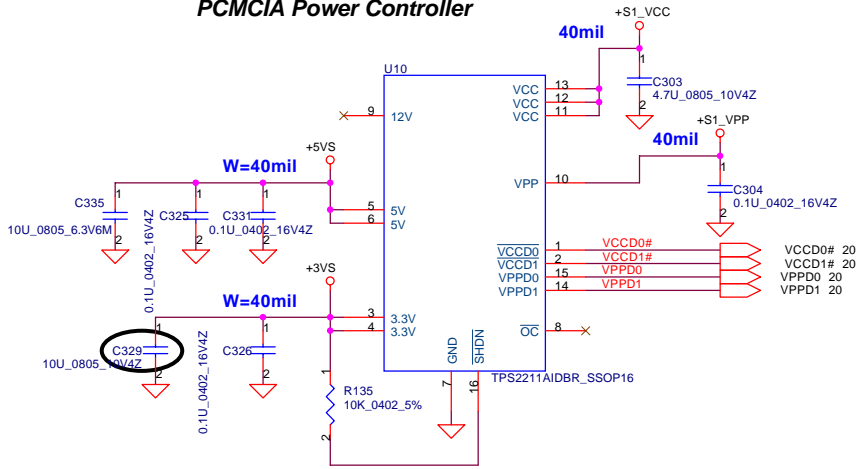


| | | | | | |
|---|-------------------------|--------------------|----------------------|--------------------------|-----------|
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| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 | Title | RTL8100CL |
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| Size | B | Document Number | HAZ00/BL10E (LA2861) | Rev | 1.0 |
| Date: | Monday, August 08, 2005 | Sheet | 19 | of | 42 |

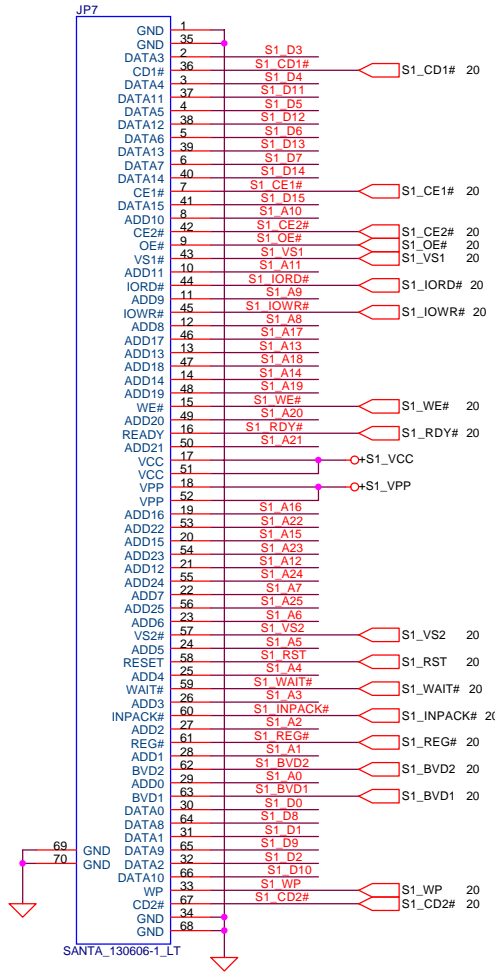


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| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 | Title | ENE-CB1410 |
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| Size B | Document Number HA200/BL10E (LA2861) | Date: | Thursday, August 04, 2005 | Sheet | 20 of 42 |
| Rev | 1.0 | | | | |

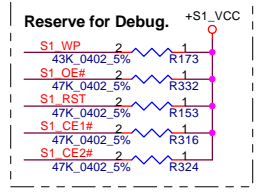
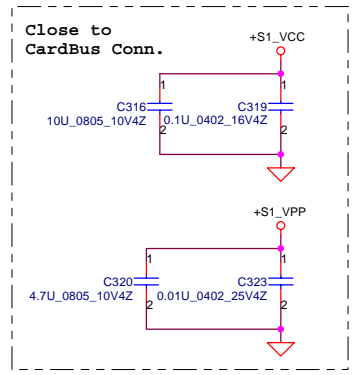
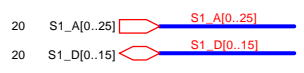
PCMCIA Power Controller



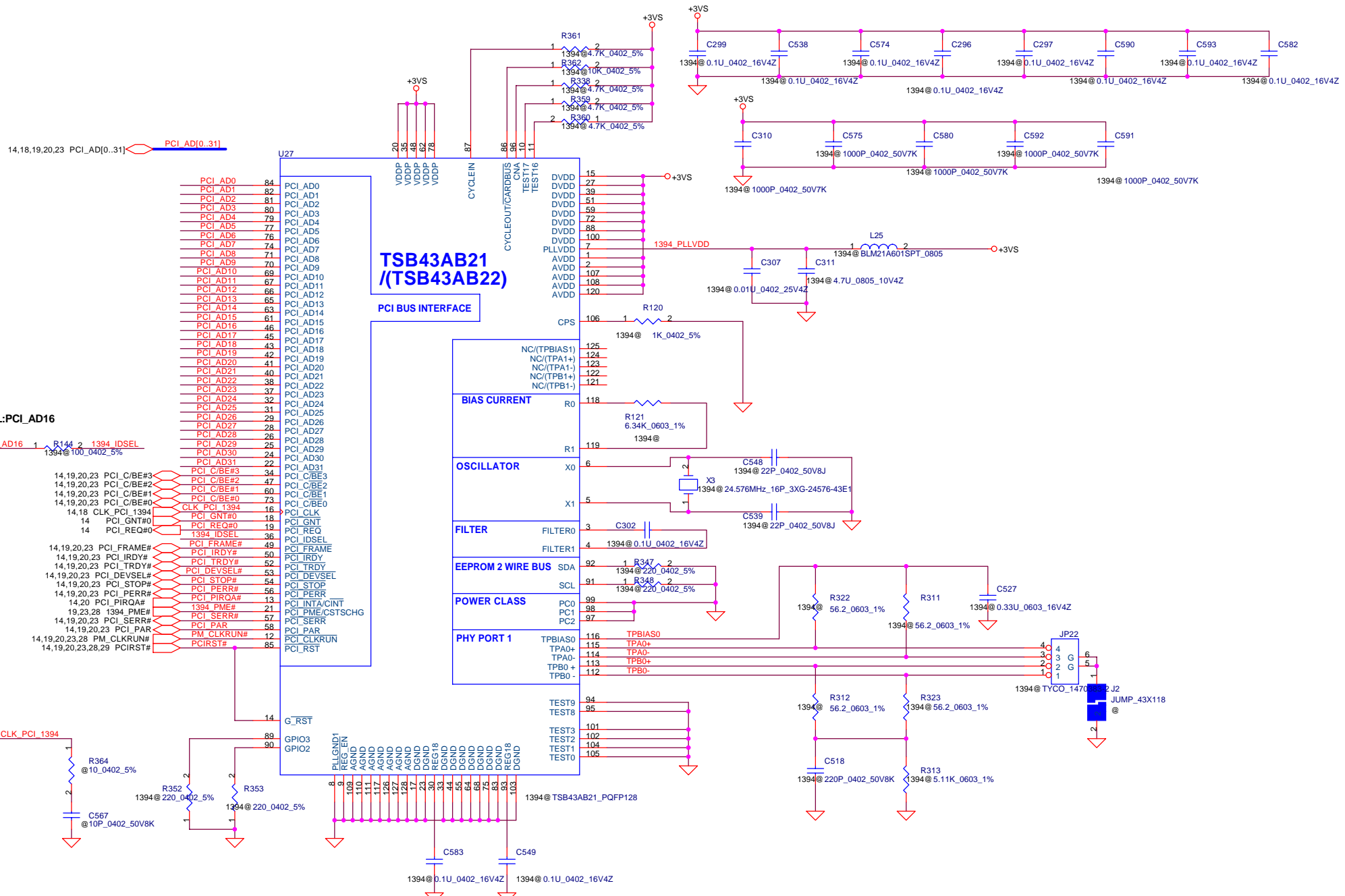
CardBus Socket



CardBus Socket

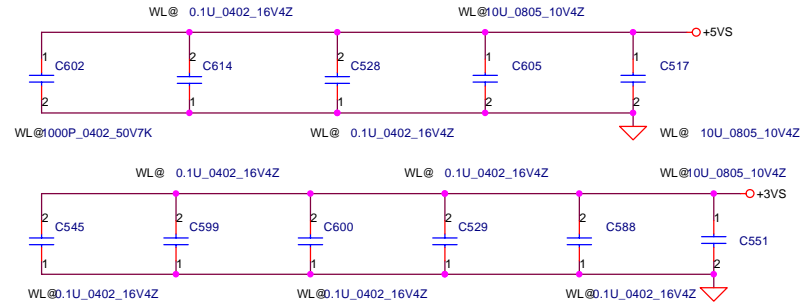
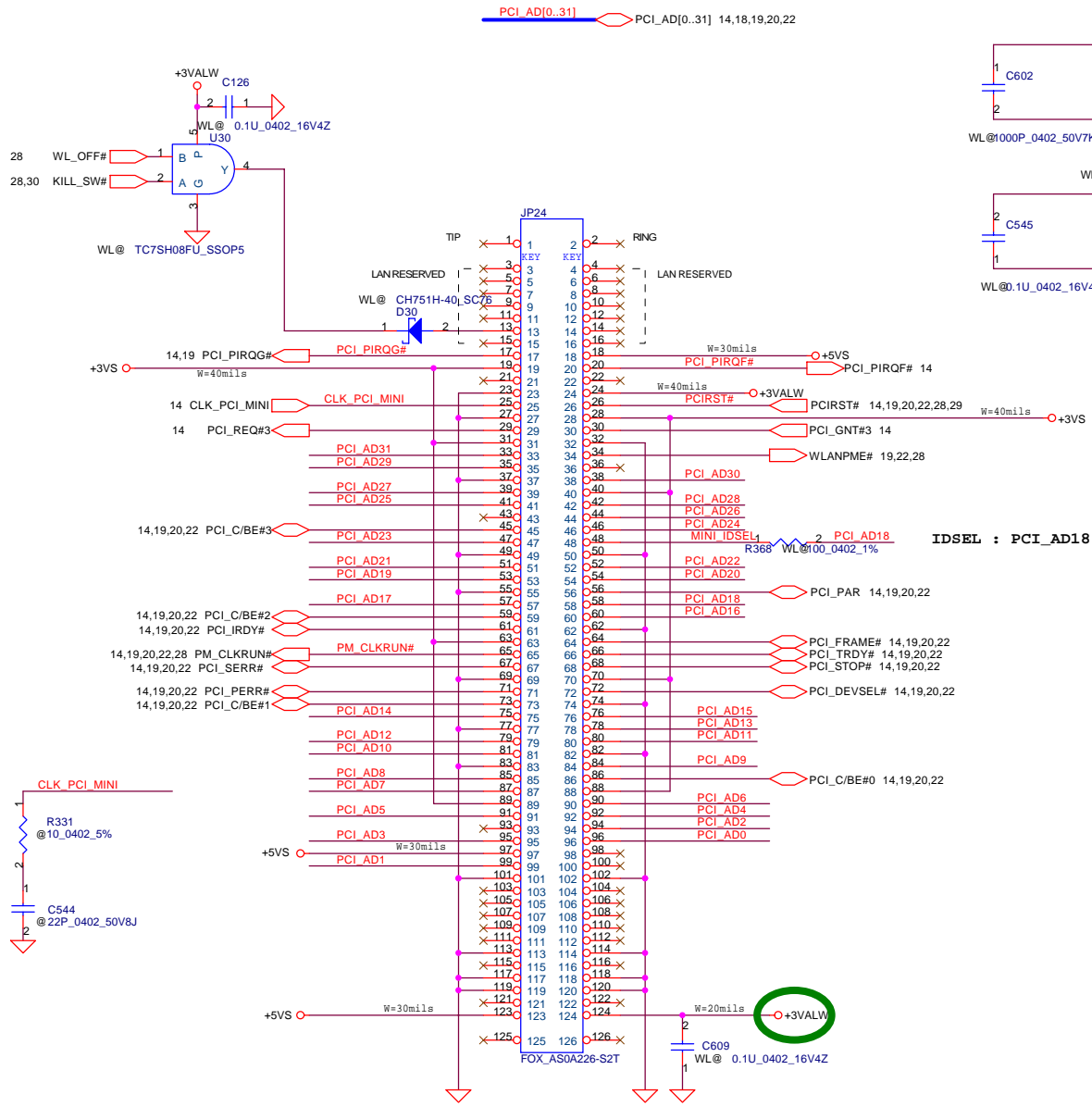


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|---|---------------------------|--------------------|------------|--------------------------|--------------------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 | Title | CARD BUS SOCKET |
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| Date: | Thursday, August 04, 2005 | Sheet | 21 of 42 | Rev | 1.0 |

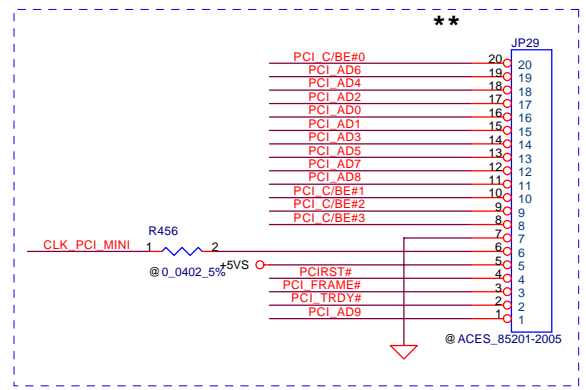


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| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 | Title | TSB43AB21 |
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| Size | B | Document Number | HAZ00/BL10E (LA2861) | Rev | 1.0 |
| Date: | Monday, August 08, 2005 | Sheet | 22 | of | 42 |

MINI_PCI SOCKET FOR WLAN (BOTTOM)

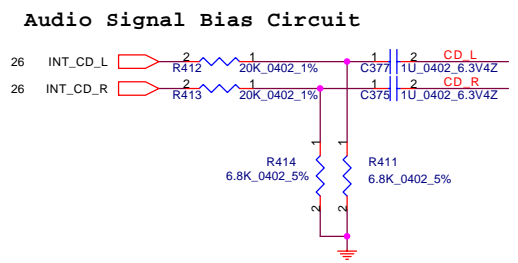
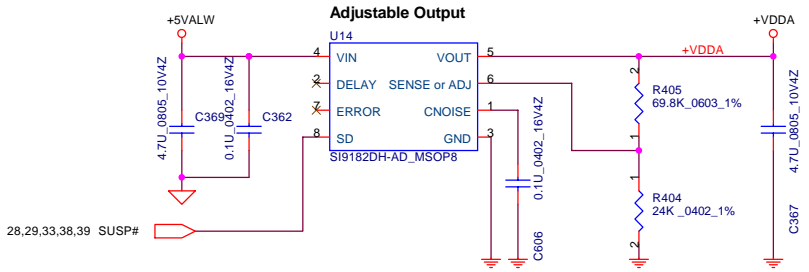


Port 80 Debug Card Connector

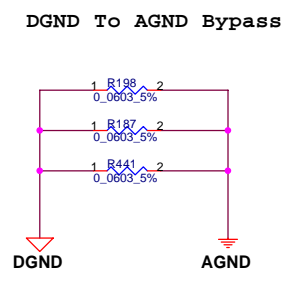
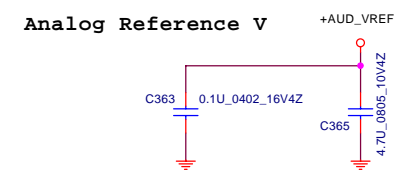
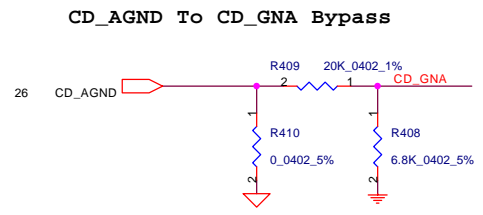
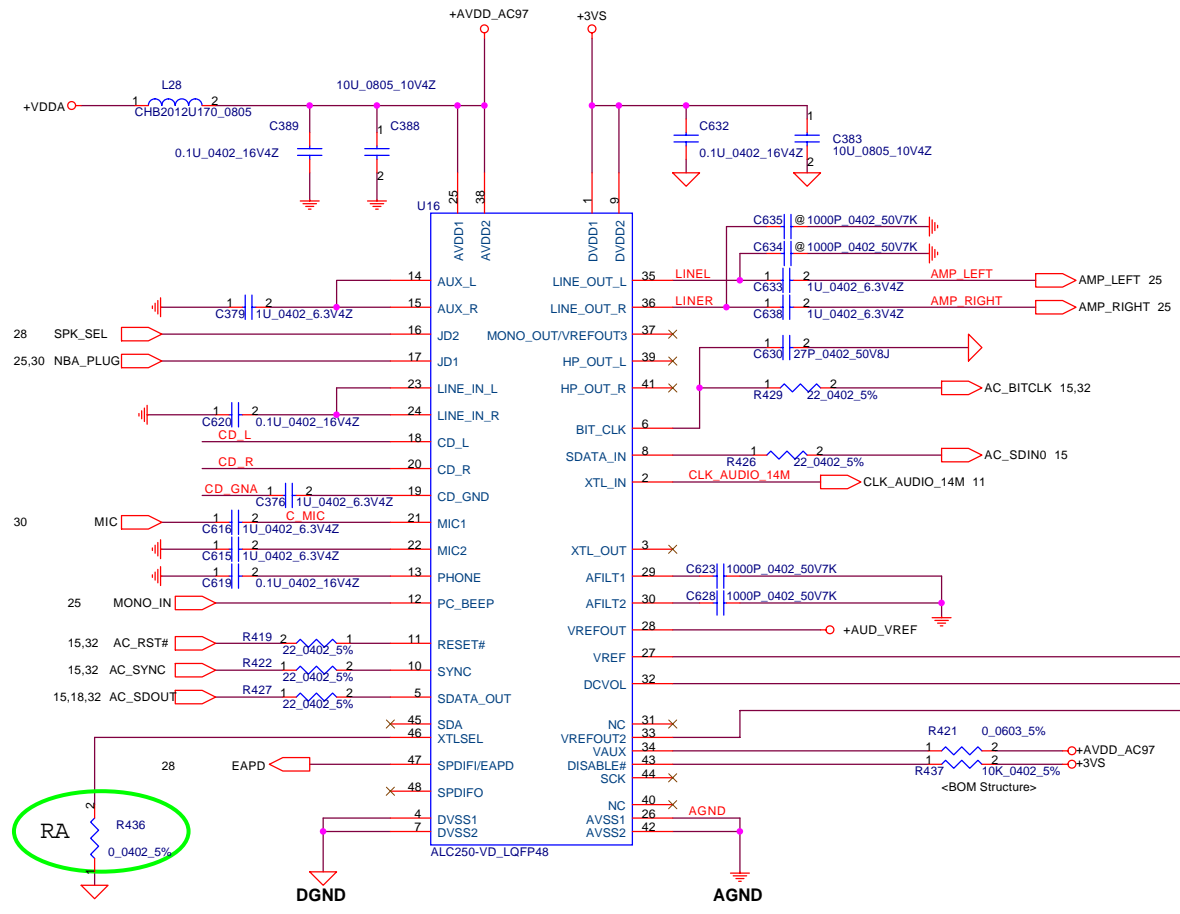


Place under MiniPCI Socket

| | | | | |
|---|-------------------------|-----------------|--------------------------|---------------|
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| Size | Document Number | | | Rev |
| B | HAZ00/BL10E (LA2861) | | | 1.0 |
| Date: | Monday, August 08, 2005 | Sheet | 23 | of 42 |

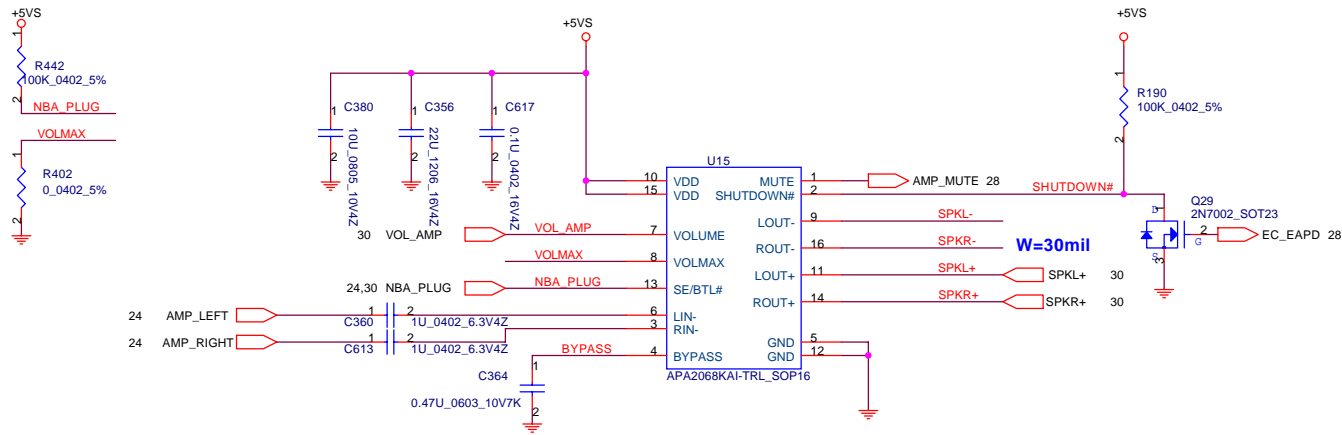


AC97 Codec

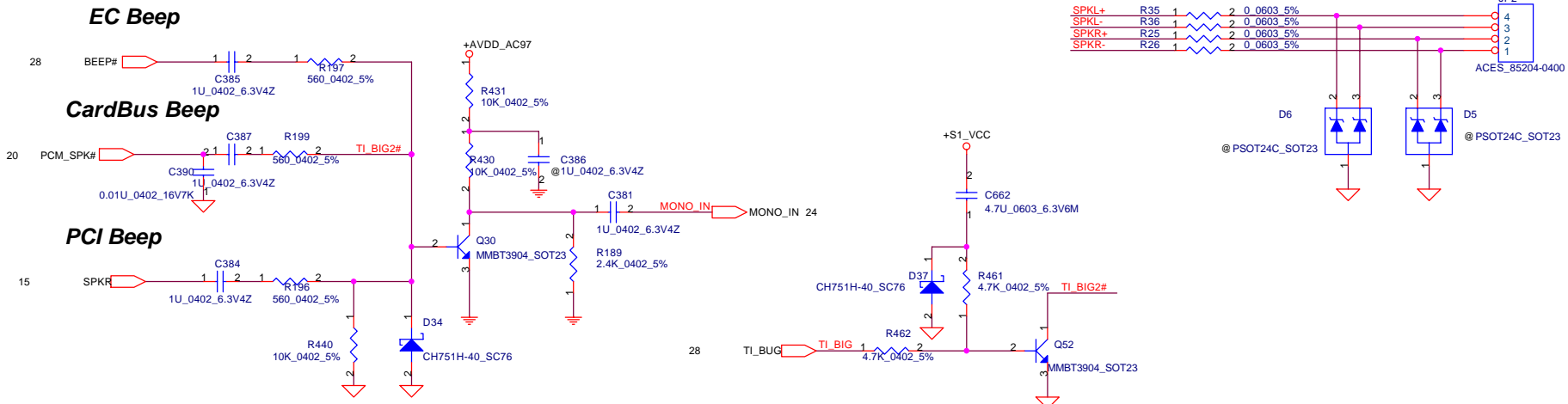


WITH 14.318MHz : RA POP
WITH 24.576MHz : RA DEPOP

| | | | | | |
|---|----------------------|-------------------------|------------|--------------------------|----------|
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| Size | Document Number | Date | | Rev | 1.0 |
| B | HA200/BL10E (LA2861) | Monday, August 08, 2005 | | Sheet | 24 of 42 |

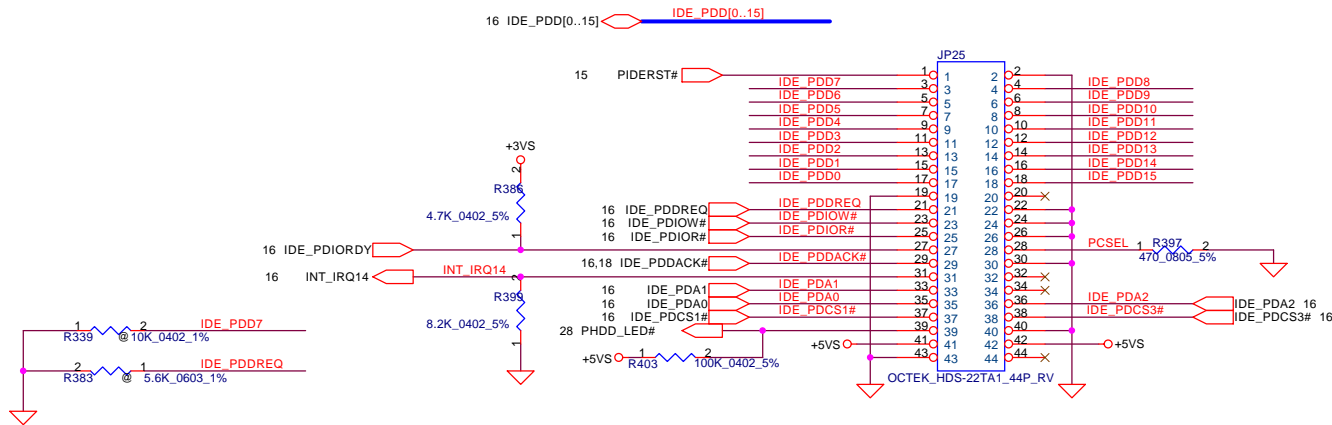


Speaker Conn.

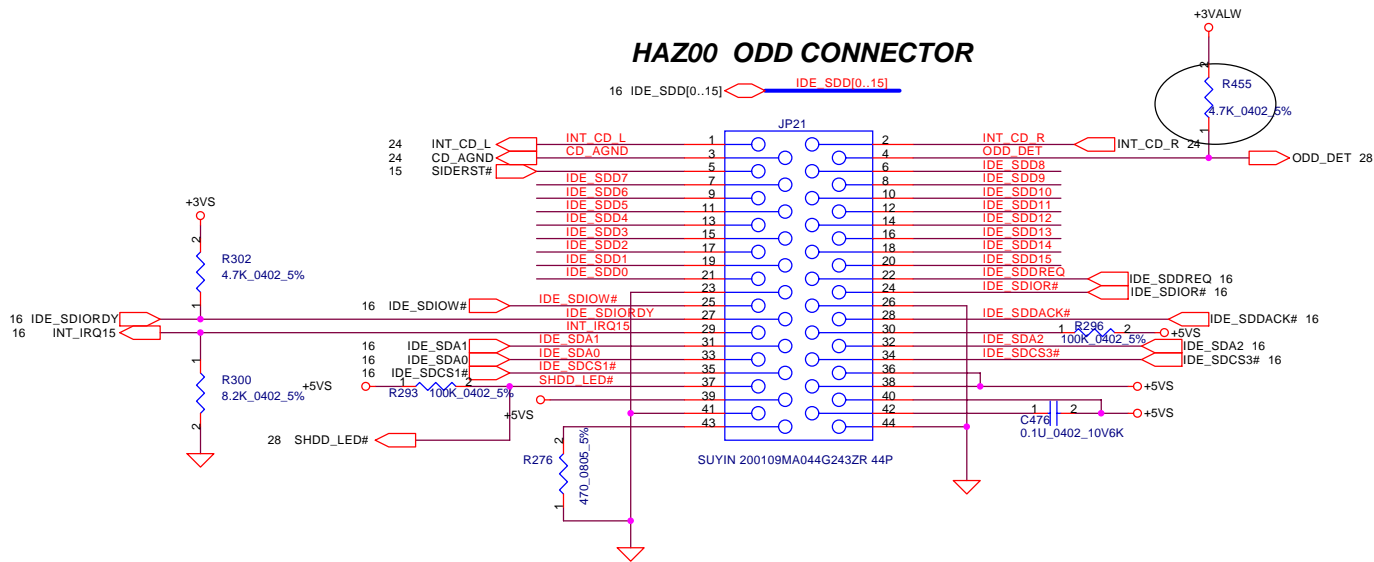


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| | | | | B | HAZ00/BL10E (LA2861) |
| | | | | Date: | Monday, August 08, 2005 |
| | | | | Sheet | 25 of 42 |
| | | | | Rev | 1.0 |

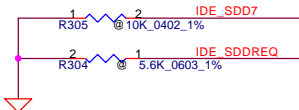
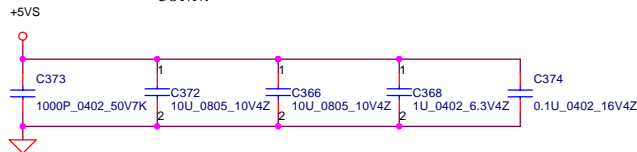
HDD CONNECTOR



HAZ00 ODD CONNECTOR

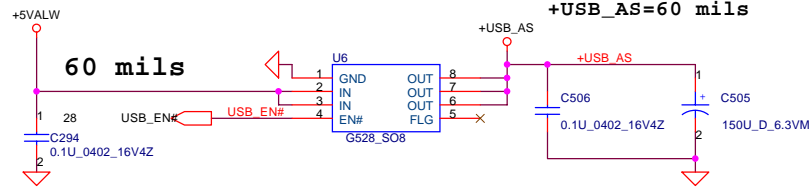


Placea caps. near HDD
CONN.

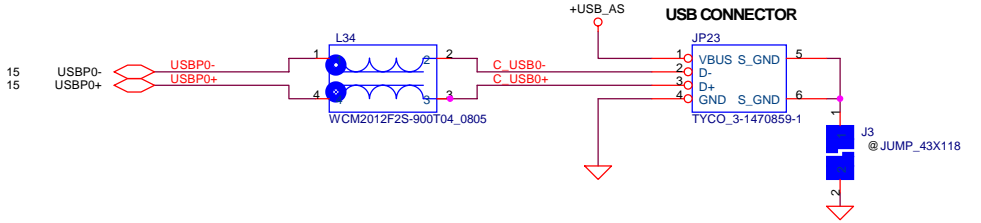


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| Size | Document Number | | | Rev |
| B | HAZ00/BL10E (LA2861) | | | 1.0 |
| Date: | Thursday, August 04, 2005 | Sheet | 26 of 42 | |

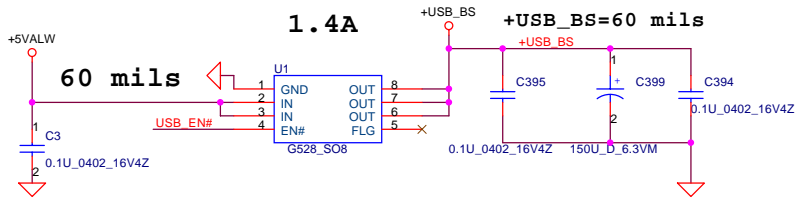
1.4A



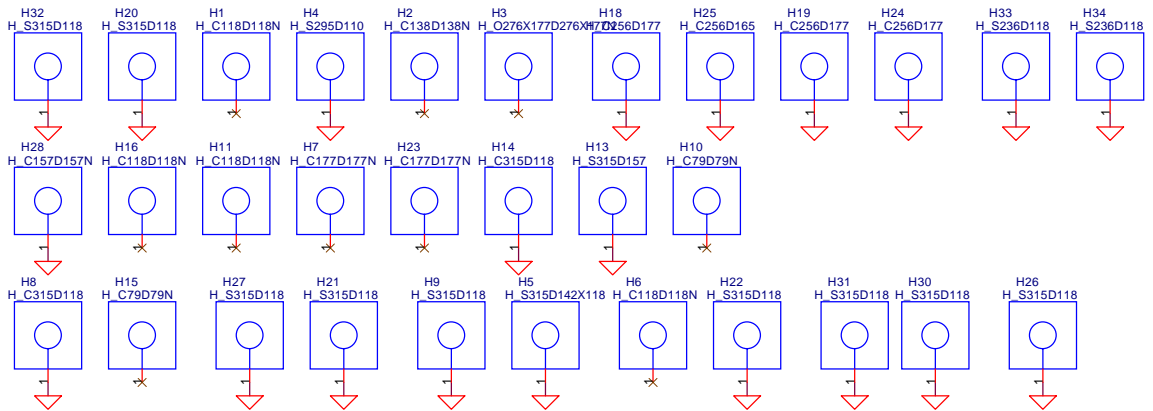
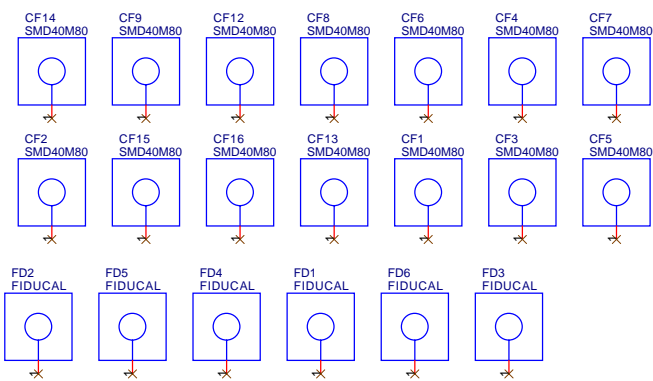
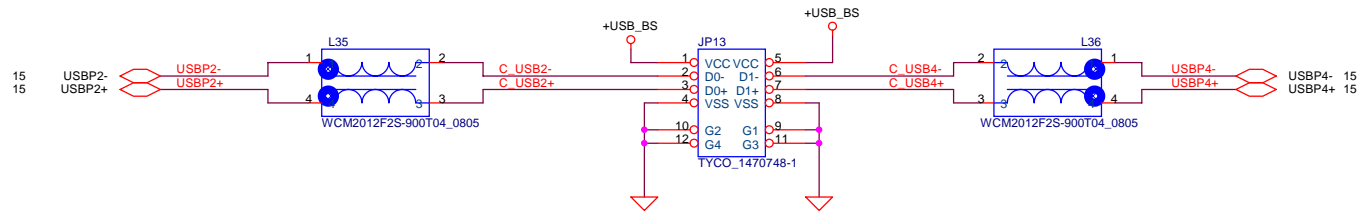
Keep 20 mils minimum spacing between USB signals and others signals



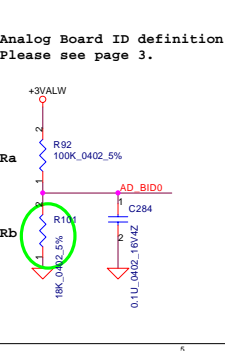
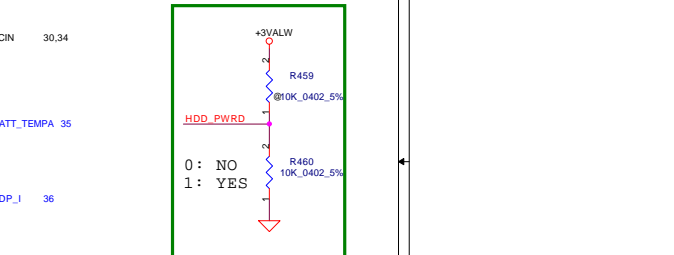
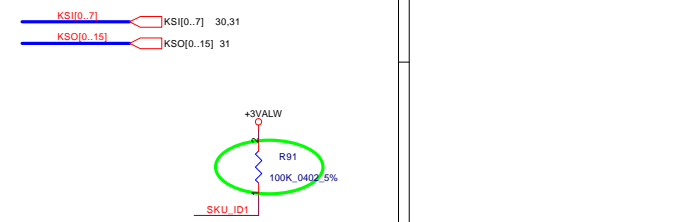
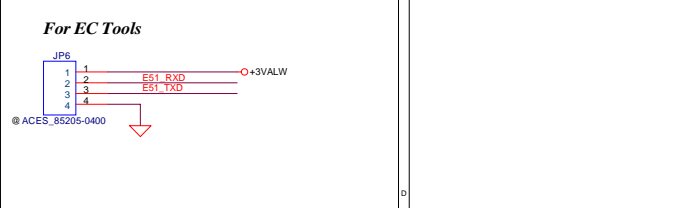
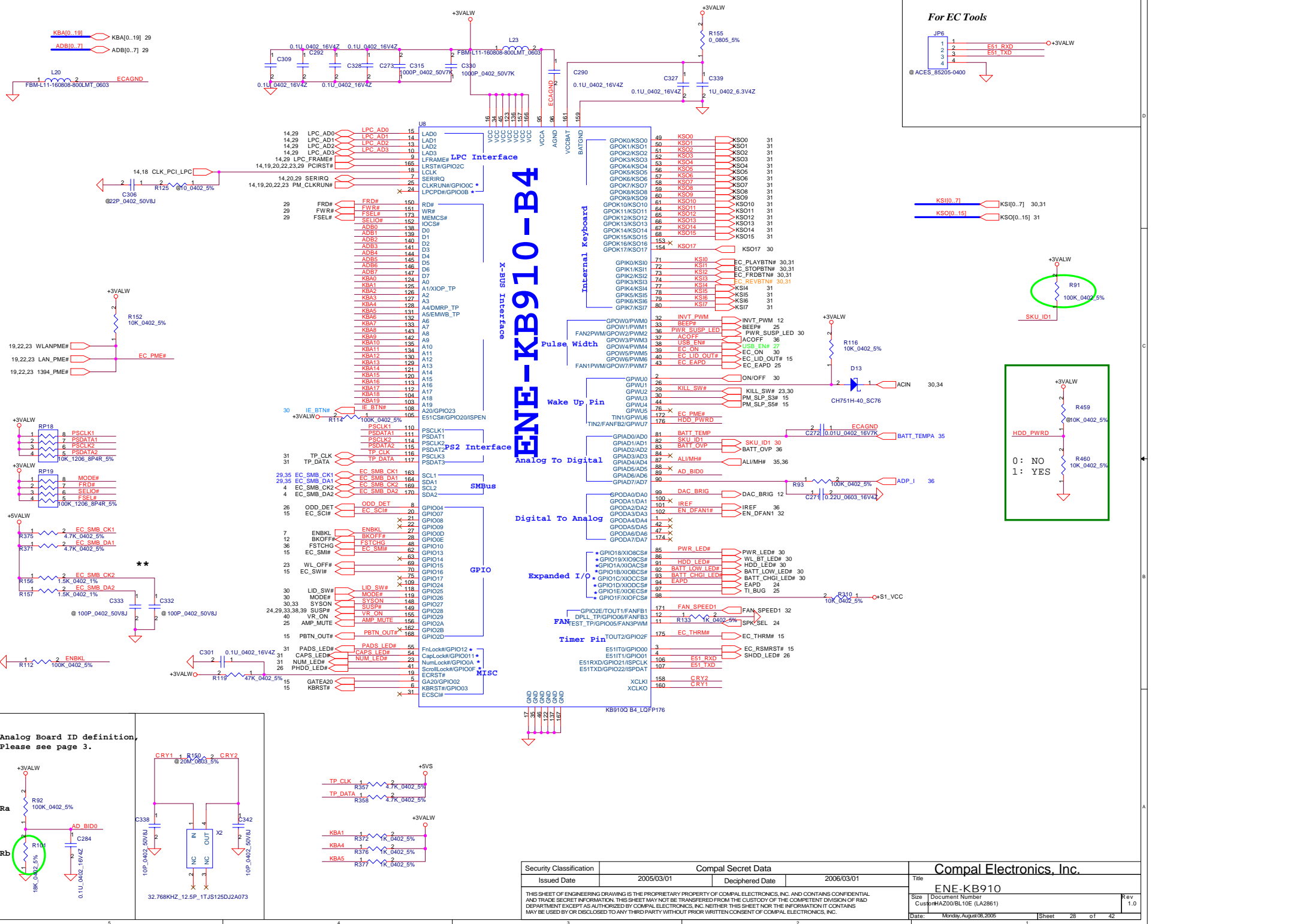
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USB CONNECTOR

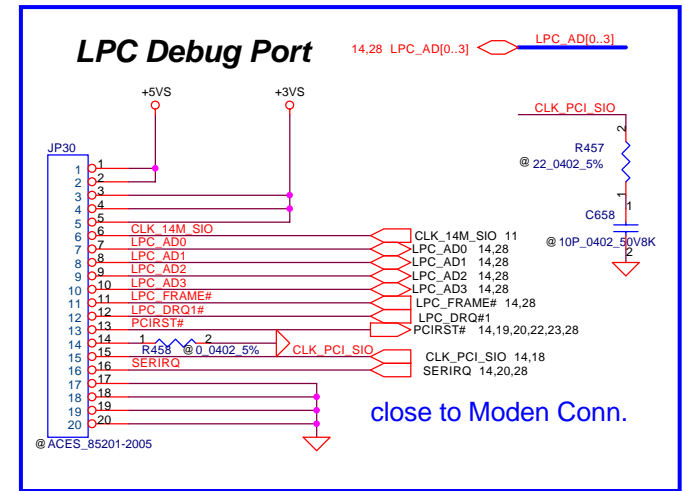
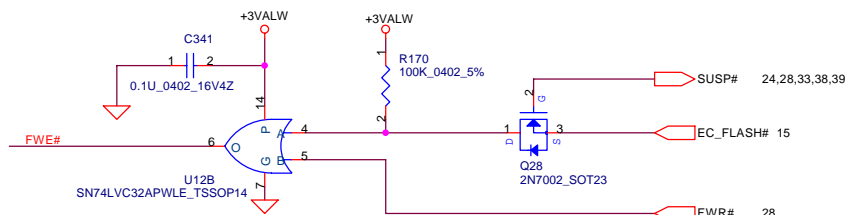
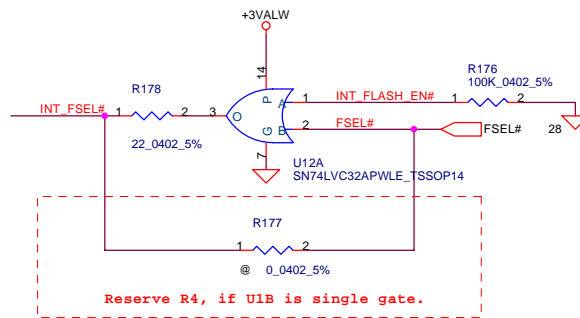
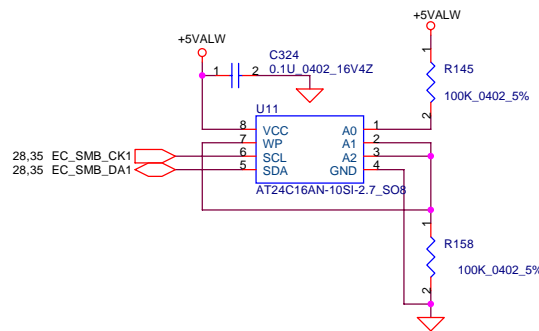


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| Size | B | Document Number | HAZ00/BL10E (LA2861) | Rev |
| Date: | Thursday, August 04, 2005 | Sheet | 27 | of 42 |

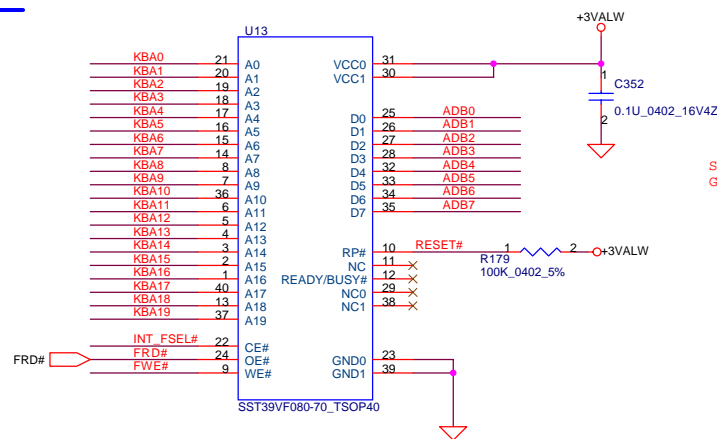


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| | | 2006/03/01 |
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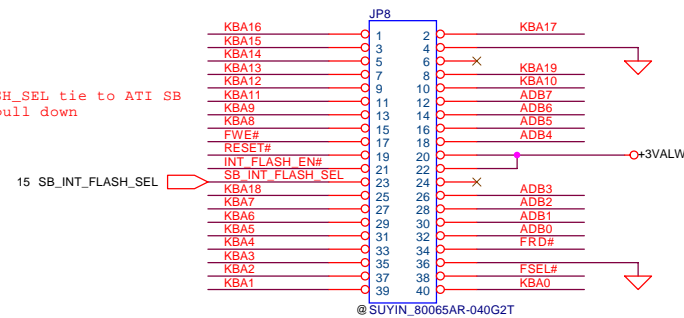
| Title | | |
|--------------------------|----------------------------|----------------|
| Compal Electronics, Inc. | | |
| ENE-KB910 | | |
| Size | Document Number | Rev |
| | Customer Reference: LA2861 | 1.0 |
| Date: | Monday, August 08, 2005 | Sheet 28 of 42 |



1MB Flash ROM

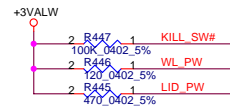
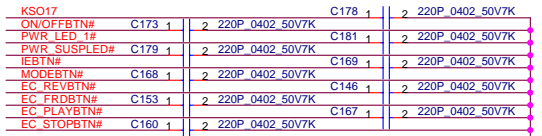
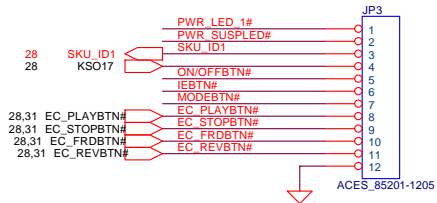


1MB ROM Socket

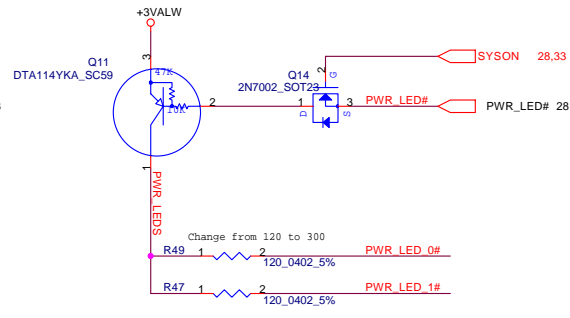
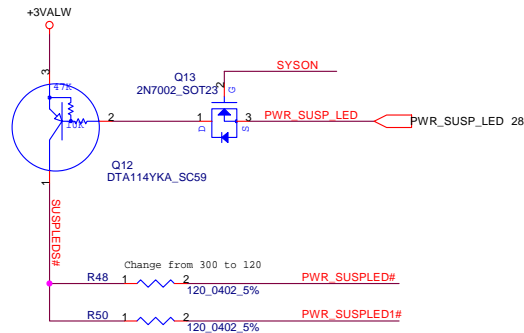
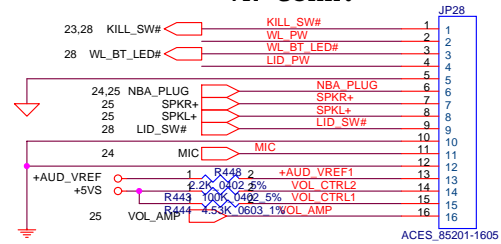


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| Size | Document Number | | | Rev |
| B | HAZ00/BL10E (LA2861) | | | 1.0 |
| Date: | Monday, August 08, 2005 | Sheet | 29 of 42 | |

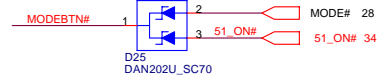
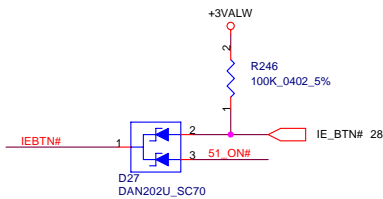
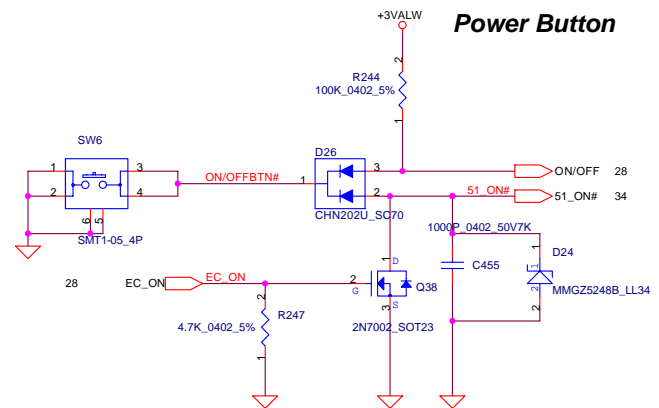
Switch Board Conn.



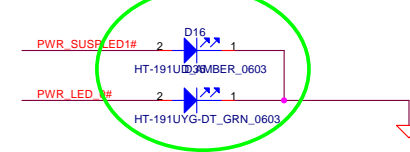
VR Conn.



Power Button



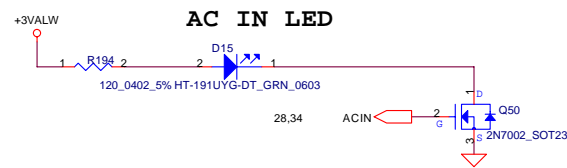
POWER/ON LED



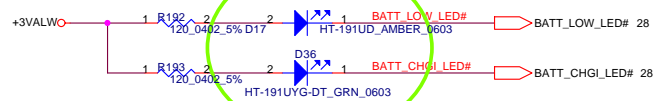
HDD LED



AC IN LED

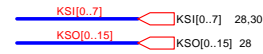


BATTERY CHG

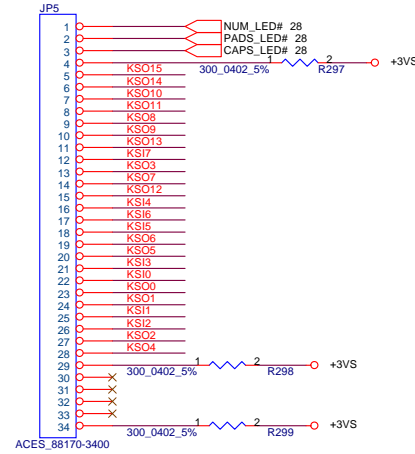
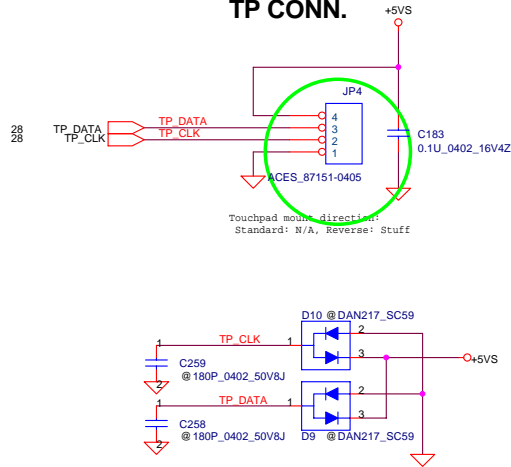


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| Date: | Thursday, August 04, 2005 | Sheet | 30 | of 42 |

INT_KBD CONN.



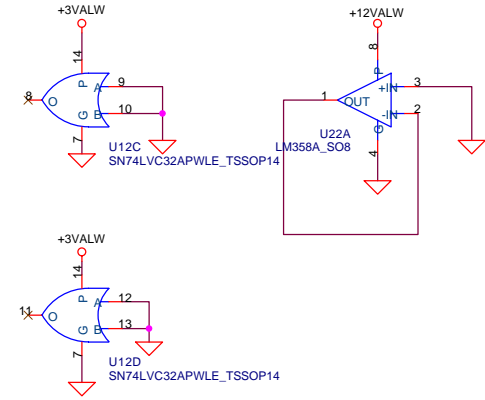
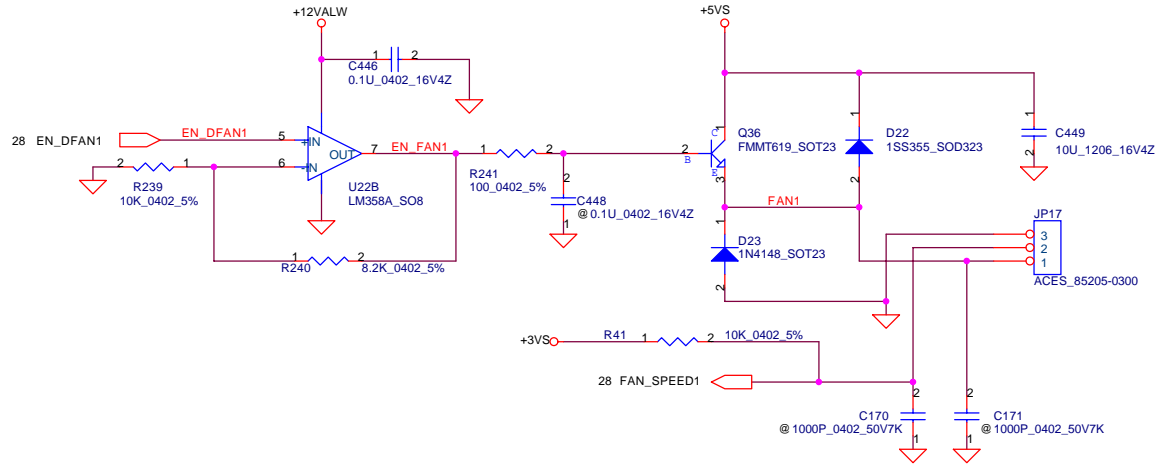
TP CONN.



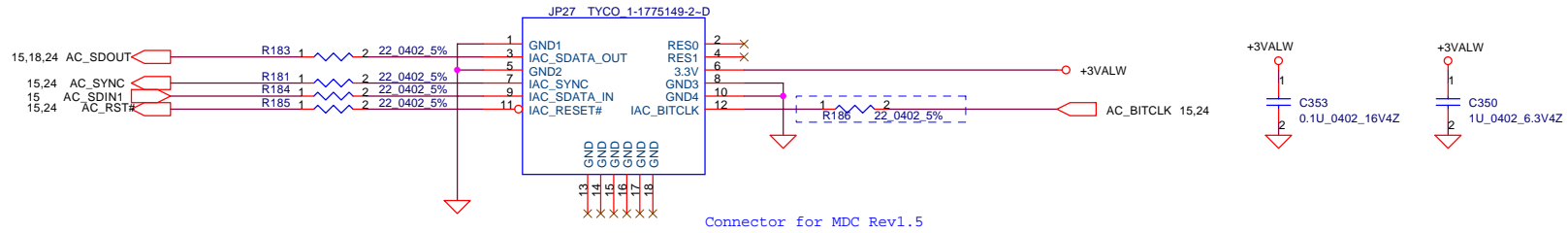
| | | | | | |
|------|------|-----------------|-----------|------|-----------------|
| KSO7 | C241 | 100P_0402_25V8K | KSO15 | C250 | 100P_0402_25V8K |
| KSO6 | C236 | 100P_0402_25V8K | KSO14 | C249 | 100P_0402_25V8K |
| KSO5 | C235 | 100P_0402_25V8K | KSO13 | C244 | 100P_0402_25V8K |
| KSO4 | C227 | 100P_0402_25V8K | KSO12 | C240 | 100P_0402_25V8K |
| KSO3 | C242 | 100P_0402_25V8K | KSI0 | C233 | 100P_0402_25V8K |
| KSI4 | C239 | 100P_0402_25V8K | KSO11 | C247 | 100P_0402_25V8K |
| KSO2 | C228 | 100P_0402_25V8K | KSO10 | C248 | 100P_0402_25V8K |
| KSO1 | C231 | 100P_0402_25V8K | KSI1 | C230 | 100P_0402_25V8K |
| KSO0 | C232 | 100P_0402_25V8K | KSI2 | C229 | 100P_0402_25V8K |
| KSI5 | C237 | 100P_0402_25V8K | KSO9 | C245 | 100P_0402_25V8K |
| KSI6 | C238 | 100P_0402_25V8K | KSI3 | C234 | 100P_0402_25V8K |
| KSI7 | C243 | 100P_0402_25V8K | PADS_LED# | C252 | 100P_0402_25V8K |
| KSO8 | C246 | 100P_0402_25V8K | NUM_LED# | C253 | 100P_0402_25V8K |
| | | | CAPS_LED# | C251 | 100P_0402_25V8K |

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| | | | | Size | Document Number | Rev |
| Date: | Thursday, August 04, 2005 | Sheet | 31 | of | 42 | 1.0 |

FAN Conn

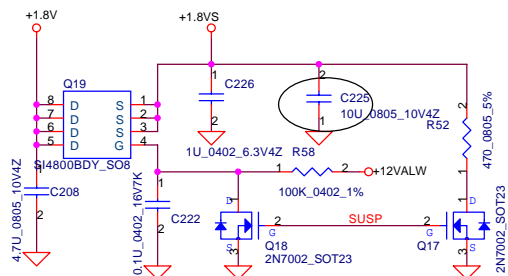


MDC CONN.

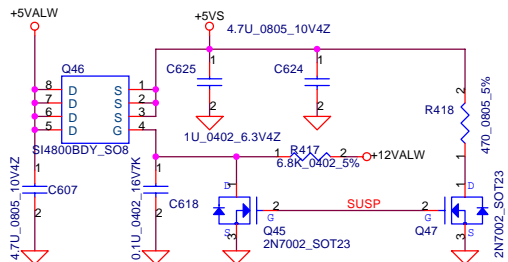


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| | | | | B | HA200/BL10E (LA2861) |
| | | | | Date: | Thursday, August 04, 2005 |
| | | | | Sheet | 32 of 42 |
| | | | | Rev | 1.0 |

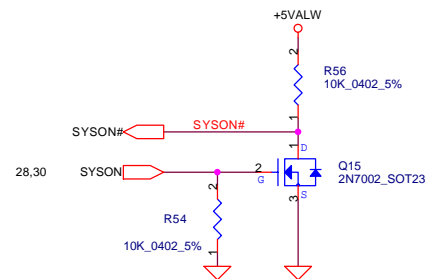
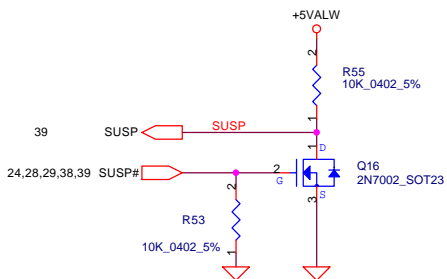
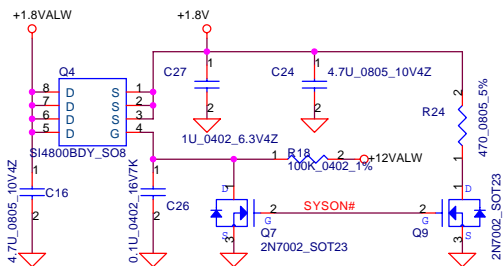
+1.8VALW TO +1.8VS



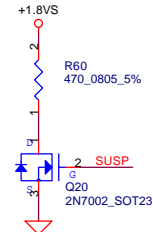
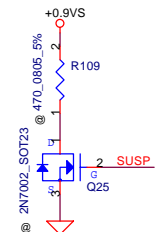
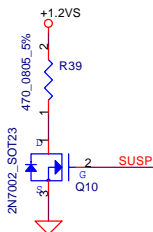
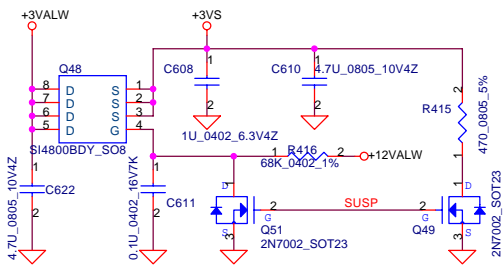
+5VALW TO +5VS



+1.8VALW TO +1.8V

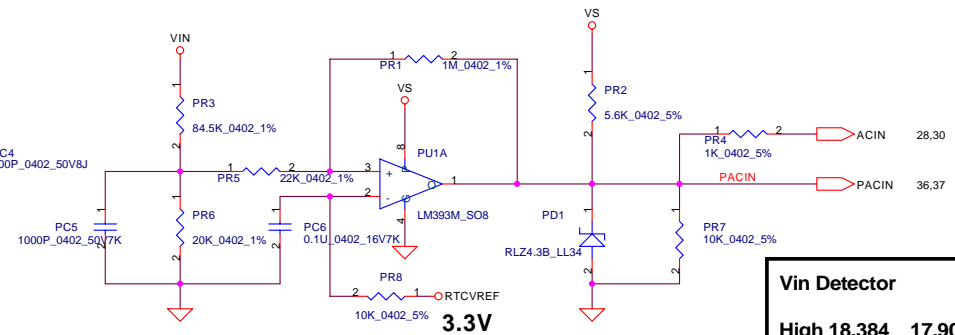
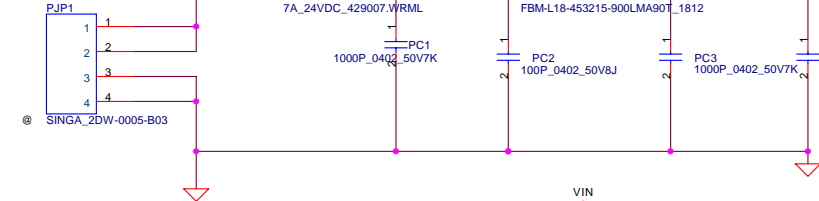


+3VALW TO +3VS

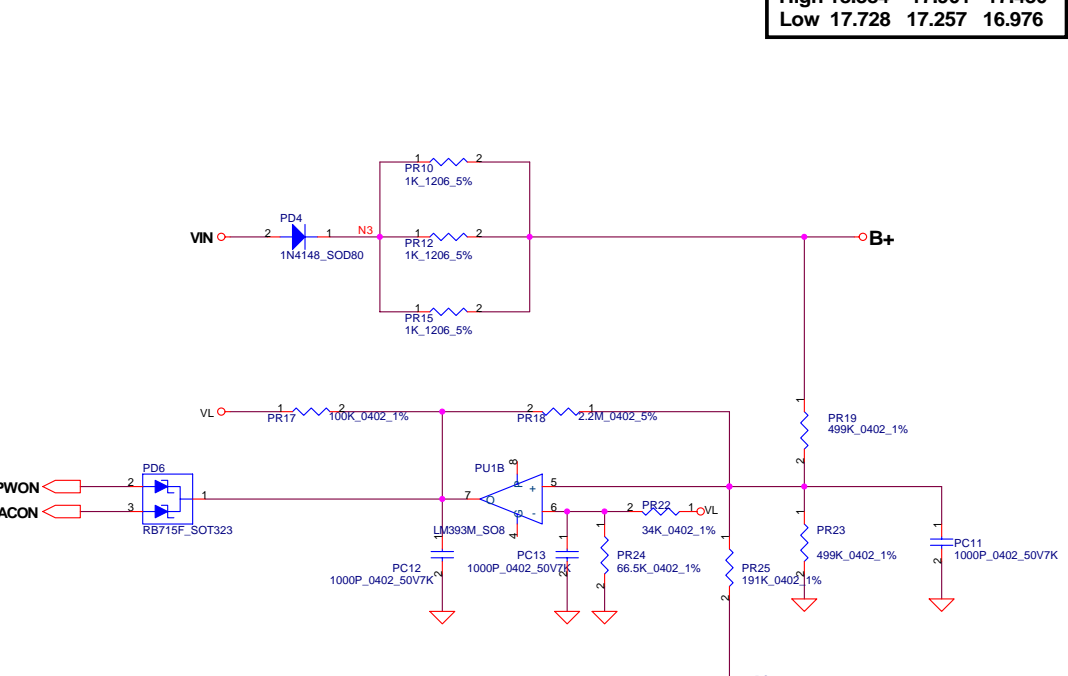
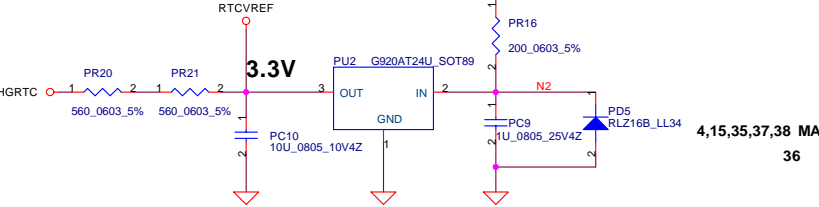
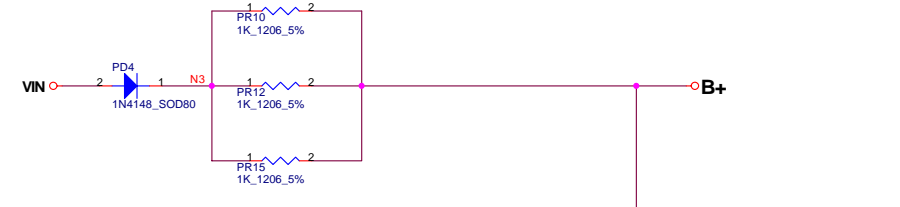
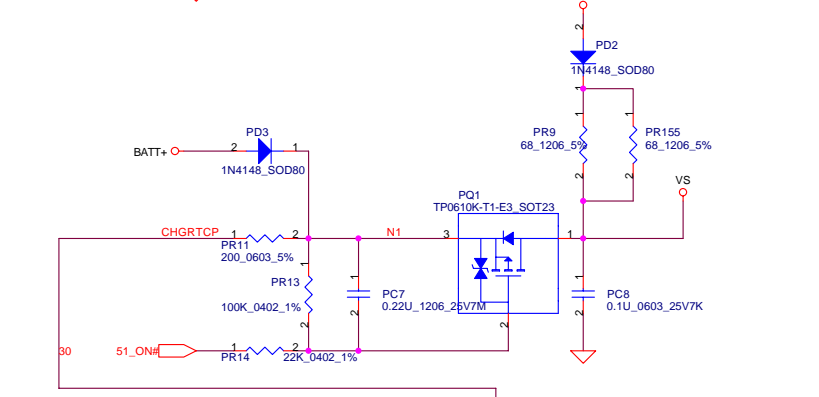


| | | | | | |
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| Size | B | Document Number | HA200/BL10E (LA2861) | Rev | 1.0 |
| Date: | Monday, August 08, 2005 | | Sheet | 33 | of 42 |

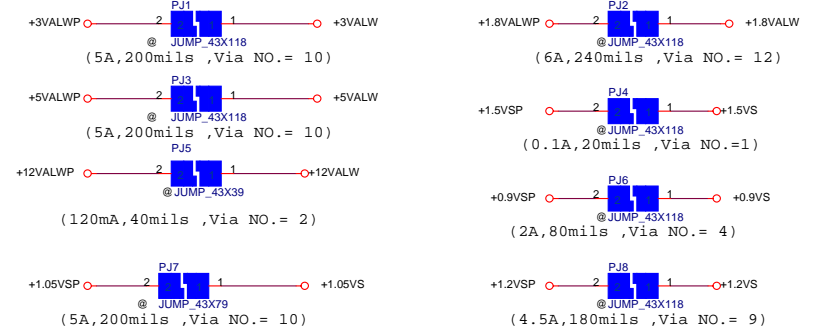
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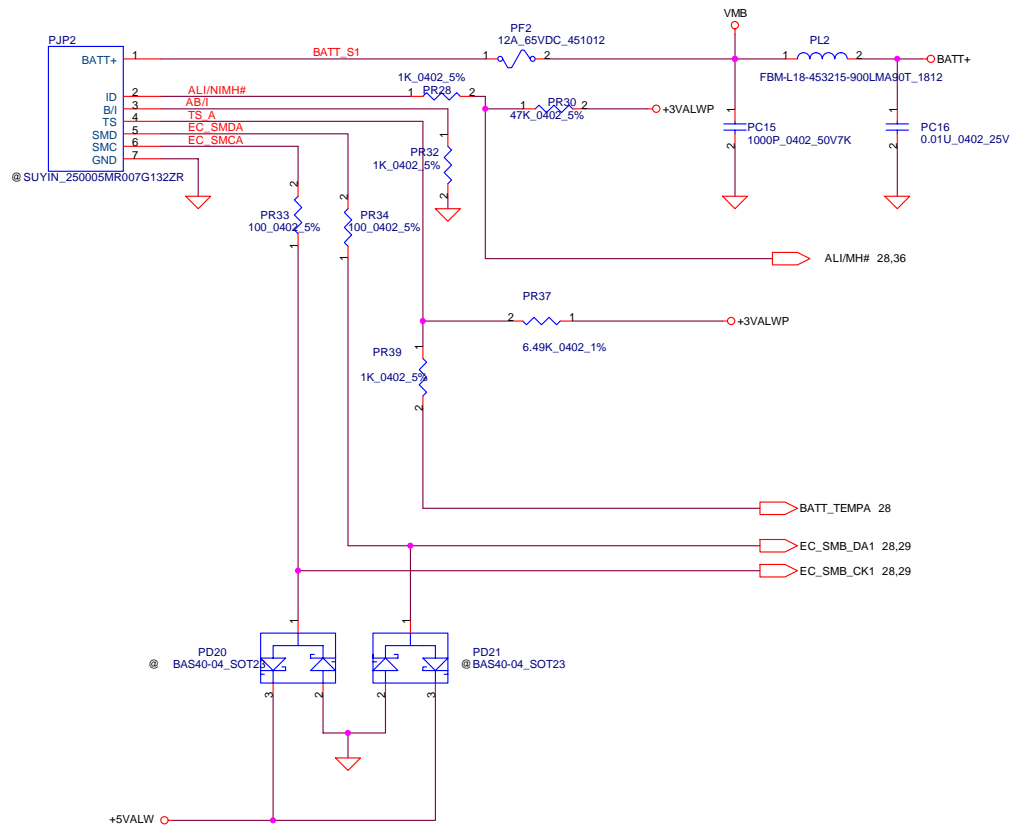
Vin Detector
 High 18.384 17.901 17.430
 Low 17.728 17.257 16.976



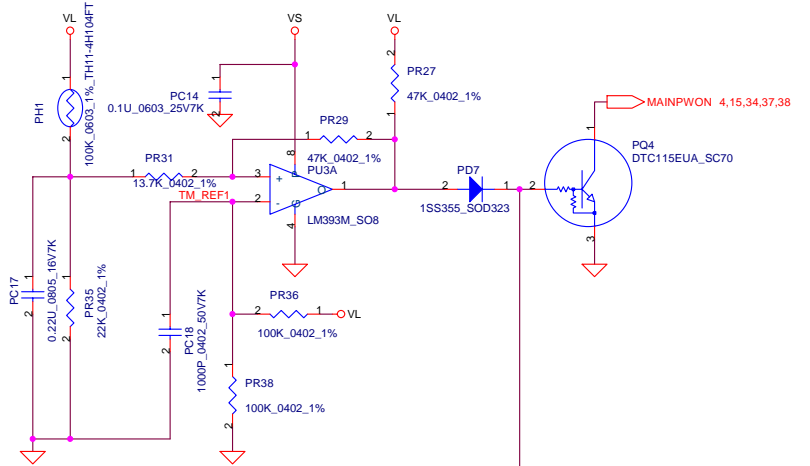
Precharge detector
 15.97V/14.84V FOR
 ADAPTOR



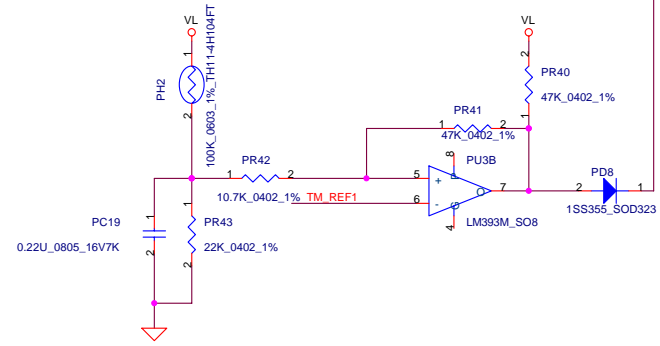
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| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 | Title | DCIN & DETECTOR |
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| Size | Document Number | | | | Rev |
| Date: Thursday, August 04, 2005 | Sheet | 34 | of | 42 | 0.3 |



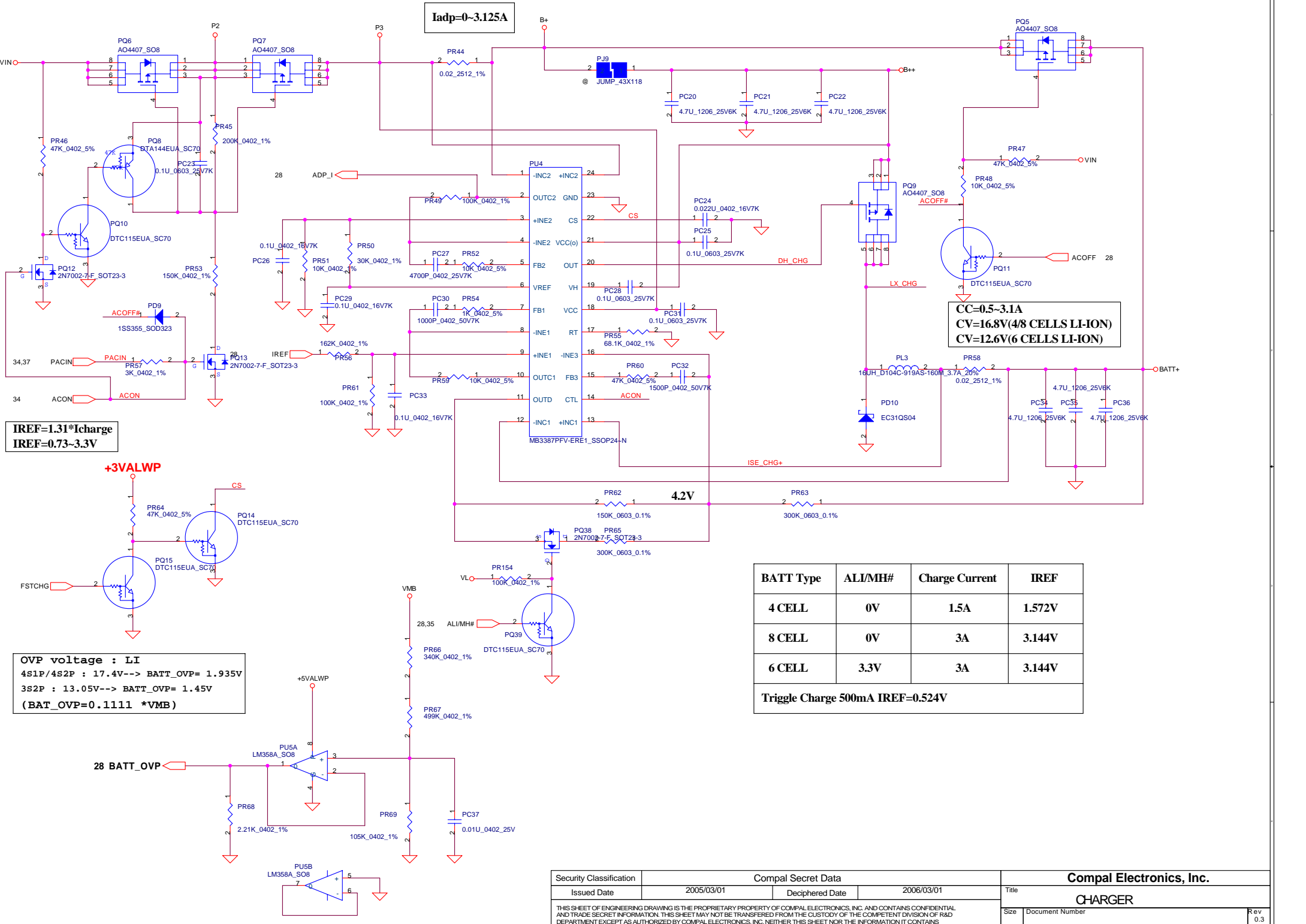
PH1 under CPU botten side :
 CPU thermal protection at 84 degree C
 Recovery at 45 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 45 degree C



| | | | | | |
|---|--------------------|-----------------|------------|---------------------------------|-----------------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | |
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| | | | | | Rev 0.3 |
| | | | | Date: Thursday, August 04, 2005 | Sheet 35 of 42 |



Iadp=0~3.125A

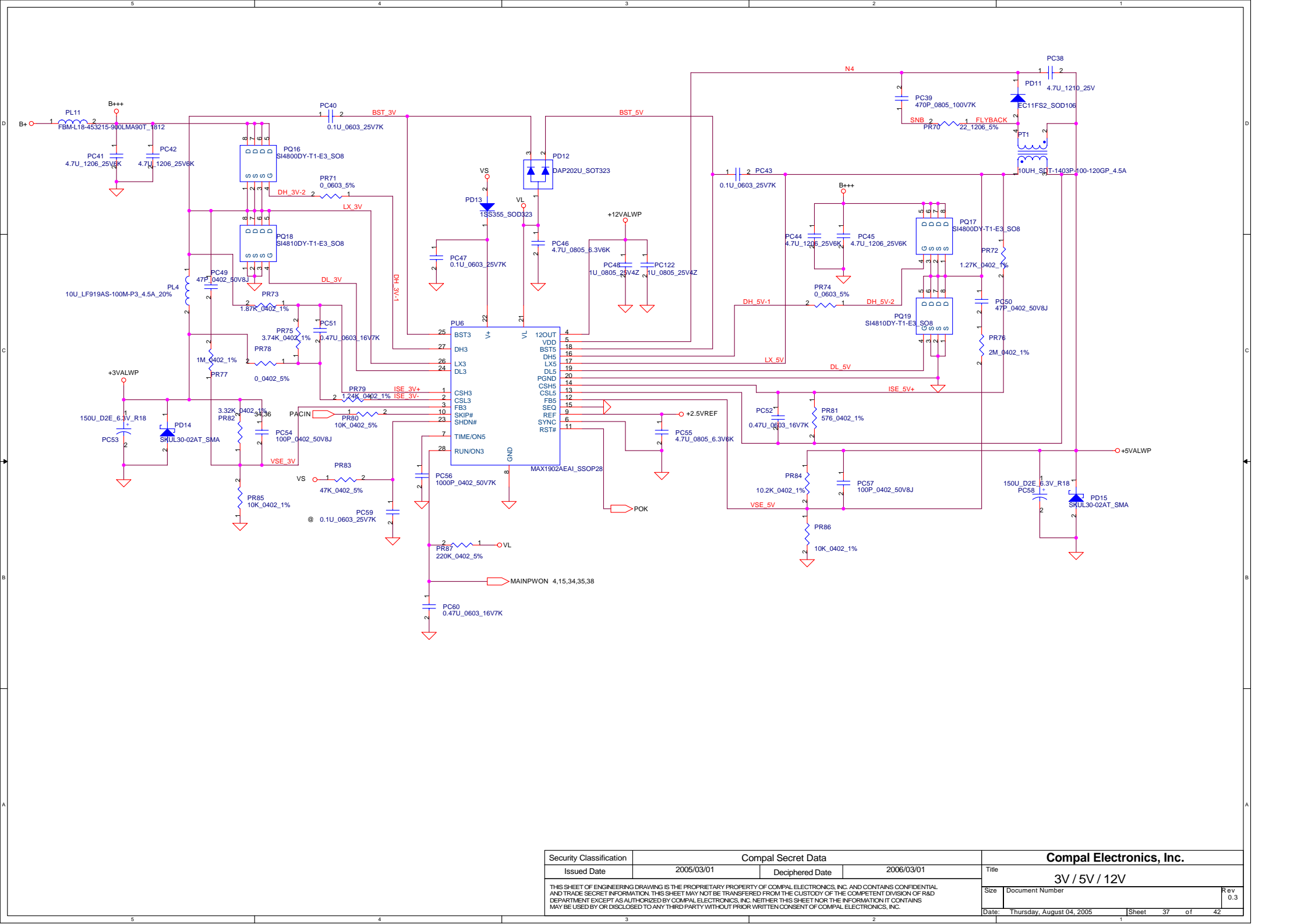
CC=0.5~3.1A
 CV=16.8V(4/8 CELLS LI-ION)
 CV=12.6V(6 CELLS LI-ION)

IREF=1.31*Icharge
 IREF=0.73~3.3V

OVP voltage : LI
 4S1P/4S2P : 17.4V--> BATT_OVP= 1.935V
 3S2P : 13.05V--> BATT_OVP= 1.45V
 (BATT_OVP=0.1111 *VMB)

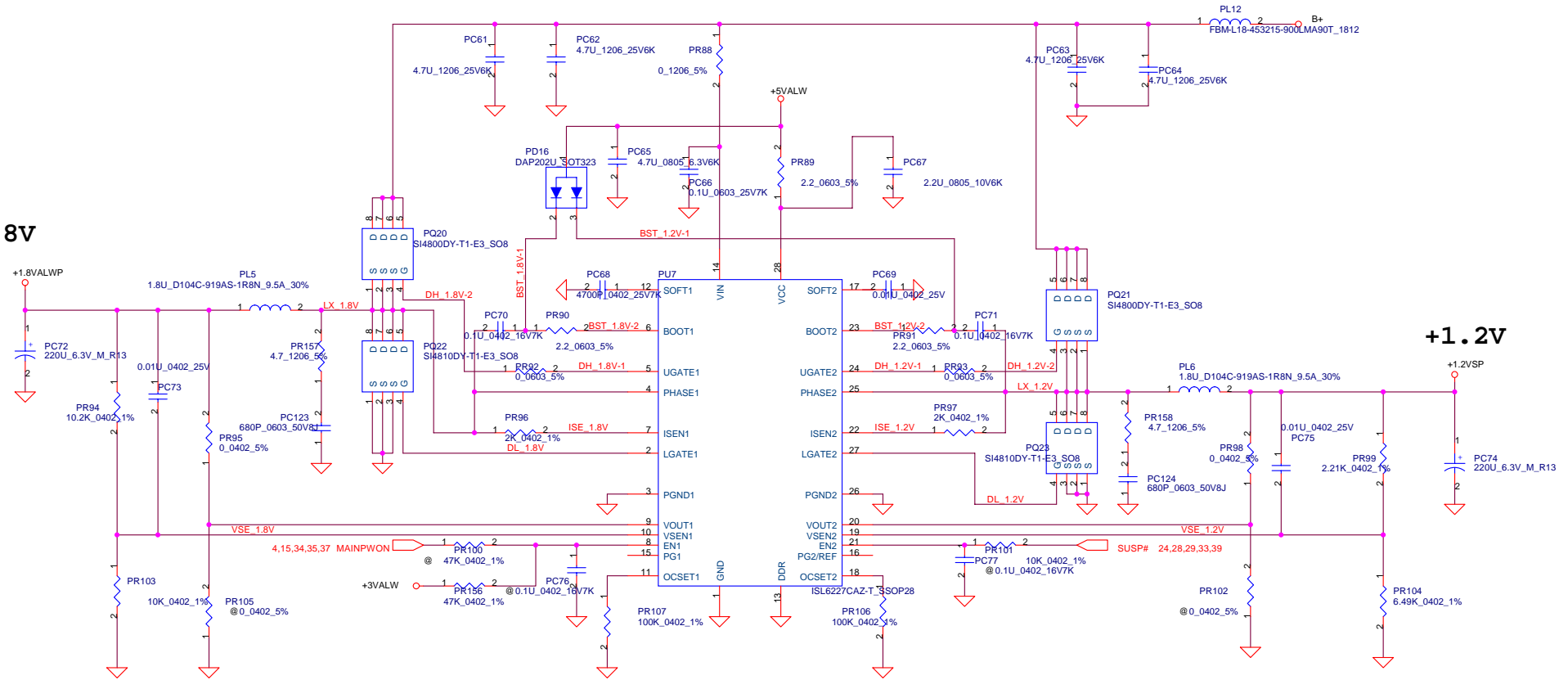
| BATT Type | ALI/MH# | Charge Current | IREF |
|-----------|---------|----------------|--------|
| 4 CELL | 0V | 1.5A | 1.572V |
| 8 CELL | 0V | 3A | 3.144V |
| 6 CELL | 3.3V | 3A | 3.144V |

Triggle Charge 500mA IREF=0.524V

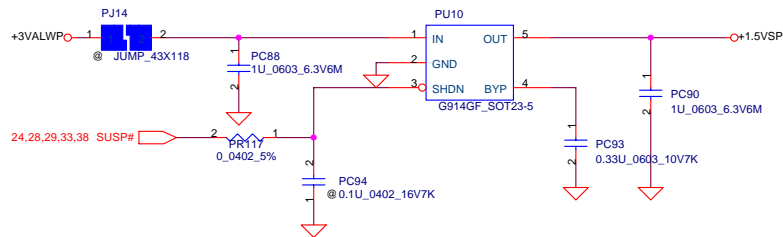
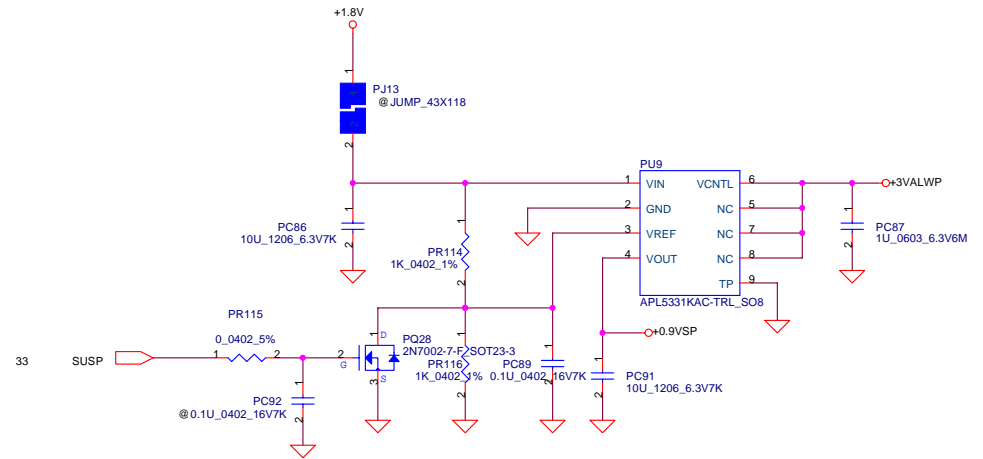
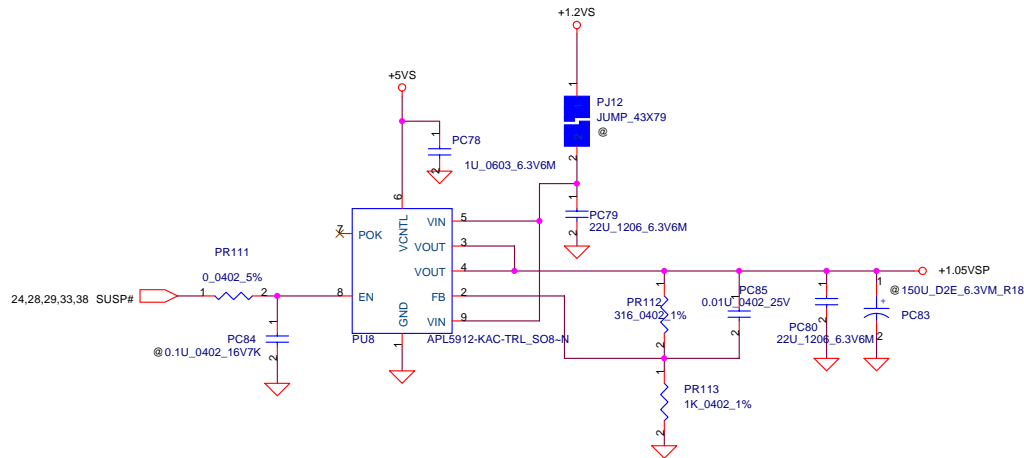


| | | | | |
|---|--------------------|-----------------|------------|---------------------------------|
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| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 | 3V / 5V / 12V |
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| | | | | Document Number |
| | | | | Rev 0.3 |
| | | | | Date: Thursday, August 04, 2005 |
| | | | | Sheet 37 of 42 |

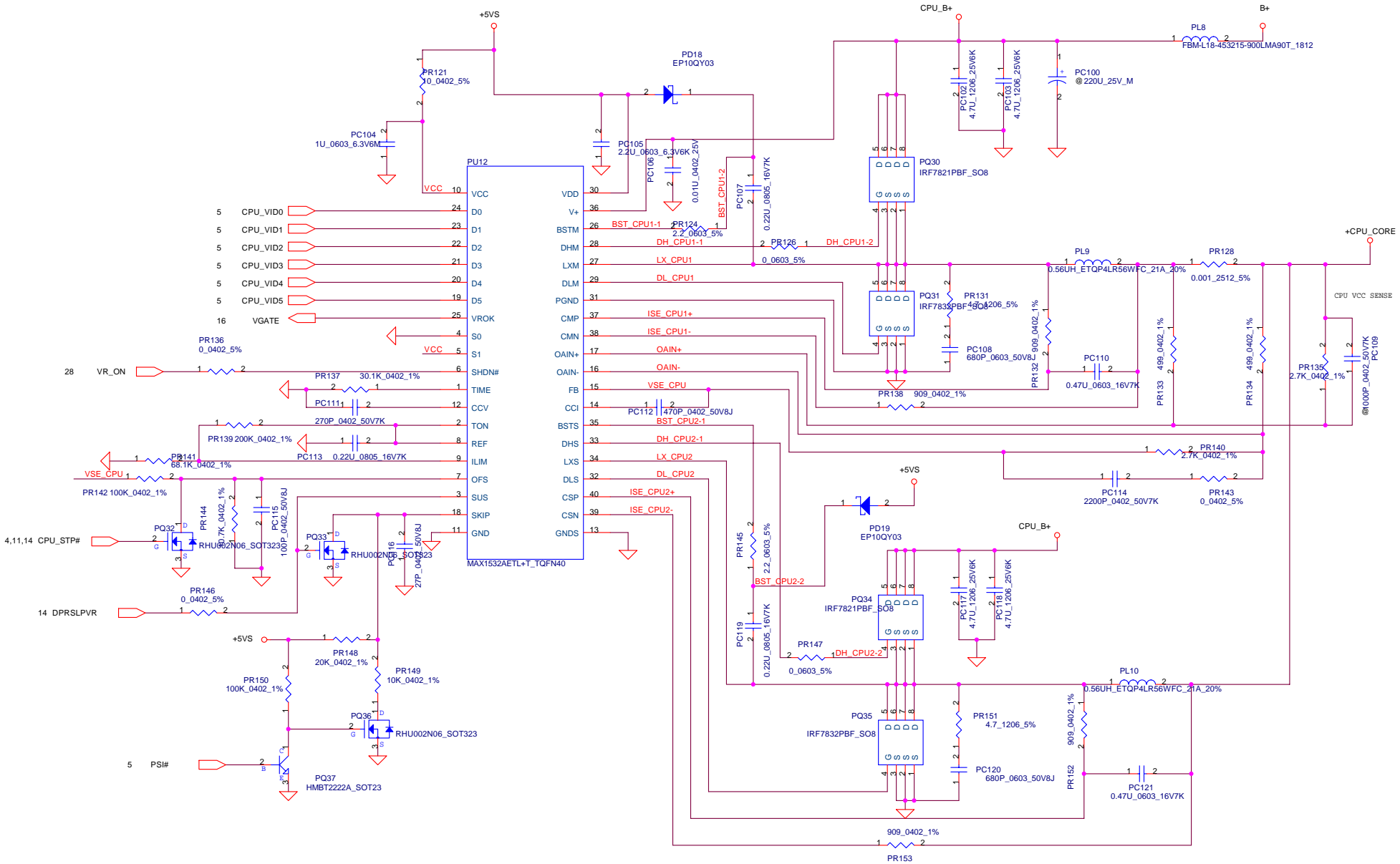
+1.8V



| | | | | | | | |
|---|-----------------|------------|--|--------------------|--|--------------------------|-----|
| Security Classification | | | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | | 2005/03/01 | | Deciphered Date | | 2006/03/01 | |
| Title | | | | | | | |
| 1.8V/VGA_CORE | | | | | | | |
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| | | | | | | | 0.3 |
| Date: Thursday, August 04, 2005 | | | | Sheet 38 of 42 | | | |



| | | | | |
|---|--------------------|-----------------|------------|---------------------|
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| Date: Thursday, August 04, 2005 | | Sheet 39 of 42 | | |



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| | | | | CPU_CORE | |
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| Size | Document Number | | | | Rev |
| | | | | | 0.3 |
| Date: | Monday, August 08, 2005 | Sheet | 40 | of | 42 |

| 0.1==>0.2 | | Written by Timo | |
|-----------|------|--------------------------------|---|
| Date | Page | Action | Purpose |
| 6/12 | 9 | Add C642, C643 and C644 | For Increase the DDR bypass capaciotrs |
| 6/12 | 10 | Add C645, C646 and C647 | For Increase the DDR bypass capaciotrs |
| | 12 | Modify JP18 circuit | Making TV out function become correct |
| | 15 | Add @ on R317 | Metting ATI reference circuit |
| | 24 | Del @ on R436 | Solving MDC issue and sound slow issue |
| | 26 | Del R306 (move to sub board) | To differentiate between HAZ00 and HTW01 BIOS |
| | 28 | Add @ on Super I/O circuit | For DVT build |
| | 29 | Modify pin74 net-name of KB910 | Solving reserve button no function |
| | 31 | Modify D16, D17 | |
| | | Add D35, D36 | Change from double colors to signal color LED |
| 6/22 | 27 | Add H34, H33 | For Me update new drawing |

| 0.2==>0.3 | | Written by Timo | |
|-----------|----|---|--|
| 7/8 | 8 | Add C648, C649 and C650 | Seperate the AVDD and DVDD for TVout and CRT |
| | 17 | Add C651~C657 | |
| | | Change C585, C587, C566, C533, C560, C573, C536 from 10 to 4.7U | For height limited of SB |
| | 34 | Change C225 from 4.7 to 10U | For height limited of SB |
| 7/11 | 25 | Del R456 | |
| | | Add Q52 | For insert card bus device beep sound issue. |
| | 27 | Del R449~R454 | For EMI request |
| 7/13 | | Del Super I/O circuit | |
| | 29 | Add JP30, R457, C658 | For LPC debug port |
| | 23 | ADD JP29, R456 | For Port80 Debug card connector |
| | 28 | ADD R459, R460 | For HDD password detect pin |
| | 12 | ADD J1, J4 | |
| | 22 | ADD J2 | |
| | 27 | ADD J3 | For EMI request |

| 0.3==>1.0 | | Written by Timo | |
|-----------|----|---|---|
| 7/28 | 25 | Add C662, R461, D37, R462, Q52 | For Insert card bus device PoPo noise sound |
| | 29 | Change R101 from 8.2k to 18kohm | For Board ID change |
| | 14 | Change C587, C585, C651, C652, C566, C553, C560, C573, C653, C654, C655, C656, C536, C657 | |
| | 17 | from 4.7U to 1U | For avoide the interfere area of HDD |
| | | Change C288 from 150U fo 470UF | Making the capacitors of 1.8VS source blance of SB |
| | | Add C660, C661 | Making the capacitors of 1.8VALW and 3VS sources blance of SB |
| 7/30 | 4 | Add @ in C261 | For throttle issue |
| | 5 | Add @ in C180 | For cost down |
| | 12 | Add L38, L39, L40 | For EMI issue |

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| Size | Document Number | | | Rev | |
| Date: | Monday, August 08, 2005 | Sheet | 41 | of | 42 |

EVT

| | | |
|-------|---|---|
| page | Reason for change | Modify list |
| 37 | 12V noise | Change PC38 from 4.7u_1206_25V to 4.7u_1210_25V |
| 37 | Lead free parts | Change PC53,PC58 to NEC lead free parts. |
| 38 | Modify 1.8V power sequence for HW requirement | Change PR100 from 0_0402_5% to 47K_0402_1% Add 0.1u_0402_16V at PC76 |
| 39 | Modify 1.05V circuit | Delete PQ24,PQ26,PL7,PD17,PC82,PC81,PR109,PQ25,PQ27,PR110 Change PU8 to APL5912-KAC-TRL Change PC85 to 0.01u_0402_25V Change PR112 to 316_0402_1% Change PR13 to 1K_0402_1% |
| 39 | Delete reserved 1.5V circuit | Delete PU11,PC95,PR118,PR120,PQ29,PR119,PC99,PC97,PC98,PC96 |
| 39 | Change 1.5V IC | Change PU10 from APL5151 to G914 |
| 40 | Add snubber for CPU CORE | Add 4.7_1206_5% to PR131,PR151 Add 680P_0603_50V to PC108,PC120 |
| 37,38 | Add bead at 3V/5V and 1.2V/1.8V input for EMI requirement | Add PL11,PL12 to replace PJ10,PJ11 |

DVT

| | | |
|----|--|---|
| 34 | Change VS resistor to 33 ohm | Change PR9 from 47_1206_5% to 33_1206_5% |
| 34 | Change 1N4148 to lead free P/N | Change PD2,PD3,PD4 P/N to SC11N414880 |
| 40 | Change HMBT2222 to lead free P/N | Change PQ37 P/N to SB322220080 |
| 38 | Raise 1.8V to 1.82V for HW requirement | Change PR94 from 10K_0402_1% to 10.2K_0402_1% |

PVT

| | | |
|----|---|--|
| 34 | Change VS resistor to standard part | Change PR9 from 33_1206_5% to 68_1206_5% Add 68_1206_5% at PR155 |
| 38 | Change 1.8VALWP power sequence for HW requirement | Change 47K_0402_1% from PR100 to PR156 Delete PC76 Change PC68 from 0.01u_0402_25V to 4700P_0402_25V |

Pre-MP

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| 38 | Add BOOST 2.2 ohm and snubber at 1.8V / 1.2V for EMI | Add 4.7_1206_5% to PR157,PR158 Add 680P_0603_50V to PC123,PC124 Change PR90,PR91 from 0_0603_5% to 2.2_0603_5% |
| 42 | Change CPU CORE mosfet for EMI | Change PQ30,PQ34 from AO4408 to IRF7821 Change PQ31,PQ35 from AO4410 to IRF7832 |
| 42 | Delete CPU VID 0 ohm debug resistor | Delete PR122,PR123,PR125,PR127,PR129,PR130 |

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|---|------------|--------------------|----------------|--------------------------|-----------------|
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