

DATA SHEET



TDA9859

Universal hi-fi audio processor for
TV

Product specification
Supersedes data of 2001 Jul 02
File under Integrated Circuits, IC02

2001 Jul 11

Universal hi-fi audio processor for TV

TDA9859

FEATURES

- Multi-source selector switches six AF inputs (three stereo sources or six mono sources)
- Each of the input signals can be switched to each of the outputs (crossbar switch)
- Outputs for loudspeaker channel and peri-TV connector (SCART)
- Switchable spatial stereo and pseudo stereo effects
- Audio surround decoder can be added externally
- Two general purpose logic output ports
- I²C-bus control of all functions.



GENERAL DESCRIPTION

The TDA9859 provides control facilities for the main and the SCART channel of a TV set. Due to extended switching possibilities, signals from three stereo sources can be handled.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _P	positive supply voltage (pin V _P)	7.2	8.0	8.8	V
I _P	supply current	–	25	–	mA
V _{i(rms)}	input signal levels for 0 dB gain (RMS value)	2	–	–	V
V _{o(rms)}	output signal levels for 0 dB gain (RMS value)	2	–	–	V
G _V	voltage gain in main channel				
	volume control (in 1 dB steps, balance included)	–63	–	+15	dB
	mute	–80	–	–	dB
	bass control (in 1.5 dB steps)	–12	–	+15	dB
	treble control (in 3 dB steps)	–12	–	+12	dB
THD	total harmonic distortion	–	0.1	–	%
S/N	signal-to-noise ratio	–	85	–	dB
T _{amb}	ambient temperature	0	–	70	°C

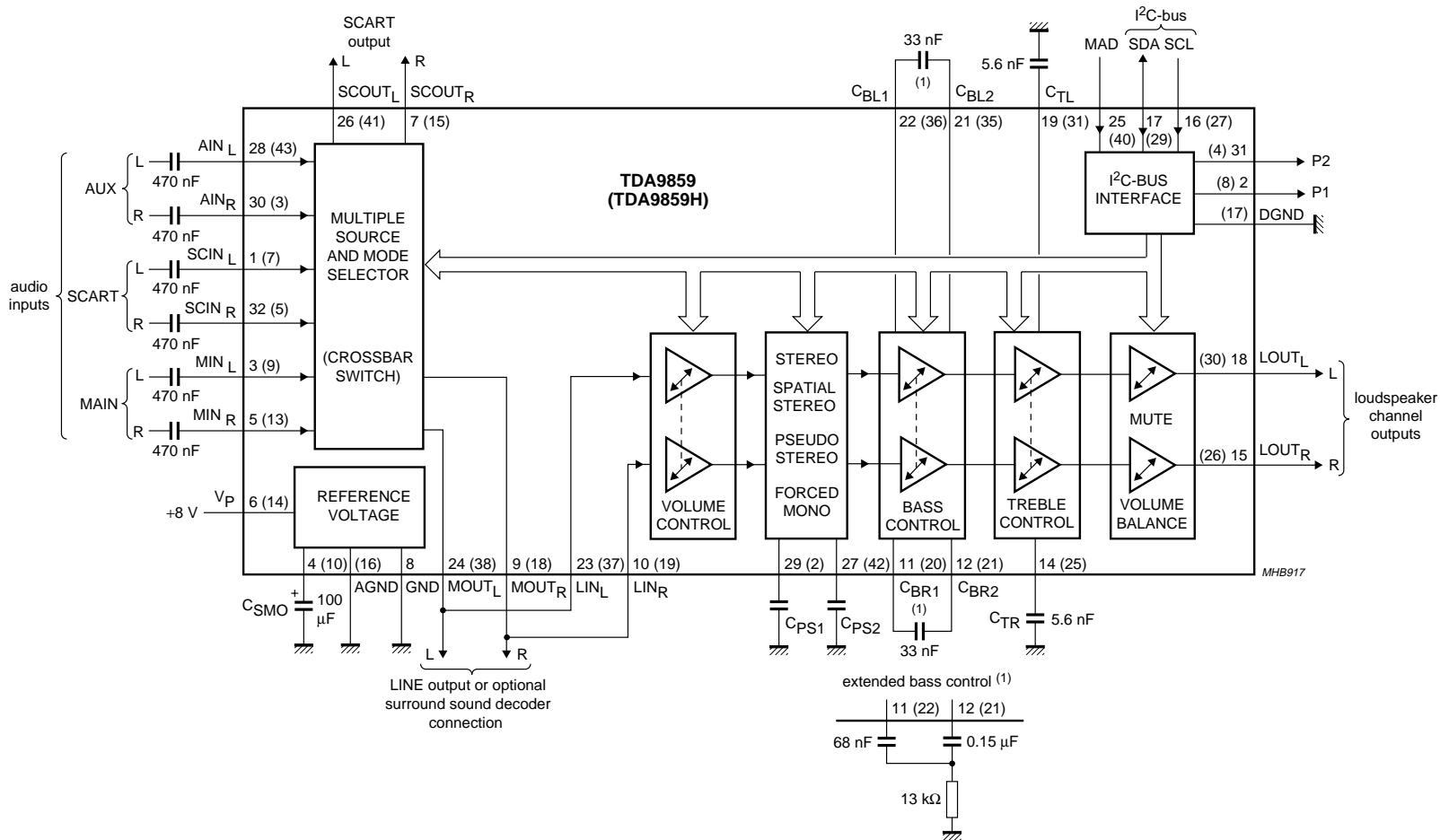
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9859	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
TDA9859H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

Universal hi-fi audio processor for TV

TDA9859

BLOCK DIAGRAM



The pin numbers given in parenthesis refer to the TDA9859H version.

(1) For extended bass control, the capacitor between C_{BR/L1} and C_{BR/L2} should be replaced by the extended bass control network.

Fig.1 Block diagram and application circuit.

Universal hi-fi audio processor for TV

TDA9859

PINNING

SYMBOL	PIN		DESCRIPTION
	TDA9859	TDA9859H	
SCIN _L	1	7	SCART input; left channel
P1	2	8	port 1 output
MIN _L	3	9	MAIN input; left channel
C _{SMO}	4	10	smoothing capacitor of reference voltage
n.c.	–	11	not connected
n.c.	–	12	not connected
MIN _R	5	13	MAIN input; right channel
V _P	6	14	supply voltage
SCOUT _R	7	15	SCART output; right channel
GND	8	–	ground
AGND	–	16	analog ground
DGND	–	17	digital ground
MOUT _R	9	18	MAIN output; right channel
LIN _R	10	19	input to right loudspeaker channel
C _{BR1}	11	20	bass capacitor connection 1; right channel
C _{BR2}	12	21	bass capacitor connection 2; right channel
n.c.	–	22	not connected
n.c.	–	23	not connected
n.c.	13	24	not connected
C _{TR}	14	25	treble capacitor connection; right channel
LOUT _R	15	26	loudspeaker output; right channel
SCL	16	27	serial clock input; I ² C-bus
n.c.	–	28	not connected

SYMBOL	PIN		DESCRIPTION
	TDA9859	TDA9859H	
SDA	17	29	serial data input/output; I ² C-bus
LOUT _L	18	30	loudspeaker output; left channel
C _{TL}	19	31	treble capacitor connection; left channel
n.c.	20	32	not connected
n.c.	–	33	not connected
n.c.	–	34	not connected
C _{BL2}	21	35	bass capacitor connection 2; left channel
C _{BL1}	22	36	bass capacitor connection 1; left channel
LIN _L	23	37	input to left loudspeaker channel
MOUT _L	24	38	MAIN output; left channel
n.c.	–	39	not connected
MAD	25	40	module address select input
SCOUT _L	26	41	SCART output; left channel
C _{PS2}	27	42	pseudo stereo capacitor 2
AIN _L	28	43	AUX input; left channel
n.c.	–	44	not connected
n.c.	–	1	not connected
C _{PS1}	29	2	pseudo stereo capacitor 1
AIN _R	30	3	AUX input; right channel
P2	31	4	port 2 output
SCIN _R	32	5	SCART input signal RIGHT
n.c.	–	6	not connected

Universal hi-fi audio processor for TV

TDA9859

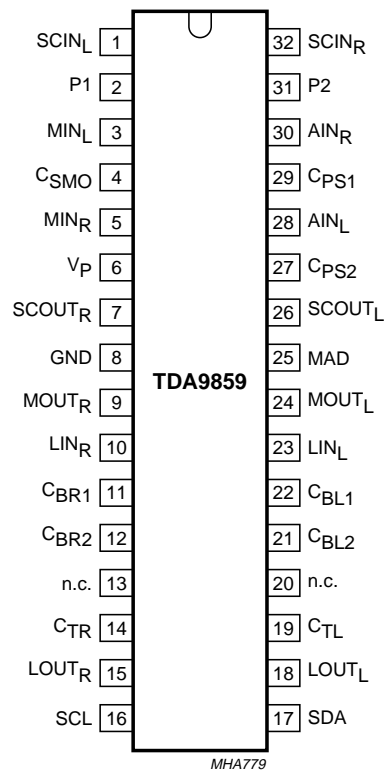


Fig.2 Pin configuration TDA9859 SDIP32 version.

Universal hi-fi audio processor for TV

TDA9859

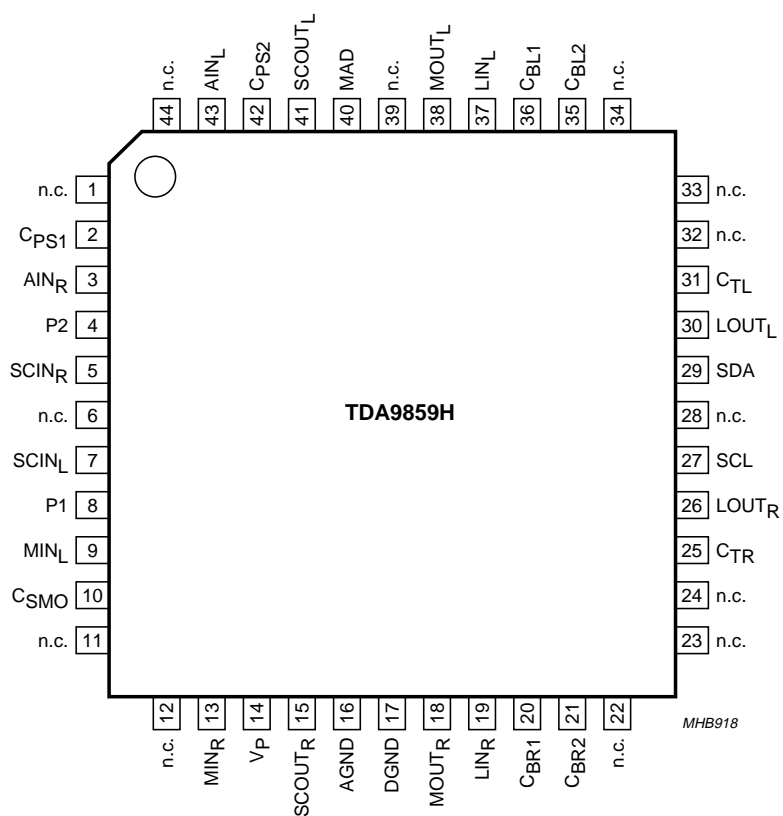


Fig.3 Pin configuration TDA9859H QFP44 version.

Universal hi-fi audio processor for TV

TDA9859

FUNCTIONAL DESCRIPTION

The TDA9859 consists of the following functions:

- Source select switching block
- Loudspeaker channel with effect controls
- Two port outputs for general purpose
- I²C-bus control.

Source select switching block

The TDA9859 selects and switches the input signals from three stereo or six mono sources MAIN, AUX and SCART (see Fig.1) to the outputs SCART and loudspeaker (crossbar-switching; Table 4). The main channel (LINE outputs) is looped outside the circuit (from pins MOUT_R and MOUT_L to pins LIN_R and LIN_L), so signals can be used as LINE output or a surround sound decoder can be inserted.

Effect controls

'Linear stereo', 'stereo with spatial effect (30% or 52% anti-phase crosstalk)' and 'forced mono with or without pseudo-stereo effect' are controlled by three bits. A muting of 85 dB is provided.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _P	supply voltage (pin V _P)	—	0	10	V
V _n	voltage on all pins, ground excluded	—	0	V _P	V
I _O	output current				
	at LOUT and SCOUT pins	—	—	2.5	mA
	at port output pins	—	—	1.5	mA
P _{tot}	total power dissipation	—	—	850	mW
T _{amb}	ambient temperature	—	0	70	°C
T _{stg}	storage temperature	—	–25	+150	°C
V _{es}	electrostatic handling voltage	all pins; note 1	—	±300	V
		all pins; note 2	—	±2000	V

Notes

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor (machine model).
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor (human body model).

Loudspeaker channel

Volume control is divided into volume control common and volume control left/right. The common part (–40 to +15 dB) controls the left and right channels simultaneously; the left/right part (–23 to 0 dB) controls the volume of left and right channels independently. Treble control provides a control range from –12 to +12 dB and bass control from –12 to +15 dB. Extended bass control can be provided by an external T-network (see Fig.1) from –15 to +19 dB (in 2 dB steps).

I²C-bus control

All control settings are stored in subaddress registers. Data transmission is simplified by auto-incrementing the subaddresses. The on-chip Power-on reset sets the mute bit to active, so both the SCART and the loudspeaker outputs are muted.

The muting can be switched off by writing a '0' (non-muted) into the mute control bits.

Universal hi-fi audio processor for TV

TDA9859

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TDA9859 (SDIP32)		60	K/W
	TDA9859H (QFP44)		65	K/W

CHARACTERISTICS

$V_P = 8\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; treble and bass in linear positions (0 dB); volume control left/right 0 dB; spatial function, pseudo-stereo function and forced-mono function in off position and measurements taken in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin V_P)		7.2	8.0	8.8	V
I_P	supply current (pin V_P)		–	25	–	mA
V_{ref}	internal reference voltage		–	$0.5V_P$	–	V
V_{SMO}	voltage at pin C_{SMO}		–	$V_P - 0.1$	–	V
DC voltage on pins						
V_I	DC input voltage at pins SCIN, MIN, LIN and AIN		–	$0.5V_P$	–	V
V_O	DC output voltage at pins SCOUT, MOUT and LOUT		–	$0.5V_P$	–	V
V_C	DC voltage on capacitors (pins C_{BR1} , C_{BR2} , C_{TR} , C_{TL} , C_{BL2} , C_{BL1} , C_{PS2} and C_{PS1})		–	$0.5V_P$	–	V
Audio select switch; line and SCART outputs (controlled via I²C-bus); see Table 4						
$V_{i(rms)}$	maximum AF input signal on pins SCIN, MIN and AIN (RMS value)	THD $\leq 0.5\%$ on output pins	2	–	–	V
R_i	input resistance at pins SCIN, MIN and AIN		20	30	40	k Ω
$B_{-0.5\text{ dB}}$	–0.5 dB bandwidth for pins SCOUT, MOUT and LOUT		20	–	20 000	Hz
$V_{o(rms)}$	maximum AF output signal on pins SCOUT and MOUT (RMS value)	THD $\leq 0.5\%$	2	–	–	V
R_L	allowed external load resistance on output pins MOUT on output pins SCOUT		10	–	–	k Ω
			5	–	–	k Ω
G_V	voltage gain from any input to SCART and MAIN outputs		–	0	–	dB
α_{cr}	switch crosstalk on outputs between AF inputs	$f = 10\text{ kHz}$; unused inputs connected to ground	–	90	–	dB

Universal hi-fi audio processor for TV

TDA9859

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Volume control common (f = 1 kHz, 55 steps)						
V _{i(rms)}	maximum input signal on pins LIN (RMS value)	G _v = 0; THD ≤ 0.5% on output pins LOUT	2	–	–	V
R _i	input resistance on pins LIN		7.5	10	–	kΩ
G _v	volume control common voltage gain nominal		–40	–	+15	dB
	minimum		–38	–	+14	dB
ΔG _v	volume control common voltage gain step width	G _v = –32 to +15 dB	0.5	1.0	1.5	dB
		G _v = –40 to –33 dB	0.25	1.0	1.75	dB
	volume control common voltage gain set error	G _v = –32 to +15 dB	–	–	1	dB
		G _v = –40 to –33 dB	–	–	2	dB
Volume control left/right (f = 1 kHz, 24 steps)						
G _v	volume control left/right voltage gain nominal		–24	–	0	dB
	minimum		–23	–	–1	dB
	mute position		–80	–85	–	dB
ΔG _v	volume control left/right voltage gain step width		0.5	1.0	1.5	dB
	volume control left/right voltage gain tracking error		–	–	2	dB
Bass control						
G _v	bass control voltage gain	C _B = 33 nF; f = 40 Hz				
	maximum boost		14	15	16	dB
	maximum attenuation		11	12	13	dB
ΔG _v	bass control voltage gain step width		1	1.5	2	dB
G _{v(extended)}	extended bass control voltage gain	see Fig.1; f = 60 Hz				
	maximum boost		18	19	20	dB
	maximum attenuation		14	15	16	dB
ΔG _{v(extended)}	extended bass control voltage gain step width		1	2	3	dB
Treble control						
G _v	treble control voltage gain	f = 15 kHz				
	maximum boost		11	12	13	dB
	maximum attenuation		11	12	13	dB
ΔG _v	treble control voltage gain step width		2.5	3	3.5	dB
Effect controls						
α _{ct(spat1)}	anti-phase crosstalk by spatial effect 1		–	52	–	%
α _{ct(spat2)}	anti-phase crosstalk by spatial effect 2		–	30	–	%
φ	phase shift by pseudo-stereo		see Fig.4			

Universal hi-fi audio processor for TV

TDA9859

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Loudspeaker channel outputs (pins LOUT_R and LOUT_L)						
V _{o(max)(rms)}	maximum output signal (RMS value)	THD ≤ 0.5%; R _L > 10 kΩ; C _L < 1.5 nF	2	–	–	V
ΔV _{DC(max)}	maximum DC offset voltage between adjoining step and any step to mute for volume control	G _V = 0 to +15 dB/mute	–	2	15	mV
		G _V = –64 to 0 dB/mute	–	0.5	10	mV
	for bass control	G _V = 0 to +15 dB/mute	–	2	15	mV
		G _V = –12 to 0 dB/mute	–	0.5	10	mV
	for treble control	G _V = –12 to +12 dB/mute	–	0.5	10	mV
R _o	output resistance		–	–	100	Ω
R _{o(L)}	allowed output load resistor		10	–	–	kΩ
C _{o(L)}	allowed output load capacitor		–	–	1.5	nF
V _{no(W)}	weighted noise voltage at output (quasi-peak level)	CCIR 468-3 weighted				
		G _V = +15 dB	–	102	–	μV
		G _V = 0 dB	–	32	–	μV
		G _V = –40 dB	–	27	–	μV
		G _V = –80 dB (mute)	–	20	–	μV
B _{–1 dB}	–1 dB bandwidth for loudspeaker channel		20	–	20000	Hz
THD	total harmonic distortion	f = 20 to 12500 Hz				
	for V _{i(rms)} = 0.2 V	G _V = –30 to +15 dB	–	0.1	0.3	%
	for V _{i(rms)} = 1 V	G _V = –30 to 0 dB	–	0.1	0.3	%
	for V _{i(rms)} = 2 V	G _V = –30 to –6 dB	–	0.1	0.3	%
α _{cs(l-r)}	stereo channel separation	f = 10 kHz; G _V = 0 dB; opposite input grounded by 1 kΩ resistor	–	75	–	dB
α _{ct(bus)}	crosstalk from I ² C-bus to AF outputs $\alpha_{bus} = 20 \log \frac{V_{bus(p-p)}}{V_{o(rms)}}$ (V _{bus} = spurious I ² C-bus signal voltage on AF output)	G _V = 0 dB	–	100	–	dB
PSRR ₁₀₀	power supply ripple rejection with 100 Hz ripple	G _V = 0 dB; V _{ripple(rms)} < 200 mV	–	55	–	dB
SCART output (pins SCOUT_R and SCOUT_L)						
V _{o(max)(rms)}	maximum output signal (RMS value)	THD ≤ 0.5%; R _L > 5 kΩ	2	–	–	V
R _{o(L)}	output load resistor		5	–	–	kΩ
Power-on reset						
V _{PONR}	increasing supply voltage	start of reset	–	–	2.5	V
		end of reset	5.2	6.0	6.8	V
	decreasing supply voltage	start of reset	4.4	5.2	6.0	V

Universal hi-fi audio processor for TV

TDA9859

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus (pins SCL and SDA)						
V _{IH}	HIGH-level input voltage		3	–	V _P	V
V _{IL}	LOW-level input voltage		0	–	1.5	V
I _I	input current		–	–	±10	µA
V _{ACK}	output voltage with acknowledge at pin SDA	I _{SDA} = –3 mA	–	–	0.4	V
Module address (pin MAD)						
V _{IL}	LOW-level input voltage		0	–	1.5	V
V _{IH}	HIGH-level input voltage		3	–	V _P	V
Port outputs (open-collector outputs pins P1 and P2)						
V _{OL}	LOW-level output voltage	I _{O(sink)} = 1 mA	–	–	0.3	V
I _{O(sink)}	port output sink current		–	–	1	mA

Universal hi-fi audio processor for TV

TDA9859

I²C-BUS PROTOCOL

This circuit operates as a slave receiver only. For more information about the I²C-bus, see *"The I²C-bus and how to use it"*, order number 9398 393 40011.

I²C-bus format

S	SLAVE ADDRESS	\overline{W}	A	SUBADDRESS	A	DATA ⁽¹⁾	A ⁽¹⁾	P
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Note

1. Multiple DATA-A (acknowledge) sequences may occur.

Table 1 Explanation of I²C-bus format

NAME	DESCRIPTION
S	START condition (SCL HIGH, SDA HIGH-to-LOW)
SLAVE ADDRESS	100 0000 (MAD = LOW) or 100 0001 (MAD = HIGH)
\overline{W}	0
A	acknowledge (SDA = LOW); generated by the device
SUBADDRESS	subaddress (byte); see Table 2
DATA ⁽¹⁾	data byte; see Table 2
P	STOP condition (SCL = HIGH, SDA = LOW-to-HIGH)

Note

1. If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed by the device.

Table 2 I²C-bus transmission

FUNCTION	SUBADDRESS		DATA BITS							
	BINARY	HEX	D7	D6	D5	D4	D3	D2	D1	D0
Loudspeaker channel										
Volume control common	0000 0000	00	0	0	V05	V04	V03	V02	V01	V00
Volume control left	0000 0001	01	0	0	0	VL4	VL3	VL2	VL1	VL0
Volume control right	0000 0010	02	0	0	0	VR4	VR3	VR2	VR1	VR0
Bass control	0000 0011	03	0	0	0	BA4	BA3	BA2	BA1	BA0
Treble control	0000 0100	04	0	0	0	0	TR3	TR2	TR1	TR0
Switching control byte										
SCART output ⁽¹⁾	0000 1000	08	0	MU1	P1	P2	I13	I12	I11	I10
Loudspeaker output	0000 1001	09	EF2	MU2	EF1	ST	I23	I22	I21	I20

Note

1. If auto-increment of the subaddress is used, it is necessary to insert three dummy data words between the treble control byte and the switching control bytes.

Universal hi-fi audio processor for TV

TDA9859

Table 3 Function of the bits in Table 2

BITS	FUNCTION
V00 to V05	volume control common for loudspeaker channel; see Table 9
VL0 to VL4	volume control for left loudspeaker channel; see Table 6
VR0 to VR4	volume control for right loudspeaker channel; see Table 6
BA0 to BA4	bass control for left and right loudspeaker channels; see Table 7
TR0 to TR3	treble control for left and right loudspeaker channels; see Table 8
I10 to I13	input selection for SCART channels; see Table 4
I20 to I23	input selection for loudspeaker channels; see Table 4
MU1 and MU2	mute control bits (MU1 for SCART channel, MU2 for loudspeaker channel) 0 = channel not muted 1 = channel muted
EF1, EF2 and ST	effect control bits for loudspeaker channel; see Table 5
P1 and P2	control bits for ports P1 and P2 control bit = 0: port output = LOW-level control bit = 1: port output = HIGH-level

Table 4 Input selection

INPUT	BITS OF DATA BYTE 8 AND 9								
	HEX	D7	D6	D5	D4	D3	D2	D1	D0
AUX LEFT	XB ⁽¹⁾	(1)	MU	(1)	(1)	1	0	1	1
AUX RIGHT	X9 ⁽¹⁾	(1)	MU	(1)	(1)	1	0	0	1
AUX STEREO	X7 ⁽¹⁾	(1)	MU	(1)	(1)	0	1	1	1
SCART LEFT	XA ⁽¹⁾	(1)	MU	(1)	(1)	1	0	1	0
SCART RIGHT	X5 ⁽¹⁾	(1)	MU	(1)	(1)	0	1	0	1
SCART STEREO	X6 ⁽¹⁾	(1)	MU	(1)	(1)	0	1	1	0
MAIN LEFT	XC ⁽¹⁾	(1)	MU	(1)	(1)	1	1	0	0
MAIN RIGHT	XD ⁽¹⁾	(1)	MU	(1)	(1)	1	1	0	1
MAIN STEREO	X8 ⁽¹⁾	(1)	MU	(1)	(1)	1	0	0	0

Note

- Byte 8 (SCART channels): The value of X depends on MU1 and control bits P1 and P2.
Byte 9 (loudspeaker channels): see Table 5 for the programming of these bits. The value of X depends on the selected effects and MU2.

Universal hi-fi audio processor for TV

TDA9859

Table 5 Effect controls

SETTING SPECIAL EFFECTS	DATA BYTE TO SUBADDRESS 09								
	HEX	EF2	MU2	EF1	ST	I23	I22	I21	I20
Stereo with spatial effect 1 (52%)	BX ⁽¹⁾	1	0	1	1	(1)	(1)	(1)	(1)
Stereo with spatial effect 2 (30%)	3X ⁽¹⁾	0	0	1	1	(1)	(1)	(1)	(1)
Stereo without spatial effect	1X ⁽¹⁾	0	0	0	1	(1)	(1)	(1)	(1)
Forced mono with pseudo stereo	2X ⁽¹⁾	0	0	1	0	(1)	(1)	(1)	(1)
Forced mono without pseudo stereo	0X ⁽¹⁾	0	0	0	0	(1)	(1)	(1)	(1)

Note

1. The value of X depends on the selected input (see Table 4).

Table 6 Volume control left/right

G _v (dB)	DATA BITS					
	HEX	VL4	VL3	VL2	VL1	VL0
		VR4	VR3	VR2	VR1	VR0
0	1F	1	1	1	1	1
-1	1E	1	1	1	1	0
-2	1D	1	1	1	0	1
-3	1C	1	1	1	0	0
-4	1B	1	1	0	1	1
-5	1A	1	1	0	1	0
-6	19	1	1	0	0	1
-7	18	1	1	0	0	0
-8	17	1	0	1	1	1
-9	16	1	0	1	1	0
-10	15	1	0	1	0	1
-11	14	1	0	1	0	0
-12	13	1	0	0	1	1
-13	12	1	0	0	1	0
-14	11	1	0	0	0	1
-15	10	1	0	0	0	0
-16	0F	0	1	1	1	1
-17	0E	0	1	1	1	0
-18	0D	0	1	1	0	1
-19	0C	0	1	1	0	0
-20	0B	0	1	0	1	1
-21	0A	0	1	0	1	0
-22	09	0	1	0	0	1
-23	08	0	1	0	0	0
Mute	07	0	0	1	1	1

Table 7 Bass control

G _v (dB)	DATA BITS					
	HEX	BA4	BA3	BA2	BA1	BA0
+15	19	1	1	0	0	1
+13.5	18	1	1	0	0	0
+12	17	1	0	1	1	1
+10.5	16	1	0	1	1	0
+9	15	1	0	1	0	1
+7.5	14	1	0	1	0	0
+6	13	1	0	0	1	1
+4.5	12	1	0	0	1	0
+3	11	1	0	0	0	1
+1.5	10	1	0	0	0	0
0	0F	0	1	1	1	1
0	0E	0	1	1	1	0
-1.5	0D	0	1	1	0	1
-3	0C	0	1	1	0	0
-4.5	0B	0	1	0	1	1
-6	0A	0	1	0	1	0
-7.5	09	0	1	0	0	1
-9	08	0	1	0	0	0
-10.5	07	0	0	1	1	1
-12	06	0	0	1	1	0

Universal hi-fi audio processor for TV

TDA9859

Table 8 Treble control

G_v (dB)	DATA BITS					
	HEX	0	TR3	TR2	TR1	TR0
+12	0A	0	1	0	1	0
+9	09	0	1	0	0	1
+6	08	0	1	0	0	0
+3	07	0	0	1	1	1
0	06	0	0	1	1	0
-3	05	0	0	1	0	1
-6	04	0	0	1	0	0
-9	03	0	0	0	1	1
-12	02	0	0	0	1	0

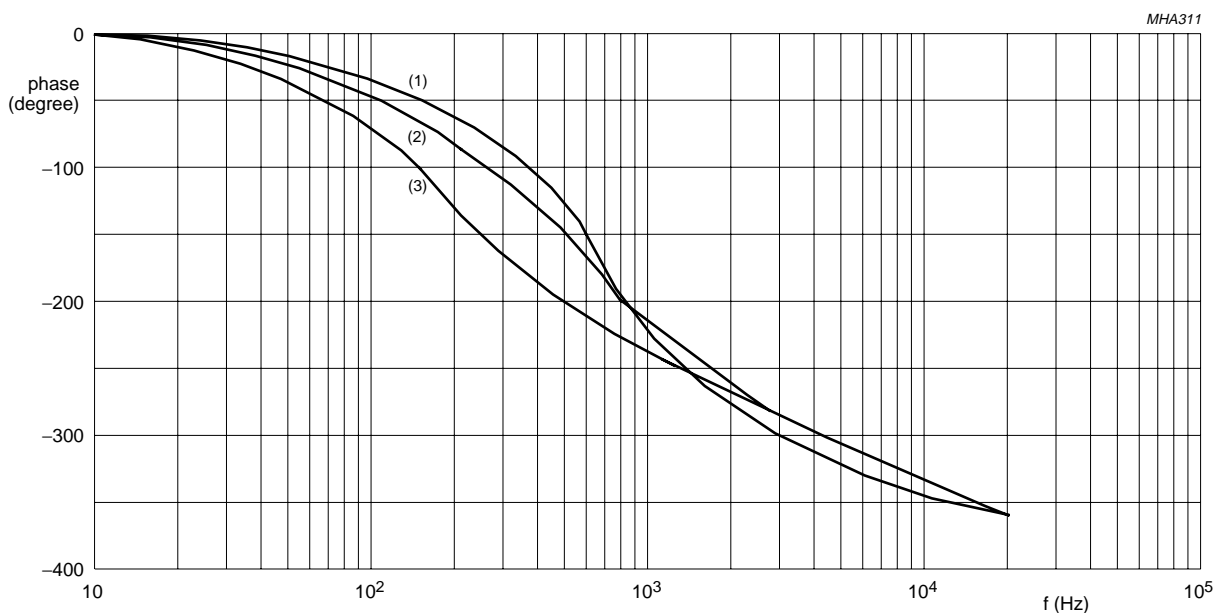
Table 9 Volume control common

G_v (dB)	DATA BITS						
	HEX	V05	V04	V03	V02	V01	V00
+15	3F	1	1	1	1	1	1
+14	3E	1	1	1	1	1	0
+13	3D	1	1	1	1	0	1
+12	3C	1	1	1	1	0	0
+11	3B	1	1	1	0	1	1
+10	3A	1	1	1	0	1	0
+9	39	1	1	1	0	0	1
+8	38	1	1	1	0	0	0
+7	37	1	1	0	1	1	1
+6	36	1	1	0	1	1	0
+5	35	1	1	0	1	0	1
+4	34	1	1	0	1	0	0
+3	33	1	1	0	0	1	1
+2	32	1	1	0	0	1	0
+1	31	1	1	0	0	0	1
0	30	1	1	0	0	0	0
-1	2F	1	0	1	1	1	1
-2	2E	1	0	1	1	1	0
-3	2D	1	0	1	1	0	1
-4	2C	1	0	1	1	0	0
-5	2B	1	0	1	0	1	1
-6	2A	1	0	1	0	1	0

G_v (dB)	DATA BITS						
	HEX	V05	V04	V03	V02	V01	V00
-7	29	1	0	1	0	0	1
-8	28	1	0	1	0	0	0
-9	27	1	0	0	1	1	1
-10	26	1	0	0	1	1	0
-11	25	1	0	0	1	0	1
-12	24	1	0	0	1	0	0
-13	23	1	0	0	0	1	1
-14	22	1	0	0	0	1	0
-15	21	1	0	0	0	0	1
-16	20	1	0	0	0	0	0
-17	1F	0	1	1	1	1	1
-18	1E	0	1	1	1	1	0
-19	1D	0	1	1	1	0	1
-20	1C	0	1	1	1	0	0
-21	1B	0	1	1	0	1	1
-22	1A	0	1	1	0	1	0
-23	19	0	1	1	0	0	1
-24	18	0	1	1	0	0	0
-25	17	0	1	0	1	1	1
-26	16	0	1	0	1	1	0
-27	15	0	1	0	1	0	1
-28	14	0	1	0	1	0	0
-29	13	0	1	0	0	1	1
-30	12	0	1	0	0	1	0
-31	11	0	1	0	0	0	1
-32	10	0	1	0	0	0	0
-33	0F	0	0	1	1	1	1
-34	0E	0	0	1	1	1	0
-35	0D	0	0	1	1	0	1
-36	0C	0	0	1	1	0	0
-37	0B	0	0	1	0	1	1
-38	0A	0	0	1	0	1	0
-39	09	0	0	1	0	0	1
-40	08	0	0	1	0	0	0

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- (1) Normal effect; $C_{PS1} = C_{PS2} = 15 \text{ nF}$.
(2) Intensified effect; $C_{PS1} = 47 \text{ nF}$; $C_{PS2} = 5.6 \text{ nF}$.
(3) More intensified effect; $C_{PS1} = 68 \text{ nF}$; $C_{PS2} = 5.6 \text{ nF}$.

Fig.4 Pseudo stereo effect (phase) as a function of frequency.

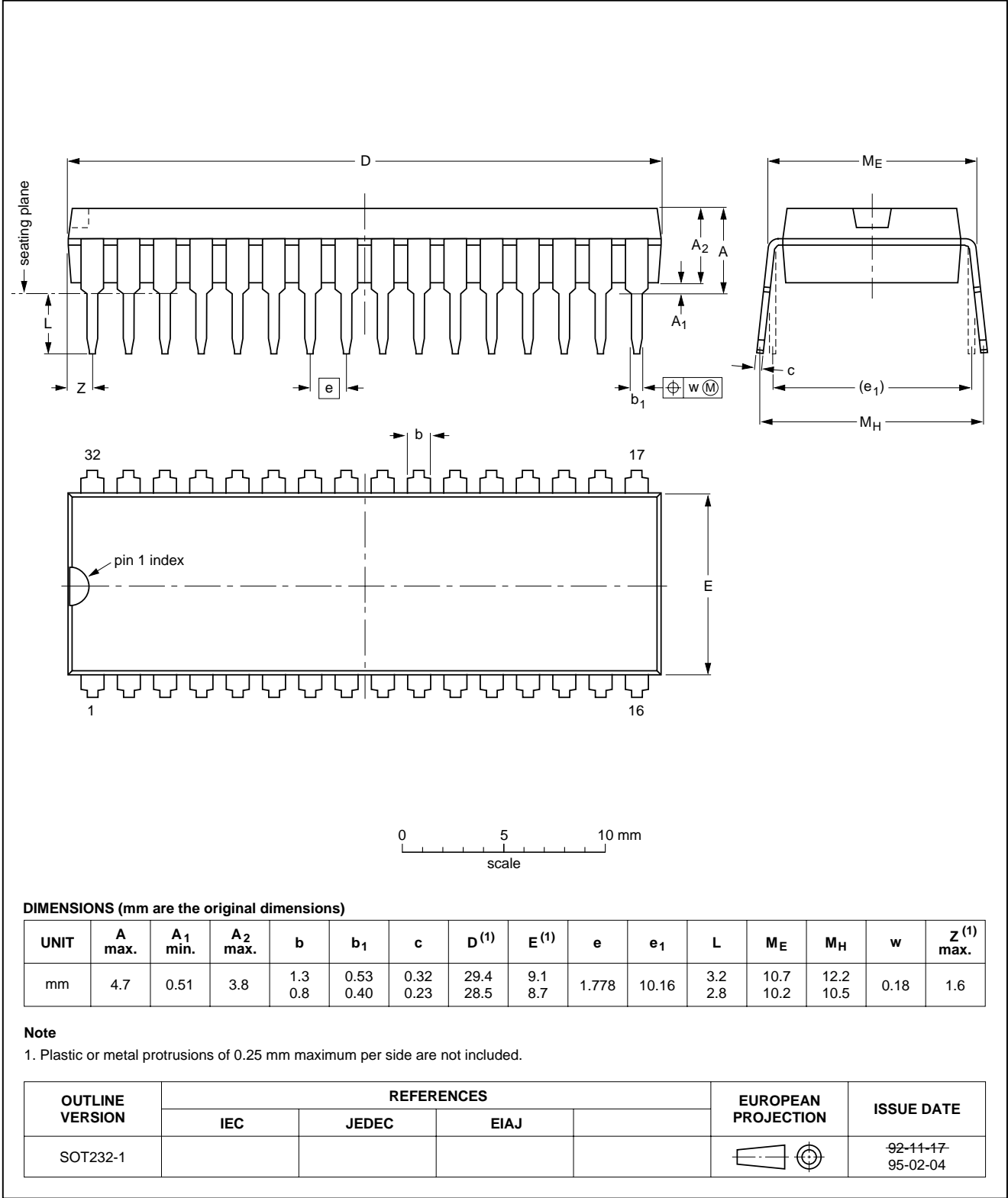
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PACKAGE OUTLINES

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil)

SOT232-1

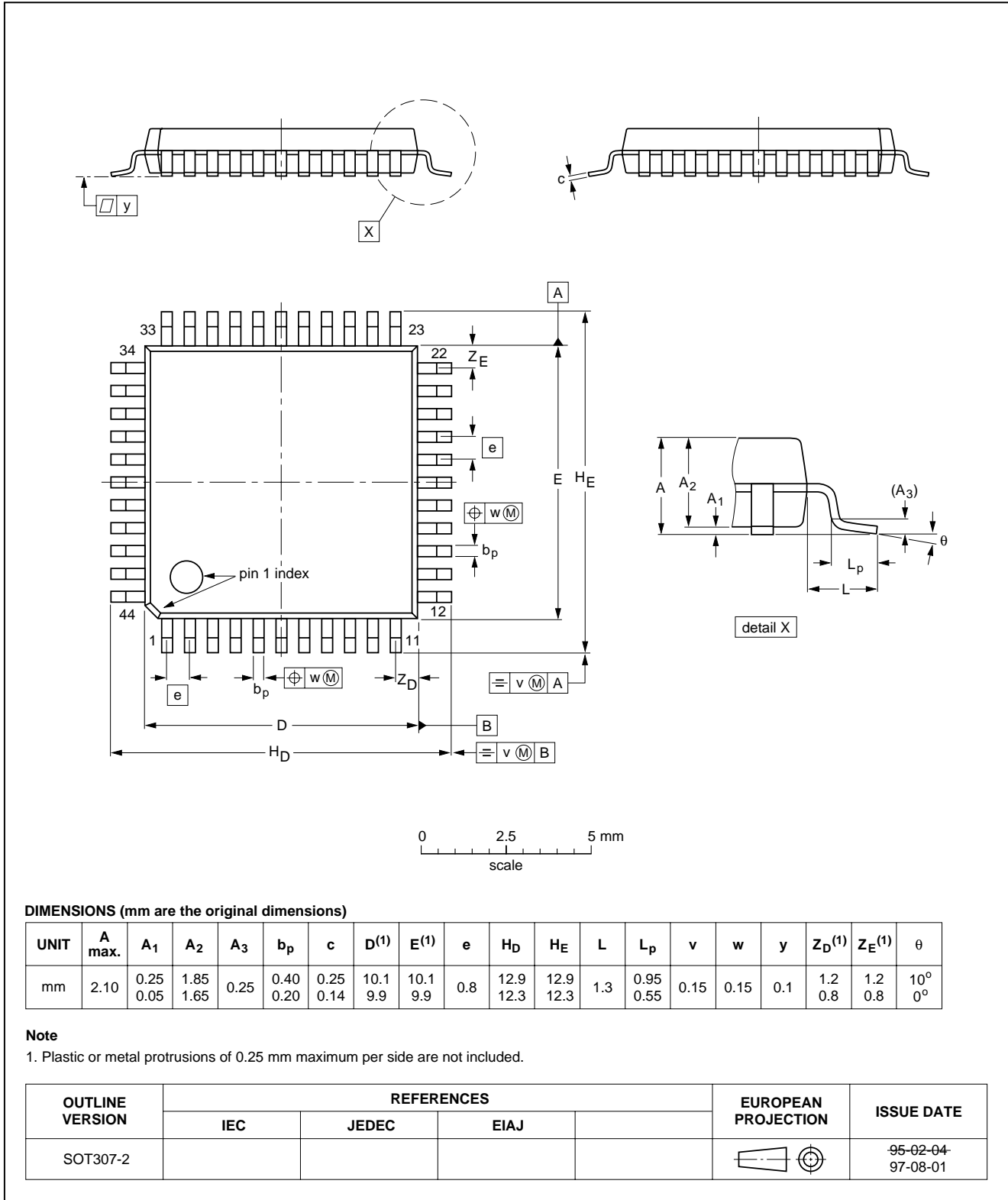


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QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

SOT307-2



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SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW ⁽¹⁾	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable ⁽²⁾	–	suitable
Surface mount	BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable	–
	HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable ⁽³⁾	suitable	–
	PLCC ⁽⁴⁾ , SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended ⁽⁴⁾⁽⁵⁾	suitable	–
	SSOP, TSSOP, VSO	not recommended ⁽⁶⁾	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “*Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*”.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
Objective specification	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary specification	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 7 - 9 Rue du Mont Valérien, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4728 6600, Fax. +33 1 4728 6638

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: Philips Hungary Ltd., H-1119 Budapest, Fehervari ut 84/A,
Tel. +36 1 382 1700, Fax. +36 1 382 1800

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 5F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2451, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
60/14 MOO 11, Bangna Trad Road KM. 3, Bagna, BANGKOK 10260,
Tel. +66 2 361 7910, Fax. +66 2 398 3447

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 3341 299, Fax. +381 11 3342 553

For all other countries apply to: Philips Semiconductors,
Marketing Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN,
The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

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SCA 72

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