Estimating Junction Temperature by Top Surface Temperature in Power MOSFETs

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Abstract

The thermal data provided on MOSFET datasheets is usually limited to thermal impedance between junction-to-lead and junction-to-ambient. While Vishay Siliconix provides the Web-based ThermaSim™ simulation tool for more accurate thermal simulation based on customized conditions, sometimes design engineers simply do not have time to run the simulation. However, measuring the top surface temperature is relatively easy, and a simple way of estimating the MOSFET junction temperature based on this top surface measurement would give designers quite a useful tool. Just such a methodology is presented by this application note.

To study the relationship between junction temperature and top surface temperature, we ran ThermaSim under specific conditions. To get better agreement with the datasheet, MOSFETs should be mounted on 1-in by 1-in square FR-4 board.

Si4800BDY: SO-8 Single-Die, Bonding-Wired Package

Figure 1 shows the ThermaSim results of the Si4800BDY when dissipating 0.5 W. The results show a die temperature of + 80.95 °C and a top temperature of + 77 °C.

MIN. TEMP.	MAX. TEMP.	DIE. TEMP.	TOP TEMP.	BOTTOM TEMP.	FLUX TO PCB
+ 62.15 °C	+ 81.01 °C	+ 80.95 °C	+ 77.00 °C	+ 67.16 °C	0.47 W

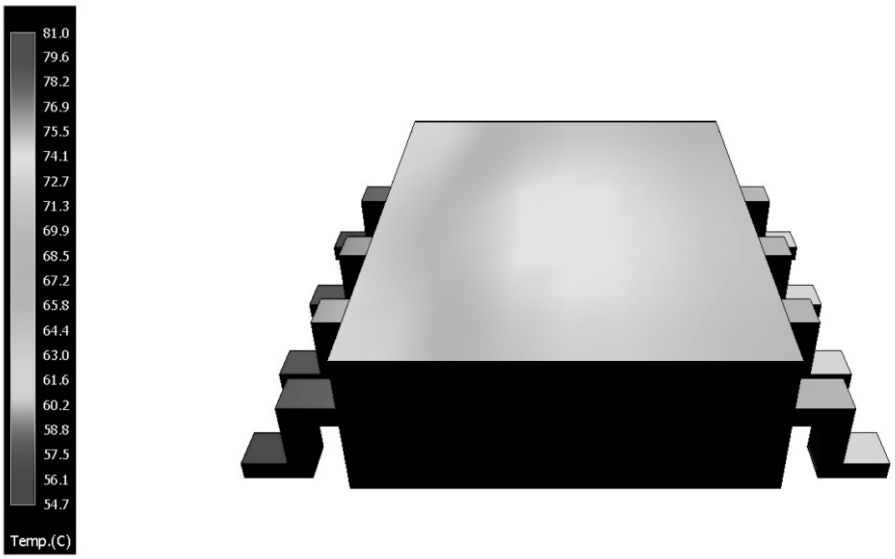

Figure 1 - ThermaSim Output Result

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Figure 2 shows the temperature rise of the top surface and die with power dissipation up to 1 W.

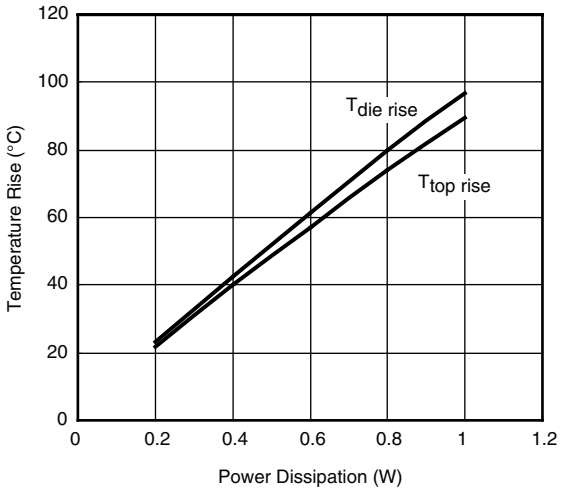

Figure 2 - Si4800BDY Top and die Temperature Rise

The simulation results for power dissipation levels of 0.2 W to 1 W are shown in table 1.
$T_{die\ rise} = T_{die} - 25$, and $T_{top\ rise} = T_{top} - 25$, respectively, and $K = [T_{die\ rise}]/[T_{top\ rise}]$. The coefficient K is consistent with the power dissipation, and by averaging K, we arrive at 1.074 as a ratio of $T_{top\ rise}$ to $T_{die\ rise}$.

TABLE 1 - THE ThermaSim RESULTS FOR SI4800BDY

P_d (W)	T_{die} (°C)	T_{top} (°C)	$T_{die\ rise}$ (°C)	$T_{top\ rise}$ (°C)	K
1	121.998	114.720	97.0	89.7	1.081
0.8	104.879	99.143	79.9	74.1	1.077
0.6	86.614	82.337	61.6	57.3	1.075
0.4	67.791	64.941	42.8	39.9	1.071
0.2	48.156	46.760	23.2	21.8	1.064
				AVG	1.074

The temperature difference between the top and the die is proportional to the power dissipation.

Another approximation line can be determined by $[T_{die\ rise}] = 1.074^* [T_{top\ rise}]$. This linear approximation line describes the actual data well, as shown in figure 3. For this particular part, the die temperature rise is approximately 7.4 % higher than the top surface temperature.

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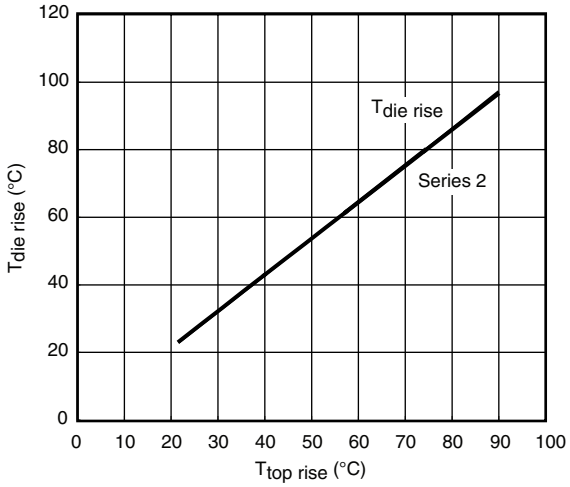

Figure 3 - Top Temperature Rise vs. Die Temperature Rise of Si4800BDY

Si4686DY: Single SO-8 Bonding-Wire-Less (BWL) Package

A bonding-wire-less (BWL) package will make some difference on the heat spread, since a clip between the die and source pins makes another heat flux to the board. Figure 4 shows the results of using Si4686DY as a sample for this simulation.

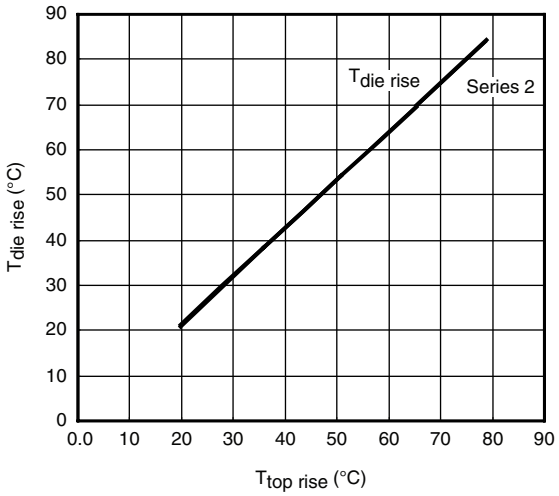

Figure 4 - Top Temperature Rise vs. Die Temperature Rise of Si4686DY

The graph shows a similar result to the Si4800BDY simulation. However, the temperature difference between the top surface to die is 6.6 % for this part.

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Si7336ADP: Single PowerPAK® SO-8 BWL Package

The next example is the PowerPAK SO-8 with a BWL package. Figure 5 shows the top temperature rise vs. the die temperature rise for the Si7336ADP.

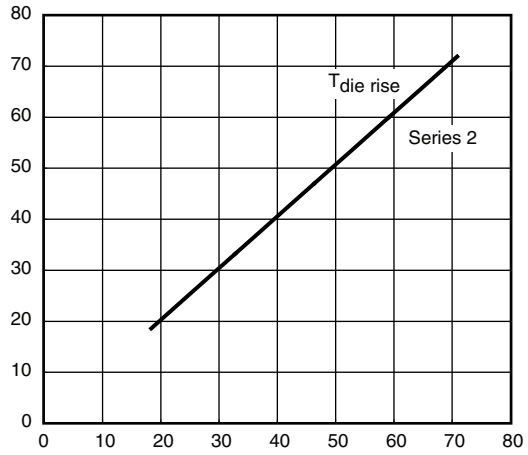

Figure 5 - Top Temperature Rise vs. Die Temperature Rise of Si7336ADP

Because it has a thinner package than the standard SO-8, the PowerPAK SO-8 shows a top temperature closer to the die temperature. It shows similar results to the previous simulations; however, the temperature difference between the top surface to die is only 1.4 % for this part, while it is 6.6 % or 7.4 % for the standard SO-8.

We have run this thermal simulation on other packages as well, as shown in table 2.

TABLE 2 - THERMAL COEFFICIENT FOR DIFFERENT PARTS

PACKAGE	PART NUMBER	COEFFICIENT
SO-8 BWL	Si4336DY	1.029
	Si4686DY	1.066
SO-8	Si4800BDY	1.074
	Si4894BDY	1.044
ChipFET	Si5404BDC	1.028
	Si5441BDC	1.035
PowerPAK1212	Si7112DN	1.016
	Si7806ADN	1.017
PowerPAKSO-8	Si7336ADP	1.014
	Si7880ADP	1.022
DPAK	SUD50N02-06	1.080
	SUD50N25-06P	1.083
D^2PAK	SUM110N04-02L	1.182
	SUM110N10-09	1.175

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The coefficients for the D^{2}PAK are the largest among all the packages because it has the thickest molding. The second largest is the DPAK, which has the second thickest molding. The PowerPAK SO-8 and PowerPAK 1212 show smaller numbers due to their thinner molding.

Conclusion:
From the investigation above, we have determined that the die temperature rise is proportional to the top surface temperature rise:

$$[T_{die\ rise}] = \mathbf{k} * [T_{top\ rise}]$$

Coefficient K depends on the package and is approximately 1.18 for the D^{2}PAK and 1.08 for the DPAK. For the PowerPAK SO-8 and PowerPAK 1212, it is roughly 1.02. For other packages it varies from 1.03 to 1.07, depending on the die size or package construction. The ThermaSim simulations have shown that the die temperature is much closer to the top surface temperature than was expected.

Reference:

1. Kandarp Pandya and Serge Jaunay, "Thermal Analysis of Power MOSFETs Using Rebecca-3D Thermal Modeling Software (From Epsilon Ingenierie) versus Physical Measurements and Possible Extractions," The 6th IEEE EuroSimE Conference Berlin.
2. Wharton McDaniel, "MOSFET Thermal Characterization in the Application," Application Note AN819, Vishay Siliconix.
3. ThermaSim™ Thermal Simulation Tool, http://www.vishay.com/mosfet/thermasim/