

FAN8732G/FAN8732BG/FAN8732CG

Spindle motor and 5-CH actuator driver

[Spindle(PWM), Sled 2-CH(PWM) 3-CH(Linear)]

Features

Common

- Built-in thermal shutdown circuit (TSD)
- Built-in power save circuit
- 4 Independent voltage sources
- Corresponds to 3.3V or 5V DSP

Spindle

- Output PWM mode control

BTL(Sled 2-channels)

- Output PWM mode control

BTL(Other 3-channels)

- Output LINEAR mode control

Description

The FAN8732G/BG/CG is a monolithic IC suitable for a PWM 3-phase BLDC spindle motor driver, 2-CH PWM motor drivers for sled motor and 3-CH linear drivers which drive the focus actuator, tracking actuator and loading motor of the optical media applications.



Typical Applications

- Compact disk ROM (CD-ROM)
- Compact disk RW (CD-RW)
- Digital video disk ROM (DVD-ROM)
- Digital video disk RAM (DVD-RAM)
- Digital video disk Player (DVDP)
- Other compact disk media

Ordering Information

Device	Package	Operating Temp.
FAN8732G	42-SSOP-EP	-20°C ~ +75°C
FAN8732GX	42-SSOP-EP	-20°C ~ +75°C
FAN8732BG	42-SSOP-EP	-20°C ~ +75°C
FAN8732BGX	42-SSOP-EP	-20°C ~ +75°C
FAN8732CG	42-SSOP-EP	-20°C ~ +75°C
FAN8732CGX	42-SSOP-EP	-20°C ~ +75°C

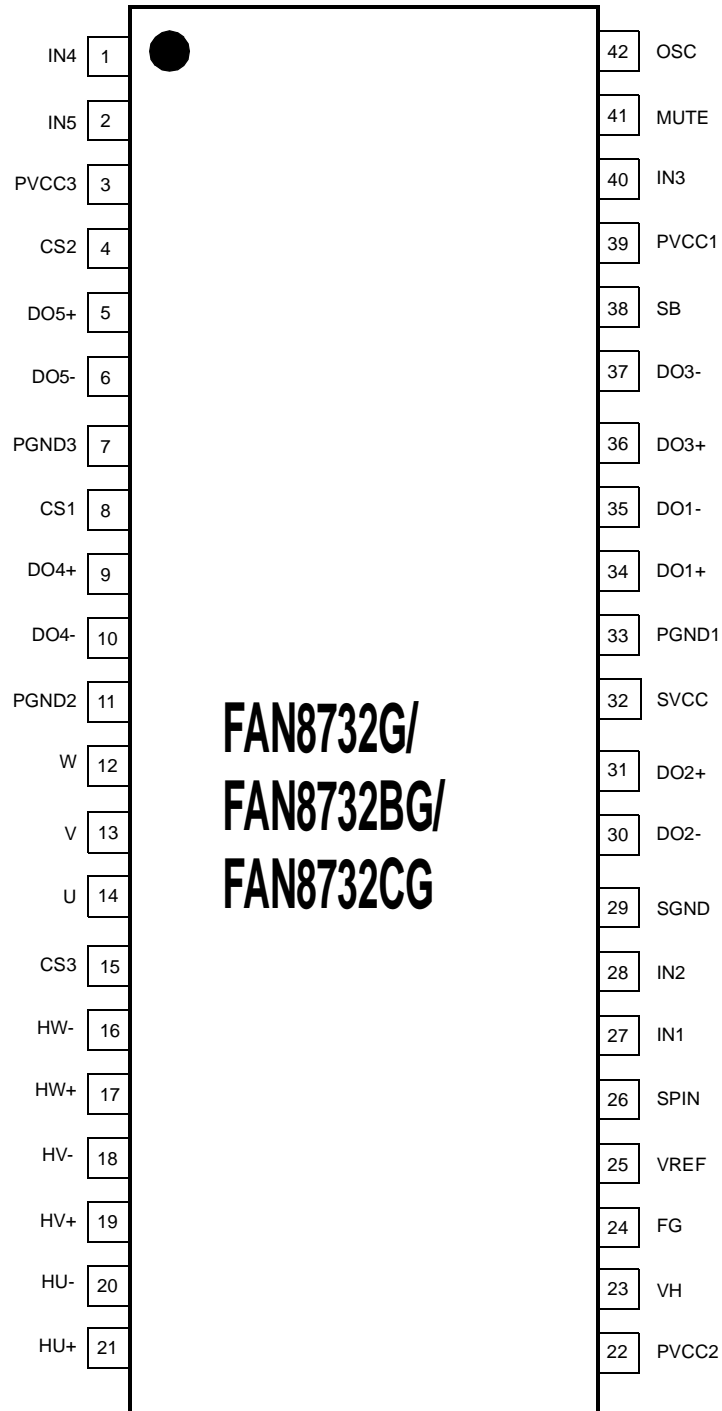
X:Tape & Reel type

FAN8732G:FG1X

FAN8732BG:FG3X

FAN8732CG:FG3X,Pull down resistor at SB pin

Pin Assignments



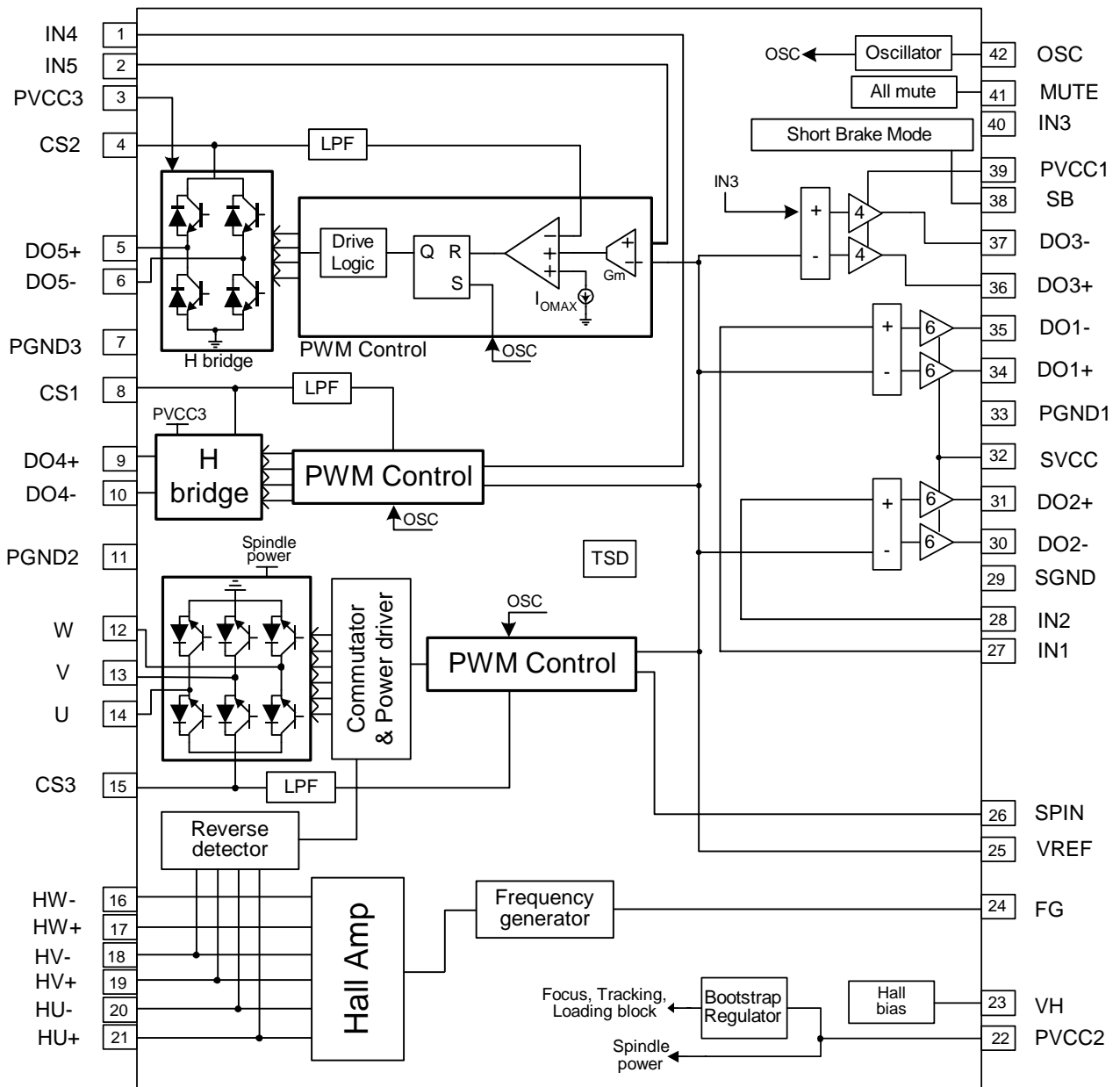
Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	IN4	I	CH4 input (typically sled1 input)
2	IN5	I	CH5 input (typically sled2 input)
3	PVCC3	-	Power supply for CH4 and CH5
4	CS2	-	Current sense for CH5
5	DO5 +	O	CH5 + drive output (typically sled2 output +)
6	DO5 -	O	CH5 - drive output (typically sled2 output -)
7	PGND3	-	Power ground 3
8	CS1	-	Current sense for CH4
9	DO4 +	O	CH4 + drive output (typically sled1 output +)
10	DO4 -	O	CH4 - drive output (typically sled1 output -)
11	PGND2	-	Power ground 2
12	W	O	3-phase output W for spindle
13	V	O	3-phase output V for spindle
14	U	O	3-phase output U for spindle
15	CS3	-	Current sense for spindle driver
16	HW -	I	Hall W(-) input
17	HW +	I	Hall W(+) input
18	HV -	I	Hall V(-) input
19	HV +	I	Hall V(+) input
20	HU -	I	Hall U(-) input
21	HU +	I	Hall U(+) input
22	PVCC2	-	Power supply for spindle driver
23	VH	I	Hall bias
24	FG	O	Frequency generator (FAN8732G:FG1X, FAN8732BG:FG3X)
25	VREF	I	Reference voltage input
26	SPIN	I	Spindle torque control
27	IN1	I	Channel 1 input (typically focus input)
28	IN2	I	Channel 2 input (typically tracking input)
29	SGND	-	Signal ground
30	DO2 -	O	CH2 - drive output (typically tracking output +)
31	DO2 +	O	CH2 + drive output (typically tracking output -)
32	SVCC	-	Power supply for signal block and CH1, CH2
33	PGND1	-	Power ground 1

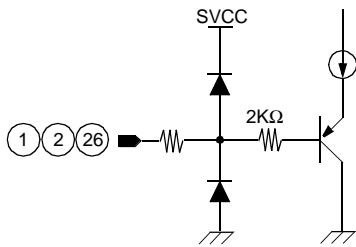
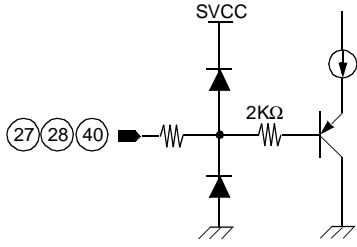
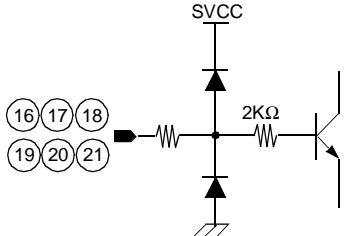
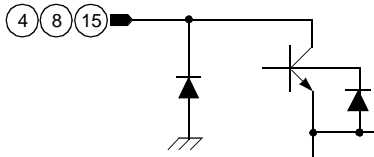
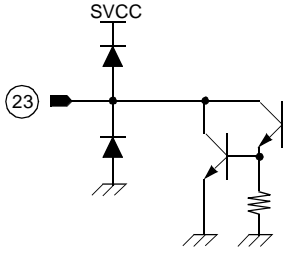
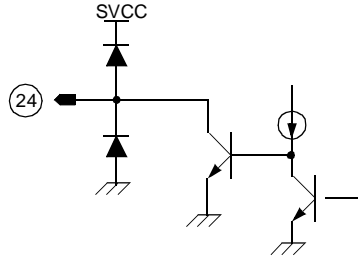
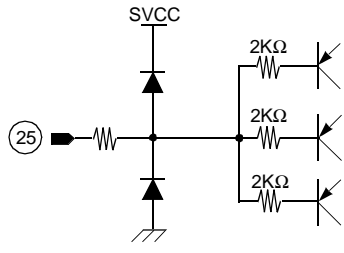
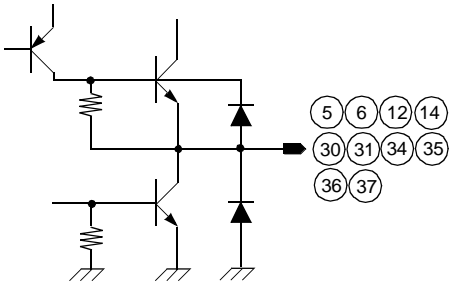
Pin Definitions (Continued)

Pin Number	Pin Name	I/O	Pin Function Description
34	DO1 +	O	CH1 + drive output ((typically focus output +)
35	DO1 -	O	CH1 - drive output (typically focus output -)
36	DO3 +	O	CH3 + drive output (typically loading output +)
37	DO3 -	O	CH3 - drive output (typically loading output -)
38	SB	I	Short Brake mode selection
39	PVCC1	-	Power supply for CH3
40	IN3	I	Channel 3 input (typically loading input)
41	MUTE	I	All channel mute
42	OSC	I	PWM carrier frequency set

Internal Block Diagram



Equivalent Circuits

Sled & Spindle Input	Actuator & Loading Input
 <p>The diagram shows a differential input circuit. A signal source (pins 1, 2, 26) is connected through a resistor to a central node. This node is connected to two diodes in series with an SVCC supply. A 2kΩ resistor connects this node to the base of a PNP transistor, which is also connected to an SVCC supply. The emitter of the transistor is grounded.</p>	 <p>The diagram shows a differential input circuit. A signal source (pins 27, 28, 40) is connected through a resistor to a central node. This node is connected to two diodes in series with an SVCC supply. A 2kΩ resistor connects this node to the base of a PNP transistor, which is also connected to an SVCC supply. The emitter of the transistor is grounded.</p>
Hall Input	Current Sense Input
 <p>The diagram shows a differential input circuit. A signal source (pins 16, 17, 18, 19, 20, 21) is connected through a resistor to a central node. This node is connected to two diodes in series with an SVCC supply. A 2kΩ resistor connects this node to the base of a PNP transistor, which is also connected to an SVCC supply. The emitter of the transistor is grounded.</p>	 <p>The diagram shows a current sense input circuit. A signal source (pins 4, 8, 15) is connected to a node that branches into two paths. One path goes through a diode to ground. The other path goes through a PNP transistor, which is also connected to an SVCC supply. The emitter of the transistor is grounded.</p>
Hall Bias Input	FG Output
 <p>The diagram shows a Hall bias input circuit. A signal source (pin 23) is connected to a node that branches into two paths. One path goes through a diode to ground. The other path goes through a PNP transistor, which is also connected to an SVCC supply. The emitter of the transistor is grounded.</p>	 <p>The diagram shows an FG output circuit. A signal source (pin 24) is connected to a node that branches into two paths. One path goes through a diode to ground. The other path goes through a PNP transistor, which is also connected to an SVCC supply. The emitter of the transistor is grounded.</p>
Vref Input	Drive Output
 <p>The diagram shows a Vref input circuit. A signal source (pin 25) is connected through a resistor to a central node. This node is connected to two diodes in series with an SVCC supply. A 2kΩ resistor connects this node to the base of a PNP transistor, which is also connected to an SVCC supply. The emitter of the transistor is grounded.</p>	 <p>The diagram shows a drive output circuit. A signal source (pins 5, 6, 12, 14, 30, 31, 34, 35, 36, 37) is connected to a node that branches into two paths. One path goes through a diode to ground. The other path goes through a PNP transistor, which is also connected to an SVCC supply. The emitter of the transistor is grounded.</p>

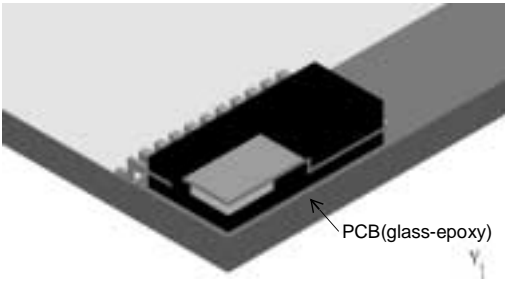
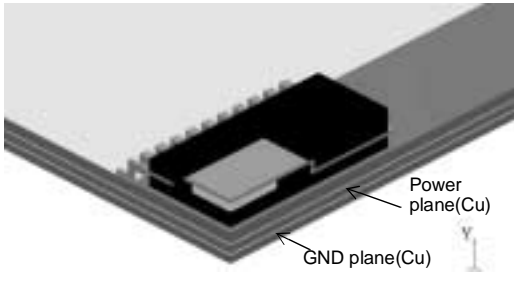
Equivalent Circuits (Continued)

Mute/SB Input(FAN8732G/BG)	Oscillation Input
SB Input(FAN8732CG)	

Absolute Maximum Ratings (Ta = 25°C)

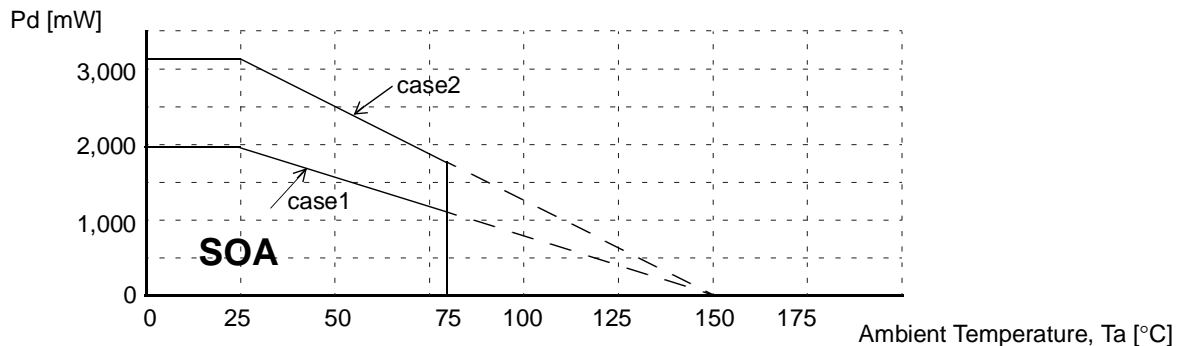
Parameter	Symbol	Value	Unit
Supply Voltage (Signal block & CH1,2)	SVCCmax	7	V
Supply Voltage (Power for CH3)	PVCC1max	15	V
Supply Voltage (Spindle driver)	PVCC2max	15	V
Supply Voltage (Power for CH4 & 5)	PVCC3max	15	V
Power dissipation	P _D	1.9 / 3.3 ^{NOTE}	W
Operating Temperature Range	T _{OPR}	-20 ~ +75	°C
Storage temperature Range	T _{STG}	-40 ~ +150	°C
Maximum Output Current (Spindle)	I _{Omax1}	1.5	A
Maximum Output Current (Focus, Tracking, Loading)	I _{Omax2}	1.0	A
Maximum Output Current (Sled)	I _{Omax3}	0.5	A

Note:

Case 1	Case 2	Remark
		Pd is measured base on the JEDEC/STD(JESD 51-2)
Pd=1.9W	Pd=3.3W	

1. Case 1: Single layer PCB with 1 signal plane only. PCB size is 76mm × 114mm × 1.6mm.
2. Case 2: Multi layer PCB with 1 signal, 1 power and 1 ground planes. PCB size is 76mm × 114mm × 1.6mm. Cu planes size for power and ground is 74mm × 62mm × 0.035mm.
3. These are experimental datum.
4. Power dissipation reduce rate of the case 1: -15.2mW/°C(Ta≥25°C)
5. Power dissipation reduce rate of the case 2: -26.4mW/°C(Ta≥25°C)
6. Should not exceed P_D and SOA (Safe Operating Area)

Power Dissipation Curve



Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Supply Voltage (Signal block & CH1,2)	SV _{CC}	4.5	5	7	V
Operating Supply Voltage (Power for CH3)	PV _{CC1}	4.5	12	13.2	V
Operating Supply Voltage (Spindle driver)	PV _{CC2}	6	12	13.2	V
Operating Supply Voltage (Power for CH4,5)	PV _{CC3}	4.5	12	13.2	V
Output current(Spindle)	IO1	-	0.5	1.0	A
Output current(Focus, Tracking, Loading)	IO2	-	0.5	0.8	A
Output current(Sled)	IO3	-	0.25	0.4	A
PWM carrier frequency	F _{osc}	30	-	120	KHz

Electrical Characteristics (Ta = 25°C)

(Ta=25°C, SVCC=PVCC1=5V, PVCC2=PVCC3=12V unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
COMMON PART						
Quiescent Circuit Current	I _{CC}	–	–	50	70	mA
Mute On Current	I _{MUTE}	MUTE=0V	–	0	30	μA
Mute On Voltage	V _{MON}	MUTE=variation	–	–	0.8	V
Mute Off Voltage	V _{MOFF}	MUTE=variation	2.5	–	–	V
Mute Input Current	I _{MUTEIN}	MUTE=5V	–	–	500	μA
PWM Carrier Frequency	F _{OSC}	C _{OSC} =330pF	–	65	–	KHz
REF input voltage range	V _{REFIN}	–	1.0	–	3.3	V
REF input current range	I _{REFIN}	V _{REF} =1.65V	-10	–	+10	μV
SB Low Voltage	V _{SBL}	SB=variation	–	–	0.8	V
SB High Voltage	V _{SBH}	SB=variation	2.5	–	–	V
SB Input Current1	I _{SB1}	SB=5V(FAN8732G/BG)	–	–	500	μA
SB Input Current2	I _{SB2}	SB=5V(FAN8732CG)	–	–	1.2	mA
SPINDLE DRIVE PART						
Maximum Output Voltage1	V _{OM1}	I _O =0.5A	10.6	11.1	–	V
Control Voltage Deadzone11	V _{DEAD11}	SPIN<VREF	-80	-40	0	mA
Control Voltage Deadzone12	V _{DEAD12}	SPIN>VREF	0	40	80	mA
Control Voltage Input Range1	V _{IN1}	–	0	–	5	V
Voltage Gain1	G _{VO1}	G _{I01} =G _{VO1} /R _{CS} [A/V]	0.85	1.0	1.15	V/V
Control Voltage Limit 1F	V _{LIMIT1F}	I _{LIMIT1F} =V _{LIMIT1F} /R _{CS} [A]	0.4	0.5	0.6	V
Control Voltage Limit 1R	V _{LIMIT1R}	I _{LIMIT1R} =V _{LIMIT1R} /R _{CS} [A]	0.22	0.28	0.34	V
Hall Amp Common Mode Input Range	V _{HCOM}	–	1.3	–	3.7	V
Hall Bias Output Voltage	V _{VH}	I _{VH} =10mA	0.6	0.85	1.2	V
VH pin Sink Current	I _{VH}	MUTE=5V	–	–	30	mA
CH4/CH5 DRIVE PART (TYPICALLY SLED DRIVER)						
Maximum Output Voltage21	V _{OM21}	I _O =0.5A, PVCC3=5V	3.4	3.8	–	V
Maximum Output Voltage22	V _{OM22}	I _O =0.5A, PVCC3=12V	10.3	10.8	–	V
Control Voltage Deadzone21	V _{DEAD21}	IN4,5<VREF	-80	-40	0	mV
Control Voltage Deadzone22	V _{DEAD22}	IN4,5>VREF	0	40	80	mV
Control Voltage Input Range2	V _{IN2}	–	0	–	5	V
Voltage Gain2	G _{VO2}	G _{I02} =G _{VO2} /R _{CS} [A/V]	0.85	1.0	1.15	V/V
Control Voltage Limit 2	V _{LIMIT2}	I _{LIMIT2} =V _{LIMIT2} /R _{CS} [A]	0.43	0.5	0.58	V
Output Leak Current	I _{LEAK}	MUTE=5V	-100	–	100	μA

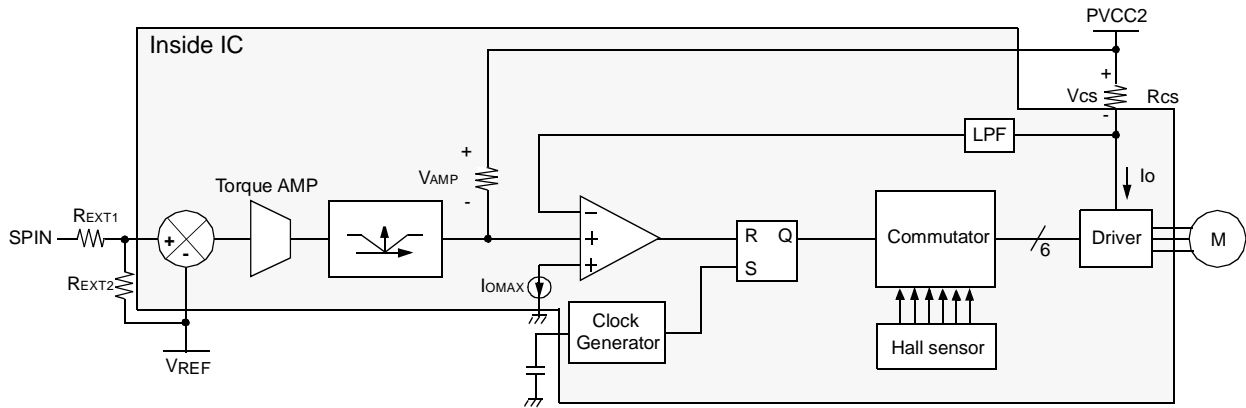
Electrical Characteristics (Ta = 25°C) (Continued)

(Ta=25°C, SVCC=PVCC1=5V, PVCC2=PVCC3=12V unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CH1,CH2 DRIVE PART (TYPICALLY ACTUATOR DRIVER)						
Maximum Output Voltage 31	V _{OM31}	I _O =0.5A, PV _{CC2} =12V	3.8	4.2	–	V
Control Voltage Input Range3	V _{IN3}	–	0	–	5	V
Closed Loop Voltage Gain	G _{V03}	–	20.2	21.6	22.8	dB
Output Offset Voltage	V _{OO1}	V _{REF} =IN1=IN2=1.65V	-45	–	45	mV
CH3 DRIVE PART (TYPICALLY LOADING DRIVER)						
Maximum Output Voltage 41	V _{OM41}	I _O =0.5A, PV _{CC1} =5V, PV _{CC2} =12V	3.95	4.2	–	V
Maximum Output Voltage 42	V _{OM42}	I _O =0.5A, PV _{CC1} =PV _{CC2} =12V	6.2	6.7	–	V
Control Voltage Input Range4	V _{IN4}	–	0	–	5	V
Closed Loop Voltage Gain	G _{V04}	–	16.7	18.1	19.3	dB
Output Offset Voltage	V _{OO2}	V _{REF} =IN3=1.65V	-50	–	50	mV

Application Information

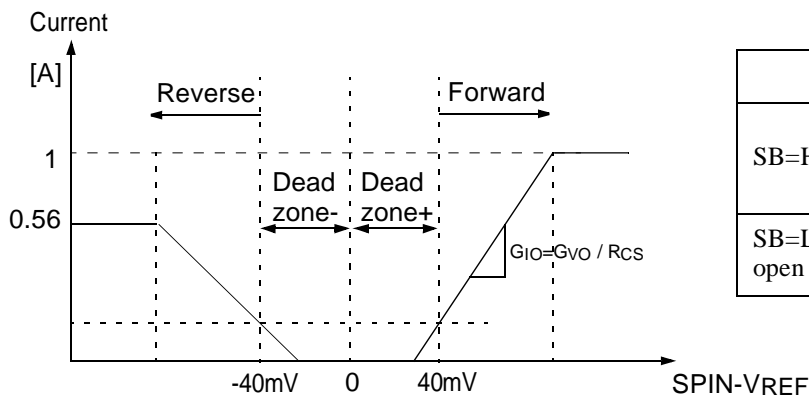
1. Torque Control & Output Current Control Of 3-phase Bldc Motor



- 1) By amplifying the voltage difference between VREF and SPIN from Servo IC(or DSP), the Torque AMP produces the input voltage(VAMP) which is input current command.
- 2) The output current (IO) is converted into the voltage (VCS) through the sense resistor (RCS) and compared with the VAMP.
- 3) The clock generator has the RS latch set periodically, this makes output driver on state and when the VCS and the VAMP is equal the state becomes off.
- 4) By the negative feedback loop, the sensed output voltage VCS equals to the VAMP.
- 5) Commutating sequence is selected by hall sensor inputs, and the minimum hall input voltage is 60mV.
- 6) The gain and limit current are calculated as below table.(Gvo=1[V/V])

Forward limit current	Reverse limit current	Input/Output gain[A/V]	Remark
$\frac{0.5}{R_{cs}}$	$\frac{0.28}{R_{cs}}$	$\frac{R_{EXT2}}{R_{EXT1} + R_{EXT2}} \cdot \frac{G_{VO}}{R_{CS}}$	$\frac{R_{EXT2}}{R_{EXT1} + R_{EXT2}}$ is gain scaler

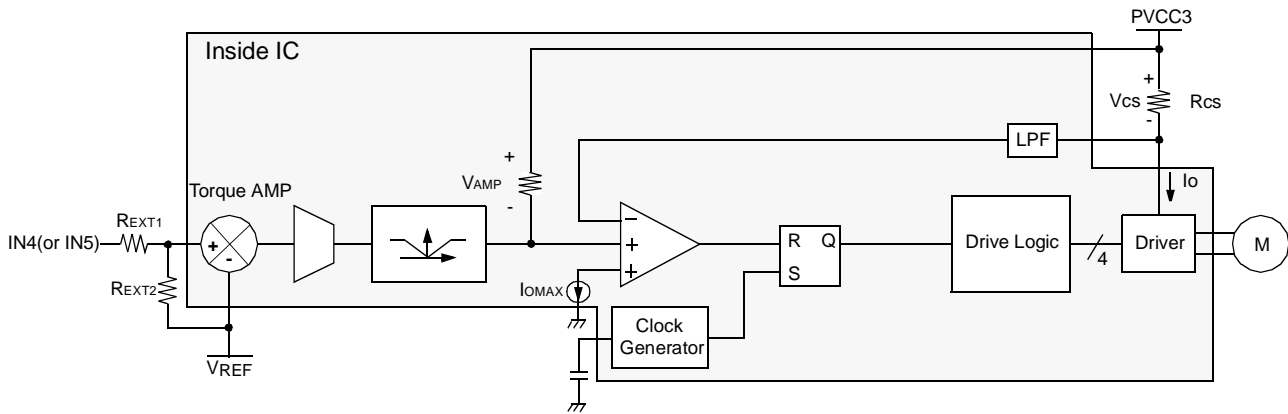
- 7) The range of the input voltage is as shown below when RCS=0.5Ω, REXT1=0 and REXT2=inf.



		Rotation
SB=H	SPIN > VREF	Forward rotation
	SPIN < VREF	Reverse brake
SB=L, open	-	Short brake

The input range of SPIN is 0 V ~ 5 V

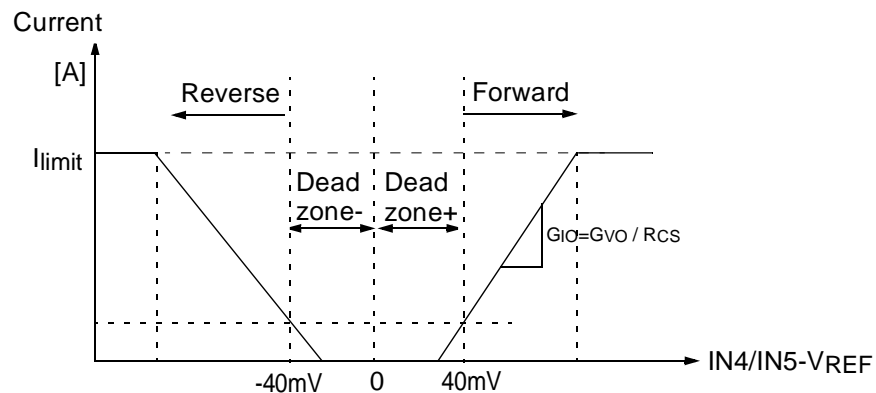
2. Torque Control & Output Current Control Of Sled Motor(2-phase Step Motor)



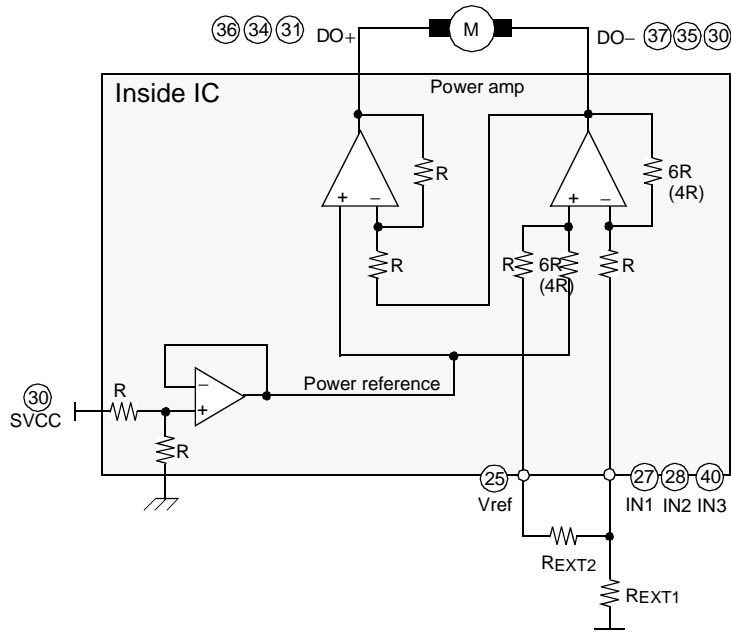
- 1) By amplifying the voltage difference between VREF and IN4(or IN5) from Servo IC(or DSP), the Torque AMP produces the input voltage(VAMP) which is input current command.
- 2) The output current (IO) is converted into the voltage (VCS) through the sense resistor (RCS) and compared with the VAMP.
- 3) The clock generator has the RS latch set periodically, this makes output driver on state and when the VCS and the VAMP is equal the state becomes off.
- 4) By the negative feedback loop, the sensed output voltage VCS equals to the VAMP.
- 5) To avoid output upper and lower transistor's short through, switch trick is needed. Turn on delay time is 1usec, turn off delay time is 2usec and the phase delay time, when the current direction is changed, is 3usec.
- 6) The gain and limit current are calculated as below table.(Gvo=1[V/V])

Torque limit current	Input/Output gain[A/V]	Remark
$\frac{0.5}{R_{cs}}$	$\frac{R_{EXT2}}{R_{EXT1} + R_{EXT2}} \cdot \frac{G_{VO}}{R_{CS}}$	$\frac{R_{EXT2}}{R_{EXT1} + R_{EXT2}}$ is gain scaler

- 8) The range of the torque voltage is as shown below when Rcs=0.5Ω, REXT1=0 and REXT2=inf.



3. CH1/CH2/CH3 Drive Part



- 1) The reference voltage, VREF, is given externally through pin 25.
- 2) The power amp circuit produces the differential output voltages and drives the two output power amplifier circuits.
- 3) The CH1/CH2 gain of DO- drive part of the power amp block is $6R/R=6$ times (and the gain of CH3 is $4R/R=4$ times). The DO+ drive part of the power amp block is just inverting circuit of DO- drive part so the total gain of power amp block is 12 times that is 21.58dB (in case of CH3, gain is 8 times that is 18.06dB).
- 4) Power reference voltage, which is the mid-point of the drive output, is set to the half of the supply voltage.
- 5) When the total gain is too high, the external resistors (R_{EXT1} & R_{EXT2}) can be used to make the gain proper.

Power amp gain	Input/Output gain[V/V]	Remark
12(21.58dB)	$\frac{R_{EXT2}}{R_{EXT1} + R_{EXT2}} \cdot 12$	$\frac{R_{EXT2}}{R_{EXT1} + R_{EXT2}}$ is gain scaler

4. Power Save & Channel Selection

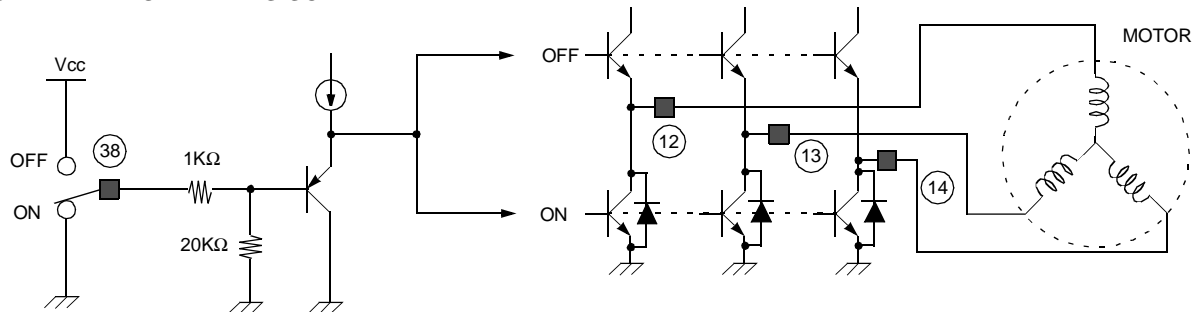
MUTE/SB logic tables are as below.

Logic Input		Drive Change					
Mute(pin41)	SB(pin38)	CH1	CH2	CH3	CH4	CH5	spindle
L	L	off	off	off	off	off	off
L	H	off	off	on	off	off	off
H	L	on	on	off	on	on	on
H	H	on	on	off	on	on	on

5. SB(Short Brake Mode Selection)

When SB pin enabled(low), the brake mechanism of 3-phase spindle driver is changed to short brake.

SHORT BRAKE OPERATING SCHEME



When short brake is enabled all lower output transistors are turned on and all upper output transistors are turned off, so the current due to the motor back EMF(electro motive force) is freewheeled through lower transistors and lower freewheeling diodes. It is general that the short brake is safer than the reverse brake in high speed applications. But it is not true in all cases because the current in the short brake is depend on the amount of the motor back EMF. So in high speed applications we suggest an optimal brake which is our patent. Please contact sales persons or offices if you need more information about the optimal brake.

6. TSD(Thermal Shut Down)

When the chip temperature rises up to about 160°C(degree), all output drivers are shut down. When the chip temperature falls off to about 130°C, then the drivers recover normal operation. TSD has the temperature hysteresis of about 30°C.

7. FG OUTPUT

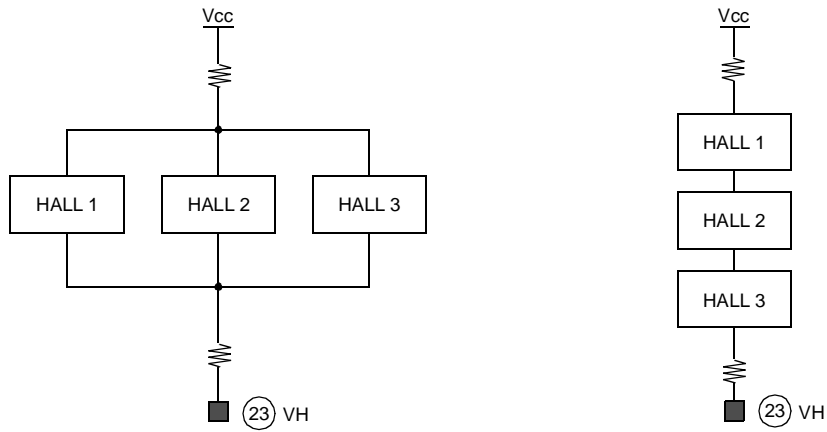
FAN8732G generates FG1X, meanwhile FAN8732BG/CG generates FG3X

8. PWM Carrier Frequency

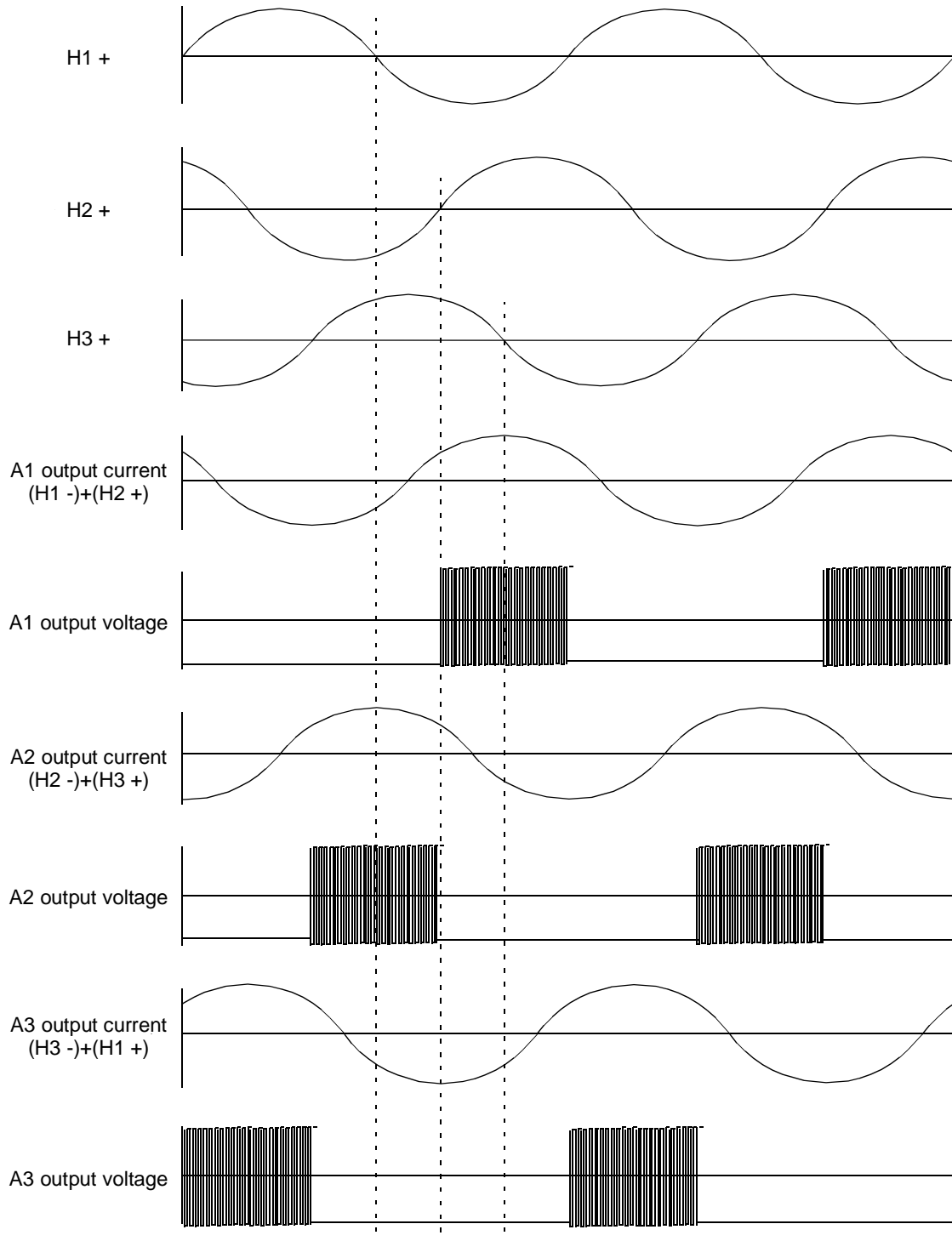
PWM carrier frequency is made from charging and discharging a capacitor which should be connected to osc(#42) pin. You can get typical pwm carrier frequency from below table.

capacitor[pF]	820	680	330	220	180	150	120
Carrier frequency[KHz]	28	32	65	90	110	143	179

9. Hall Sensor Connection

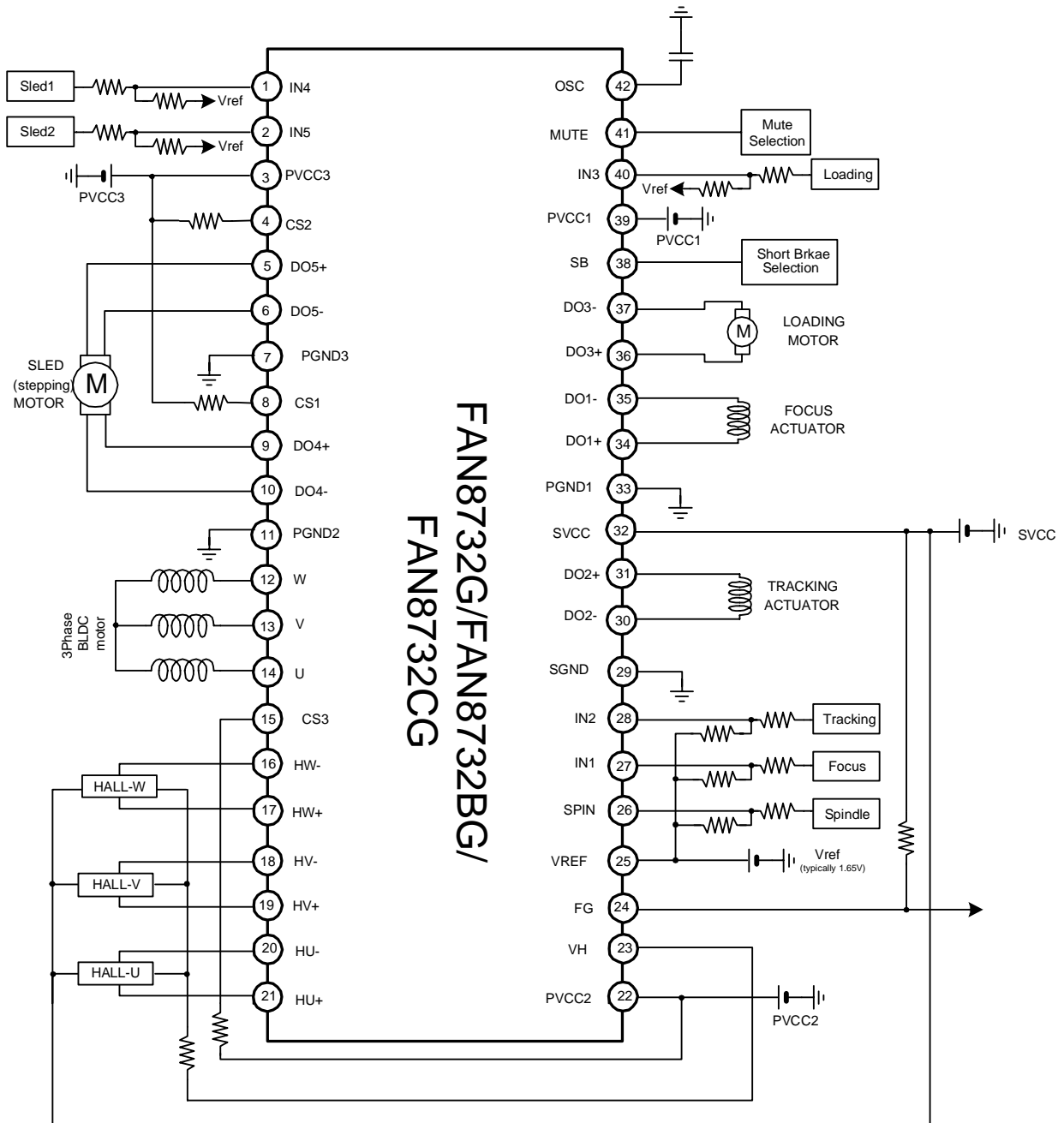


10. Spindle Part Input-output Timing Chart



The waveforms are different in accordance with motor types.

Typical Application Circuits



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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.