F4066/34066
QUAD BILATERAL SWITCHES

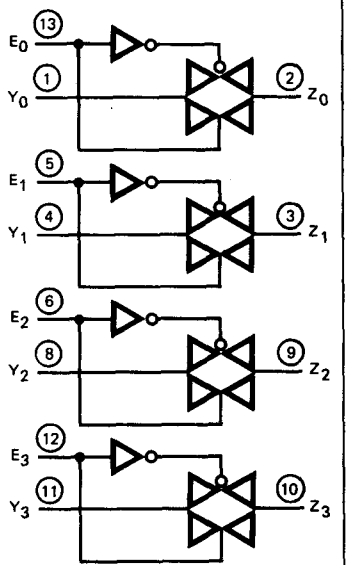
DESCRIPTION – The F4066 has four independent bilateral analog switches (transmission gates). Each switch has two Input/Output Terminals (Y_n, Z_n) and an active HIGH Enable Input (E_n). A HIGH on the Enable Input establishes a low impedance bidirectional path between Y_n and Z_n (ON condition). A LOW on the Enable Input disables the switch; high impedance between Y_n and Z_n (OFF condition).

- **DIGITAL OR ANALOG SIGNAL SWITCHING**
- **INDIVIDUAL ENABLE INPUTS (ACTIVE HIGH)**

PIN NAMES

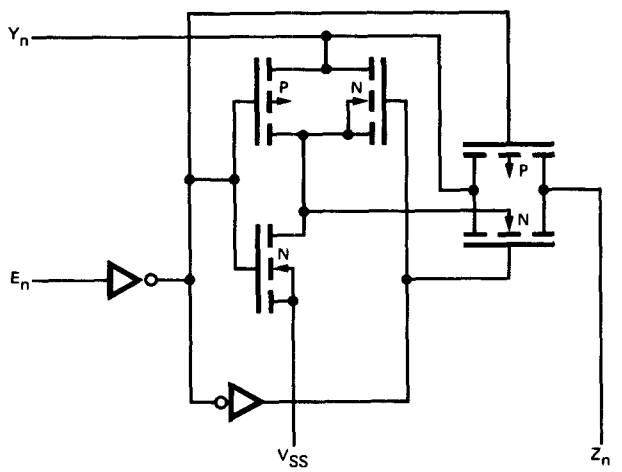
$E_0 - E_3$	Enable Inputs
$Y_0 - Y_3$	Input/Output Terminals
$Z_0 - Z_3$	Input/Output Terminals

LOGIC SYMBOL

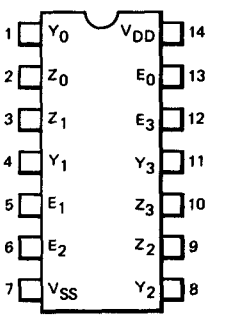


V_{DD} = Pin 14
V_{SS} = Pin 7
○ = Pin Numbers

LOGIC DIAGRAM (1/4 OF A F4066)



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

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DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
R_{ON}	ON Resistance	XC		190	900		100	450		80	250	Ω	MIN	R_L = 10 kΩ
				270	1000		120	500		80	280		25°C	E_n = V_{DD},
				330	1090		170	520		130	300		MAX	V_{is} = V_{DD} to V_{SS}
		XM		160	850		85	400		60	220	Ω	MIN	R_L = 10 kΩ
				270	1000		120	500		80	280		25°C	E_n = V_{DD},
				360	1150		190	550		145	320		MAX	V_{is} = V_{DD} to V_{SS}
ΔR_{ON}	"Δ" ON Resistance Between Any Two Switches						10			5		Ω	25°C	V_{is} = V_{DD} to V_{SS}, E_n = V_{DD} R_L = 10 kΩ
I_Z	OFF State Leakage Current, Any Y to Z							100			100	nA	25°C	V_{is} = V_{DD} or V_{SS}, E_n = V_{SS}
I_{DD}	Quiescent Power Supply Current	XC			0.25			0.5		0.1		μA	MIN, 25°C	All inputs common and at V_{DD} or V_{SS}
					25			30		6			MAX	
		XM			0.25			0.5		0.1		μA	MIN, 25°C	
					25			30		6			MAX	

Notes on following page.

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AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C(See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		4 3			1.5 1.5			1 1		ns	C_L = 15 pF, R_L = 10 kΩ Input Transition Times ≤ 20 ns E_n = V_{DD} V_{is} = V_{DD} (square wave)
t_{PZL} t_{PZH}	Output Enable Time		24 24			14 14			10 10		ns ns	C_L = 15 pF, R_L = 300Ω E_n = V_{DD} (square wave)
t_{PLZ} t_{PHZ}	Output Disable Time		160 160			170 170			182 182		ns ns	Input Transition Times ≤ 20 ns V_{is} = V_{DD}
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		8 8			3 4			2 2.5		ns ns	C_L = 50 pF, R_L = 10 kΩ Input Transition Times ≤ 20 ns E_n = V_{DD} V_{is} = V_{DD} (square wave)
t_{PZL} t_{PZH}	Output Enable Time		32 32			16 16			13 13		ns ns	C_L = 50 pF, R_L = 300Ω E_n = V_{DD} (square wave)
t_{PLZ} t_{PHZ}	Output Disable Time		380 380			380 380			400 400		ns ns	Input Transition Times ≤ 20 ns V_{is} = V_{DD}
	Distortion, Sine Wave Response		0.31			0.31			0.31		%	C_L = 15 pF, R_L = 10 kΩ Input Frequency = 1 kHz E_n = V_{DD} V_{is} = $V_{DD}/2$ (sine wave)
	Crosstalk Between Any Two Switches					0.9					MHz	R_L = 1 kΩ E_A = V_{DD}, E_B = V_{SS} V_{is} = $V_{DD}/2$ (sine wave) at -50 dB, 20 Log_{10} [V_{os} (B)/V_{is} (A)] = -50 dB
	Crosstalk, Enable Input to Output					50					mV	Input Transition Times ≤ 20 ns $R_{L(OUT)}$ = 10 kΩ , $R_{L(IN)}$ = 1 kΩ E_n = V_{DD} (square wave)
	OFF State Feedthrough					1.25					MHz	R_L = 1 kΩ E_n = V_{SS}, V_{is} = $V_{DD}/2$(sine wave) 20 Log_{10} (V_{os}/V_{is}) = -50 dB
	ON State Frequency Response					90					MHz	R_L = 1 kΩ V_{is} = $V_{DD}/2$ (sine wave) E_n = V_{DD}, 20 Log_{10} (V_{os}/V_{is}) = -3 dB
f_{MAX}	Enable Input Frequency (Note 3)					10					MHz	C_L = 15 pF, R_L = 1 kΩ Input Transition Times ≤ 20 ns E_n = V_{DD} (square wave) V_{is} = V_{DD}

NOTES:
1. Additional DC Characteristics for the Enable Inputs are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. V_{is}/V_{os} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).

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