

## **FDS6676**

# 30V N-Channel PowerTrench® MOSFET

### **General Description**

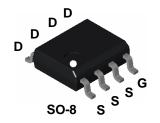
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{\text{DS(ON)}}$  and fast switching speed.

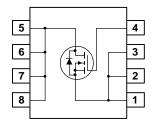
### **Applications**

DC/DC converter

### **Features**

- 14.5 A, 30 V.  $R_{DS(ON)}=7~m\Omega$  @  $V_{GS}=10~V$   $R_{DS(ON)}=8~m\Omega$  @  $V_{GS}=4.5~V$
- High performance trench technology for extremely low  $R_{\mbox{\scriptsize DS}(\mbox{\scriptsize ON})}$
- Low gate charge (45 nC typ)
- High power and current handling capability





## Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage		30	V
V <sub>GSS</sub>	Gate-Source Voltage		± 16	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	14.5	A
	- Pulsed		50	
P <sub>D</sub>	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1.0	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Tempera	ture Range	-55 to +175	°C

## **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1c)	125	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

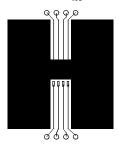
**Package Marking and Ordering Information** 

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6676 FDS6676		13"	12mm	2500 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics			•	I.	
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V
ΔBV <sub>DSS</sub> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		24		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage, Forward	V <sub>GS</sub> = 16 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	$V_{GS} = -16 \text{ V},  V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	1	1.5	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		<b>-</b> 5		mV/°C
R <sub>DS(on)</sub>	Static Drain-Source	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 14.5 A		4.8	7	mΩ
	On–Resistance	$V_{GS} = 4.5 \text{ V},  I_{D} = 13.5 \text{ A}$		5.4	8	
	On Otata Busin Comment	$V_{GS} = 10 \text{ V}, I_D = 14.5 \text{ A}, T_J = 125^{\circ}\text{C}$		7.3	11.5	
I <sub>D(on)</sub>	On–State Drain Current	$V_{GS} = 10 \text{ V}, \qquad V_{DS} = 5 \text{ V}$	50			Α
<b>g</b> FS	Forward Transconductance	$V_{DS} = 5 \text{ V}, \qquad I_{D} = 14.5 \text{ A}$		80		S
Dynamic	Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$		5103		pF
Coss	Output Capacitance	f = 1.0 MHz		836		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			361		pF
Switchin	g Characteristics (Note 2)					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 15 \text{ V}, \qquad I_D = 1 \text{ A},$		15	27	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 5 \text{ V},  R_{GEN} = 6 \Omega$		9	18	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			87	139	ns
t <sub>f</sub>	Turn-Off Fall Time			40	64	ns
Q <sub>g</sub>	Total Gate Charge	$V_{DS} = 15 \text{ V}, \qquad I_{D} = 14.5 \text{ A},$		45	63	nC
Q <sub>gs</sub>	Gate-Source Charge	$V_{GS} = 5 \text{ V}$		13		nC
$Q_{gd}$	Gate-Drain Charge			12		nC
Drain-Se	ource Diode Characteristics	and Maximum Ratings		•		•
Is	Maximum Continuous Drain-Sourc				2.1	Α
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, \qquad I_S = 2.1 \text{ A (Note 2)}$		0.7	1.2	V

#### Notes:

<sup>1.</sup>  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 50°C/W when mounted on a 1in² pad of 2 oz copper



b) 105°C/W when mounted on a .04 in<sup>2</sup> pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.



Scale 1:1 on letter size paper

**2.** Pulse Test: Pulse Width <  $300\mu s$ , Duty Cycle < 2.0%

## **Typical Characteristics**

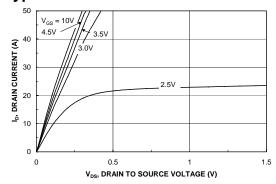
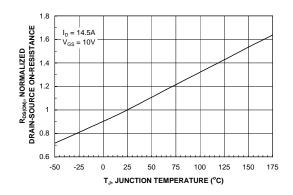


Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.



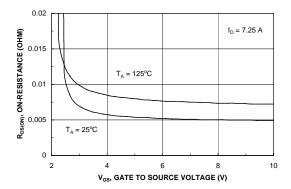
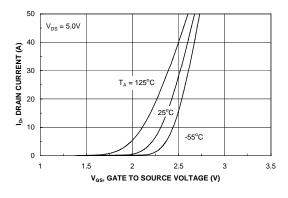


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



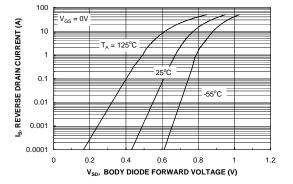
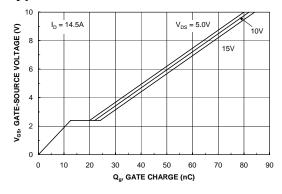


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## **Typical Characteristics**



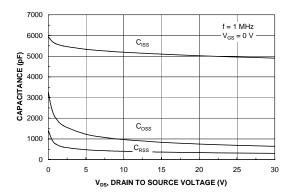
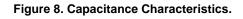
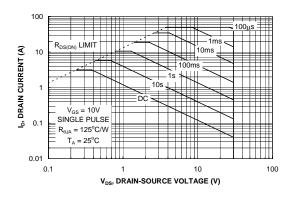


Figure 7. Gate Charge Characteristics.





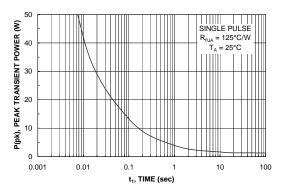


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

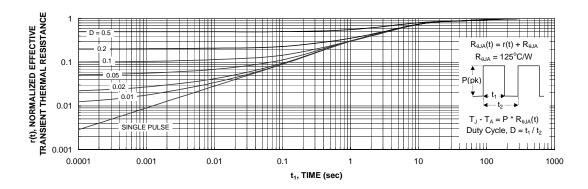


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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