

Features

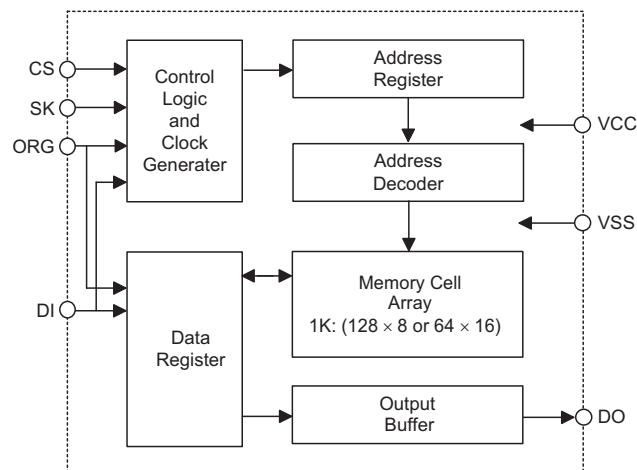
- Operating voltage: 2.2V~5.5V for temperature -40°C to +85°C
- Low power consumption
 - Operating: 5mA max.
 - Standby: 2μA max.
- User selectable internal organization
 - 1K(HT93LC46): 128×8 or 64×16
- 3-wire Serial Interface
- Write cycle time: 5ms max.
- Automatic erase-before-write operation
- Word/chip erase and write operation
- Write operation with built-in timer
- Software controlled write protection
- 40-year data retention
- 10⁶ rewrite cycles per word
- Industrial temperature range (-40°C to +85°C)
- 8-pin DIP/SOP/TSSOP package

General Description

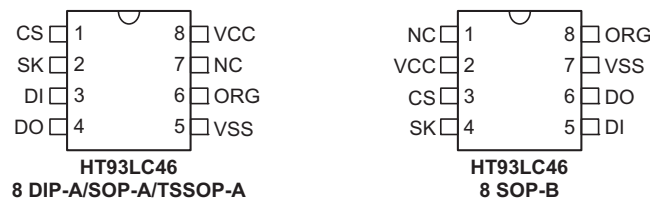
The HT93LC46 is a 1K-bit low voltage nonvolatile, serial electrically erasable programmable read only memory device using the CMOS floating gate process. Its 1024 bits of memory are organized into 64 words of 16 bits each when the ORG pin is connected to VCC or organized into 128 words of 8 bits each when it is tied to VSS. The device is

optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. By popular microcontroller, the versatile serial interface including chip select (CS), serial clock (SK), data input (DI) and data output (DO) can be easily controlled.

Block Diagram



Pin Assignment



Pin Description

| Pin Name | I/O | Description |
|----------|-----|--|
| CS | I | Chip select input |
| SK | I | Serial clock input |
| DI | I | Serial data input |
| DO | O | Serial data output |
| VSS | — | Negative power supply, ground |
| ORG | I | Internal Organization When ORG is connected to VDD or ORG is floated, the ($\times 16$) memory organization is selected. When ORG is tied to VSS, the ($\times 8$) memory organization is selected. There is an internal pull-up resistor on the ORG pin. |
| NC | — | No connection |
| VCC | — | Positive power supply |

Absolute Maximum Ratings

| | | | |
|----------------------|--------------------------------|----------------------------|----------------------------------|
| Supply Voltage | $V_{SS}-0.3V$ to $V_{SS}+6.0V$ | Storage Temperature | $-50^{\circ}C$ to $125^{\circ}C$ |
| Input Voltage..... | $V_{SS}-0.3V$ to $V_{DD}+0.3V$ | Operating Temperature..... | $-40^{\circ}C$ to $85^{\circ}C$ |

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------|----------------------------------|----------------------|------|--------------------|---------|
| | | V _{CC} | Conditions | | | | |
| V _{CC} | Operating Voltage | — | $-40^{\circ}C$ to $+85^{\circ}C$ | 2.2 | — | 5.5 | V |
| I _{CC1} | Operating Current (TTL) | 5V | DO unload, SK=1MHz | — | — | 5 | mA |
| I _{CC2} | Operating Current (CMOS) | 5V | DO unload, SK=1MHz | — | — | 5 | mA |
| | | 2.2V~5.5V | DO unload, SK=250kHz | — | — | 5 | mA |
| I _{STB} | Standby Current (CMOS) | 2.2V~5.5V | CS=SK=DI=0V | — | — | 2 | μA |
| I _{LI} | Input Leakage Current | 5V | $V_{IN}=V_{SS}-V_{CC}$ | 0 | — | 1 | μA |
| I _{LO} | Output Leakage Current | 5V | $V_{OUT}=V_{SS}-V_{CC}$, CS=0V | 0 | — | 1 | μA |
| V _{IL} | Input Low Voltage | 5V | — | 0 | — | 0.8 | V |
| | | 2.2V~5.5V | — | 0 | — | 0.1V _{CC} | V |
| V _{IH} | Input High Voltage | 5V | — | 2 | — | V _{CC} | V |
| | | 2.2V~5.5V | — | 0.9V _{CC} | — | V _{CC} | V |
| V _{OL} | Output Low Voltage | 5V | I _{OL} =2.1mA | — | — | 0.4 | V |
| | | 2.2V~5.5V | I _{OL} =10 μA | — | — | 0.2 | V |
| V _{OH} | Output High Voltage | 5V | I _{OH} =-400 μA | 2.4 | — | — | V |
| | | 2.2V~5.5V | I _{OH} =-10 μA | V _{CC} -0.2 | — | — | V |
| C _{IN} | Input Capacitance | — | $V_{IN}=0V$, f=250kHz | — | — | 5 | pF |
| C _{OUT} | Output Capacitance | — | $V_{OUT}=0V$, f=250kHz | — | — | 5 | pF |

A.C. Characteristics

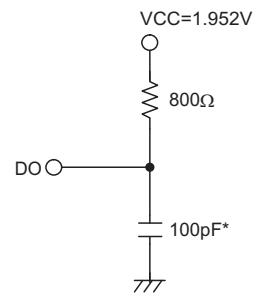
| Symbol | Parameter | V _{CC} =5V±10% | | V _{CC} =3V±10% | | V _{CC} =2.2V | | Unit |
|------------------|-------------------|-------------------------|------|-------------------------|------|-----------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| f _{SK} | Clock Frequency | 0 | 2000 | 0 | 1000 | 0 | 500 | kHz |
| t _{SKH} | SK High Time | 250 | — | 500 | — | 1000 | — | ns |
| t _{SKL} | SK Low Time | 250 | — | 500 | — | 1000 | — | ns |
| t _{CSS} | CS Setup Time | 50 | — | 100 | — | 100 | — | ns |
| t _{CSH} | CS Hold Time | 0 | — | 0 | — | 0 | — | ns |
| t _{CDS} | CS Deselect Time | 250 | — | 250 | — | 500 | — | ns |
| t _{DIS} | DI Setup Time | 100 | — | 150 | — | 200 | — | ns |
| t _{DIH} | DI Hold Time | 100 | — | 150 | — | 200 | — | ns |
| t _{PD1} | DO Delay to "1" | — | 250 | — | 500 | — | 1000 | ns |
| t _{PD0} | DO Delay to "0" | — | 250 | — | 500 | — | 1000 | ns |
| t _{SV} | Status Valid Time | — | 250 | — | 250 | — | 250 | ns |
| t _{HZ} | DO Disable Time | — | 100 | — | 200 | — | 400 | ns |
| t _{PR} | Write Cycle Time | — | 5 | — | 5 | — | 5 | ms |

A.C. Test Conditions

Input rise and fall time: 5ns (1V to 2V)

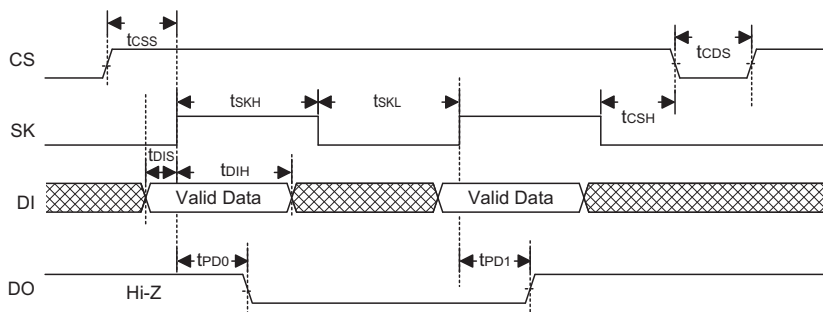
Input and output timing reference levels: 1.5V

Output load: See Figure right



*Including scope and jig

Output Load Circuit



Functional Description

The HT93LC46 is accessed via a three-wire serial communication interface. The device is arranged into 64 words by 16 bits or 128 words by 8 bits depending whether the ORG pin is connected to VCC or VSS. The HT93LC46 contains seven instructions: READ, ERASE, WRITE, EWEN, EWDS, ERAL and WRAL. When the user selectable internal organization is arranged into 64×16 (128×8), these instructions are all made up of 9(10) bits data: 1 start bit, 2 op code bits and 6(7) address bits.

By using the control signal CS, SK and data input signal DI, these instructions can be given to the HT93LC46. These serial instruction data presented at the DI input will be written into the device at the rising edge of SK. During the READ cycle, DO pin acts as the data output and during the WRITE or ERASE cycle, DO pin indicates the BUSY/READY status. When the DO pin is active for read data or as a BUSY/READY indicator the CS pin must be high; otherwise DO pin will be in a high-impedance state. For successful instructions, CS must be low once after the instruction is sent. After power on, the device is by default in the EWDS state. And, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. The following are the functional descriptions and timing diagrams of all seven instructions.

READ

The READ instruction will stream out data at a specified address on the DO pin. The data on DO pin changes during the low-to-high edge of SK signal. The 8 bits or 16 bits data stream is preceded by a logical "0" dummy bit. Irrespective of the condition of the EWEN or EWDS instruction, the READ command is always valid and independent of these two instructions. After the data word has been read the internal address will be automatically incremented by 1 allowing the next consecutive data word to be read out without entering further address data. The address will wrap around with CS High until CS returns to LOW.

EWEN/EWDS

The EWEN/EWDS instruction will enable or disable the programming capabilities. At both the power on and power off state the device automatically entered the disable mode. Before a WRITE, ERASE, WRAL or ERAL instruction is given, the programming enable instruction EWEN must be issued, otherwise the ERASE/WRITE instruction is invalid. After the EWEN instruction is issued, the programming enable condition remains until power is turned off or a EWDS instruction is given. No data can be written into the device in the programming disabled state. By so doing, the internal memory data can be protected.

ERASE

The ERASE instruction erases data at the specified addresses in the programming enable mode. After the ERASE op-code and the specified address have been issued, the data erase is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signals for the internal erase, so the SK clock is not required. During the internal erase, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over, the DO pin will return to high and further instructions can be executed.

WRITE

The WRITE instruction writes data into the device at the specified addresses in the programming enable mode. After the WRITE op-code and the specified address and data have been issued, the data writing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signal for the internal writing, so the SK clock is not required. The auto-timing write cycle includes an automatic erase-before-write capability. So, it is not necessary to erase data before the WRITE instruction. During the internal writing, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over, the DO pin will return to high and further instructions can be executed.

ERAL

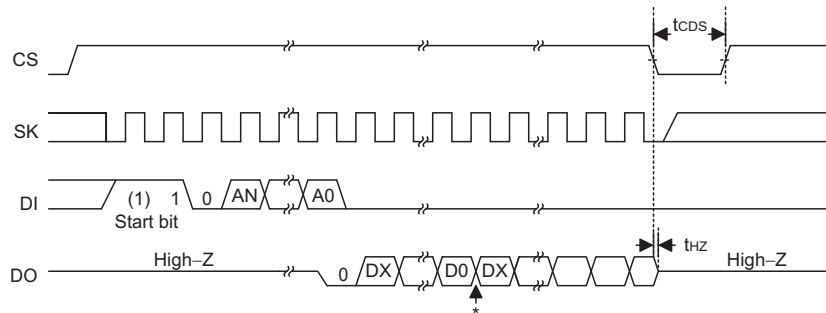
The ERAL instruction erases the entire 64×16 or 128×8 memory cells to logical "1" state in the programming enable mode. After the erase-all instruction set has been issued, the data erase feature is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signal for the erase-all operation, so the SK clock is not required. During the internal erase-all operation, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over, the DO pin will return to high and further instruction can be executed.

WRAL

The WRAL instruction writes data into the entire 64×16 or 128×8 memory cells in the programming enable mode. After the write-all instruction set has been issued, the data writing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signals for the write-all operation, so the SK clock is not required. During the internal write-all operation, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over the DO pin will return to high and further instruction can be executed.

Timing Diagrams

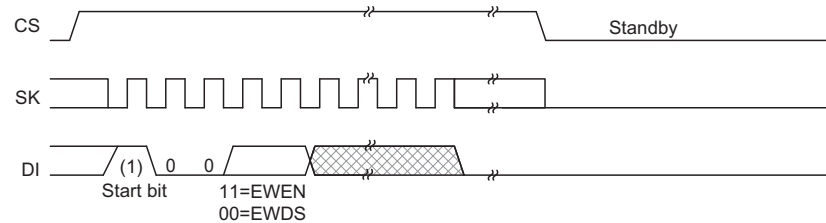
READ



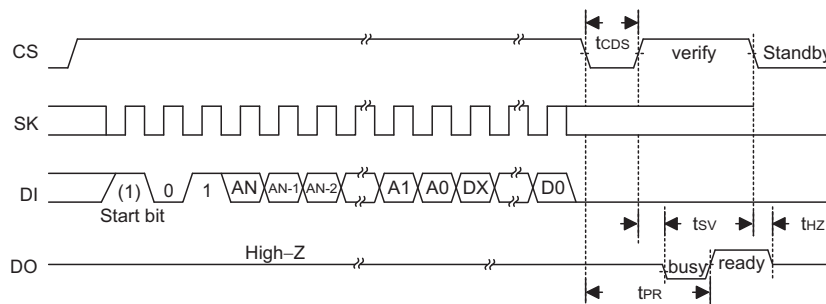
* Address pointer automatically cycles to the next word

| | | |
|------|-------|------|
| Mode | (X16) | (X8) |
| AN | A5 | A6 |
| DX | D15 | D7 |

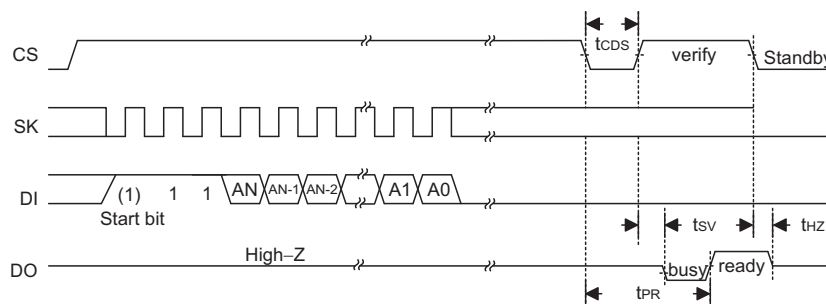
EWEN/EWDS

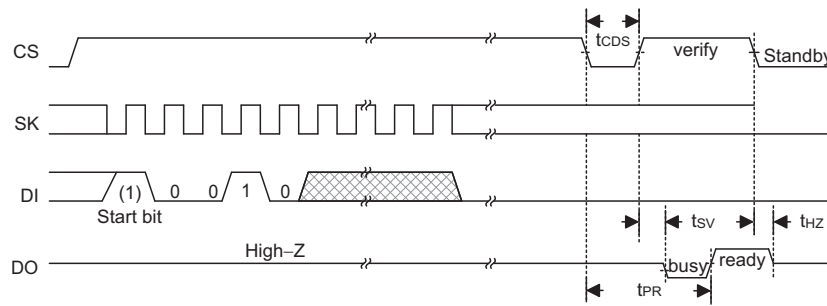
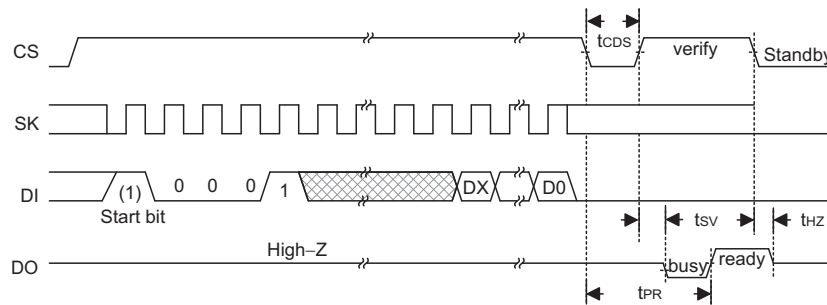


WRITE



ERASE



ERAL

WRAL

Instruction Set Summary

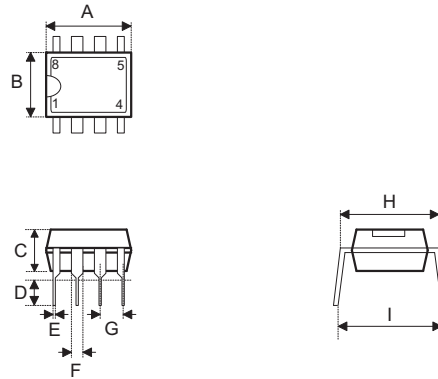
| Instruction | Comments | Start bit | Op Code | Address | | Data | |
|-------------|---------------------|-----------|---------|----------|-----------|----------|-----------|
| | | | | ORG=0 X8 | ORG=1 X16 | ORG=0 X8 | ORG=1 X16 |
| READ | Read data | 1 | 10 | A6~A0 | A5~A0 | D7~D0 | D15~D0 |
| ERASE | Erase data | 1 | 11 | A6~A0 | A5~A0 | — | — |
| WRITE | Write data | 1 | 01 | A6~A0 | A5~A0 | D7~D0 | D15~D0 |
| EWEN | Erase/Write Enable | 1 | 00 | 11XXXXX | 11XXXX | — | — |
| EWDS | Erase/Write Disable | 1 | 00 | 00XXXXX | 00XXXX | — | — |
| ERAL | Erase All | 1 | 00 | 10XXXXX | 10XXXX | — | — |
| WRAL | Write All | 1 | 00 | 01XXXXX | 01XXXX | D7~D0 | D15~D0 |

Note: "X" stands for "don't care"

Data should be written to the EEPROM in the format (8-bit or 16-bit mode) in which it is to be read.

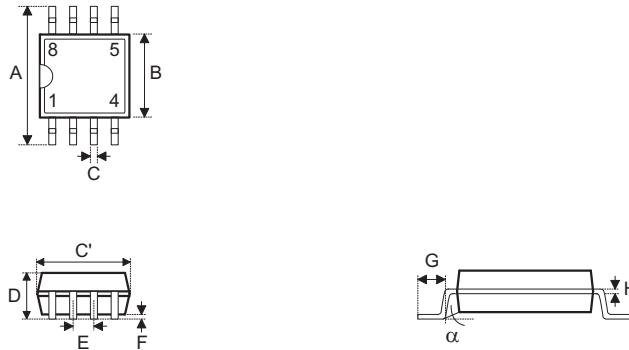
Package Information

8-pin DIP (300mil) Outline Dimensions



| Symbol | Dimensions in inch | | |
|--------|--------------------|-------|-------|
| | Min. | Nom. | Max. |
| A | 0.355 | — | 0.375 |
| B | 0.240 | — | 0.260 |
| C | 0.125 | — | 0.135 |
| D | 0.125 | — | 0.145 |
| E | 0.016 | — | 0.020 |
| F | 0.050 | — | 0.070 |
| G | — | 0.100 | — |
| H | 0.295 | — | 0.315 |
| I | — | 0.375 | — |

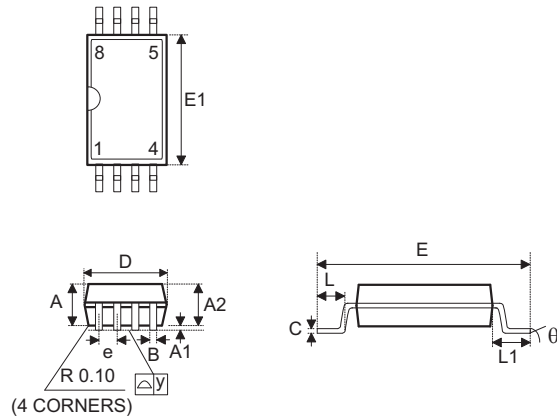
| Symbol | Dimensions in mm | | |
|--------|------------------|------|------|
| | Min. | Nom. | Max. |
| A | 9.02 | — | 9.53 |
| B | 6.10 | — | 6.60 |
| C | 3.18 | — | 3.43 |
| D | 3.18 | — | 3.68 |
| E | 0.41 | — | 0.51 |
| F | 1.27 | — | 1.78 |
| G | — | 2.54 | — |
| H | 7.49 | — | 8.00 |
| I | — | 9.53 | — |

8-pin SOP (150mil) Outline Dimensions


• MS-012

| Symbol | Dimensions in inch | | |
|----------|--------------------|-------|-------|
| | Min. | Nom. | Max. |
| A | 0.228 | — | 0.244 |
| B | 0.150 | — | 0.157 |
| C | 0.012 | — | 0.020 |
| C' | 0.188 | — | 0.197 |
| D | — | — | 0.069 |
| E | — | 0.050 | — |
| F | 0.004 | — | 0.010 |
| G | 0.016 | — | 0.050 |
| H | 0.007 | — | 0.010 |
| α | 0° | — | 8° |

| Symbol | Dimensions in mm | | |
|----------|------------------|------|------|
| | Min. | Nom. | Max. |
| A | 5.79 | — | 6.20 |
| B | 3.81 | — | 3.99 |
| C | 0.30 | — | 0.51 |
| C' | 4.78 | — | 5.00 |
| D | — | — | 1.75 |
| E | — | 1.27 | — |
| F | 0.10 | — | 0.25 |
| G | 0.41 | — | 1.27 |
| H | 0.18 | — | 0.25 |
| α | 0° | — | 8° |

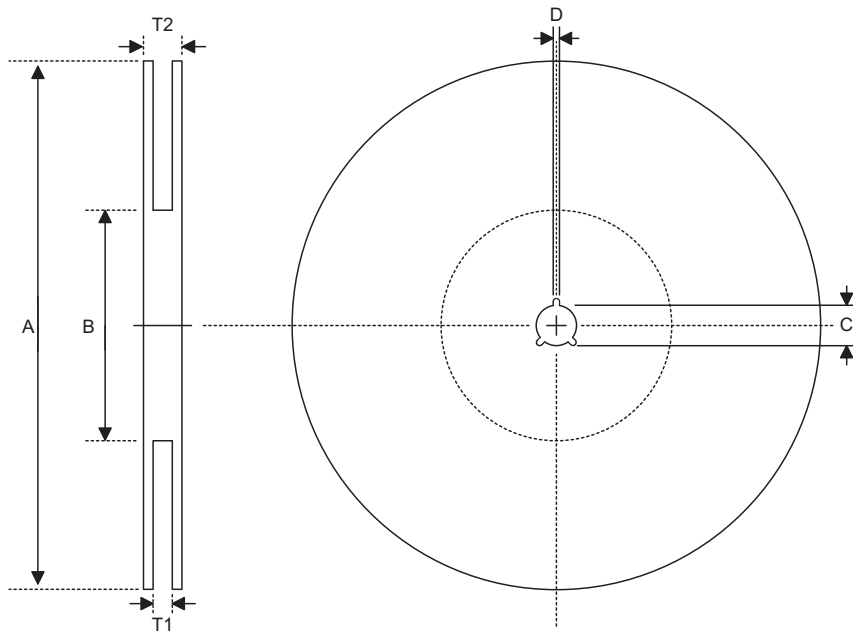
8-pin TSSOP Outline Dimensions


| Symbol | Dimensions in inch | | |
|----------|--------------------|-------|-------|
| | Min. | Nom. | Max. |
| A | 0.041 | — | 0.047 |
| A1 | 0.002 | — | 0.006 |
| A2 | 0.031 | — | 0.041 |
| B | — | 0.010 | — |
| C | 0.004 | — | 0.006 |
| D | 0.114 | — | 0.122 |
| E | 0.244 | — | 0.260 |
| E1 | 0.169 | — | 0.177 |
| e | — | 0.026 | — |
| L | 0.020 | — | 0.028 |
| L1 | 0.035 | — | 0.043 |
| y | — | — | 0.004 |
| θ | 0° | — | 8° |

| Symbol | Dimensions in mm | | |
|----------|------------------|------|------|
| | Min. | Nom. | Max. |
| A | 1.05 | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.80 | — | 1.05 |
| B | — | 0.25 | — |
| C | 0.11 | — | 0.15 |
| D | 2.90 | — | 3.10 |
| E | 6.20 | — | 6.60 |
| E1 | 4.30 | — | 4.50 |
| e | — | 0.65 | — |
| L | 0.50 | — | 0.70 |
| L1 | 0.90 | — | 1.10 |
| y | — | — | 0.10 |
| θ | 0° | — | 8° |

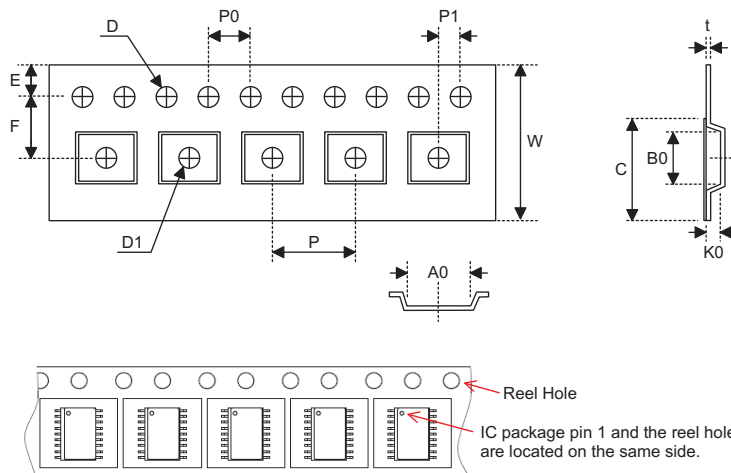
Product Tape and Reel Specifications

Reel Dimensions



SOP 8N, TSSOP 8L

| Symbol | Description | Dimensions in mm |
|--------|-----------------------|---------------------------|
| A | Reel Outer Diameter | 330.0±1.0 |
| B | Reel Inner Diameter | 100.0±1.5 |
| C | Spindle Hole Diameter | 13.0 ^{+0.5/-0.2} |
| D | Key Slit Width | 2.0±0.5 |
| T1 | Space Between Flange | 12.8 ^{+0.3/-0.2} |
| T2 | Reel Thickness | 18.2±0.2 |

Carrier Tape Dimensions

SOP 8N

| Symbol | Description | Dimensions in mm |
|--------|--|---------------------------|
| W | Carrier Tape Width | 12.0 ^{+0.3/-0.1} |
| P | Cavity Pitch | 8.0±0.1 |
| E | Perforation Position | 1.75±0.1 |
| F | Cavity to Perforation (Width Direction) | 5.5±0.1 |
| D | Perforation Diameter | 1.55±0.10 |
| D1 | Cavity Hole Diameter | 1.50±0.25 |
| P0 | Perforation Pitch | 4.0±0.1 |
| P1 | Cavity to Perforation (Length Direction) | 2.0±0.1 |
| A0 | Cavity Length | 6.4±0.1 |
| B0 | Cavity Width | 5.2±0.1 |
| K0 | Cavity Depth | 2.1±0.1 |
| t | Carrier Tape Thickness | 0.30±0.05 |
| C | Cover Tape Width | 9.3±0.1 |

TSSOP 8L

| Symbol | Description | Dimensions in mm |
|--------|--|---------------------------|
| W | Carrier Tape Width | 12.0 ^{+0.3/-0.1} |
| P | Cavity Pitch | 8.0±0.1 |
| E | Perforation Position | 1.75±0.10 |
| F | Cavity to Perforation (Width Direction) | 5.5±0.5 |
| D | Perforation Diameter | 1.5 ^{+0.1/-0.0} |
| D1 | Cavity Hole Diameter | 1.5 ^{+0.1/-0.0} |
| P0 | Perforation Pitch | 4.0±0.1 |
| P1 | Cavity to Perforation (Length Direction) | 2.0±0.1 |
| A0 | Cavity Length | 7.0±0.1 |
| B0 | Cavity Width | 3.6±0.1 |
| K0 | Cavity Depth | 1.6±0.1 |
| t | Carrier Tape Thickness | 0.300±0.013 |
| C | Cover Tape Width | 9.3±0.1 |

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