

**LC75347E**

## Six-Channel Single-Chip Electronic Volume Control System

Preliminary



### Overview

The LC75347E is a 6-channel 97-step electronic volume control system IC that provides a 2-channel input selector, bass and treble tone controls, external output ports, and a zero-cross volume switching function.

### Functions

- Volume: 0 to -95 dB (in 1 dB steps) and  $-\infty$ , for a total of 97 positions.  
Each of the six input channels can be controlled independently.
- Bass and treble: Each band can be controlled over a  $\pm 12$  dB range in 2 dB steps.  
The bass control provides peaking characteristics and the treble control provides shelving characteristics.
- Selector: 2-channel input selector
- Zero cross: Provides independent zero-cross detection for each of the 6 channels and a timer overflow detection circuit.
- External muting: Mute in/mute out function using zero-cross detection and dedicated pins.
- External output ports: Provides 4 n-channel transistor open-drain outputs.

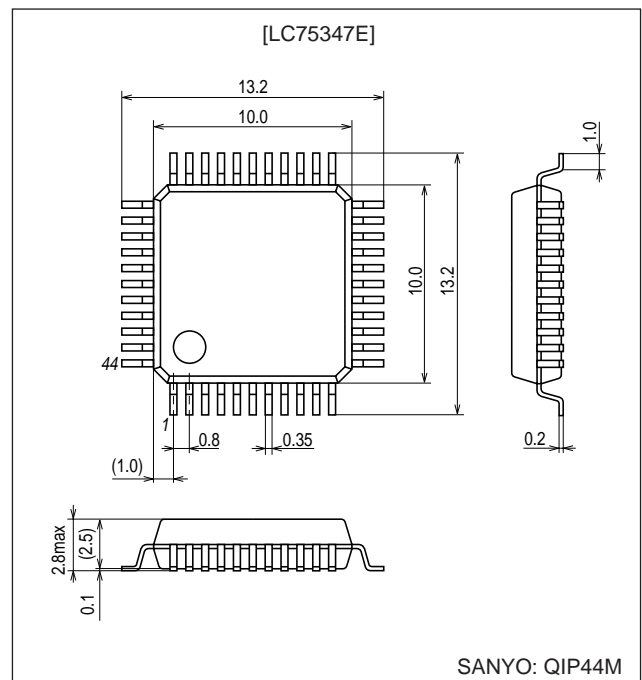
### Features

- Built-in buffer amplifiers reduce the number of external components to a minimum.
- Fabricated in a silicon-gate CMOS process for minimal noise generation from internal switches.

- Built-in analog ground reference voltage generator circuit
- All settings are controlled by serial data transmitted over a CCB interface.

### Package Dimensions

unit: mm

**3148A-QIP44M**

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## LC75347E

### Specifications

#### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Pin	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$	$V_{DD}$		11	V
Maximum input voltage	$V_{IN1\text{ max}}$	CE, DI, CL, MUTE OUTP1 to OUTP4		-0.3 to +11	V
	$V_{IN2\text{ max}}$	FL, FR, RL, RR, C, SBW, FLTON, FRTON, FLIN, FRIN		$V_{SS} - 0.3$ to $V_{DD} + 0.3$	
Output current	$I_{OUT}$	OUTP1 to OUTP4		0 to 1	mA
Allowable power dissipation	$P_{dmax}$		$T_a \leq 85^\circ\text{C}$ *1. When mounted on a PCB	600	mW
Operating temperature	$T_{opr}$			-40 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$			-50 to +125	$^\circ\text{C}$

\*1: PCB dimensions:  $76.1 \times 114.3 \times 1.6\text{ mm}$ , PCB materials: glass epoxy

#### Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Supply voltage	$V_{DD}$	$V_{DD}$		4.5		10.5	V
High-level input voltage	$V_{IH}$	CL, DI, CE, MUTE OUTP1 to OUTP4		2.5		10.5	V
Low-level input voltage	$V_{IL}$	CL, DI, CE, MUTE	$7.5 \leq V_{DD} \leq 10.5$	$V_{SS}$		0.8	V
			$4.5 \leq V_{DD} < 7.5$	$V_{SS}$		0.3	
Input amplitude	$V_{IN}$	FL, FR, RL, RR, C, SBW, FLTON, FRTON, FLIN, FRIN		$V_{SS}$		$V_{DD}$	Vp-p
Input pulse width	$t_{\theta W}$	CL		1			$\mu\text{s}$
Setup time	$t_{setup}$	CL, DI, CE		1			$\mu\text{s}$
Hold time	$t_{hold}$	CL, DI, CE		1			$\mu\text{s}$
Operating frequency	$f_{opg}$	CL				500	kHz

#### Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $V_{DD} = 9\text{ V}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
[Volume and Selector Blocks]							
Input resistance	$R_{in}$	FL, FR, RL, RR, C, SBW, FLTON, FRTON, FLIN, FRIN			50		$\text{k}\Omega$
[[Treble Band Equalizer Control Block]							
Control range	$G_{eq}$		max. boost/cut	$\pm 10$	$\pm 12$	$\pm 14$	dB
Step resolution	$E_{step}$			1	2	3	dB
Internal feedback resistance	$R_{feed}$				51.7		$\text{k}\Omega$
[Bass Band Equalizer Control Block]							
Control range	$G_{eq}$		max. boost/cut	$\pm 10$	$\pm 12$	$\pm 14$	dB
Step resolution	$E_{step}$			1	2	3	dB
Internal feedback resistance	$R_{feed}$				38.9		$\text{k}\Omega$
[Output Port Block]							
Low-level output voltage	$V_0$	OUTP1 to OUTP4	$R_h = 10\text{ k}\Omega$ , $V_d = 5\text{ V}$			0.5	V

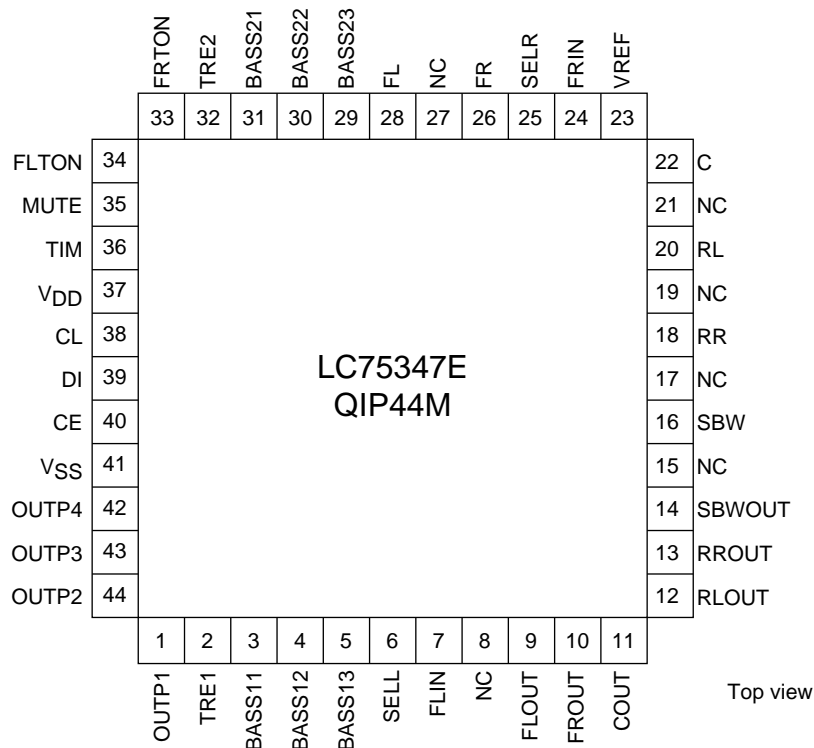
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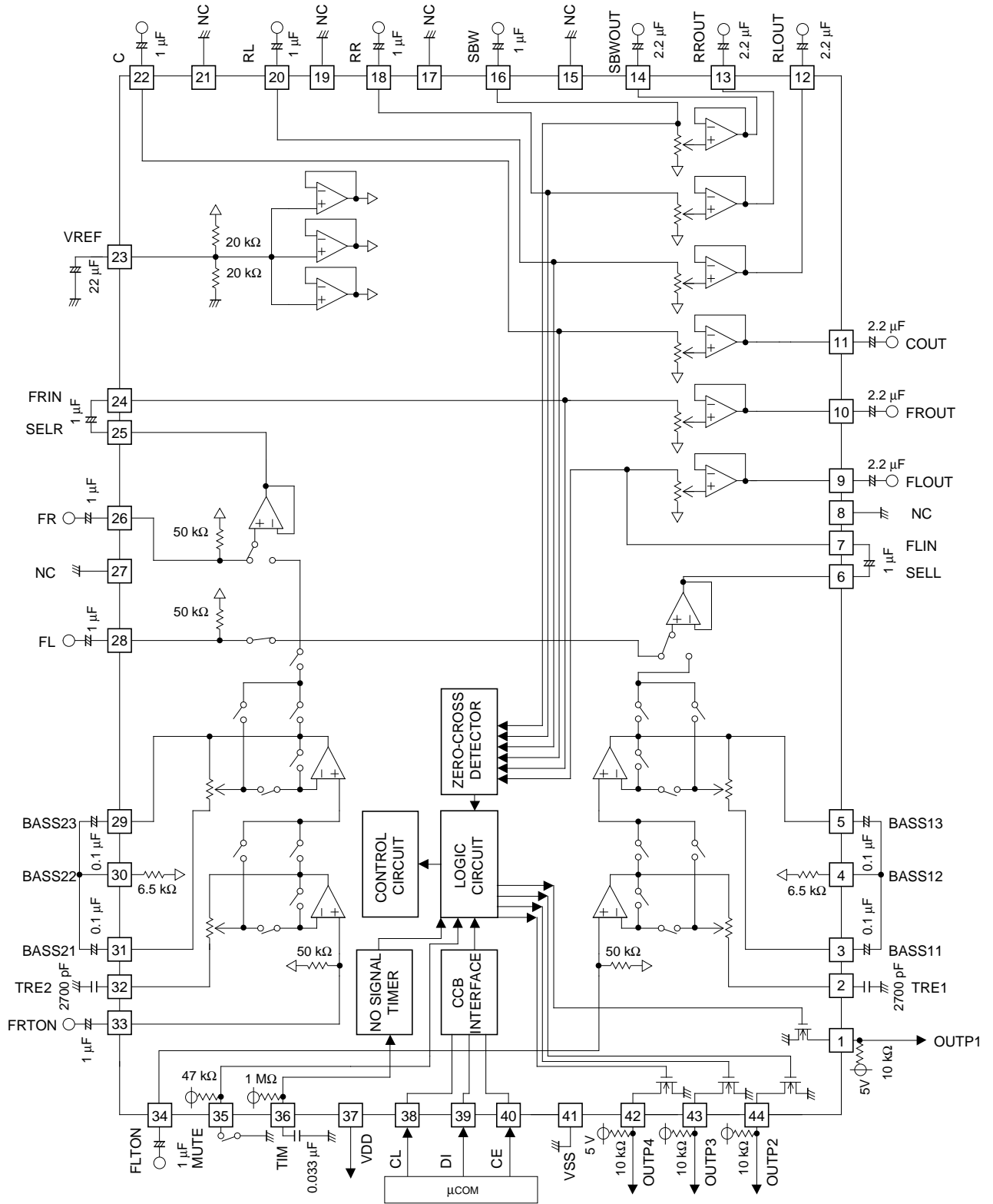
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>[Overall Characteristics]</b>						
Total harmonic distortion (RL, RR, C and SBW inputs, direct output)	THD1	$V_{IN} = 1 \text{ V}_{rms}$ , $f = 1 \text{ kHz}$ , 80 kHz LPF Flat overall		0.001	0.01	%
Total harmonic distortion (FL and FR inputs, direct output)	THD2	$V_{IN} = 1 \text{ V}_{rms}$ , $f = 1 \text{ kHz}$ , 80 kHz LPF Flat overall FL and FR selected, direct output		0.002	0.01	
Total harmonic distortion (FLTON and FRTON inputs, FLOUT and FROUT outputs)	THD3	$V_{IN} = 1 \text{ V}_{rms}$ , $f = 1 \text{ kHz}$ , 80 kHz LPF Flat overall FLTON and FRTON selected, output after passing through tone controls.		0.003	0.01	
Output noise voltage (RL, RR, C and SBW inputs, direct output)	VN1	80 kHz LPF, $R_g = 1 \text{ k}\Omega$ All controls flat overall		6		$\mu\text{V}$
		A-WIGHT, $R_g = 1 \text{ k}\Omega$ All controls flat overall		2.5		
Output noise voltage (FL and FR inputs, direct output)	VN2	80 kHz LPF, $R_g = 1 \text{ k}\Omega$ All controls flat overall		7		
		A-WIGHT, $R_g = 1 \text{ k}\Omega$ All controls flat overall		3		
Output noise voltage (FLTON and FRTON inputs, FLOUT and FROUT outputs)	VN3	80 kHz LPF, $R_g = 1 \text{ k}\Omega$ All controls flat overall		9		
		A-WIGHT, $R_g = 1 \text{ k}\Omega$ All controls flat overall		4		
Characteristics at maximum attenuation	Vomin	$V_{IN} = 1 \text{ V}_{rms}$ , $f = 1 \text{ kHz}$ , 80 kHz LPF All controls flat overall		-95		dB
Crosstalk	CT	$V_{IN} = 1 \text{ V}_{rms}$ , $f = 1 \text{ kHz}$ , $R_g = 1 \text{ k}\Omega$ All controls flat overall	80			dB
Current drain	$I_{DD}$	$V_{DD} - V_{SS} = +9 \text{ V}$		38		mA
High-level input current	$I_{IH}$	CL, DI, CE, MUTE: $V_{IN} = 10.5 \text{ V}$ , $V_{DD} = 10.5 \text{ V}$			10	$\mu\text{A}$
Low-level input current	$I_{IL}$	CL, DI, CE, MUTE: $V_{IN} = 0 \text{ V}$ , $V_{DD} = 10.5 \text{ V}$	-10			$\mu\text{A}$

### Pin Assignment



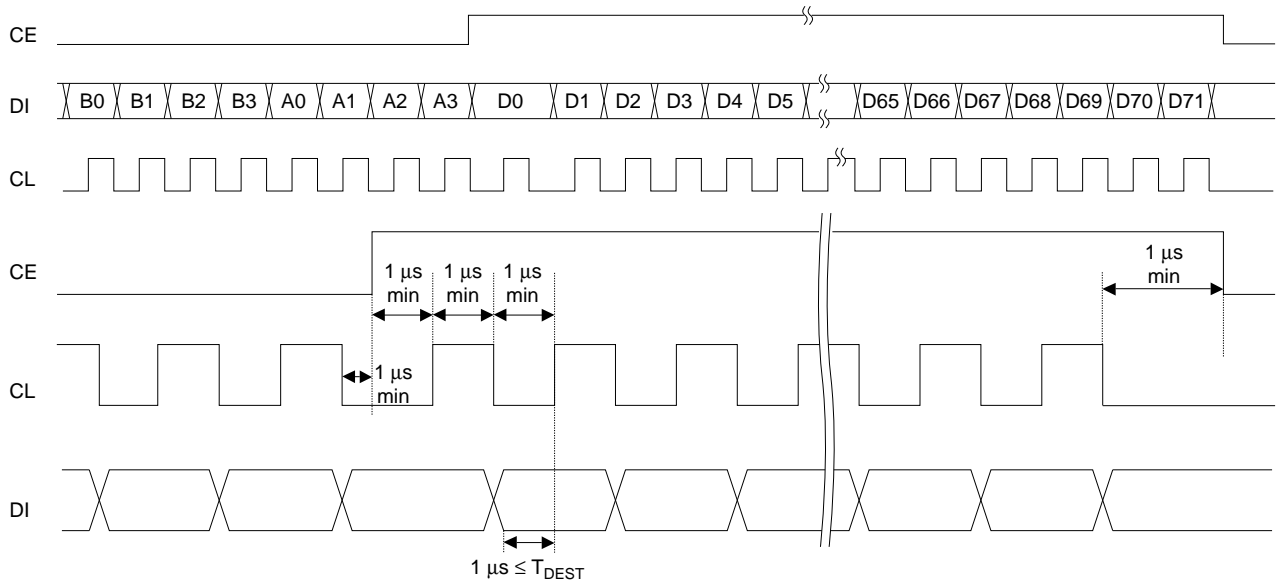
NC: No Connect

Equivalent Circuit/Application Circuit Example



**Control System Timing and Data Format**

The stipulated serial data must be applied to the CL, DI, and CE pins to control the LC75347E. The data consists of 80 bits, of which 8 bits are address and 72 bits are data.



• Address Code (B0 to A3)

This IC has an 8-bit address code and can be used with the same specifications as other Sanyo CCB serial bus ICs.

Address code	B0	B1	B2	B3	A0	A1	A2	A3
(LSB) (82HEX)	0	1	0	0	0	0	0	1

## LC75347E

### • Control Code Allocations

#### Volume Control

D0	D1	D2	D3	D4	D5	D6	D7	SBW setting
D8	D9	D10	D11	D12	D13	D14	D15	RR setting
D16	D17	D18	D19	D20	D21	D22	D23	RL setting
D24	D25	D26	D27	D28	D29	D30	D31	C setting
D32	D33	D34	D35	D36	D37	D38	D39	FRIN setting
D40	D41	D42	D43	D44	D45	D46	D47	FLIN setting
0	0	0	0	0	0	0	0	0 dB
1	0	0	0	0	0	0	0	-1 dB
0	1	0	0	0	0	0	0	-2 dB
1	1	0	0	0	0	0	0	-3 dB
0	0	1	0	0	0	0	0	-4 dB
1	0	1	0	0	0	0	0	-5 dB
0	1	1	0	0	0	0	0	-6 dB
1	1	1	0	0	0	0	0	-7 dB
0	0	0	1	0	0	0	0	-8 dB
1	0	0	1	0	0	0	0	-9 dB
0	1	0	1	0	0	0	0	-10 dB
1	1	0	1	0	0	0	0	-11 dB
0	0	1	1	0	0	0	0	-12 dB
1	0	1	1	0	0	0	0	-13 dB
0	1	1	1	0	0	0	0	-14 dB
1	1	1	1	0	0	0	0	-15 dB
0	0	0	0	1	0	0	0	-16 dB
1	0	0	0	1	0	0	0	-17 dB
0	1	0	0	1	0	0	0	-18 dB
1	1	0	0	1	0	0	0	-19 dB
0	0	1	0	1	0	0	0	-20 dB
1	0	1	0	1	0	0	0	-21 dB
0	1	1	0	1	0	0	0	-22 dB
1	1	1	0	1	0	0	0	-23 dB
0	0	0	1	1	0	0	0	-24 dB
1	0	0	1	1	0	0	0	-25 dB
0	1	0	1	1	0	0	0	-26 dB
1	1	0	1	1	0	0	0	-27 dB
0	0	1	1	1	0	0	0	-28 dB
1	0	1	1	1	0	0	0	-29 dB
0	1	1	1	1	0	0	0	-30 dB
1	1	1	1	1	0	0	0	-31 dB
0	0	0	0	0	1	0	0	-32 dB
1	0	0	0	0	1	0	0	-33 dB
0	1	0	0	0	1	0	0	-34 dB
1	1	0	0	0	1	0	0	-35 dB
0	0	1	0	0	1	0	0	-36 dB
1	0	1	0	0	1	0	0	-37 dB
0	1	1	0	0	1	0	0	-38 dB
1	1	1	0	0	1	0	0	-39 dB
0	0	0	1	0	1	0	0	-40 dB
1	0	0	1	0	1	0	0	-41 dB
0	1	0	1	0	1	0	0	-42 dB
1	1	0	1	0	1	0	0	-43 dB
0	0	1	1	0	1	0	0	-44 dB
1	0	1	1	0	1	0	0	-45 dB
0	1	1	1	0	1	0	0	-46 dB

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D0	D1	D2	D3	D4	D5	D6	D7	SBW setting
D8	D9	D10	D11	D12	D13	D14	D15	RR setting
D16	D17	D18	D19	D20	D21	D22	D23	RL setting
D24	D25	D26	D27	D28	D29	D30	D31	C setting
D32	D33	D34	D35	D36	D37	D38	D39	FRIN setting
D40	D41	D42	D43	D44	D45	D46	D47	FLIN setting
1	1	1	1	0	1	0	0	-47 dB
0	0	0	0	1	1	0	0	-48 dB
1	0	0	0	1	1	0	0	-49 dB
0	1	0	0	1	1	0	0	-50 dB
1	1	0	0	1	1	0	0	-51 dB
0	0	1	0	1	1	0	0	-52 dB
1	0	1	0	1	1	0	0	-53 dB
0	1	1	0	1	1	0	0	-54 dB
1	1	1	0	1	1	0	0	-55 dB
0	0	0	1	1	1	0	0	-56 dB
1	0	0	1	1	1	0	0	-57 dB
0	1	0	1	1	1	0	0	-58 dB
1	1	0	1	1	1	0	0	-59 dB
0	0	1	1	1	1	0	0	-60 dB
1	0	1	1	1	1	0	0	-61 dB
0	1	1	1	1	1	0	0	-62 dB
1	1	1	1	1	1	0	0	-63 dB
0	0	0	0	0	0	1	0	-64 dB
1	0	0	0	0	0	1	0	-65 dB
0	1	0	0	0	0	1	0	-66 dB
1	1	0	0	0	0	1	0	-67 dB
0	0	1	0	0	0	1	0	-68 dB
1	0	1	0	0	0	1	0	-69 dB
0	1	1	0	0	0	1	0	-70 dB
1	1	1	0	0	0	1	0	-71 dB
0	0	0	1	0	0	1	0	-72 dB
1	0	0	1	0	0	1	0	-73 dB
0	1	0	1	0	0	1	0	-74 dB
1	1	0	1	0	0	1	0	-75 dB
0	0	1	1	0	0	1	0	-76 dB
1	0	1	1	0	0	1	0	-77 dB
0	1	1	1	0	0	1	0	-78 dB
1	1	1	1	0	0	1	0	-79 dB
0	0	0	0	1	0	1	0	-80 dB
1	0	0	0	1	0	1	0	-81 dB
0	1	0	0	1	0	1	0	-82 dB
1	1	0	0	1	0	1	0	-83 dB
0	0	1	0	1	0	1	0	-84 dB
1	0	1	0	1	0	1	0	-85 dB
0	1	1	0	1	0	1	0	-86 dB
1	1	1	0	1	0	1	0	-87 dB
0	0	0	1	1	0	1	0	-88 dB
1	0	0	1	1	0	1	0	-89 dB
0	1	0	1	1	0	1	0	-90 dB
1	1	0	1	1	0	1	0	-91 dB
0	0	1	1	1	0	1	0	-92 dB
1	0	1	1	1	0	1	0	-93 dB
0	1	1	1	1	0	1	0	-94 dB
1	1	1	1	1	0	1	0	-95 dB
1	1	1	1	1	1	1	0	-∞

Zero cross control

D48	SBW setting	Operation
D49	RR setting	
D50	RL setting	
D51	C setting	
D52	FRIN setting	
D53	FLIN setting	
0	Zero cross operation	
1	Zero cross operation is disabled (This setting takes effect on the fall of CE.)	

Tone Switch Selection

D54	D55	Setting
0	0	The analog switches are set so that FL and FR bypass the tone circuit.
1	0	The analog switches are set so that FL is connected to, and FR bypass the tone circuit.
0	1	The analog switches are set so that FR is connected to, and FL bypass the tone circuit.
1	1	The analog switches are set so that FL and FR are connected to the tone circuit.

Bass

D56	D57	D58	D59	FLTON setting FRTON setting
0	1	1	0	+12 dB
1	0	1	0	+10 dB
0	0	1	0	+8 dB
1	1	0	0	+6 dB
0	1	0	0	+4 dB
1	0	0	0	+2 dB
0	0	0	0	0 dB
1	0	0	1	-2 dB
0	1	0	1	-4 dB
1	1	0	1	-6 dB
0	0	1	1	-8 dB
1	0	1	1	-10 dB
0	1	1	1	-12 dB

Treble

D60	D61	D62	D63	FLTON setting FRTON setting
0	1	1	0	+12 dB
1	0	1	0	+10 dB
0	0	1	0	+8 dB
1	1	0	0	+6 dB
0	1	0	0	+4 dB
1	0	0	0	+2 dB
0	0	0	0	0 dB
1	0	0	1	-2 dB
0	1	0	1	-4 dB
1	1	0	1	-6 dB
0	0	1	1	-8 dB
1	0	1	1	-10 dB
0	1	1	1	-12 dB

Tone Mode

D64	D65	Setting
0	0	FLTON and FRTON not changed
1	0	Only FLTON changed
0	1	Only FRTON changed
1	1	Both FLTON and FRTON changed

Output Ports

	Setting
D66	OUTP1 (VSS: 1, OPEN: 0)
D67	OUTP2 (VSS: 1, OPEN: 0)
D68	OUTP3 (VSS: 1, OPEN: 0)
D69	OUTP4 (VSS: 1, OPEN: 0)

Test Mode

D70	D71	Setting
0	0	These bits are used for IC testing. They must be set to 0 during normal operation.



Pin Functions

Pin No.	Pin	Function	Notes
7 24 20 18 22 16	FLIN FRIN RL RR C SBW	<ul style="list-style-type: none"> <li>Volume control inputs</li> </ul>	
9 10 11 12 13 14	FLOUT FROUT COUT RLOUT RROUT SBWOUT	<ul style="list-style-type: none"> <li>Volume control outputs</li> </ul>	<p>FLOUT FROUT RLOUT RROUT COUT SBWOUT</p>
28 26	FL FR	<ul style="list-style-type: none"> <li>Selector volume inputs</li> </ul>	<p>From TONE</p> <p>FL RL</p> <p>VDD VREF</p> <p>SELL SELR</p>
6 25	SELL SELR	<ul style="list-style-type: none"> <li>Selector volume outputs</li> </ul>	
36	TIM	<ul style="list-style-type: none"> <li>Zero cross circuit timer</li> </ul> <p>If a zero cross is not detected during the period from the completion of the data transfer to the point the timer overflows, the control data is enabled forcibly.</p>	<p>VDD</p>
23	VREF	<ul style="list-style-type: none"> <li>0.5 × V<sub>DD</sub> voltage generator used for analog ground</li> </ul> <p>A capacitor of several ten μF must be connected between VREF and V<sub>SS</sub> to minimize power supply ripple.</p>	<p>VDD</p> <p>VREF</p>
41	V <sub>SS</sub>	<ul style="list-style-type: none"> <li>Ground</li> </ul>	
37	V <sub>DD</sub>	<ul style="list-style-type: none"> <li>Power supply</li> </ul>	
40	CE	<ul style="list-style-type: none"> <li>Chip enable</li> </ul> <p>Data is written to the internal latch when this pin goes from high to low. The analog switches operate at that time. Data transfer is enabled when CE is high.</p>	<p>VDD</p>
39 38	DI CL	<ul style="list-style-type: none"> <li>Serial data and clock inputs for the control data.</li> </ul>	<p>VDD</p>

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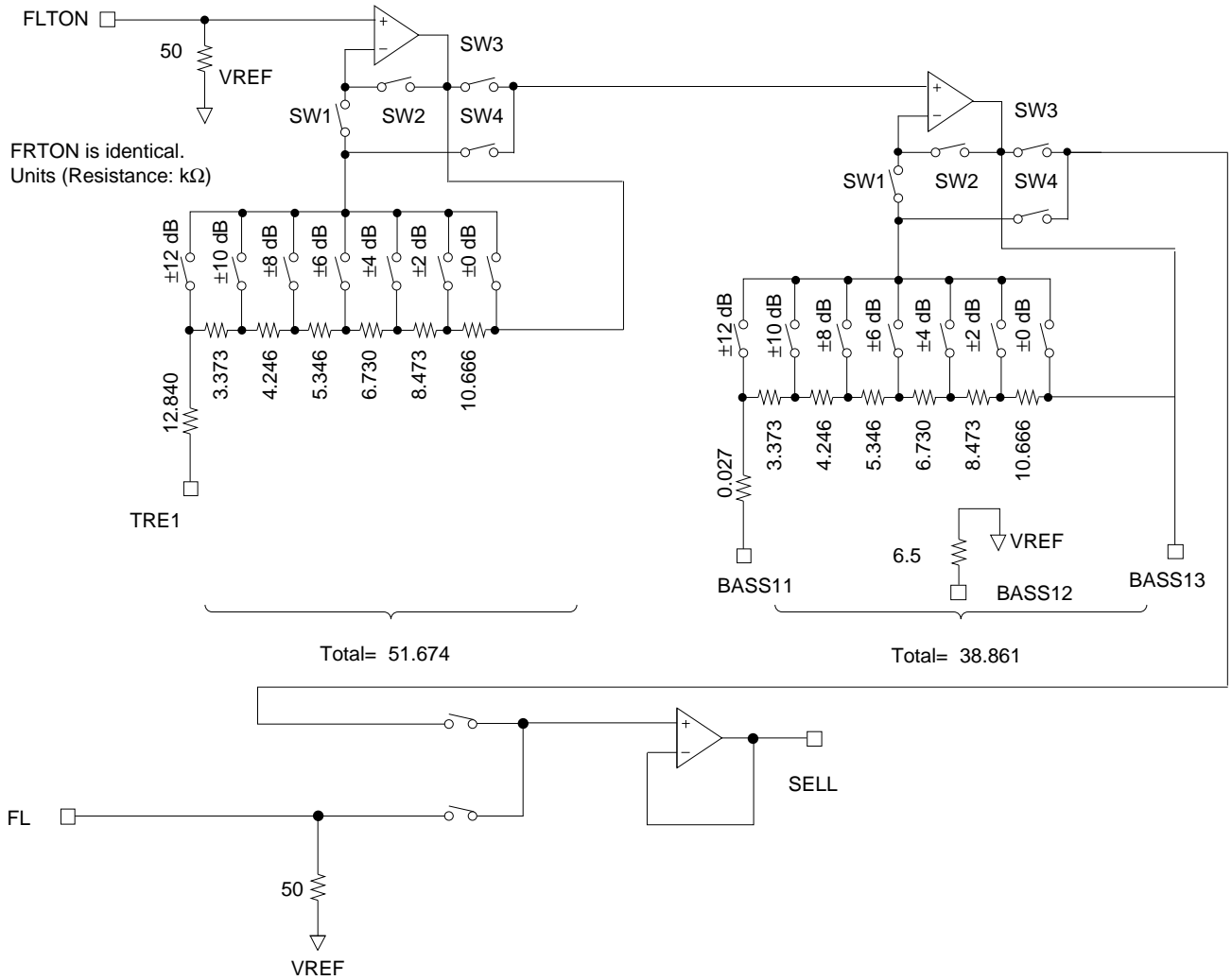
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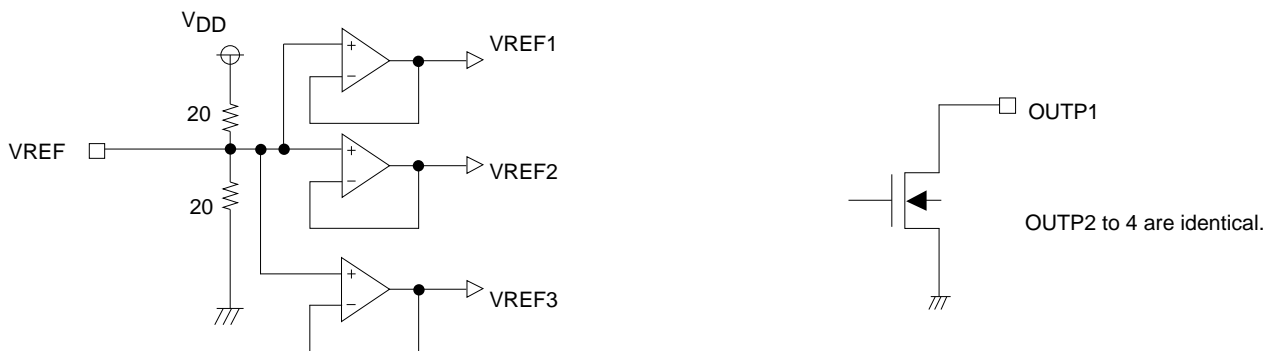
Pin No.	Pin	Function	Notes
35	MUTE	<ul style="list-style-type: none"> <li>External control mute pin</li> </ul> <p>Applying the <math>V_{SS}</math> level to this pin forcibly sets the volume level for all channels to <math>-\infty</math>.</p>	
34 33	FLTON FRTON	<ul style="list-style-type: none"> <li>Tone control block inputs</li> </ul> <p>After passing through the tone control circuit, the audio signals are output to the selector amplifier.</p>	
3 5 31 29	BASS11 BASS13 BASS21 BASS23	<ul style="list-style-type: none"> <li>Connections for the capacitors that form the bass filters</li> </ul>	
4 30	BASS12 BASS22	<ul style="list-style-type: none"> <li>Connections for the resistors that form the bass filters</li> </ul>	
2 32	TRE1 TRE2	<ul style="list-style-type: none"> <li>Connections for the capacitors that form the treble filters</li> </ul>	
1 44 43 42	OUTP1 OUTP2 OUTP3 OUTP4	<ul style="list-style-type: none"> <li>N-channel transistor open-drain outputs</li> </ul> <p>When off, these outputs are in the high-impedance state.</p>	<p>OUTP1 OUTP2 OUTP3 OUTP4</p>
8 15 17 19 21 27	NC	<ul style="list-style-type: none"> <li>Unused pins</li> </ul> <p>These pins must either be left open or connected to <math>V_{SS}</math>.</p>	

**Internal Equivalent Circuits**

- Selector, Bass/Treble, VREF Amplifier, Output Ports



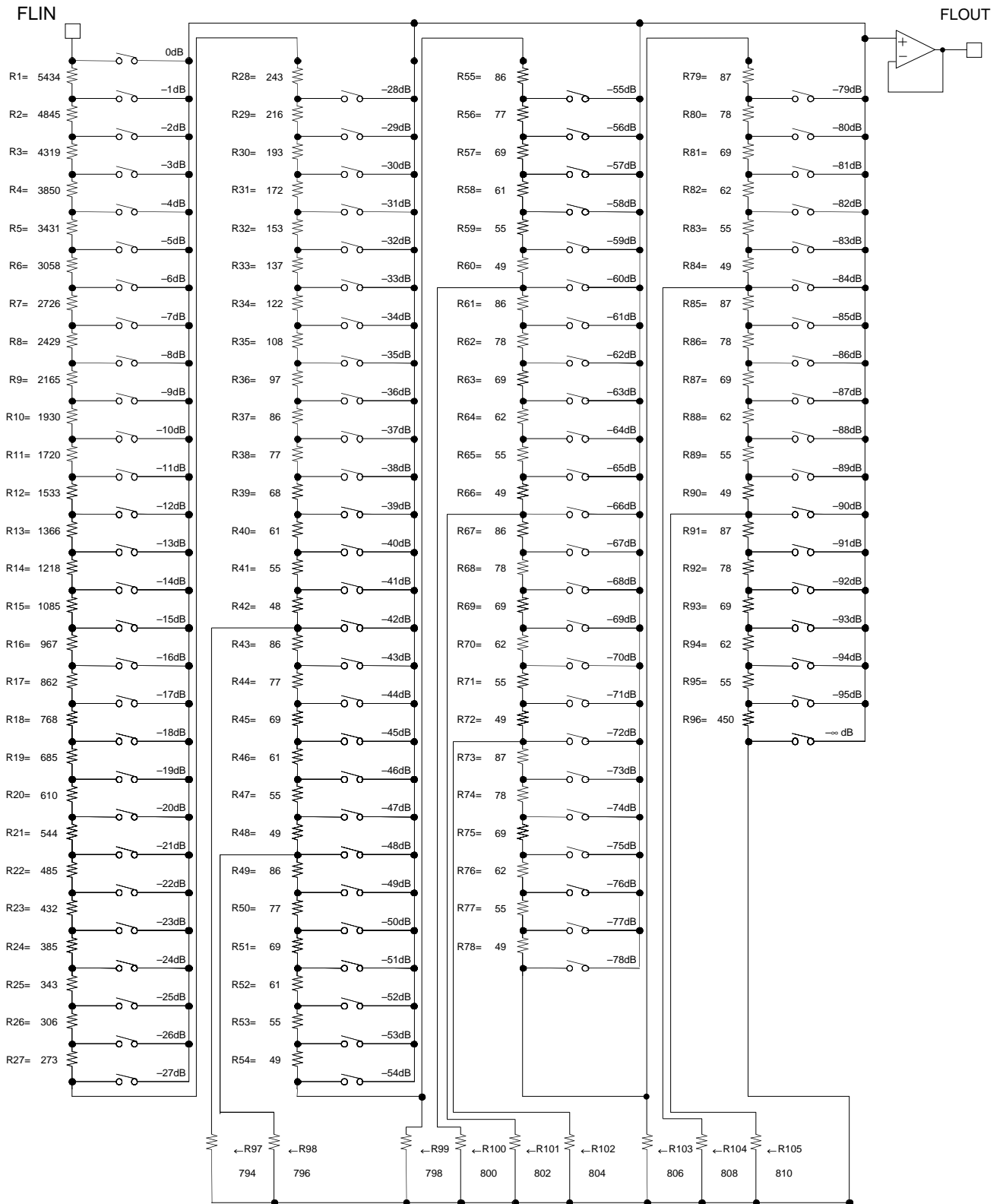
For boost, set switches 1 and 3 to the on position, for cut, set switches 2 and 4 to the on position, and for 0 dB, set switches 2, 3 and 0 dB switch to the on position.



# LC75347E

- Volume Block

Total resistance: 50 k $\Omega$  (Parallel resistors)



Resistor units:  $\Omega$   
 FRIN, RL, RR, C and SBW are identical.

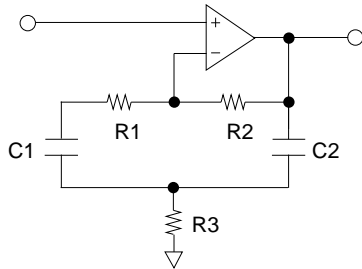
VREF

### Calculating the Equalizer External Component Values

#### 1. Bass Band Circuit

Here we show the equivalent circuit and the formulas for calculating the capacitor and resistor values for a center frequency of 100 Hz.

##### • Bass band equivalent circuit



##### • Sample calculation

Specifications: Center frequency,  $f_0 = 100$  Hz

Gain at maximum boost:  $G = 12$  dB

Assume  $R1 = 27 \Omega$ ,  $R2 = 38,834 \Omega$ , and  $C1 = C2 = C$ .

(1) Determine  $R3$  from the fact that  $G = 12$  dB.

$$G_{+12\text{dB}} = 20 \times \text{LOG}_{10} \left( 1 + \frac{R2}{2R3 + R1} \right)$$

$$R3 = \frac{\left| \frac{R2}{(10^{G/20} - 1)} - R1 \right|}{2} = \frac{\frac{38834}{(3.981 - 1)} - 27}{2} \approx 6500 \Omega$$

(2) Determine  $C$  from the fact that the center frequency,  $f_0$ , is 100 Hz.

$$f_0 = \frac{1}{2\pi \sqrt{(R1 + R2) R3 C1 C2}}$$

$$C = \frac{1}{2\pi f_0 \sqrt{(R1 + R2) R3}} = \frac{1}{2\pi \times 100 \sqrt{(38834 + 27) \times 6500}} \approx 0.1 \mu\text{F}$$

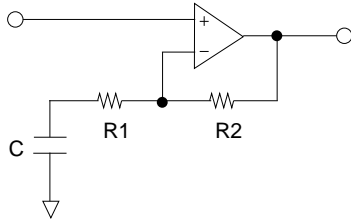
(3) Determine  $Q$ .

$$Q = \frac{(R1 + R2) R3}{2R3 + R1} \cdot \frac{1}{\sqrt{(R1 + R2) R3}} \approx 1.22$$

## 2. Treble Band Circuit

The treble band circuit can provide shelving characteristics. Here we present the equivalent circuit when the circuit is providing boost and the circuit calculation formulas.

- Treble band equivalent circuit



- Sample calculation

Specifications: Set frequency,  $f = 26,000$  Hz

Gain at maximum boost:  $G_{+12\text{ dB}} = 12$  dB

Assume  $R1 = 12,840 \Omega$  and  $R2 = 38,834 \Omega$ .

Substituting the above values into the following formulas allows us to solve for C.

$$G = 20 \times \text{LOG}_{10} \left( 1 + \frac{R2}{\sqrt{R1^2 + (1/\omega C)^2}} \right)$$

$$C = \frac{1}{2\pi f \sqrt{\left( \frac{R2}{10^{G/20} - 1} \right)^2 - R1^2}}$$

$$= \frac{1}{2\pi 26000 \sqrt{\left( \frac{38834}{3.98 - 1} \right)^2 - 12840^2}} \neq 2700 \text{ (pF)}$$

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## Usage Notes

### 1. Data Transmission after Power is First Applied

The states of the internal analog switches are undefined when power is first applied. Applications should set up the initial data immediately after power is applied (after  $V_{DD}$  rises above 4.5 V). Applications should also mute the outputs until the data has been set up and the outputs are stable.

To establish the states of the internal latches, set the bits D64 and D65 to 1 in the first data transferred after power is first applied.

### 2. Zero Cross Switching Control

Zero cross switching is used by setting up data in which the zero cross control bits specify zero cross detection mode (by setting bits D48 to D53 to 0) and transfer that data. Since these control bits are latched first, immediately after the data is transferred, that is, on the fall of the CE signal, zero cross control can be performed with a single data transfer operation when updating the volume control settings. If the zero cross control bits specify zero cross detection disabled mode (by setting bits D48 to D53 to 1), the volume is switched on the fall of the CE signal at the end of the data transfer.

### 3. Zero Cross Timer Setting

When the input signal is less than the detection sensitivity of the zero cross comparator, or if only a low-frequency signal is being input, the state where the IC does not detect a zero cross will continue and the data will not be latched. The zero cross timer allows applications to set a time at which data will be latched forcibly if the state where no zero cross is detected continues.

For example, to set a time of 25 ms:

$$T = 0.69CR$$

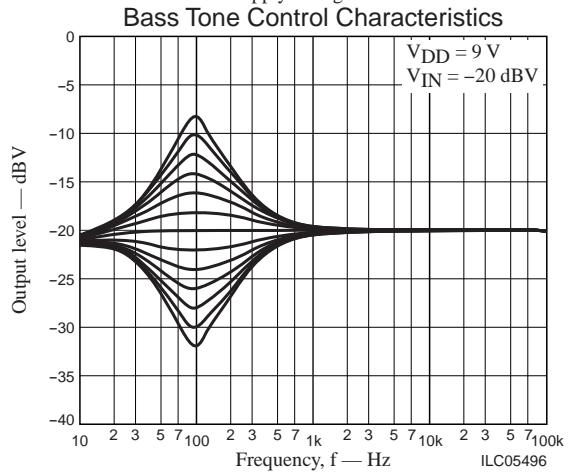
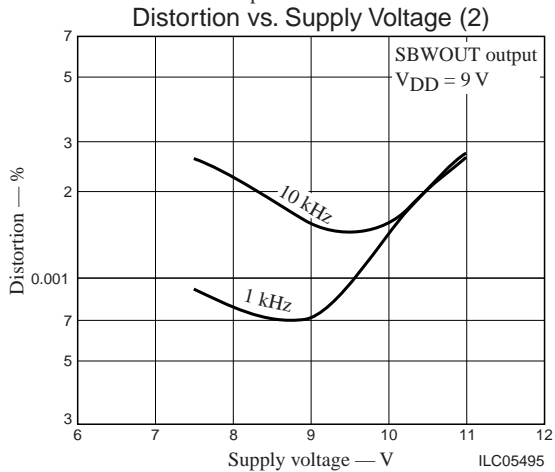
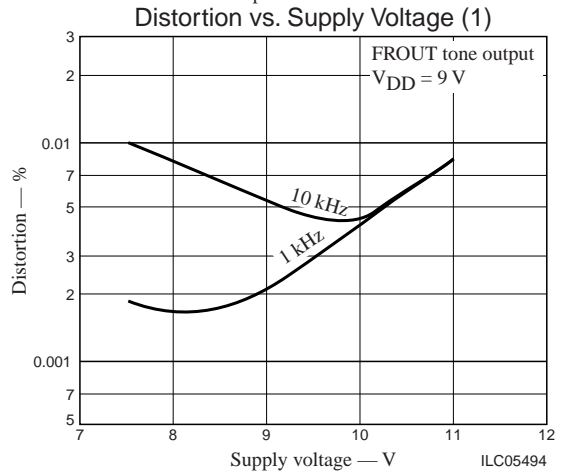
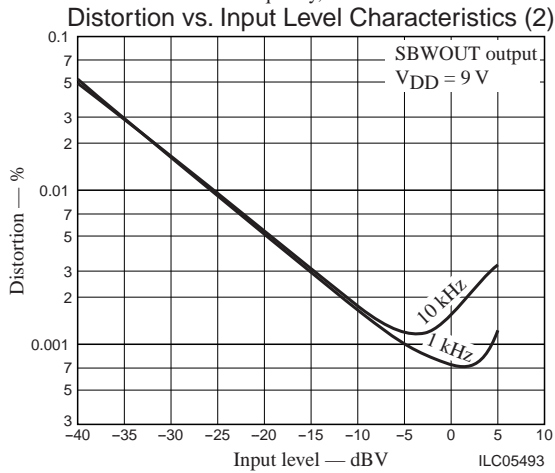
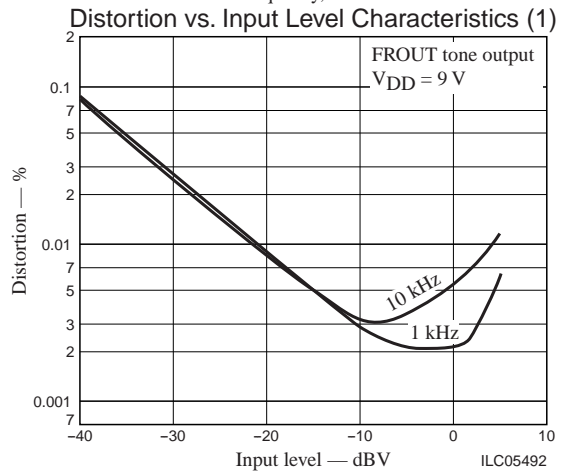
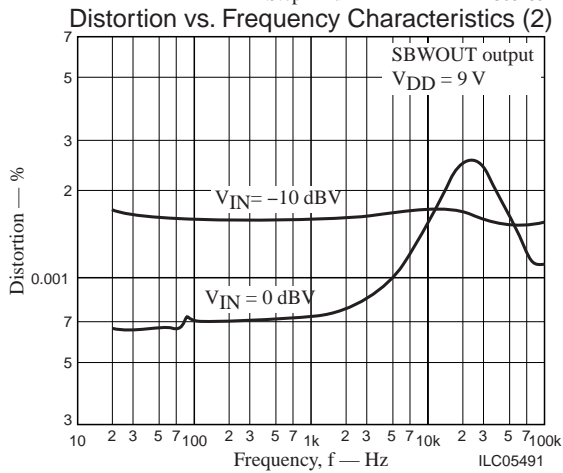
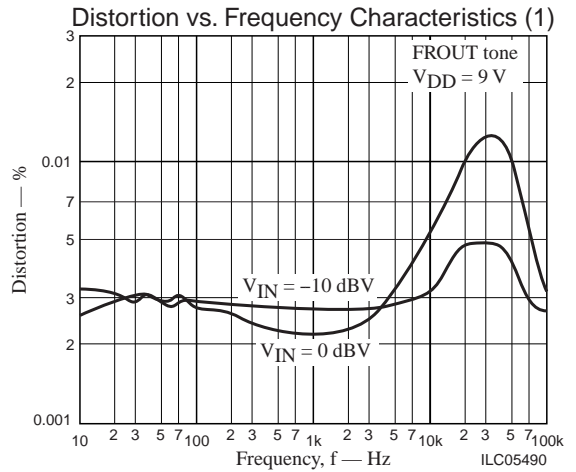
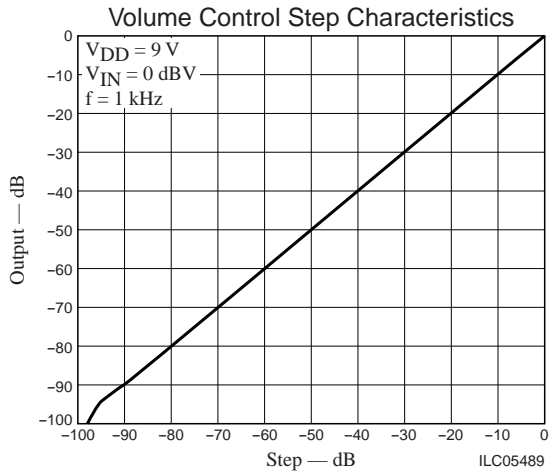
Since the internal pull-up resistor is about 1 M $\Omega$ :

$$C = \frac{25 \times 10^{-3}}{0.69 \times 1.0 \times 10^6} \doteq 0.036 \mu\text{F}$$

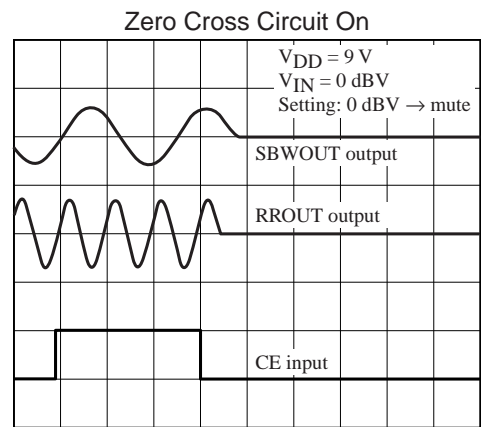
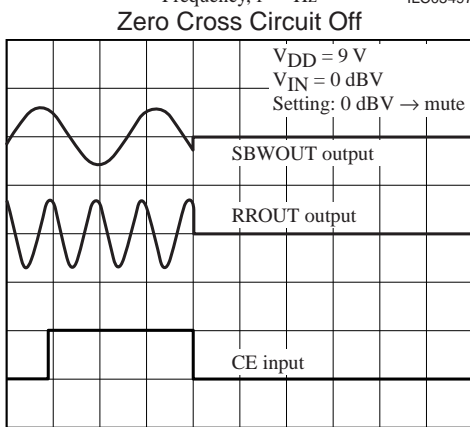
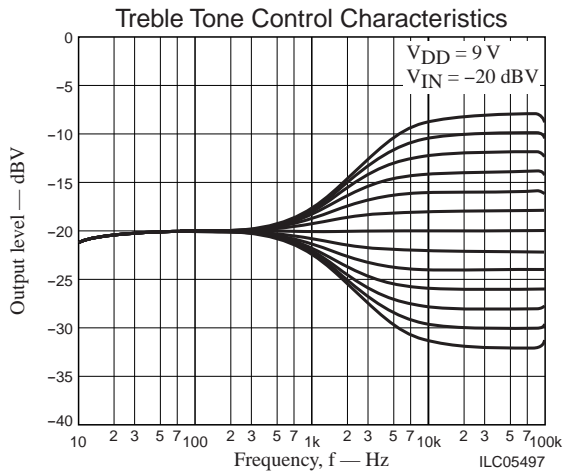
Applications usually set a time in the range 10 to 50 ms.

### 4. Notes on Serial Data Transfer

Cover the CL, DI, and CE pin signal lines with the ground pattern, or use shielded cables for these signals so that the high-frequency digital signals transmitted on these lines do not enter the analog signal system.







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