7.2 Timing recovery

7.2.1 Timing control

The loop is parametrized by two coefficients: ALPHA_TMG and BETA_TMG (register RTC at 0x11). ALPHA_TMG can take values from 0 to 8, and BETA_TMG from 0 to 12. When the parameter is 0, the coefficient value is zero.

The symbol frequency registers (MSB, middle bits and LSB) are at addresses 0x28 (SFRH), 0x29 (SFRM) and 0x2A (SFRL). These must be programmed with the expected symbol frequency. The units are:

$$F_{M\_CLK} / 2^{20}$$

The value of the timing frequency register RTFM and RTFL (at 0x22 and 0x23), when the system is locked, is an image of the frequency offset. The unit is $F_S/2^{19}$ (about 2 ppm). It should be as close as possible to 0 (by adjusting symbol frequency register value) in order to have a symmetrical capture range. Reading RTFM and RTFL allows optimal trimming of the timing range.

The actual symbol frequency is:

$$F_S = \frac{F_{M\_CLK}}{2^{20}}\left[F_{S\_REG}\left(1 + T_{MG\_REG}\frac{F_{S\_REG}}{2^{19}}\right)\right]$$

where F_{S_REG} is the content of the symbol frequency register and T_{MG_REG} the content of the timing frequency registers (RTFM and RTFL).

7.2.2 Loop equation

The timing loop may be considered as a second order loop. The natural frequency and the damping factor may be calculated using the following formula:

$F_N = 1.849 \times 10^{-6} \times F_S \sqrt{(m2 \times \beta)}$

where, F_S is the symbol frequency, m2 is the AGC2 reference level and β is programmed by the timing register:

$\beta = 2^{BETA\_TMG}$

The damping factor is:

$\xi = \{47.6 \times 10^{-3} \times \sqrt{m2} \times 2^{ALPHA\_TMG}\} / \sqrt{2}^{BETA\_TMG}$

Table 4 shows the natural frequency in DVB, with nominal reference level m2 = 72, for different values of BETA_TMG and ALPHA_TMG, without noise.

Table 4: Natural frequency for different values of BETA_TMG and ALPHA_TMG

	ALPHA_TMG	1	2	3	4	5
BETA_TMG	Natural frequency for F_S = 20 Msymbols/s	Damping factor				
0001	0.32kHz	0.57	1.14	2.28	4.57	9.14
0010	0.44kHz	0.4	0.81	1.62	3.23	6.46
0011	0.54kHz	0.29	0.57	1.14	2.28	4.57
0100	0.63 kHz	0.2	0.4	0.81	1.62	3.23
0101	0.70 kHz	0.14	0.29	0.57	1.14	2.28
0110	0.77kHz	0.1	0.2	0.4	0.81	1.62
0111	0.89 kHz	0.07	0.14	0.29	0.57	1.14
1000	0.94 kHz	0.04	0.1	0.2	0.4	0.81

Table 4: Natural frequency for different values of BETA_TMG and ALPHA_TMG

	ALPHA_TMG	1	2	3	4	5
BETA_TMG	Natural frequency for F_S = 20 Msymbols/s	Damping factor				
1001	0.99 kHz	0.03	0.07	0.14	0.29	0.57
1010	1.04 kHz	0.02	0.05	0.1	0.2	0.4

7.2.3 Timing lock indicator

The timing lock indicator reports a value dependent upon the signal-to-noise ratio and on the signal lock state.The timing lock registers are STEP1 and STEP2 (step increment for indicator 1 and 2), TLIRM,TLIRL (timing lock indicator and final indicator), TH1, TH2 and THH (indicator 1, 2 and hysteresis thresholds) and IND1MAX (second level threshold apply on indicator 1).

The timing lock indicator is a function of the lock condition, but also of the current signal to noise ratio. The timing lock parameters must be programmed as a function of the AGC2 reference level m2 (rounded to the closest value):

- TH1=2.15*m2,
- TH2=7.45*m2,
- IND1MAX=0.4*m2.

When the timing is locked, the indicator is positive; otherwise it is negative. The value needs 10 to 20 Ksymbols to stabilize.

In order to avoid wrong information, some hysteresis is provided by register THH:

- lock flag is set if timing lock indicator goes above THH,
- lock flag is reset if timing lock indicator goes under -THH.

Recommended value is THH=8.

7.3 Carrier recovery and derotator loop

The tracking range of the derotator is $\pm F_{M\_CLK}/2$ ($\pm F_{SAMPLING}/2$). The initial frequency search may therefore be performed on several MHz ranges without reprogramming the tuner.

Three phase detectors are selectable using software as follows:

- phase detector algorithm 0: this algorithm should only be used for BPSK reception,
- phase detector algorithm 1: this algorithm is used with QPSK reception, over a small range of capture phases and with a channel noise value over 4.5 dB,
- phase detector algorithm 2: for QPSK reception, it is used after locking, to minimize the bit error rate in low channel noise conditions. Algorithm 2 is recommended for most applications.

The loop is controlled through α and β parameters.

The carrier loop control registers are at addresses 0x16 (ACLC alpha carrier), 0x17 (BCLC beta carrier), 0x2B and 0x2C (CFRM and CFRL respectively, MSB and LSB carrier frequency).

7.3.1 Loop parameters

As for the timing loop, the carrier loop is a 2nd-order system where two parameters, α and β, may be programmed with ALPHA and BETA respectively. In QPSK, the natural frequency (F_N) is:

$$F_N = 2.485 \times 10^{-6} \times F_{M\_CLK} \sqrt{\{(m2 \times \beta) \times (F_S / F_{M\_CLK})\}}$$

The damping factor is:

$$\xi = 7.807 \times 10^{-6} \times \alpha \sqrt{\{(m2 / \beta) \times (F_S / F_{M\_CLK})\}}$$

where $\alpha = (2 + a) \times 2^{11+alpha}$, with $1 \geq a \geq 0$, and $\beta = (4 + c + d) \times 2^{beta-1}$, with $1 \geq d \geq 0$ and $1 \geq c \geq 0$. m2 is the reference level in register AGC2COEFF.

7.3.2 Carrier lock detector

The carrier lock detector provides an indicator with a high value when the carrier is locked, dependent on the channel noise. When the carrier is not locked, the indicator value is low.

The indicator value is compared to two programmable 8-bit thresholds: LOCK_THRESHOLD (LDT) and LOCK_THRESHOLD2 (LDT2), with LOCK_THRESHOLD2 ≤ LOCK_THRESHOLD, to give some hysteresis to the system. The result of this comparison (1 if greater than LOCK_THRESHOLD, 0 if less than LOCK_THRESHOLD2) is written as the carrier found flag (CF) and may be read in VSTATUS.

The lock detector threshold registers LDT and LDT2, and the lock detector value register LDI are addresses 0x19, 0x1A and 0x25 respectively.

7.3.3 Derotator frequency

The derotator frequency can be either measured (read operation) or forced (write operation).

$$(freq)_{kHz} = (Derot\_freq / 2^{16}) \times (F_{M\_CLK}) \text{ kHz}$$

The derotator frequency is a 16-bit signed value in registers are CFRM (MSB at 0x2B) and CFRL (LSB at 0x2C).

7.3.4 Carrier frequency offset detector

The carrier recovery loop features a carrier frequency offset detector and two phase detectors. When the carrier frequency offset detector is enabled, the central loop frequency is modified proportionally to the carrier offset. The gain and time constants of the detector are set by register CFD bits BETA_FC and FDCT respectively. When the carrier loop is about to phase lock with the carrier, the frequency detector stops automatically, and the phase lock is ensured by the selected phase detector. This switchover point is determined by the threshold (CFD).

For stability reasons, the gain BETA_FC should not exceed the coefficient e of BCLC[5:2].

The carrier frequency offset detector register CFD is at address 0x15.

7.3.5 I, Q symbol monitoring and bypass

The IQ symbol values presented to the FEC can be read out through registers ISYMB and QSYMB. This allows a symbol diagram of the IQ symbols entering the FEC to be displayed during debug.

Symbol information can be routed directly to the FEC from various points in the demodulator. See SYMBCTRL register. These are:

- directly from the input (input samples),
- after derotation and before Nyquist filter,
- after Nyquist filter,
- after all demodulator stages (normal operation).

7.4 Noise indicator

The noise indicator may be used to facilitate antenna pointing or to give an idea about RF signal quality and about the front-end installation (dish, LNB, cable, tuner or ADC).

A simple C/N estimator can be easily implemented by comparing the current indications with a primarily-recorded look-up table.

The time constant ranges from 4 K to 256 K symbols as described in register ACLC (0x16). The 16 MSB of the result may be read by the microprocessor in NIRM (0x2D) and NIRL (0x2E).

7.5 Forward error correction

7.5.1 FEC modes

As the STV0288 is a multistandard decoder, several combinations are possible at different levels:

- The demodulator can accept either QPSK or BPSK signals: the only impact is on the carrier algorithm choice. The algorithm choice also affects the carrier lock detector and the noise evaluation.
- There are two primary options concerning FEC operation, between DVB, DIRECTV system and reserved mode.
- There are two options concerning FEC feeding. The first is IQ flow, which is the usual case in QPSK modes DVB or DIRECTV system. The second mode is I-only flow, used for BPSK.

The FEC mode register FECM is at address 0x30.

In DVB and DIRECTV system modes, data is fed to the Viterbi decoder. Other parts of the decoding may be bypassed.

7.5.2 Viterbi decoder and synchronization

The convolutive codes are generated by the polynomial G_X = 171 octets and G_Y = 133 octets in modes DVB or DIRECTV system.

The Viterbi decoder computes the metrics of the four possible paths for each symbol, proportional to the square of the Euclidian distance between the received I and Q and the theoretical symbol value.

The puncture rate and phase are estimated on the error rate basis. Several rates are allowed and may be enabled or disabled through register programming: the rates are 1/2, 2/3, 3/4, 5/6, 6/7, 7/8 in DIRECTV system or DVB.

For each enabled rate, the current error rate is compared to a programmable threshold. If it is greater than this threshold, another phase (or another rate) is tried until the right rate is obtained.

A programmable hysteresis is added to avoid losing the phase during short term perturbation.

The rate may also be imposed by external software, and the phase is incremented only upon request by the microprocessor. The error rate may be read at any time in order to use an algorithm other than that implemented.

The Viterbi decoder produces an absolute decoding. The decoder is controlled through several Viterbi threshold registers: VTH12 (0x31), VTH23 (0x32), VTH34 (0x33), VTH56 (0x34), VTH67 (0x35) and VTH78 (0x36). For each Viterbi threshold register, bits 6 to 0 represent an error rate threshold, the average number of errors occurring during 256-bit periods.

The maximum programmable value is 127/256 (higher error rates are of no practical use).

The puncture rate register PR is at address 0x37. Sync is controlled through register FECM (0x30). The automatic rate research is only performed through the enabled rates (see the corresponding bit set in PR).

Note: In order to minimize the Viterbi search time, the puncture rates 3/4, 5/6, 7/8 must be disabled in DIRECTV system. In DVB, the puncture rate 6/7 must be disabled.

Register VSEARCH is at address 0x38. Bits AM and F program the automatic/manual (or computer aided) search mode as follows:

- If AM = 0 and F = 0, automatic mode is set. Successive enabled punctured rates are tried with all possible phases until the system is locked and the block sync is found. This is the default (reset) mode.
- If AM = 0 and F = 1, the current puncture rate is frozen. If no sync is found, the phase is incremented, but not the rate number. This mode shortens recovery time under noisy conditions. The puncture rate is not supposed to change in a given channel. In a typical computer-aided implementation, the search begins in automatic mode. The microprocessor reads the error rate (VERROR) or flag PRF (VSTATUS) to detect the capture of a signal, then it switches F to 1 until a new channel is requested by the remote control.
- If AM = 1, manual mode is set. In this case, only one puncture rate should be validated. The system is forced to this rate on the current phase, ignoring bit TO (time-out in VSEARCH) and the error rate. In this mode, each 0 to 1 transition of bit F leads to a phase incrementation, allowing full control of the operation by an external microprocessor by choosing the lowest error rate.

The reset values are AM = 0 and F = 0 (automatic search mode).

Register VERROR (read only) is at address 0x2F. The last value of the error rate may be read at any time in the register. Unlike the Viterbi threshold, the possible range is from 0 to 255/256.

Register VSTATUS (read only) is at address 0x24.

7.5.3 Error monitoring

A 16-bit counter, ERRCNT, counts errors at different levels. ERRCNT is fed by one of the following:

- the input QPSK bit errors (that are corrected by the Viterbi decoder),
- the bit,
- the byte errors (that are corrected by the Reed-Solomon decoder),
- the packet error (not correctable, leading to a pulse at the ERROR output).

The content of ERRCNT may be transferred to the read only error-count registers ECNTM (MSB at 0x26) and ECNTL (LSB at 0x27).

Two functional modes are proposed, depending on control register ERRCTRL (0x3B) bit 7:

- ERRMODE = 0: error rate measurement. This provides the number of errors occurring within a specified number of output bytes, NB. NB has four possible values defined by bits NOE. Every NB bytes, the state of the error counter is transferred to the 16-bit error-count registers, then the error counter is reset. The error-count registers may be read by the microprocessor through the I^2C bus. Two ways of reading may be used: 16-bit reading, starting with the MSB, or 8-bit reading (LSB only or MSB only).
- ERRMODE = 1: the error counter just counts the errors, and directly transfers the content of the error counter. When the MSB byte is read, the error counter is reset.

In both modes, the 16-bit counter is saturated to its maximum value.

A second error monitor is added, with an identical control register ERRCTRL2 at address 0x3D, and the contents of ERRCNT2 may be transferred to ECNTM2 (0x3E) and ECNTL2 (0x3F). With this second error monitor, two error rates may be simultaneously monitored, for example, QPSK bit error and packet error rate.

7.5.4 Convolutive de-interleaver

In DVB, the convolutive de-interleaver is 17 x 12. The periodicity of 204 bytes per sync byte is retained. In DIRECTV system, the convolutive de-interleaver is 146 x 13, and there is also a periodicity of 147 bytes per sync byte. The de-interleaver may be bypassed.

7.5.5 Reed-Solomon decoder and descrambler

The input blocks are 204 byte long with 16 parity bytes in DVB. The sync byte is the first byte of the block. Up to 8 byte errors may be fixed.

The code generator polynomial is:

$$g(x) = (x - \omega^0)(x - \omega^1)...(x - \omega^{15})$$

over the Galois Field generated by:

$$x^8 + x^4 + x^3 + x^2 + 1 = 0$$

Energy dispersal descrambler and output energy dispersal descrambler generator:

$$x^{15} + x^{14} + 1$$

The polynomial is initialized every eight blocks with the sequence 100 1010 1000 0000.

The sync words are unscrambled and the scrambler is reset every 8 packets.

7.5.6 Synchronization

In DVB, the packet length after inner decoding is 204. The sync word is the first byte of each packet. Its value is 0x47, but this value is complemented every 8 packets. In DIRECTV system, the packet length is 147 and the sync word is 0x1D.

An up/down sync counter counts whenever a sync word is recognized with the correct timing, and counts down during each missing sync word. This counter is bounded by a programmable maximum. When this value is reached, bit LK (locked) is set in register VSTATUS. When the event counter counts down to 0, this flag is reset.

8 Output interface

In both parallel and serial modes, the clock polarity is selected with bit CLK_POL in RS register. When CLK_POL is 0, the output signals are valid during the rising edge of signal CLK_OUT (falling edge if CLK_POL is 1).The ERROR flag is set during the duration of uncorrected packets or as long as the descrambler is not synchronized in DVB standard.

D/P (data/parity signal) is low when the FEC block is not locked (LK = 0 in register VSTATUS).

8.1 Parallel output modes

The STV0288 features three different parallel output modes.

In all parallel output modes, signal STR_OUT is high during the sync word byte.

If bit CLK_CFG (in RS register) is low, the parity bytes are output (CLK_OUT operating), if CLK_CFG is 1, CLK_OUT is low during the parity field.

8.1.1 Conventional parallel output mode

See Figure 11: *Parallel output interface* on page 26. Data is output directly from the FEC block. The D/P signal is high during valid data. The D/P signal is a single pulse that never returns to low during the 188 consecutive bytes in DVB mode (130 bytes in DIRECTV mode). In this mode, the byte clock signal CLK_OUT may have a variable duty cycle ranging from 40% to 60%. This operating mode is selected when register RSOUT bits ENA8_LEVEL = 0000.

8.1.2 DVB common interface parallel output mode

See Figure 13: *Parallel mode options* on page 27. Data goes through a FIFO memory before being output, and the byte clock signal CLK_OUT features a perfect 50% duty cycle. The CLK_OUT frequency is derived from the master clock frequency according to bits ENA8_LEVEL of register RSOUT. For correct operation, the frequency of CLK_OUT must be such that $F_{CLK\_OUT} >$ (bit rate/8).

To compensate for the difference in rates, signal D/P returns to low during CLK_OUT pulses not corresponding to true data (punctured D/P signal). This operating mode is controlled by the rate compensation mode bit of register RSOUT.

8.1.3 Parallel output mode with punctured clock

See Figure 13: *Parallel mode options* on page 27. This mode is similar to the above parallel output mode and the frequency F_{CLK_OUT} of CLK_OUT is derived from the master clock frequency according to ENA8_LEVEL of register RSOUT. However, the difference in rates is compensated by puncturing of CLK_OUT, and D/P is not punctured. This operating mode is controlled by bit EN_STBACKEND of register RSOUT.

8.2 Serial output modes

The STV0288 features three different serial output modes. The data is output at pin 28 (DATA_7/ SERIAL_DAT), and the MSB comes first. Outputs DATA_0 to DATA_6 are automatically set in high impedance. The bit clock is output at pin CLK_OUT. The bit clock runs continuously even during the parity field, whatever the value of bit CLK_CFG. STR_OUT is high during the first bit of the packet payload. ERROR has the same function as in parallel output mode.

8.2.1 Conventional serial output mode

See Figure 12: *Serial output interface on page 27*. The data is directly output from the FEC block, and CLK_OUT is directly derived from the master clock. To compensate for the difference in rates, the master-clock signal is punctured. Note that in this mode, the maximum instantaneous CLK_OUT signal might be F_{M_CLK} (for example, 120 MHz), and must exceed 2 x F_S x PR_{max}.

The D/P (data parity) signal is a single pulse that never returns to low during the 188 consecutive bytes in DVB (130 bytes in the DIRECTV mode).

This operating mode is selected when register RSOUT bits ENA8_LEVEL = 0000.

8.2.2 Serial output mode (S1) with reduced CLK_OUT frequency

See Figure 14: *Serial mode options on page 27*. The data goes through a FIFO memory before being output. The bit clock signal has a stable frequency that is derived from the master clock frequency according to the truth table of register RSOUT bits ENA8_LEVEL. For correct operation, the frequency of CLK_OUT must be such that: $F_{CLK-OUT}$ > bit rate.

To compensate for the difference in rates, D/P signal returns to low during CLK_OUT pulses not corresponding to true data (punctured D/P signal).

8.2.3 Serial output mode (S2) with reduced CLK_OUT frequency

See Figure 14: *Serial mode options on page 27*. This mode is similar to mode S1, but the difference in rates is compensated by puncturing the CLK_OUT signal The instantaneous bit clock frequency CLK_OUT is derived from the master clock frequency according to the truth table of register RSOUT bits ENA8_LEVEL.

Figure 11: Parallel output interface

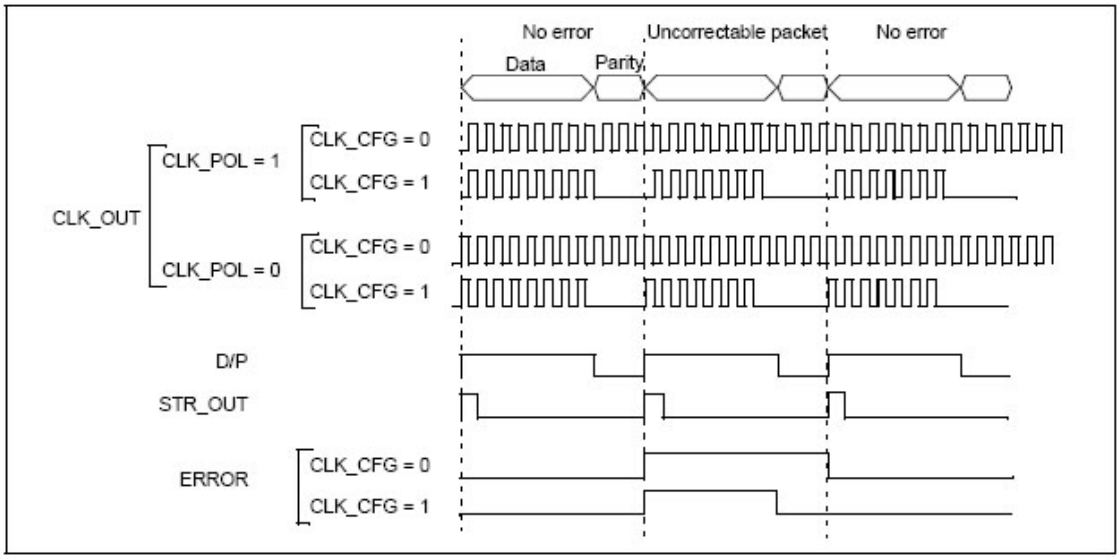


Figure 12: Serial output interface

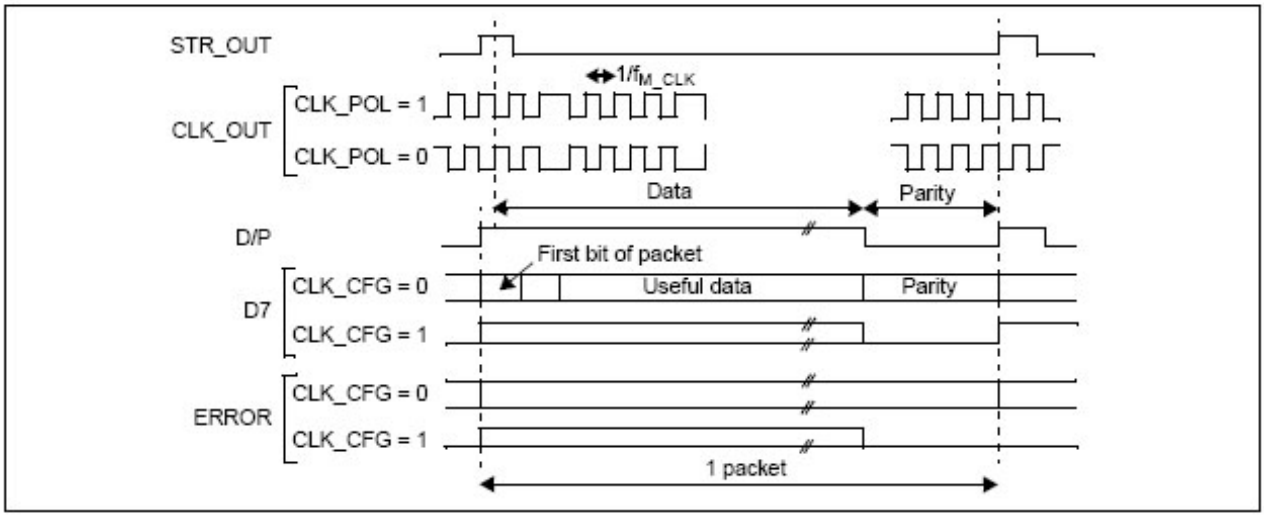


Figure 13: Parallel mode options

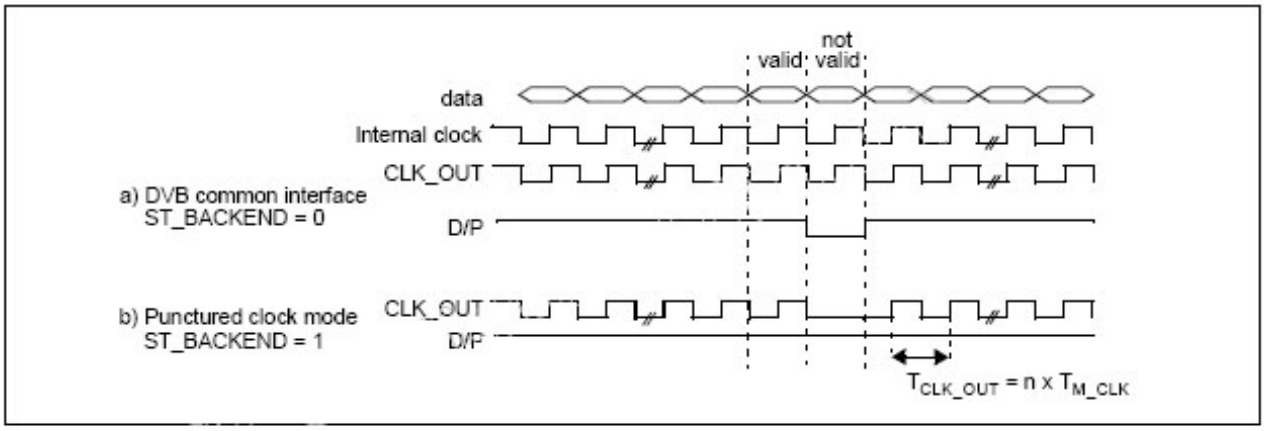
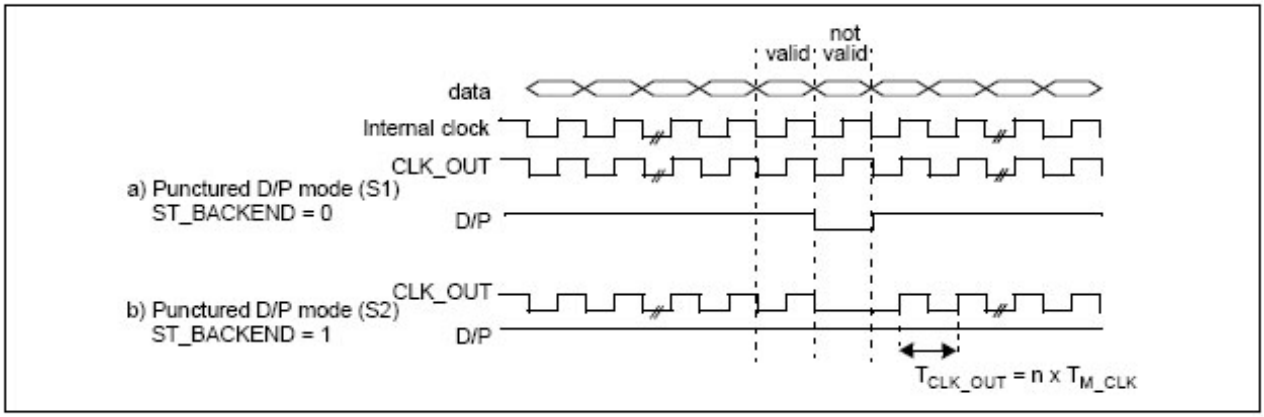


Figure 14: Serial mode options

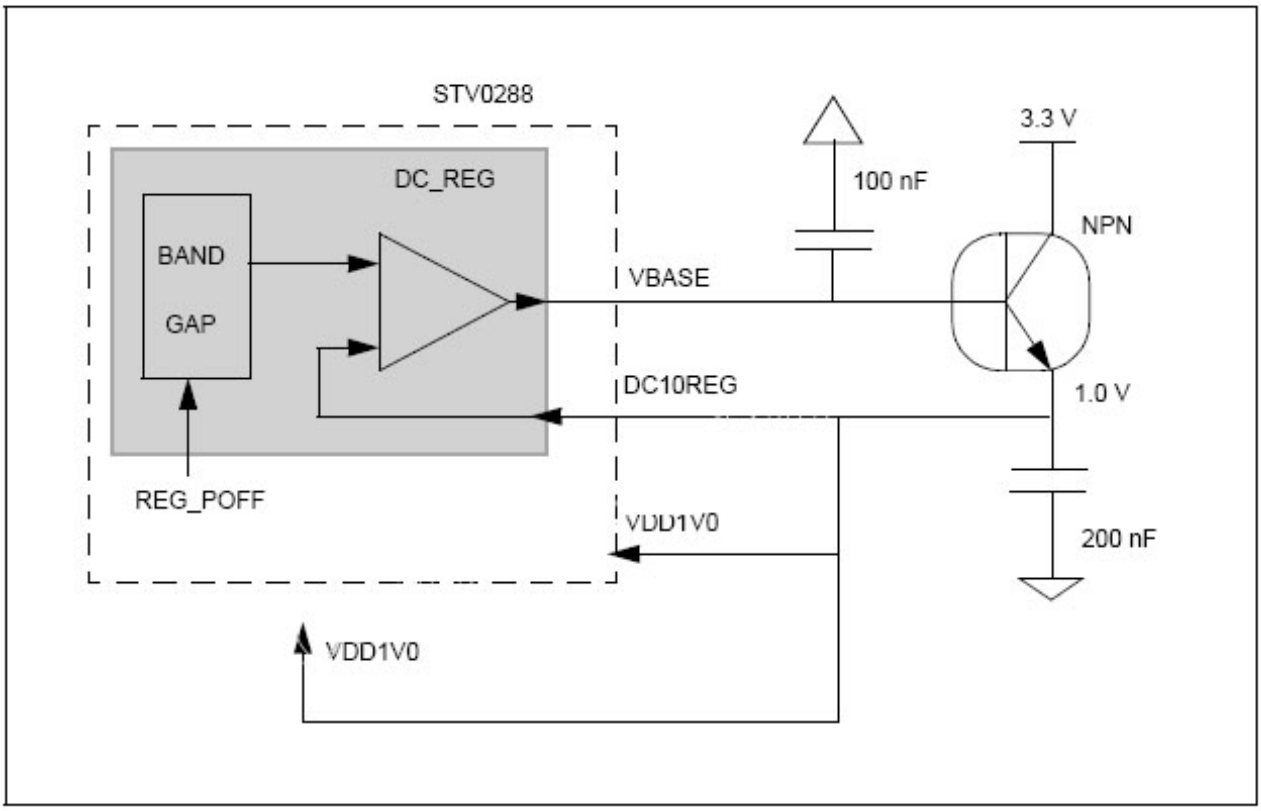


9 DC regulator

To reduce the BOM, the STV0288 integrates a DC regulator. The regulator consists of band gap and amplification stages, associated with a standard external transistor and two external capacitors. This regulator removes the need for a dedicated 1.0 V DC power supply.

If DC_REG is not used, set the bit REG_POFF in TSTNTR1 register to 1 and connect the DC10REG pin to VDD1V0

Figure 15: DC regulator



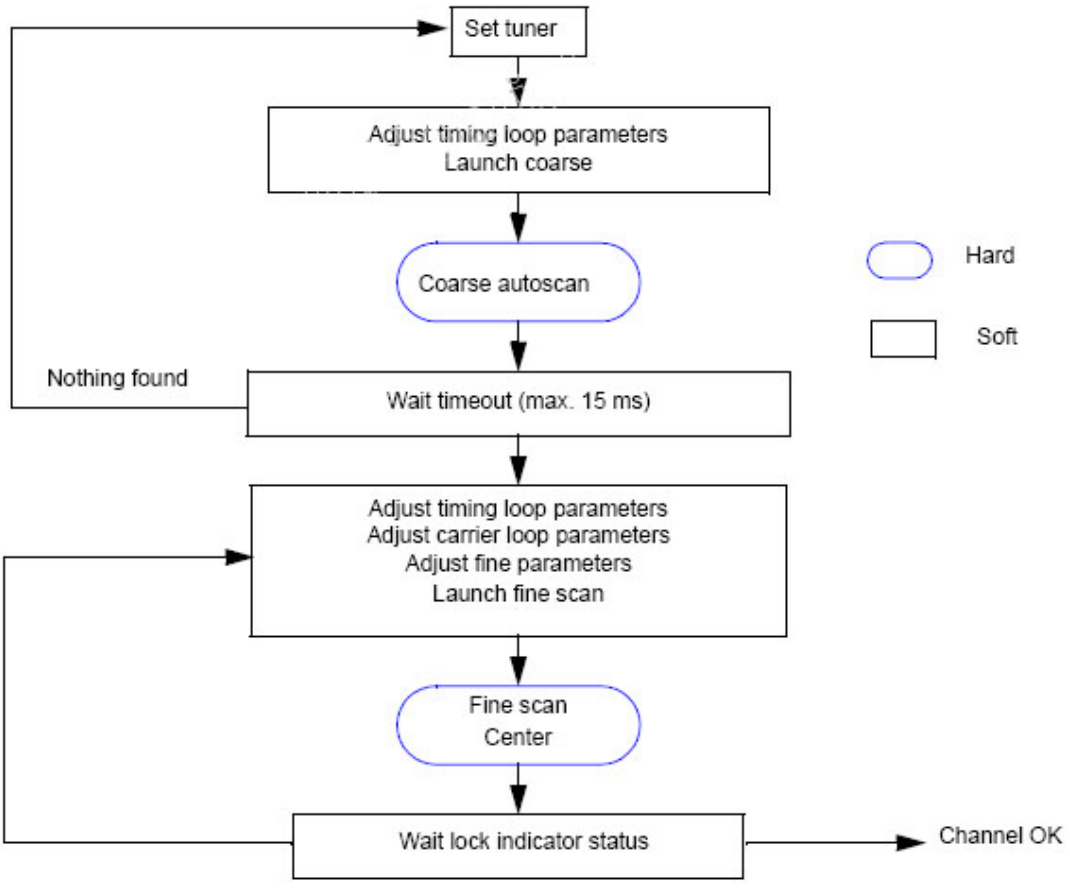
10 Fast channel acquisition and blind search

Automatic symbol rate search, signal acquisition and signal tracking are built into the STV0288 using a simple state machine, controlled by I^2C commands. This state machine significantly reduces the required software, and also decreases the duration of the transponder acquisition. The result is simplified scanning software routines, full satellite band scanning in seconds, and fast channel acquisition.

10.1 Control

The fast channel acquisition is performed in two steps. The first step, coarse autosearch, enables the rough estimation of the QPSK carrier within a given RF bandwidth. The second step, fine scan, enables automatic lock to the previously estimated QPSK carrier. The timing lock indicator indicates success. See Figure 16.

Figure 16: Example channel scan algorithm



10.1.1 First step: coarse autosearch

This mode is only valid for symbol frequencies lower than half the ADC frequency. The IC is set in this mode by I^2C bit COARSE in the ASCTRL register.

In this mode, the symbol frequency registers (SFRH, SFRM and SFRL) and carrier frequency registers (CFRM and CFRL) are updated by a loop in order to reach the approximate input baud rate and carrier position.

The coarse carrier frequency loop is controlled by the KC field in the COARP2 register as follows:

- KC=0: the carrier frequency is frozen,
- KC= 1 to 4: the loop is active; the value KC=4 gives the minimum time constant to recover any carrier frequency up to +/- to Fadc/2.

Decreasing KC by one unit doubles the time constant, and halves the variance on the carrier frequency.

The coarse baud rate loop is controlled by the KS field in the COARP2 register as follows:

- KS=0: the symbol frequency is frozen,
- KS= 1 to 4: the loop is active; the value KS=4 gives the minimum time constant to recover any symbol frequency up to Fadc/2.

Decreasing KS by one unit doubles the time constant and decreases the variance on the symbol frequency rate.

The baud rate loop converges to a value close to the symbol frequency, depending on the signal to noise ratio, and on the roll off of the transmitter. It may be altered by changing the value of the field KT in the COARP1 register.

KI in the ASCTRL register must be set to 2.

10.1.2 Second step: fine scan

In this mode, the normal timing and carrier loops are enabled, and the symbol frequency register is incremented with a programmable value at each symbol period.

Two 16 bit registers, FMIN and FMAX, contains the 15 MSB's of the boundaries of the scanning. A mode bit (STOP_ON_FMIN, STOP_ON_FMAX), selects the system behavior when a bound is reached as follows:

- if the bit is set, the scanning stops,
- if reset, the scanning is automatically reversed with the same step.

The scanning is automatically and definitively stopped when the timing lock flag, TMG_LOCK in the TLIRM register is set.

Channel centering

After decoding a lock condition, which stops the symbol frequency scanning, the current symbol frequency is obtained by a combination of the symbol frequency register and the timing register.

When the CENTER bit is set in the ASCTRL register, and the timing lock indicator is set (see Section 7.2.3: *Timing lock indicator on page 20*), an automatic process allows pulling the timing register close to 0 by adjusting the symbol frequency register accordingly.

The adjusting speed is controlled by the scan step, and the action stops when the residual timing offset is under 61 ppm.

11 Register map

Registers marked with an asterisk (*) are addressable in standby mode. Full register descriptions are included in Chapter 12: *Registers on page 3.*

Table 5: Registers map

Name	Addr	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ID*	0X00	CHIP_IDENT				RELEASE			
12CRPT*	0x01	12CT_ON				SCLT_DELAY	SCLT_VALUE	STOP ENABLE	SDAT_VALUE
ACR	0x02	PRESCALER			DIVIDER				
F22FR	0x03	FFTX_REG							
F22RX	0x04	FFRX_REG							
Dise qc	0x05	TIM_OFF	DIS_RESET	TIM_CMD		NA	DIS_PRECHARGE	DISE qc MODE	
Dise qc FIFO	0x06	Dise qc FIFO							
Dise qc sta1	0x07	TX_FAIL	FIFO_FULL	TX_IDLE	READ_WRITE_COUNT				
Dise qc sta2	0x08	NA	NA	NA	NA	NA	NA	NA	NA
Dise qc2	0x09	RE CEIVER_ON	IGNORE_ SH22K	ONE CHIP_TRX	EXT_ENVEL	PINSELECT		IRQ_RXEND	IRQ_HALF_FIFO
DISRX_ST0	0x0A	RX_END	RX_ACTIVE	SHORT_22K	CONT_TONE	BBFIFORDY	FIFO_EMPTY	RX_NO_BYT	ABORT
DISRX_ST1	0x0B	RX_FAIL	PARITY_ FAIL	FIFO_ VOERFLOW	FIFO_BYTENBR				
TSREG*	0x0D	NA	NA	NA	NA	NA	NA	NA	NA
AGC1C	0x0E	ENA-DCADJ	AVERAGE-ON	AGC OPDRAIN	IAGC	AGCIQ_BETA			
AGC1REF	0x0F	AGC1_REF							
AGC1IN	0x10	AGC1_VALUE							
RTC	0x11	ALPHA_TMG				BETA_TMG			
AGC2COEF	0x12	NA	NA	NA	NA	NA	AGC2_COEFF		
AGC2REF	0x13	NA	AGC2_RFF						
STEP1	0x14	STEP_MINUS				STEP_PLUS			
CFD	0x15	CFD_ON	BETA_FC			FDCT		LDL	
ACLC	0x16	DEROT_ON_ OFF	ACLC_A	NOISE		ALPHA			
BCLC	0x17	ALGO		BETA					
ROLLOFF	0x18	NA	NA	NA	NA	NA	MODE_COEF	NA	NA
LDT	0x19	LOCK_THRE SHOLD							
LDT2	0x1A	LOCK_THRE SHOLD2							
DACR1*	0x1B	DAC_MODE			NA	DACI			
DACR2*	0x1C	DAC							
TLIRM	0x1E	TMG-LOCK	NA	NA	TMG_IND_MSB(128)				
TLIRL	0x1F	TMG_IND_LSB(7.0)							
AGC2IM	0x20	AGC2_INTEGRATOR_MSB							
AGC2IL	0x21	AGC2_INTEGRATOR_LSB							
RTFM	0x22	TIMING_LOOP_FREQ_MSB							
RTFL	0x23	TIMING_LOOP_FREQ_LSB							
VSTATUS	0x24	CF_LOCK	Reserved		PRF	LK	PR		
LDI	0x25	LOCK_DET_INTEGR							

Table 5: Registers map

Name	Addr	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ECNTM	0x26	ERROR_COUNT_MSB							
ECNTL	0X27	ERROR_COUNT_LSB							
SFRH	0X28	SYMB_FREQ_HSB							
SFRM	0X29	SYMB_FREQ_MSB							
SFRL	0X2A	SYMB_FREQ_LSB				Reserved			
CFRM	0X2B	CARRIER_FREQUENCY_MSB							
CFRL	0X2C	CARRIER_FREQUENCY_LSB							
NIRM	0X2D	NOISE_IND_MSB							
NIRL	0X2E	NOISE_IND_LSB							
VERROR	0X2F	ERROR_VAL							
FECM	0x30	Reserved	FECMODE			Reserved		SYNC	SYM
VTH12	0x31	Reserved	VTH12(1/2 puncture rate)						
VTH23	0x32	Reserved	VTH23(2/3 puncture rate)						
VTH34	0x33	Reserved	VTH34(3/4 puncture rate)						
VTH56	0x34	Reserved	VTHt56(5/6 puncture rate)						
VTH67	0x35	Reserved	VTH67(6/7 puncture rate)						
VTH78	0x36	Reserved	VTH78(7/8 puncture rate)						
PR	0X37	Reserved		PR_7_8	PR_6_7	PR_5_6	PR_3_4	PR_2_3	PR_2_1
VSEARCH	0X38	AM	F	SN		TO		H	
RS	0X39	DEINT	OUTRS_PS	RS	DESCRAM	EPR_BIT	MPEG	CLK_POL	CLK_CFG
RSOUT	0X3A	INV_DVALID	INV_ DSTART	INV_ DERROR	EN_STBAC KEND	ENA8_LEVEL			
ERRCTRL	0X3B	ERRMODE	Reserved	ERR_SOUROE		Reserved	RESET_CNT	NOE	
VITPROG	0X3C	NA	NA	NA	SWAP_EN	NA	NA	MDIVIDER	
ERRCTRL2	0X3D	ERRMODE2	Reserved	ERR_SOUROE2		Reserved	RESET_CNT2	NOE2	
ECNTM2	0X3E	ERROR_COUNT2_MSB							
ECNTL2	0X3F	ERROR_COUNT2_LSB							
PLLCTRL*	0x40	PLL_MDIV							
SYNTCTRL*	0x31	STANDBY	NA	NA	PLL-STOP	SEL_OSCI	PLL-SELR	NA	BYP_PLL
TSTTNR1*	0x42	NA	NA	ADC_PON	ADC_INMOD	NA	NA	OSCI	REGPOFF
IRQMSK2*	0x43	IRQ_MSK(15:8)							
IRQMSK1*	0x44	IRQ_MSK(7:0)							
IRQSTAT2*	0x45	IRQ_STATUS(15:8)							
IRQSTAT1*	0x46	IRQ_ STATUS (7:0)							
SYMBCTRL	0X4A	NA	NA	NA	NA	NA	NA	SYMB_CHOICE	
ISYMB	0X4B	ISYMB(7:0)							
QSYMB	0X4C	QSYMB(7:0)							
ASCTRL	0x50	NA	NA	FROZE_LK	KI		CENTER	FINE	COARSE
COAPP1	0x51	NA	KT						
COAPP2	0x52	NA	NA	KC			KS		
FMINM	0x53	STOP_ON_FMIN	FMIN(14:8)						
FMINL	0x54	FMAX(7:0)							
FMAXM	0x55	STOP_ON_FMAX	FMAX(14:8)						
FMAXL	0x56	FMAX(7:0)							
FINEINC	0x57	FINE_INCR(7:0)							

Table 5: Registers map

Name	Addr	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STEP2	0X58	STEP2_MINUS				STEP2_PLUS			
TH2	0X59	TH2(9:2)							
TH2&TH1	0X5A	TH2(1:0)		NA	NA	NA	NA	TH1(9:8)	
TH1	0X5B	TH1(7:0)							
THH	0X5C	NA	NA	THH					
IND1MAX	0X5D	IND1_TRESH(7:0)							
ACCU1VAL	0X5E	IND1_ACC(7:0)							
ACCU2VAL	0X5F	IND2_ACC(7:0)							
GPIO0CFG*	0x60	GPIO0_OD	GPIO0_CFG						GPIO0_XOR
GPIO1CFG*	0x61	GPIO1_OD	GPIO1_CFG						GPIO1_XOR
GPIO2CFG*	0x62	GPIO2_OD	GPIO2_CFG						GPIO2_XOR
GPIO3CFG*	0x63	GPIO3_OD	GPIO3_CFG						GPIO3_XOR
GPIO4CFG*	0x64	GPIO4_OD	GPIO4_CFG						GPIO4_XOR
GPIO5CFG*	0x65	GPIO5_OD	GPIO5_CFG						GPIO5_XOR
GPIO6CFG*	0x66	GPIO6_OD	GPIO6_CFG						GPIO6_XOR
GPIO7CFG*	0X67	GPIO7_OD	GPIO7_CFG						GPIO7_XOR
GPIO8CFG*	0X68	GPIO8_OD	GPIO8_CFG						IOP8_XOR
GPIO9CFG*	0X69	GPIO9_OD	GPIO9_CFG						GPIO9_XOR
GPIOVAL0*	0X6A	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
GPIOVAL1*	0X6B	CS1	CS0	STDBY	AUXCLK	DIRCLK	AGC	GPIO9	GPIO8
GPIOVAL2*	0X6C	NA	NA	NA	NA	NA	NA	NA	DISECQOUT
SDATCFG*	0xB0	SDAT_OD	SDAT_CFG						SDAT_XOR
SCLTCFG*	0xB1	SDCL_OD	SDCL_CFG						SDCL_XOR
AGCCFG*	0xB2	AGC_OD	AGC_CFG						AGC_XOR
DIRCLKCFG*	0xB3	DIRCLK_OD	DIRCLK_CFG						DIRCLK_XOR
AUXCKCFG*	0xB4	AUXCK_OD	AUXCK_CFG						AUXCK_XOR
STDBYCFG*	0xB5	STDBY_OD	STDBY_CFG						STDBY_XOR
CS0CFG*	0XB6	STDBY_OD	STDBY_CFG						STDBY_XOR
CS1CFG*	0XB7	STDBY_OD	STDBY_CFG						STDBY_XOR
DISEQCOCFG*	0X68	DISEQO_OD	DISEQO_CFG						DISEQO_XOR

12 Registers

Note: All register addresses are hexadecimal values. Signed registers are 2's complement. All registers not listed below, between 0x00 and 0x6C, should be programmed to 0.

ID **Identification register**

7	6	5	4	3	2	1	0
CHIP_IDENT				RELEASE			

Address: 0x00
Type: Read only (accessible in standby mode)
Reset: 0x10 (0001 0000)
Description: See also Section 4.5: *Identification register* on page 11.

[7:4] **CHIP_IDENT**: provides the identity of the circuit.

[3:0] **RELEASE**: provides the release number of the circuit in order to ensure software compatibility.

12.1 DiSEqC registers

DiSEqC **DiSEqC control register 1**

7	6	5	4	3	2	1	0
TIM_OFF	DIS_RESET	TIM_CMD		Reserved	DiS_PRECHARGE	DiSEqCMODE	

Address: 0x05
Type: Read/write
Reset: 0x16
Description: See also Chapter 6: *DiSEqC interface* on page 14.

[7] **TIM_OFF:** disable timer.
0: active timer 1: no timer

[6] **DIS_RESET:** control reset of FIFO content
0: active 1: reset the fifo content

[5:4] **TIM_CMD[1:0]:** timer control:
00: Tim = 15 ms at f_{22} = 22 kHz 01: Tim = 20 ms at f_{22} = 22 kHz
10: Tim = 25 ms at f_{22} = 22 kHz 11: Tim = 30 ms at f_{22} = 22 kHz

[3] **Reserved:** This bit must be programmed to zero.

[2] **DiS_PRECHARGE:** FIFO precharge mode
0: enable 1: disable

[1:0] **DiSEqCMODE[1:0]:** control mode

DISEQC2 DiSEqC control register 2

7	6	5	4	3	2	1	0
RECEIVER_ON	IGNO_SH2K	ONESHIP_TRX	EXT_ENVEL	PINSELECT		IRQ_RXEND	IRQ_HALF_FIFO

Address: 0x09
Type: Read/write
Buffer: 0x00
Description: See also Chapter 6: *DiSEqC interface* *on page 14*.

[7] **RECEIVER_ON:** control state of receiver.
0: receiver off 1: receiver on

[6] **IGNO_SH2K:** control check of short 2kmode
0: check it 1: ignore short 2k mode

[5] **ONESHIP_TRX:** control.

[4] **EXT_ENVEL:** control.

[3:2] **PINSELECT[1:0]:** control.

[1] **IRQ_RXEND:** enable trig of IT in case of end of reception

[0] **IRQ_HALF_FIFO:** enable trig of IT when fifo is half full

DiSEqCFIFO DiSEqC FIFO register

7	6	5	4	3	2	1	0
DiSEqCFIFO							

Address: 0x06
Type: Read/write
Reset: 0x00
Description: See also Chapter 6: *DiSEqC interface* *on page 14*.

[7:0] **DiSEqCFIFO**: FIFO byte

DiSEqCSTA1 DiSEqC status register 1

7	6	5	4	3	2	1	0
TX_FAIL	FIFO_FULL	TX_IDDLE	READ_WRITE_COUNT				

Address: 0x07
Type: Read only
Reset: 0x00
Description: See also Chapter 6: *DiSEqC interface* *on page 14*.

[7] **TX_FAIL**: when high transmit failed.

[6] **FIFO_FULL**: when high FIFO full.

[5] **TX_IDDLE:**

[4:0] **READ_WRITE_COUNT[4:0]**: number of bytes in FIFO.

DISEqCSTA2 DiSEqC status register 2

7	6	5	4	3	2	1	0
Reserved							GAPBURST_FLAG

Address: 0x08
Type: Read only
Reset: 0x00
Description: See also Chapter 6: *DiSEqC interface* *on page 14*.

[7:1] **Reserved**: must be programmed to zero.

[0] **GAPBURST_FLAG**

DISRX_ST0 DiSEqC receiver control register 1

7	6	5	4	3	2	1	0
RX_END	RX_ACTIVE	SHORT_22KHz	CONT_TONE	8BFIFORDY	FIFO_EMPTY	RX_NON_BYTE	ABORT_DIS

Address: 0x0A
Type: Read/write
Reset: 0x00
Description: See also Chapter 6: *DiSEqC interface* *on page 14*.

[7] **RX_END:** status, when high, reception ended.

[6] **RX_ACTIVE:** status, when high, receiver is activated.

[5] **SHORT_22KHz:** control, when high, short 22kHz mode is enabled.

[4] **CONT_TONE:** control, when high, programmed modulation tone is continuous.

[3] **8BFIFORDY:** status, when high, 8 bytes are ready in the FIFO.

[2] **FIFO_EMPTY:** status, when high, FIFO is empty.

[1] **RX_NON_BYTE**: control.

[0] **ABORT_DIS**: control.
0: continue 1: abort reception.

DISRX_ST1 DiSEqC receiver control register 2

7	6	5	4	3	2	1	0
RX_FAIL	PARITY_FAIL	FIFO_OVER	FIFO_BYTENBR				

Address: 0x0B
Type: Read/write
Reset: 0x00
Description: See also Chapter 6: *DiSEqC interface* *on page 14*.

[7] **RX_FAIL:** status, when high, reception failed.

[6] **PARITY_FAIL:** status, when high, wrong parity found in FIFO.

[5] **FIFO_OVER:** status, when high, receiver FIFO is overflow.

[4:0] **FIFO_BYTENBR[4:0]:** status, number of bytes in receiver FIFO.

F22FR F22 transmit frequency register

7	6	5	4	3	2	1	0
FFTX_REG							

Address: 0x03
Type: Read/write
Reset: 0x8E (1000 1110)
Description: See also Chapter 6: *DiSEqC interface* on page 14.

[7:0] **FFTX_REG**: The actual frequency is f_{M_CLK}/(32 R[7:0]). When this register is accessed, the divider by 16 (also common to AUX_CLK) and the divider by R[7:0] are initialized.

F22RX F22 receive frequency register

7	6	5	4	3	2	1	0
FFRX_REG							

Address: 0x04
Type: Read/write
Reset: 0x8E (10001110)
Description: See also Chapter 6: *DiSEqC interface* on page 14.

[7:0] **FFRX_REG**: The actual frequency is f_{M_CLK}/(32 R[7:0]). When this register is accessed, the divider by 16 (also common to AUX_CLK) and the divider by R[7:0] are initialized.

12.2 DVB-S and DirecTV registers

AGC1C AGC1 control register

7	6	5	4	3	2	1	0
ENA_DCADJ	AVERAGE_ON	AGC_OPDRAIN	IAGC	AGCIQ_BETA			

Address: 0x0E
Type: Read/write
Reset: 0xC4 (1100 0100)
Description: See also Section 7.1.2: *AGC1* on page 17.

[7] **ENA_DCADJ**: enable DC offset compensation acquisition

[6] **AVERAGE_ON:** apply DC offset compensation

[5] **AGC_OPDRAIN:** set AGC pad in open drain configuration
0: pushpull pad 1: op drain pad

[4] **IAGC:** inverted shape of AGC pin
0: no inversion 1: polarity is inverted

[3:0] **AGCIQ_BETA[3:0]:** Automatic gain control gain configuration
0000: 0001:

AGC1REF AGC1 reference control register

7	6	5	4	3	2	1	0
AGC1_REF							

Address: 0x0F
Type: Read/write
Reset: 0x2A (0010 1010)
Description: See also Section 7.1.2: *AGC1 on page 17*.

[7:0] **AGC1_REF[7:0]:** unsigned I&Q module reference

AGC1IN AGC1 accumulator status register

7	6	5	4	3	2	1	0
AGC1_VALUE							

Address: 0x10
Type: Read only
Description: See also Section 7.1.2: *AGC1 on page 17*.

[7:0] **AGC1_VALUE[7:0]:** read accumulator value (unsigned value).

TSREG Transport Stream control register

7	6	5	4	3	2	1	0
Reserved						SERIAL_O_D0	OUTRS_HZ

Address: 0x0D
Type: Read/write (accessible in standby mode)
Reset: 0x00 (0000 0000)
Description:

[7:2] **Reserved**: must be programmed to zero.

[1] **SERIAL_O_D0:** in serial mode data on bit 7 or 0
0: serial on bit 7 1: data on bit 0

[0] **OUTRS_HZ:** TS in high Z or not.

RTC Timing recovery control register

7	6	5	4	3	2	1	0
ALPHA_TMG[3:0]				BETA_TMG[3:0]			

Address: 0x11
Type: Read/write
Reset: 0x35 (0011 0101)
Description: See also Section 7.2.1: *Timing control on page 19*.

[7:4] **ALPHA_TMG:** timing loop control, refer to timing recovery loop section for details.

RTFM **Timing recovery control register**

7	6	5	4	3	2	1	0
TIMING_LOOP_FREQ_MSB							

Address: 0x22
Type: Read/write
Reset:
Description: See also Section 7.2.1: *Timing control* *on page 19*.

[7:0] **TIMING_LOOP_FREQ_MSB**: timing frequency register MSB (signed number)

RTFL **Timing recovery control register**

7	6	5	4	3	2	1	0
TIMING_LOOP_FREQ_LSB							

Address: 0x23
Type: Read/write
Reset:
Description: See also Section 7.2.1: *Timing control* *on page 19*.

[7:0] **TIMING_LOOP_FREQ_LSB**: timing frequency register LSB

SFRH **Timing recovery control register**

7	6	5	4	3	2	1	0
SYMB_FREQ_HSB							

Address: 0x28
Type: Read/write
Reset: 0x80 (1000 0000)
Description: See also Section 7.2.1: *Timing control* *on page 19*.

[7:0] **SYMB_FREQ_HSB**: symbol frequency register (MSBs). The reset value corresponds to $f_{M\_CLK}/2$.

SFRM **Timing recovery control register**

7	6	5	4	3	2	1	0
SYMB_FREQ_MSB							

Address: 0x29
Type: Read/write
Reset: 0x00
Description: See also Section 7.2.1: *Timing control* *on page 19*.

[7:0] **SYMB_FREQ_MSB**: symbol frequency register (middle byte)

SFRL **Timing recovery control register**

7	6	5	4	3	2	1	0
SYMB_FREQ_LSB				Reserved			

Address: 0x2A
Type: Read/write
Reset: 0x00
Description: See also Section 7.2.1: *Timing control on page 19*.

[7:4] **SYMB_FREQ_LSB**: symbol frequency register (LSBs)

[3:0] **Reserved:** must be programmed to zero.

STEP1 **Timing lock control register**

7	6	5	4	3	2	1	0
STEP1_MINUS				STEP1_PLUS			

Address: 0x14
Type: Read/write
Reset: 0x84 (1000 1000)
Description: Section 7.2.3: *Timing lock indicator on page 20*.

[7:4] **STEP1_MINUS**: timing lock setting register. Must be programmed to 8.

[3:0] **STEP1_PLUS**: timing lock setting register. Must be programmed to 4.

TLIRM **Timing lock control register**

7	6	5	4	3	2	1	0
TMG_LOCK			TMG_FINAL_IND_MSB				

Address: 0x1E
Type: Read only
Reset:
Description: See also Section 7.2.3: *Timing lock indicator on page 20*.

[7] **TMG_LOCK:** timing lock flag.

[4:0] **TMG_FINAL_IND_MSB:** timing lock indicator register (not signed)

TLIRL **Timing lock control register**

7	6	5	4	3	2	1	0
TMG_FINAL_IND_LSB							

Address: 0x1F
Type: Read only
Reset:
Description: See also Section 7.2.3: *Timing lock indicator on page 20*.