

DATA SHEET

TDA8566Q

**2 x 25 W BTL stereo car radio
power amplifier with differential
inputs and diagnostic outputs**

Preliminary specification
Supersedes data of 1995 Nov 20
File under Integrated Circuits, IC01

1996 Apr 17

2 x 25 W BTL stereo car radio power amplifier with differential inputs and diagnostic outputs

TDA8566Q

FEATURES

- Differential inputs
- Very high Common Mode Rejection Ratio (CMRR)
- High common mode input signal handling
- Requires very few external components
- High output power
- 4 Ω and 2 Ω load driving capability
- Low offset voltage at output
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature pre-warning)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- Short-circuit proof to ground, to V_P and across the load
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Protected against electrostatic discharge
- No switch-on/switch-off pop
- Flexible leads
- Low thermal resistance.

GENERAL DESCRIPTION

The TDA8566Q is an integrated class-B output amplifier contained in a 17-lead single-in-line (SIL; bent to DIL) plastic power package. The device contains two amplifiers in a Bridge-Tied Load configuration (BTL). The output power is 2 x 25 W in a 4 Ω load or 2 x 40 W in a 2 Ω load. It has a differential input stage and two diagnostic outputs. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	7.5	A
$I_{q(tot)}$	total quiescent current		–	115	–	mA
I_{stb}	stand-by current		–	0.1	100	μ A
I_{sw}	switch-on current		–	–	40	μ A
Z_i	input impedance		100	120	–	k Ω
P_{out}	output power	$R_L = 4 \Omega$: THD = 10%	–	25	–	W
		$R_L = 2 \Omega$: THD = 10%	–	40	–	W
SVRR	supply voltage ripple rejection	$R_s = 0 \Omega$	–	60	–	dB
α_{cs}	channel separation	$R_s = 10 \text{ k}\Omega$	–	50	–	dB
CMRR	common mode rejection ratio		–	75	–	dB
G_v	closed loop voltage gain		25	26	27	dB
V_{no}	noise output voltage	$R_s = 0 \Omega$	–	–	120	μ V
V_{os}	DC output offset voltage		–	–	100	mV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8566Q	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

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BLOCK DIAGRAM

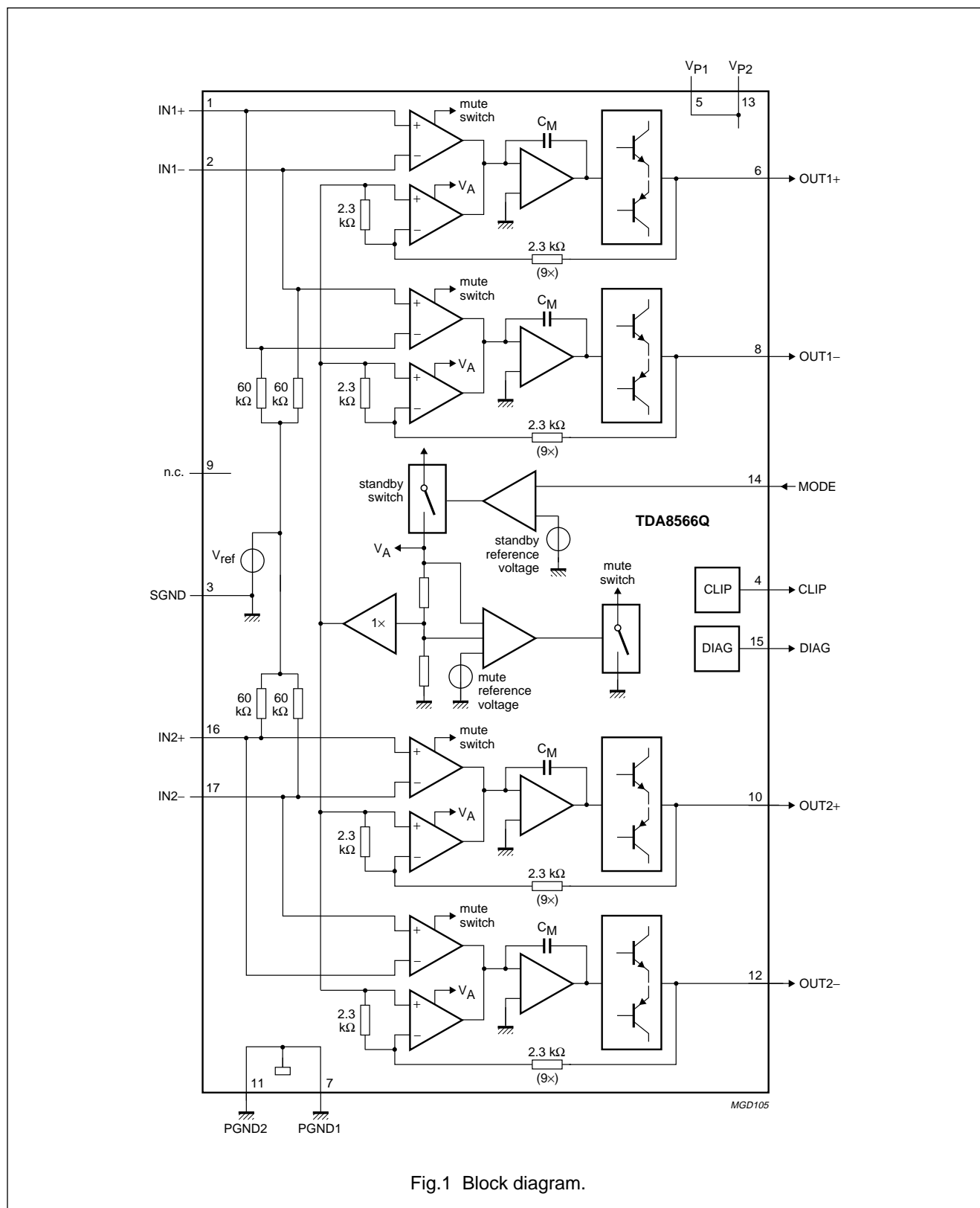


Fig.1 Block diagram.

2 x 25 W BTL stereo car radio power amplifier with differential inputs and diagnostic outputs

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PINNING

SYMBOL	PIN	DESCRIPTION
IN1+	1	channel 1 input positive
IN1–	2	channel 1 input negative
SGND	3	small signal ground
CLIP	4	clip-detection
V _{P1}	5	supply voltage 1
OUT1+	6	channel 1 speaker output positive
PGND1	7	channel 1 negative power supply (ground)
OUT1–	8	channel 1 speaker output negative
n.c.	9	not connected
OUT2+	10	channel 2 speaker output positive
PGND2	11	channel 2 negative power supply (ground)
OUT2–	12	channel 2 speaker output negative
V _{P2}	13	supply voltage 2
MODE	14	mode select switch (stand-by/mute/operating)
DIAG	15	short-circuit and temperature pre-warning diagnostic
IN2+	16	channel 2 input positive
IN2–	17	channel 2 input negative

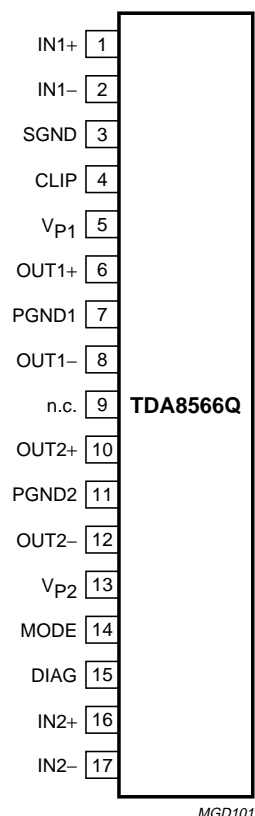


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8566Q contains two identical amplifiers and can be used for BTL applications. The gain of each amplifier is fixed at 26 dB. Special features of this device are:

1. Mode select switch
2. Clip detection
3. Short-circuit diagnostic
4. Temperature pre-warning
5. Open-collector outputs
6. Differential inputs.

Mode select switch (pin 14)

- Standby: low supply current ($< 100 \mu\text{A}$)
- Mute: input signal suppressed
- Operating: normal on condition.

Since this pin has a very low input current ($< 40 \mu\text{A}$), a low cost supply switch can be applied. To avoid switch-on pops, it is advisable to keep the amplifier in the mute mode for a period of $\geq 150 \text{ ms}$ (charging the input capacitors at pins 1, 2, 16 and 17). This can be realized by microcontroller control or by an external timing circuit (see Fig.7).

Clip detection (pin 4)

When clipping occurs at one or more output stages, the dynamic distortion detector becomes active and pin 4 goes low. This information can be used to drive a sound processor or DC volume control to attenuate the input signal and so limit the level of distortion. The output level of pin 4 is independent of the number of channels that are being clipped. The clip detection circuit is disabled in a short-circuit condition, so if a fault condition occurs at the outputs, pin 4 will remain at a high level. The clip detection waveforms are illustrated in Fig.3.

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Short-circuit diagnostic (pin 15)

When a short-circuit occurs at one or more outputs to ground or to the supply voltage, the output stages are switched off until the short-circuit is removed and the device is switched on again (with a delay of approximately 20 ms after the removal of the short-circuit). During this short-circuit condition, pin 15 is continuously low.

When a short-circuit occurs across the load of one or both channels, the output stages are switched off for approximately 20 ms. After approximately 50 μ s the load condition is again checked to see if the short-circuit is still present. Due to this duty cycle of 50 μ s/20 ms the average current consumption during this short-circuit condition is very low (approximately 40 mA). During this short-circuit condition, pin 15 is low for 20 ms and high for 50 μ s (see Fig.4). The power dissipation in any short-circuit condition is very low.

Temperature pre-warning (pin 15)

When the junction temperature (T_{vj}) reaches 145 °C, pin 15 will become continuously low.

Open-collector outputs

Pins 4 and 15 are open-collector outputs, therefore more devices can be tied together. Pins 4 and 15 can also be tied together. An external pull-up resistor is required.

Differential inputs

The input stage is a high-impedance fully differential balanced input stage that is also capable of operating in a single-ended mode with one of the inputs capacitively coupled to an audio ground. It should be noted that if a source resistance is added (input voltage dividers) the CMRR degrades to lower values.

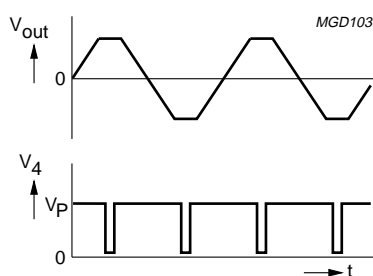


Fig.3 Clip detection waveforms.

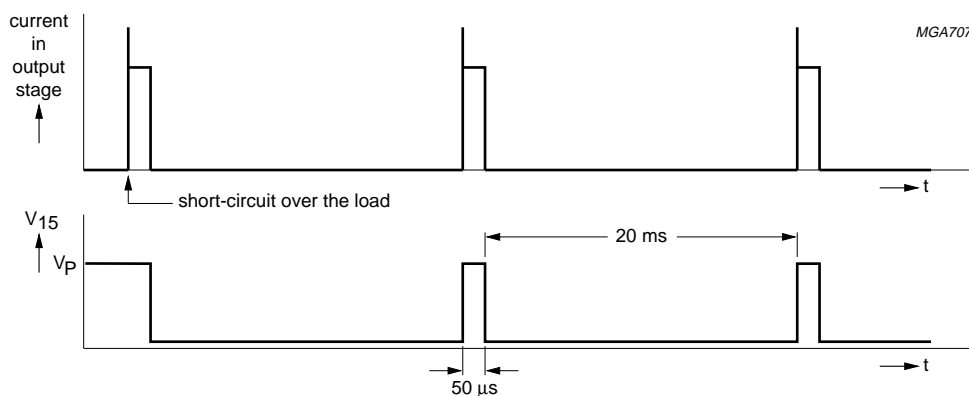


Fig.4 Short-circuit diagnostic timing diagram.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _P	supply voltage	operating	–	18	V
		non-operating	–	30	V
		during 50 ms; load dump protection t _{rise} ≥ 2.5 ms	–	45	V
I _{OSM}	non-repetitive peak output current		–	10	A
I _{ORM}	repetitive peak output current		–	7.5	A
T _{stg}	storage temperature		–55	+150	°C
T _{vj}	virtual junction temperature		–	+150	°C
T _{amb}	operating ambient temperature		–40	+85	°C
V _{psc}	short-circuit safe voltage		–	18	V
V _{pr}	reverse polarity		–	6.0	V
P _{tot}	total power dissipation		–	60	W

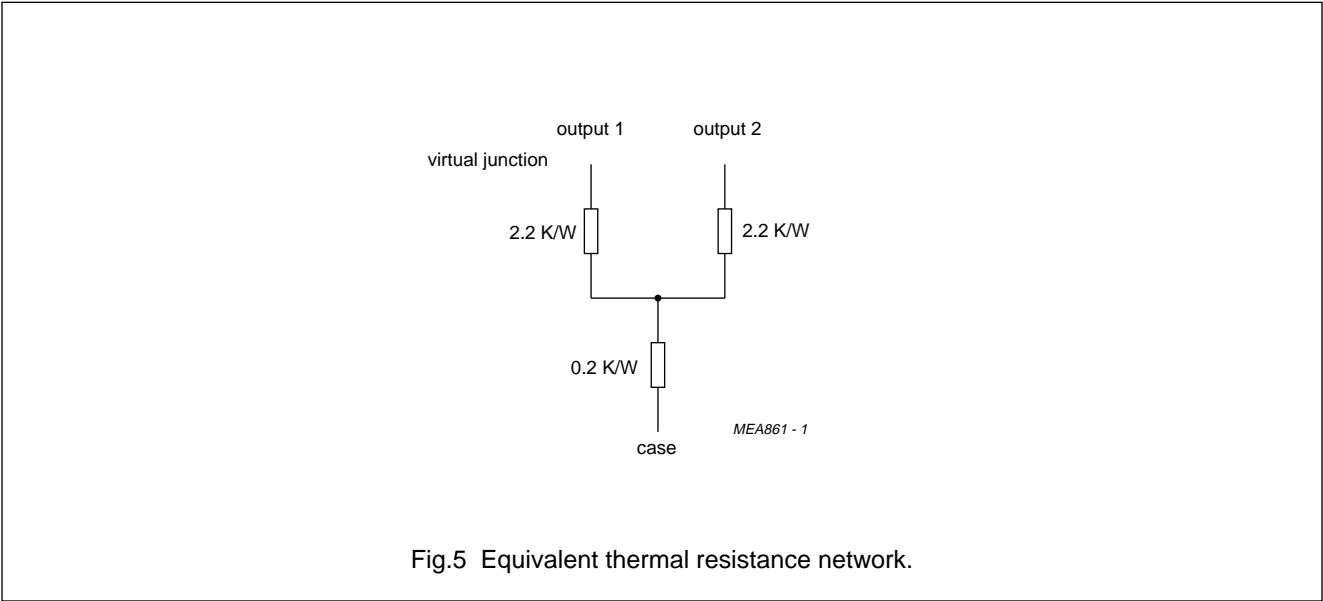
QUALITY SPECIFICATION

Quality specification in accordance with *UZW-FQ-611-E*, if this type is used as an audio amplifier. The number of the quality specification can be found in the “*Quality Reference Handbook*”. The handbook can be ordered using the code 9397 750 00192.

THERMAL CHARACTERISTICS

Thermal characteristics in accordance with (IEC 747-1).

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-c}	thermal resistance from junction to case	1.3	K/W
R _{th j-a}	thermal resistance from junction to ambient in free air	40	K/W



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DC CHARACTERISTICS

$V_P = 14.4\text{ V}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; measured in test circuit of Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage						
V_P	supply voltage	note 1	6	14.4	18	V
I_q	quiescent current	$R_L = \infty$	–	115	180	mA
Operating condition						
$V_{\text{ms(op)}}$	mode select switch level		8.5	–	V_P	V
I_{14}	mode select switch current	$V_{14} = 14.4\text{ V}$	–	15	40	μA
V_o	output voltage	note 2	–	7.0	–	V
V_{os}	output offset voltage		–	–	100	mV
Mute condition						
$V_{\text{ms(mute)}}$	mode select switch level		3.3	–	6.4	V
V_o	output voltage	note 2	–	7.0	–	V
V_{os}	output offset voltage		–	–	100	mV
Standby condition						
$V_{\text{ms(stb)}}$	mode select switch level		0	–	2	V
I_{stb}	standby current		–	0.1	100	μA
Diagnostic						
V_{15}	diagnostic output voltage	during any fault condition	–	–	0.6	V
T_{vj}	temperature pre-warning	$V_{15} = 0.6\text{ V}$	–	145	–	$^{\circ}\text{C}$

Notes

1. The circuit is DC adjusted at $V_P = 6$ to 18 V and AC operating at $V_P = 8.5$ to 18 V .
2. At $V_P = 18$ to 30 V the DC output voltage $\leq 0.5V_P$.

AC CHARACTERISTICS

$V_P = 14.4\text{ V}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; $R_L = 4\text{ }\Omega$; $f_i = 1\text{ kHz}$; measured in test circuit of Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_{out}	output power	THD = 0.5%	16	19	–	W
		THD = 10%	21	25	–	W
		THD = 30%	28	35	–	W
THD	total harmonic distortion	$P_{\text{out}} = 1\text{ W}$	–	0.05	–	%
P_{out}	output power	$V_P = 13.5\text{ V}$; THD = 0.5%	–	14	–	W
		$V_P = 13.5\text{ V}$; THD = 10%	–	22	–	W
B	power bandwidth	THD = 0.5%; $P_{\text{out}} = -1\text{ dB}$ with respect to 16 W	–	20 to 20000	–	Hz
f_l	low frequency roll off	-1 dB , note 1	–	25	–	Hz
f_h	high frequency roll off	-1 dB	20	–	–	kHz
G_v	closed loop voltage gain		25	26	27	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SVRR	supply voltage ripple rejection	on; note 2	50	—	—	dB
		mute; note 2	50	—	—	dB
		standby; note 2	80	—	—	dB
Z_i	input impedance	differential	100	120	150	k Ω
		single-ended	50	60	75	k Ω
$ \Delta Z_i $	input impedance mismatch		—	2	—	%
V_{no}	noise output voltage	on; B = 20 Hz to 20 kHz; $R_s = 0 \Omega$	—	85	120	μ V
		on; B = 20 Hz to 20 kHz; $R_s = 10 \text{ k}\Omega$	—	100	—	μ V
		mute; B = 20 Hz to 20 kHz; independent of R_s	—	60	—	μ V
α_{cs}	channel separation	$P_{out} = 16 \text{ W}$; $R_s = 10 \text{ k}\Omega$	45	—	—	dB
$ \Delta G_v $	channel unbalance		—	—	1	dB
V_o	output signal voltage in mute	$V_i = V_{i(max)} = 1 \text{ V (RMS)}$	—	—	2	mV
THD	total harmonic distortion	note 3; $V_4 = 0.6 \text{ V}$	—	8	—	%
CMRR	common mode rejection ratio	$R_s = 0 \Omega$; note 4	60	75	—	dB
		$R_s = 45 \text{ k}\Omega$, note 5	40	—	—	dB
P_{out}	output power	THD = 0.5%; $R_L = 2 \Omega$	—	30	—	W
		THD = 10%; $R_L = 2 \Omega$	—	40	—	W
		THD = 30%; $R_L = 2 \Omega$	—	55	—	W
		$V_P = 13.5 \text{ V}$; THD = 0.5%; $R_L = 2 \Omega$	—	25	—	W
		$V_P = 13.5 \text{ V}$; THD = 10%; $R_L = 2 \Omega$	—	35	—	W
THD	total harmonic distortion	$P_{out} = 1 \text{ W}$; $R_L = 2 \Omega$	—	0.1	—	%

Notes

- Frequency response externally fixed.
- $V_{ripple} = V_{ripple(max)} = 2 \text{ V (p-p)}$, $R_s = 0 \Omega$.
- Dynamic Distortion Detector (DDD) active, pin 4 is low.
- Common mode rejection ratio measured at the output (over R_L) with both inputs tied together, $V_{common} \leq 3.5 \text{ V (RMS)}$, $f = 100 \text{ Hz to } 10 \text{ kHz}$, $R_s = 0 \Omega$.
- Common mode rejection ratio measured at the output (over R_L) with both inputs tied together, $V_{common} \leq 3.5 \text{ V (RMS)}$, $f = 1 \text{ kHz}$, $R_s = 45 \text{ k}\Omega$. The mismatch of the input coupling capacitors is excluded.

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TEST AND APPLICATION INFORMATION

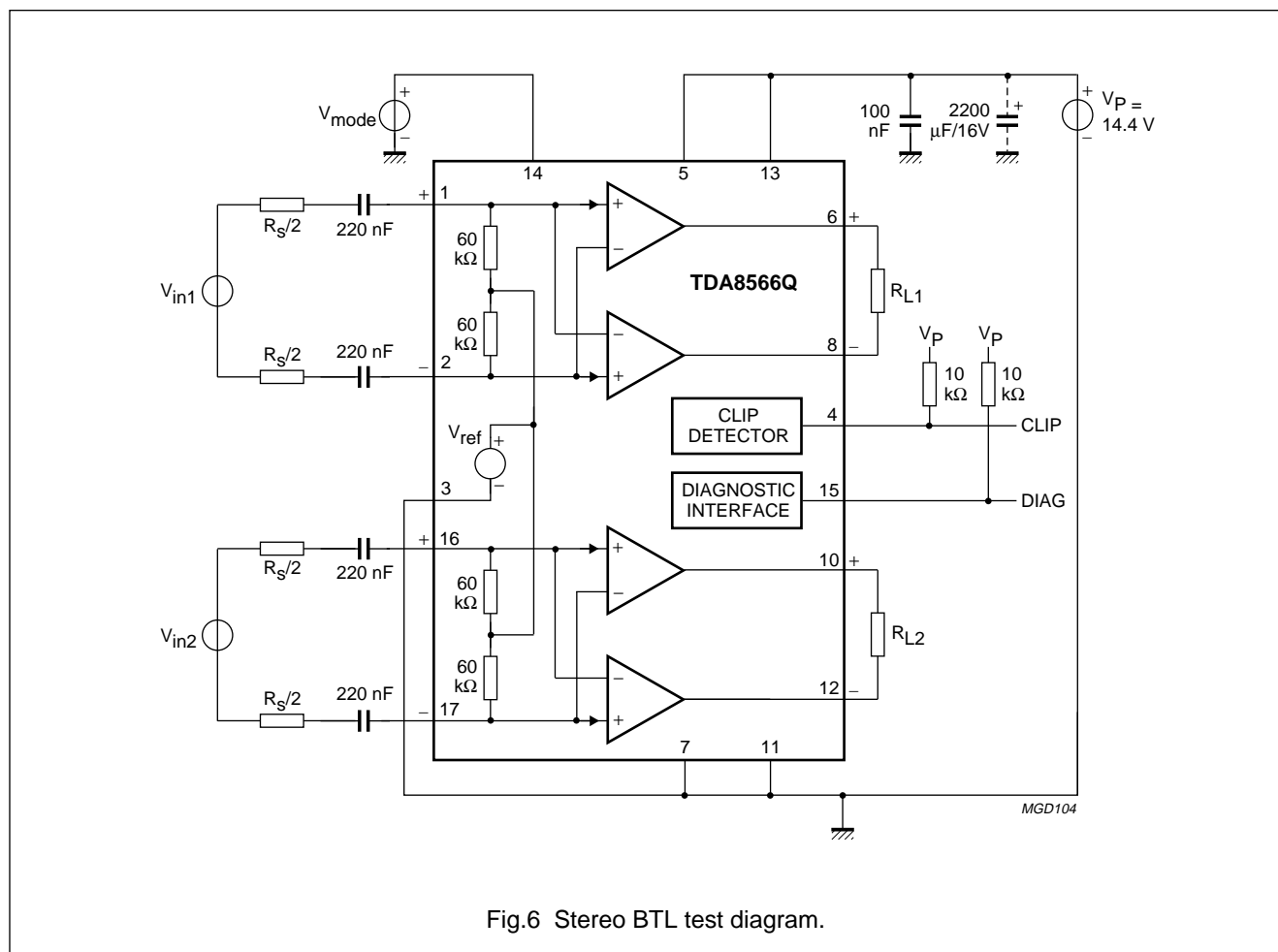


Fig.6 Stereo BTL test diagram.

Application notes

DIAGNOSTIC OUTPUT

Special care must be taken in the PCB layout to separate pin 4 from pins 1, 2, 16 and 17 to minimize the crosstalk between the CLIP output and the inputs.

MODE SELECT SWITCH

To avoid switch on plops, it is advisable to keep the amplifier in the mute mode during ≥ 150 ms (charging of the input capacitors at pins 1, 2, 16 and 17). The circuit in Fig.7 slowly ramps-up the voltage at the mode select switch pin when switching on and results in fast muting when switching off.

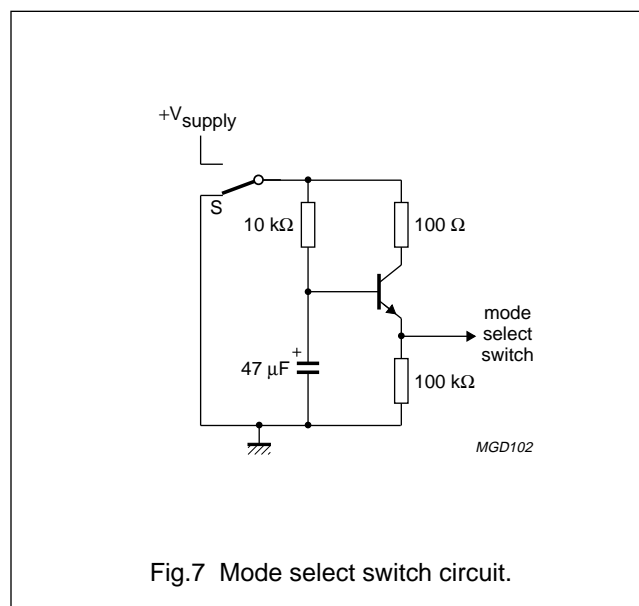


Fig.7 Mode select switch circuit.

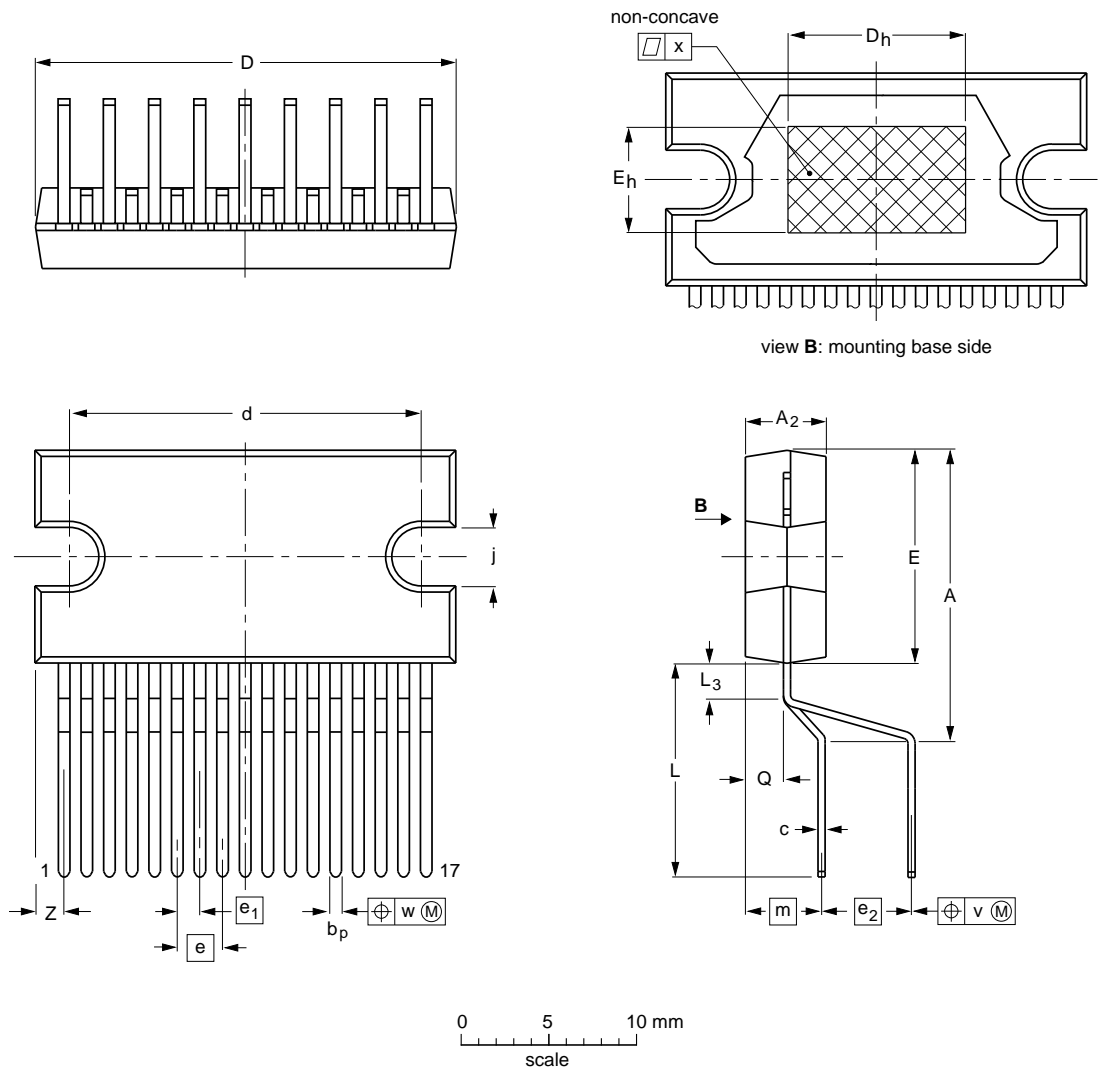
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PACKAGE OUTLINE

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)

SOT243-1



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₂	b _p	c	D ⁽¹⁾	d	D _h	E ⁽¹⁾	e	e ₁	e ₂	E _h	j	L	L ₃	m	Q	v	w	x	Z ⁽¹⁾
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						92-11-17 95-03-11

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{\text{stg max}}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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