TLC320AD80C
Data Manual

Audio Processor Subsystem

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1 Introduction

The TLC320AD80 is an audio processing subsystem designed to meet the audio needs of a broad range of set-top box applications. This device includes a high-performance stereo audio DAC, analog volume and balance control, analog TV monaural decoder, de-emphasis filter, and an analog wide-band multiplexer. The sigma-delta DAC performs data conversion with 85-dB performance. The architecture provides much flexibility, giving the user the option to use all or a subset of the functional blocks.

There are two serial digital interfaces for digital audio data and four analog audio inputs. The analog output of the device can be selected to be the output of the DAC, the output of the TV baseband filter, or pass-through of one of the analog inputs.

The digital interfaces enable ease of use by providing compatibility with the industry standard I^2S digital audio port, and with the SPI™ serial control interface. In addition, the digital audio interface supports additional interface protocols.

1.1 Features

- Highly Integrated Analog Audio Functions
- Flexible Architecture Allows Variable Interconnects Between Functions
- Sigma-Delta DAC With 16-Bit Resolution and 82-dB Performance Typical
- Internal Monaural Decoder for TV Baseband Audio
- Four Analog Audio Inputs: Two Stereo and Two Mono
- Volume and Balance Control: 69 Step at 1 dB per Step With Mute
- Selectable 50/15 ms De-Emphasis Analog Filter
- Uncommitted Wide-Band Analog 2:1 Multiplexer
- Multiplexed Analog Output can Select the Output of the DAC or Analog Data Pass-Through From One of the Analog Audio Inputs
- Two Flexible Digital Serial Data Ports (Philips I^2S Protocol, Left-Justified, and Right-Justified Formats)
- SPI Bus-Compatible Serial Control Port
- Sample Rates Supported in DAC: 8 kHz to 48 kHz
- Digital Serial Ports Support 16-Bit or 18-Bit PCM Digital Audio Data Format
- Analog Stereo Inputs can be Configured as Mono Inputs Through the Left Channel
- Analog Output With 600-Ω Load Drive and Short Circuit Protection
- Internal Voltage Reference
- TTL/CMOS Compatible
- Single 5-V Power Supply, 64-Pin TQFP Package

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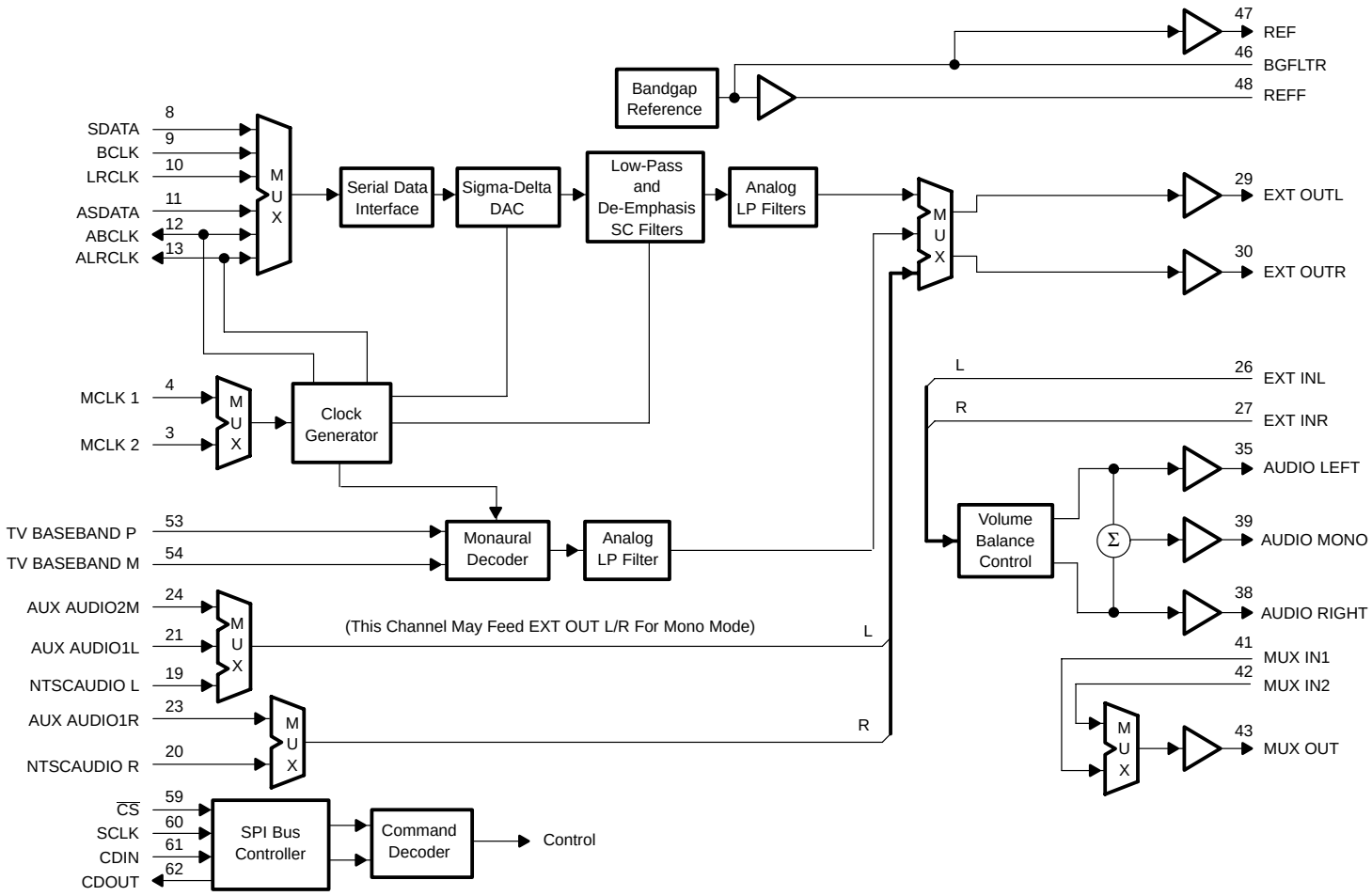
1.2 Applications

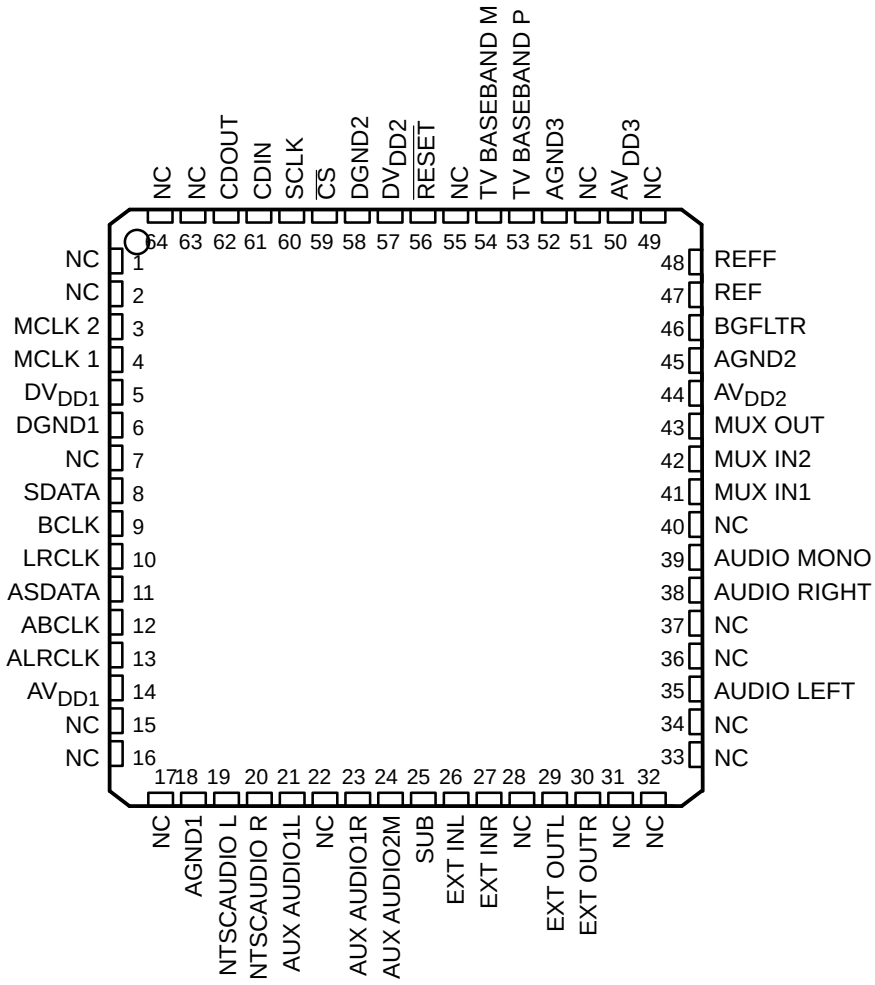
- Direct Broadcast Satellite (DBS) Set-Top Boxes
- Digital Cable or Telco Set-Top Boxes
- High Definition Television (HDTV), Digital Audio Broadcast Receivers
- Video Laser Disks, Video CD, and CD-I Players

1.3 Functional Block Diagram



1.4 Terminal Assignments

PM PACKAGE
TOP VIEW)



1.5 Ordering Information

T_A	PACKAGE
	CHIP CARRIER (PM)
0°C to 70°C	TLC320AD80CPM

1.6 Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND1	18	I	Analog ground for sigma-delta DAC
AGND2	45	I	Analog ground for analog audio output drivers
AGND3	52	I	Analog ground for bandgap reference
AUDIO LEFT	35	O	Left channel line-level analog audio output. The AUDIO LEFT output driver provides line level signals (1 V_{rms} max) for line output. The AUDIO LEFT output is capable of driving a 600-Ω load.
AUDIO MONO	39	O	Monaural variable line-level analog audio output. The AUDIO MONO output signal is the sum of the AUDIO RIGHT and AUDIO LEFT outputs divided by 2. The output is capable of driving a 10-kΩ load.
AUDIO RIGHT	38	O	Right channel variable line-level analog audio output. The AUDIO RIGHT output driver provides line level signals (1 V_{rms} max) for line output. The AUDIO RIGHT output is capable of driving a 600-Ω load.
AUX AUDIO1L	21	I	Left channel auxiliary analog audio input 1
AUX AUDIO1R	23	I	Right channel auxiliary analog audio input 1
AUX AUDIO2M	24	I	Mono channel auxiliary analog audio input 2
ABCLK	12	I/O	Auxiliary serial bit clock input. The ABCLK bit clock signal clocks the serial PCM data (ASDATA) into the TLC320AD80.
ALRCLK	13	I/O	Auxiliary left/right channel indicator. ALRCLK signifies whether the serial PCM data is associated with the left channel DAC or the right channel DAC.
ASDATA	11	I	Auxiliary serial PCM data input port. ASDATA can be configured as 16 or 18 bits with the most significant bit (MSB) first, 2's complement format.
AV_{DD1}	14	I	Analog 5-V power supply for the sigma-delta DAC
AV_{DD2}	44	I	Analog 5-V power supply for the analog audio output drivers
AV_{DD3}	50	I	Analog 5-V power supply for the bandgap reference
BCLK	9	I	Serial bit clock input. BCLK clocks the serial PCM data (SDATA) into the device.
BGFLTR	46	I	Bandgap reference filter. BGFLTR provides for noise filtering of the internal bandgap reference (2.25 V). BGFLTR requires a 0.1 μF capacitor to analog ground. This voltage node should be loaded only with a high-impedance dc load.
CDIN	61	I	SPI bus serial control data input. Data is transferred MSB first. CDIN specifies the channel specific attenuation and mute, serial PCM data format and rates, de-emphasis mode, audio input port selection, and stereo or monaural analog inputs.
CDOUT	62	O	SPI bus serial control data output port
$\overline{CS}$	59	I	SPI bus chip select input (active low)
DGND1	6	I	Digital ground for the sigma-delta DAC
DGND2	58	I	Digital ground for the serial interface
DV_{DD1}	5	I	Digital 5-V power supply for the sigma-delta DAC
DV_{DD2}	57	I	Digital 5-V power supply for the serial interface
EXT INL	26	I	Left channel external analog audio input
EXT INR	27	I	Right channel external analog audio input

1.6 Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EXT OUTL	29	O	Left channel fixed line level analog audio output. The EXT OUTL output driver provides line level signals (1 V_{rms} max) for line output. The EXT OUTL output is capable of driving a 10-kΩ load.
EXT OUTR	30	O	Right channel fixed line level analog audio output. The EXT OUTR output driver provides line level signals (1 V_{rms} max) for line output. The EXT OUTR output is capable of driving a 10-kΩ load.
LRCLK	10	I	Left/right channel indicator. LRCLK signifies whether the serial PCM data (SDATA) is associated with the left channel DAC or the right channel DAC.
MCLK 1	4	I	Master clock, sigma-delta DAC oversampling clock input. The TLC320AD80 defaults to MCLK 1. The TLC320AD80 can run off of MCLK 1 or MCLK 2.
MCLK 2	3	I	Auxiliary master clock, DAC oversampling clock input. The TLC320AD80 can run off of either MCLK 1 or MCLK 2.
MUX IN1	41	I	Wideband multiplexer input 1
MUX IN2	42	I	Wideband multiplexer input 2
MUX OUT	43	O	Wideband multiplexer output. The multiplexer can output one of two inputs (MUX IN1, MUX IN2) or perform an audio mute. The MUX OUT output is capable of driving a 600-Ω load.
NTSCAUDIO L	19	I	Left channel NTSC analog audio input
NTSCAUDIO R	20	I	Right channel NTSC analog audio input
REF	47	I	Voltage reference. The REF voltage provides a common mode reference of 2.25 V for all audio output drivers. The REF voltage can also be used as an external common mode reference with the restriction that only a high-impedance dc load should be applied. REF should be bypassed with a 0.1 μF capacitor.
REFF	48	I	Voltage reference filter. REFF is provided for low-pass filtering of the internal voltage reference (3.2 V) for the sigma-delta DAC. REFF should be bypassed with 10 μF and 0.1 μF capacitors. This voltage node should be loaded only with a high-impedance dc load.
$\overline{\text{RESET}}$	56	I	Power down/reset. When $\overline{\text{RESET}}$ is held low, the TLC320AD80 is placed in a power-down state. The TLC320AD80 is reset on the rising edge of $\overline{\text{RESET}}$.
SCLK	60	I	SPI bus serial clock input. Control input data (CDIN) must be valid on the rising edge of SCLK. SCLK may be continuous or gated.
SDATA	8	I	Serial PCM data input port. SDATA can be configured as 16 or 18 bits with the MSB first, 2s complement format.
SUB	25	I	Substrate ground connected to AGND plane.
TV BASEBAND P	53	I	TV aural baseband multiplex noninverting input
TV BASEBAND M	54	I	TV aural baseband multiplex inverting input

2 Functional Description

The TLC320AD80 is an audio processing subsystem that includes a high-performance stereo audio DAC, analog volume and balance control, analog TV monaural decoder, de-emphasis filter, and an analog wide-band multiplexer. The sigma-delta DAC performs data conversion with 85-dB performance. The architecture provides much flexibility with the option to use all or some of the functional blocks.

The digital interfaces enable ease of use by providing compatibility with the industry standard I^2S digital audio port, and with the SPI serial control interface. The digital audio serial interface also supports additional interface protocols and 16-bit or 18-bit data formats.

The analog interface provides much flexibility. Four analog audio sources are supported including two stereo audio sources, a TV baseband audio signal, and one mono source. In addition, the inputs to the volume and balance and the wideband mux are external to the chip. This allows the option to connect intermediate analog functions between functional blocks. As a default, these connections should include dc blocking capacitors to eliminate analog offsets. Finally, the primary analog output of the device is provided by a multiplexer. This allows selection from one of the following sources: the DAC, the output of the monaural decoder, or pass-through of one of the analog inputs. The multiplexer also allows the two stereo inputs to be used as mono inputs. In this case, the left channel is routed into both the left and right outputs.

The TLC320AD80 integrates several audio functions into one device. Following is a brief description of the device. Subsections of this chapter describe the details. The functions include:

- Sigma-delta stereo DAC
- 50/15 ms de-emphasis analog filter
- Analog volume and analog balance control
- Output multiplexer to select between the various audio sources
- TV baseband monaural audio decoder
- Additional uncommitted 2:1 mono multiplexer
- Two flexible digital audio input ports
- A SPI compatible serial control interface
- Voltage reference with buffered output

The DAC audio input can be selected from either of the digital serial ports. Several sample rates are supported. In addition, a software-selectable 50/15 μs de-emphasis filter is provided in the analog section of the DAC. The output of the DAC is fed into the output multiplexer. The aforementioned serial ports provide several timing protocols (Phillips I^2S, left justified, right justified, DSP mode), each with 16-bit or 18-bit data formats.

The TV baseband monaural decoder receives differential audio inputs from two external terminals (TV BASEBAND P, TV BASEBAND M). The output of this decoder is fed into the output multiplexer. The decoder is a differential eighth order elliptic switched capacitor filter used to reject high frequency audio signals that may be present in the NTSC audio broadcast multiplex. Proper operation of this section requires that the master clock (MCLK) correspond to an audio sample rate of 32 kHz.

The analog volume and balance control receives inputs from external terminals. The output of this section provides independent stereo and mono outputs on three terminals. All three outputs are also short-circuit protected. The functionality of this block provides either ganged or individual gain control for the left and the right channel. There are 69 volume settings which range from 6 dB to –62 dB of gain in 1 dB/step increments.

The external connections to this function allow for dc blocking capacitors to be included on the board, thus eliminating dc offsets present on the source. A typical implementation would connect the output of the analog multiplexer (EXT OUTL, EXT OUTR) to the input of this function.

The analog output multiplexer allows selection of the several analog sources input to the device. One of these audio sources is the output of the DAC. The others are the output of the TV monaural decoder, either of the two stereo analog inputs, or auxiliary mono input. Mono sources are sent to both right and left channels. The output of this multiplexer provides stereo outputs on two terminals, each with 10 kΩ drive capability. Both terminals are short-circuit protected.

The master clock for the device is derived from an external clock source. Control register 01h selects MCLK 1, or MCLK 2 to be the master clock source. This clock is then used to clock the DAC, the digital audio serial ports, and the monural decoder, switched-capacitor filter. The serial ports can be selected independent form the MCLK 1 and MCLK 2 selection. However, the clock rate of the selected clock source partly determines the sampling rate of the device. Refer to Table 2–1, and the description of control register 00h.

The TLC320AD80 also provides an uncommitted 2:1 mono analog multiplexer. The inputs and outputs of this device are connected to external terminals.

The voltage reference is used internally for the analog sections of the device. The external terminals must be connected to decoupling capacitors. In addition, the reference terminals can be externally buffered for use with external support circuitry.

2.1 Audio Input Ports

The audio inputs consist of: two digital serial interfaces, two stereo analog inputs, one analog TV baseband audio input, and one mono analog input. The TV baseband audio input is a differential input. All other analog inputs are single-ended.

The audio input is selected by programming control register 01h. Only one of these inputs is active at any one time. The others are disabled. That is, if an analog input is selected, then the digital serial interfaces are inactive.

The two digital serial interfaces provide the input to the DAC through a digital multiplexer. These interfaces support several serial protocols including I^2S, left-justified, and right-justified formats. The data format is 16-bit or 18-bit precision, with MSB first. There is also a DSP-compatible mode available.

All single-ended analog inputs can be passed through to the main output of the device by means of an analog multiplexer. The differential TV baseband audio input (TV BASEBAND P, TV BASEBAND M) feeds a monaural decoder which then feeds the same multiplexer.

2.1.1 Serial PCM Data Ports

The device includes two serial ports used to transfer digital audio data from an external digital source to the DAC: The AUX serial port (ASDATA, ABCLK, and ALRCLK) can be configured to operate in either master or slave mode. The main serial PCM port (SDATA, BCLK, and LRCLK) always operates in the slave mode. Note, that the only exclusion is that the AUX port does not support the DSP mode when configured as master.

Configuration of these serial ports is accomplished by means of the SPI-compatible control serial interface port. Specifically, the protocol (Philips I^2S protocol, left-justified, right-justified, or DSP mode), and data format (16-bit or 18-bit) are selected by programming control register 00h. The multiplexer selection is programmed with control register 01h which will also enable or disable these serial data ports.

2.1.1.1 Main Serial PCM Port

The main serial PCM (SDATA, BCLK, and LRCLK) port always operates in slave mode. That is, all clocks are inputs to the device. The LRCLK and BCLK clocks must be synchronous with MCLK.

A typical set-top-box application would connect this input to an MPEG/AC3 audio decoder.

2.1.1.2 Aux Serial PCM Data Port

The aux serial port (ASDATA, ABCLK, and ALRCLK) operates in either the master or slave mode. The master mode supports all the documented interface protocols with the exception of the DSP mode. The slave mode supports all documented protocols without exception.

The aux serial PCM data port receives non-compressed data from an auxillary audio source. The slave mode is identical to the clock mode of main serial PCM port. In the master mode, this device generates the required BCLK and LRCLK clocks synchronously with the applied MCLK.

2.1.1.3 Serial Interface Protocols Supported

The serial ports comprise the signals in Table 2–1.

Table 2–1. Serial Port Signals

MAIN PORT	AUXILIARY PORT	DESCRIPTION
SDATA	ASDATA	PCM audio data. 16-bit or 18-bit data precision
BCLK	ABCLK	Bit clock. Rate is equal to 32x, 48x, or 64x the sample rate
LRCLK	ALRCLK	Left/right clock. Rate is equal to the sample rate

Figure 2–1 through Figure 2–4 are for a bit clock (BCLK) set to 48× the sample rate and 16-bit data precision. All serial protocols supported are shown.

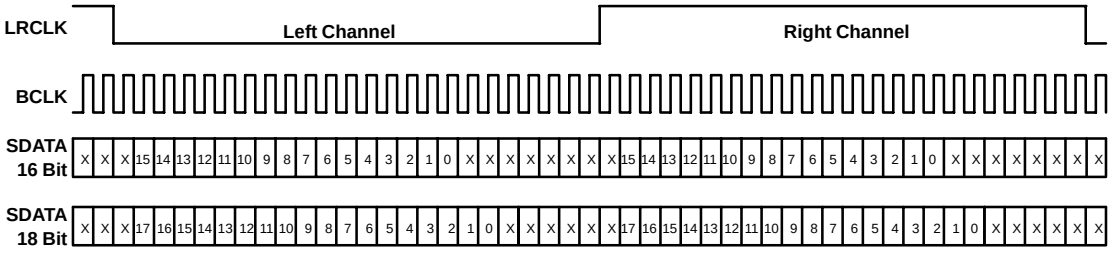


Figure 2–1. Philips I²S Protocol Serial PCM Data Format

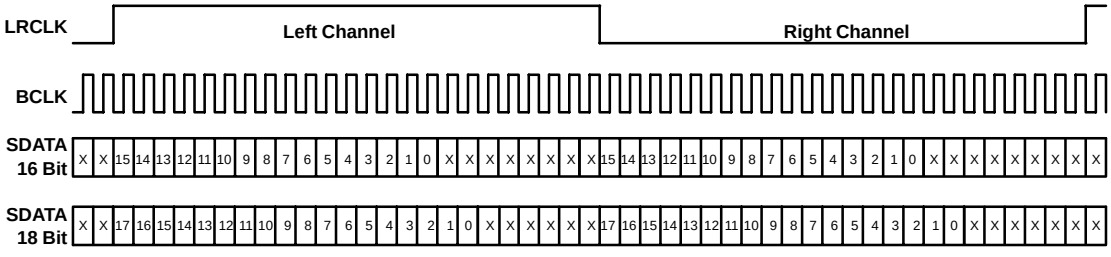


Figure 2–2. Left-Justified Serial PCM Data Format

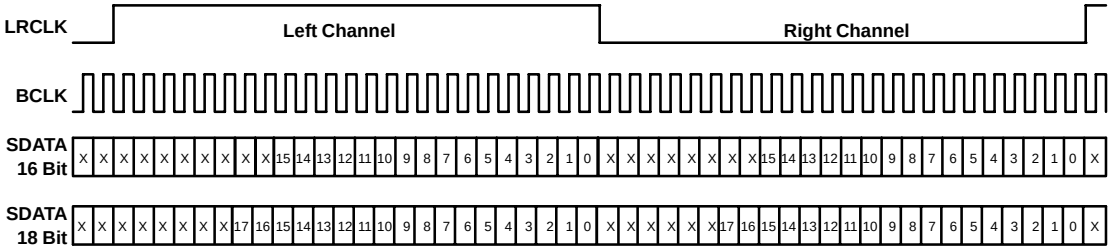


Figure 2–3. Right-Justified Serial PCM Data Format

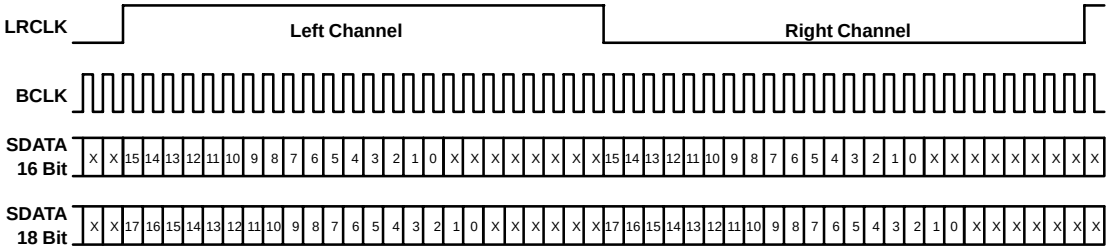


Figure 2–4. Left-Justified DSP Serial PCM Data Format (Inverted BCLK)

Table 2–2. Control Register 00h Allowable Settings

PRECISION	MCLK	BCLK	DIVIDER	JUSTIFICATION
16-Bit	256×	64×	4	Left, right, I^2S
16-Bit	256×	32×	8	Left, right, I^2S
16-Bit	384×	64×	6	Left, right, I^2S
16-Bit	384×	48×	8	Left, right, I^2S
16-Bit	384×	32×	12	Left, right, I^2S
16-Bit	512×	64×	8	Left, right, I^2S
16-Bit	512×	32×	16	Left, right, I^2S
16-Bit	256×	64×	4	Left, right, I^2S
18-Bit	384×	64×	6	Left, right, I^2S
18-Bit	384×	48×	8	Left, right, I^2S
18-Bit	512×	64×	8	Left, right, I^2S

Table 2–3. Master Clock (MCLK) Rates Supported For Various Sample Rates (LRCLK)

LRCLK (kHz)	MCLK (MHz)		
	256 × LRCLK	**384 × LRCLK**	**512 × LRCLK**
48	12.288	18.432	N/A
44.1	11.2896	16.9344	N/A
32	8.192	12.288	N/A
24	6.144	9.216	N/A
22.05	5.6448	8.4672	N/A
16	N/A	N/A	8.192
12	N/A	N/A	6.144
11.025	N/A	N/A	5.6448
8	N/A	N/A	4.096

2.1.2 Analog Audio Input Ports

The main analog audio input ports consist of two stereo audio inputs, one mono audio input, and one TV baseband audio input. The stereo inputs and the mono input can be passed through to the output (EXT OUTL, EXT OUTR) by means of the analog output multiplexer. The TV baseband audio is a differential input that feeds an internal monaural decoder before it is sent to the same output multiplexer.

The secondary analog audio inputs consist of one stereo input to the volume and balance control and two mono inputs to the wideband multiplexer. These inputs are intended primarily for interconnecting functional blocks by means of dc blocking capacitors. However, it also provides the user with the ability to combine internal functions with additional external analog functions. All inputs should be connected through dc-blocking capacitors.

2.1.2.1 Stereo Analog Input Ports

The two stereo audio input ports (NTSCAUDIO L, NTSCAUDIO R, AUX AUDIO1L, AUX AUDIO1R) are single-ended inputs. These inputs are sent to the output multiplexer without additional analog processing. The output of the multiplexer can be externally connected to another functional block such as the volume and balance control. These stereo inputs also have the ability to function in mono mode. In this mode, the left channel of the selected input is sent to both the left and right outputs (EXT OUTL, EXT OUTR). Control register 01h is used to program the mono or stereo mode for these inputs.

A typical application would connect the NTSC audio input to the output of a MTS stereo decoder. The AUX AUDIO1 port would be connected to an alternate nonbroadcast audio source.

2.1.2.2 Mono Analog Input Port

The one mono audio port (AUX MONO 2M) is a single-ended input. This input is sent to the output multiplexer without additional analog processing. However, the output of the multiplexer can be externally connected to another functional block such as the volume and balance control. This input is internally applied to both the left and right audio channels.

A typical application would connect the AUX MONO 2M input to receive the second audio program (SAP) channel output of an MTS stereo decoder.

2.1.2.3 TV Audio Baseband Input

The TV baseband audio audio port (TV BASEBAND P, TV BASEBAND M) is a mono differential input. This input feeds an internal a monaural decoder used to extract the mono (left and right) signal from the TV baseband. The output of the monaural decoder is sent to the output multiplexer.

The monaural decoder is a differential, eighth-order switched-capacitor filter. Proper operation requires that the master clock (MCLK 1 or MCLK 2) and control register settings correspond to a sample rate of 32 kHz. These settings ensure the filter requirements for proper stopband rejection. The purpose of the filter is to reject specific signals from the NTSC audio broadcast multiplex. The signals rejected include the 15.73425 kHz BTSC stereo pilot tone, left and right stereo subcarriers, SAP channel, Pro channel, and data channel as allowed by the FCC.

A typical connection would connect this input to the output of a TV IF detector. Therefore, composite TV aural baseband signal would be demodulated by the TV analog IF detector (without an MTS stereo decoder) and then input to the TLC320AD80.

A passive single pole low-pass filter with a 3-dB bandwidth of 2.12 kHz should be connected to the TV baseband differential input to provide the required 75 μs de-emphasis filter. This external filter also acts as an anti-aliasing filter for the internal switched capacitor monaural decoder.

2.1.2.4 Volume and Balance External Analog Input

This stereo audio input (EXT INL, EXT INR) is primarily intended to receive the external stereo audio output (EXT OUTL, EXT OUTR) of the TLC320AD80. However, the user has the option to connect additional analog functions in between these ports. The input should be ac-coupled to remove dc offsets that may be present in the incoming signal.

The input resistance of this port varies as a function of the volume control setting. The input resistance is lowest ($\geq$ 20 kΩ) when the volume control is at its maximum setting of 6 dB. The input resistance is reduced to approximately 2 kΩ when the capacitor precharge mode is selected from control register 01h. The capacitor precharge mode is provided to charge and discharge the external ac coupling capacitor quickly, overriding the input resistance of the volume control setting.

2.1.2.5 Wideband Multiplexer Analog Inputs

The MUX IN1 and MUX IN2 signals are the analog inputs to an uncommitted wideband multiplexer. A typical application would use this multiplexer to provide source selection for the input to a channel 3/4 RF modulator.

2.1.3 Audio Source Selection Procedure

Changing the audio source selection between any two of the six audio inputs can produce an audible click depending on the difference between the corresponding signal values at the time of switching. This difference between signals could be as large as 2.8 V peak-to-peak which would produce a very loud audible click. This audible click can be eliminated on the variable audio outputs (AUDIO RIGHT, AUDIO LEFT, and AUDIO MONO) by using the zero crossing mute function in conjunction with source selection changes. This procedure will not eliminate audible clicks on the fixed audio outputs (EXT OUTR, EXT OUTL) since the zero crossing mute function is located in the volume control block.

Prior to each audio source selection change, the audio output should be muted by writing 00h to volume control register 03h. The output signal follows the currently selected audio input until the next zero crossing occurs which activates the mute. After a recommended time delay of 4096 LRCLK cycles, the audio source can be changed by writing to control register 01h. The capacitor precharge mode and the audio input port mute should also be enabled by setting bit D1 to 1 and clearing bit D0 to 0 of control register 01h. After a second recommended time delay of 512 LRCLK cycles, the precharge mode and audio input port mute should be disabled and then the audio can be unmuted by restoring the original volume control setting to control registers 03h and 04h. The output signal remains muted until the next zero crossing occurs and then follows the newly selected audio input. The second delay time of 512 LRCLK cycles is required to allow

enough time for the voltage across the capacitors connecting the external stereo output to the external stereo input to reach a steady state condition.

A similar approach is required to prevent audible clicks on the output of the wideband multiplexer. Prior to each multiplexer input selection change, the multiplexer output should be muted by clearing bit D5 to 0 of control register 02h. The output signal follows the currently selected multiplexer input until the next zero crossing occurs which activates the mute. After a recommended time delay of 4096 LRCLK cycles, the multiplexer input selection can be changed by writing to bit D2 of control register 01h. The multiplexer output can then be unmuted by setting bit D5 to 1 of control register 02h. The output signal remains muted until the next zero crossing occurs and then follows the newly selected multiplexer input.

2.1.4 Audio Input Port Mute and Capacitor Precharge Mode

The sigma-delta DAC and the monaural decoder may introduce offset errors that could cause audible clicks or pops to occur during volume control changes. To prevent this audible noise, the external audio output (EXT OUTL, EXT OUTR) should be connected to the external audio inputs (EXT INL, EXT INR) through ac coupling capacitors to remove this offset error.

During source selection changes, sufficient time needs to be provided to allow the voltage across these external capacitors to reach a steady state condition before returning the audio to an unmuted condition. In order to minimize this required settling time, the input resistance of the external audio inputs can be reduce by a factor of 10 by selecting the capacitor precharge mode. The input resistance of this port normally varies as a function of the volume control setting. The input resistance is lowest ($\geq$ 20 kΩ) when the volume control is at its maximum setting of 6 dB. When the capacitor precharge mode is selected by setiing control register 01h to 1, the input resistance is reduced to approximately 2 kΩ.

The audio input port mute should be enabled when using the capacitor precharge mode by clearing bit D0 of control register 01h to 0. When the audio input port mute is enabled, the serial PCM audio data is disabled (forced to 0) at the input to the sigma-delta DAC, the differential input to the monaural decoder is shorted, and the remaining analog audio inputs are muted. This removes the signal content but not the offset error of a particular audio channel which is necessary in the capacitor precharge mode since the time constant may be insufficient to find the long term average of the selected audio signal.

The audio input port mute feature may also be used in conjunction with the volume control mute to provide increased audio mute attenuation for the serial PCM audio inputs. This improved mute attenuation occurs following 30 LRCLK cycles when the 0 input data propagates to the output of the sigma-delta DAC. The serial PCM audio data is enabled and disabled at the beginning of an audio sample period (rising edge of LRCLK) for an audio input port mute or unmute operation. The serial PCM data must be re-enabled prior to requesting an unmuted volume control setting to provide the audio signal necessary to perform a zero crossing unmute at the volume control stage.

2.2 Analog Audio Outputs

The TLC320AD80 analog outputs consist of two stereo outputs and two mono outputs. All are single-ended analog outputs.

2.2.1 Variable Stereo Audio Outputs

The variable stereo audio output (AUDIO LEFT, AUDIO RIGHT) provides the output of the volume and balance functional block. This output is intended as the final output of the TLC320AD80. In addition, one of the mono outputs (AUDIO MONO) is derived from this stereo audio pair. The AUDIO MONO output is the summation of the AUDIO LEFT and AUDIO RIGHT channels divided by 2.

The variable stereo audio output (AUDIO LEFT, AUDIO RIGHT) provides the selected audio input after application of the volume control. The full-scale analog output of each channel is typically 2.8 V peak-to-peak. These analog outputs can drive load impedances as low as 600 Ω and are short circuit protected to 10 mA.

A typical set-top-box application would connect AUDIO MONO output to one of the inputs of the wideband multiplexer after applying external 75 μs pre-emphasis. If selected by the wideband multiplexer, the monaural audio output would then be processed by the channel 3/4 RF modulator and then connected to an external TV or VCR receiver (with a coaxial cable). The full-scale analog output is typically 2.8 V peak-to-peak. This analog output (AUDIO MONO) can drive load impedances as low as 10 kΩ and is short circuit protected to 7 mA.

2.2.2 External Stereo Audio Output

The external stereo output (EXT OUTL, EXT OUTR) provides the output of the analog multiplexer (connected to the analog inputs, the DAC, and the monaural decoder). A typical connection would ac couple this output to the volume and balance external inputs. Alternate connections may include external analog functions located before the volume and balance input.

The selected audio input is output at a fixed volume of 0 dB on the external stereo audio output (EXT OUTL, EXT OUTR). The full-scale analog output of each channel is typically 2.8 V peak-to-peak. The analog outputs can drive load impedances as low as 10 kΩ and are short circuit protected to 7 mA.

2.2.3 Wideband Multiplexer Output

The wideband multiplexer output is a single-ended output provided by the wide-band multiplexer. The inputs and output of this multiplexer are provided by external terminals. A typical application would use this function to provide source selection for a channel 3/4 RF modulator. The modulator would then be connected to a TV or VCR by means of a coaxial cable.

The wideband multiplexer can output one of two inputs (MUX IN1 AND MUX IN2) or perform an audio mute. A typical connection would connect one input to the composite TV baseband audio signal. The other input would connect to the AUDIO MONO output of the TLC320AD80 with external 75 μs pre-emphasis. This feature allows remodulating an analog audio program which was broadcast in stereo without sacrificing the stereo content.

The wideband multiplexer has a 3-dB bandwidth greater than 90 kHz to provide a flat response for the SAP channel of a TV aural baseband signal. The volume control mute does not have any effect on the wideband multiplexer output. The wideband multiplexer has an independent mute control located at bit D5 of control register 02h. The full-scale analog output is typically 2.8 V peak-to-peak. The analog output can drive load impedances as low as 600 Ω and is short circuit protected to 10 mA.

2.3 Volume/Balance/Mute Control

The inputs and outputs of the volume and balance control are provided by external terminals. The inputs to this block (EXT INL, EXT INR) are typically ac-coupled to the EXT OUTL and EXT OUTR outputs. The outputs consist of a stereo pair (AUDIO LEFT, AUDIO RIGHT) and a mono output (AUDIO MONO). The volume of the left and right audio channels can be controlled independently for stereo balance control. The lowest volume control setting corresponds to audio mute.

2.3.1 Volume Control

The TLC320AD80 provides a volume control range from 6 dB to –62 dB in 1 dB increments. Volume changes can be executed in each channel (left or right) independently or in ganged mode. All volume transitions take effect at zero-crossing to avoid clicks during volume transitions.

Volume control changes are programmed by means of control registers 03h and 04h (see *Appendix A, Register Set*). These changes will take effect during zero crossing of the data on a given channel. A zero crossing is defined by when the relative magnitude of the signal is zero (i.e., equal to the V_{ref} voltage level). However, if no zero crossing occurs within 4096 LRCLK periods, the gain is forced to change. Independent left channel and right channel zero crossing detectors are provided to minimize pops or clicks on stereo signals.

The time-out feature of 4096 LRCLK periods can be eliminated by setting D7 of control register 04h, in which case the data values must have a zero crossing for the next gain setting to be sent to the amplifier. This feature is useful in applications where severe data latency is either expected or needed and an audio pop is to be avoided. Many other multimedia applications such as acoustic echo cancellation will benefit from this feature.

The 70th volume control setting corresponds to audio mute. Mute provides greater than 80 dB of attenuation from a full-scale audio output.

It is possible for an audible click or pop to occur immediately after a zero crossing unmute. If an audio amplifier needs to slew rate limit immediately after being unmuted to catch up with a rapidly changing audio input, then that amplifier may subsequently overshoot causing an audible click or pop. By utilizing the programmable volume control feature of the TLC320AD80, a soft mute function can be implemented in software that eliminates this potential cause of audible noise. A soft mute would provide a gradual attenuation change over an appropriate time interval when entering a muted condition rather than an allowing an abrupt change to occur. The original volume control setting would be gradually restored upon leaving a muted condition.

2.4 Sigma-Delta DAC

The sigma-delta DAC contains an interpolation filter and single bit modulator with 64 times oversampling. The switched-capacitor and continuous time analog filter which follows, provides the smoothed analog signal output.

2.4.1 Interpolator / Modulator

The interpolation filter receives 16-bit or 18-bit data at the sample rate and interpolates new values at a rate of 64-times the sample rate. These values are provided to the sigma-delta modulator for noise shaping. The output of the digital modulator is a one bit data stream which is sent to a switched capacitor filter.

2.4.2 Continuous Time and Switched Capacitor Filters

The switched capacitor filter performs the low-pass filter function. The filter characteristics are stated in the specification section. The corner frequency of this filter is directly proportional to the selected sample rate. The continuous time filter is used to reduce the switching frequency energy of the switched capacitor filter, and any remaining high frequency energy. This switched-capacitor filter also provides the selectable 50/15 µs de-emphasis under control of register 02h.

2.5 Serial Control Port

The SPI-compatible serial port controls all the programmable states of the TLC320AD80. The 4-wire SPI compatible interface is composed of a serial clock (SCLK), an active low chip select ($\overline{CS}$), a command data input (CDIN), and a command data output (CDOUT). There are five 8-bit control registers within the TLC320AD80.

2.5.1 Serial Control Port Description

The serial control port is activated when the active low $\overline{CS}$ signal is asserted. The $\overline{CS}$ input must be asserted low prior to a data transfer and must remain low for the duration of the transfer as shown in Figure 2–5.

The serial command data input (CDIN) is sampled with the rising edge of SCLK. The CDIN data is MSB first and unsigned.

While the $\overline{CS}$ input is low, the SCLK input must idle high when there is no valid data to be transferred. The first byte of CDIN data after $\overline{CS}$ activation is the serial control command. The serial control command includes a 4-bit control register address [D(3–0)] and a control port direction bit (D7). The second byte of data is the register data.

The $\overline{CS}$ input must make a low to high transition in order to specify a new control register address. When the $\overline{CS}$ input is set to 1, the serial command data output (CDOUT) is placed in a high-impedance state. When the $\overline{CS}$ input is cleared to 0, the CDOUT output is held low during nonvalid data intervals.

The serial control port is activated when the $\overline{CS}$ signal (active low) goes low. The $\overline{CS}$ line must be low prior to data transactions and must remain low for the duration of the transaction. The serial command data input (CDIN) is sampled on the rising edge of SCLK. The CDIN data is MSB first and unsigned. While the $\overline{CS}$ input is low, the SCLK input must idle high when there is no valid data to be transferred. The first byte of CDIN data after $\overline{CS}$ activation is set up as a serial control command. The serial control command includes a 4-bit control register address [D(3–0)] and a control port direction bit (D7). The second byte of data is set up as control register data. The $\overline{CS}$ input must make a low-to-high transition in order to specify a new control register address. When the $\overline{CS}$ input goes high, the serial command data output (CDOUT) is placed in a high-impedance state. When the $\overline{CS}$ input goes low, the CDOUT output is held low during nonvalid data intervals.

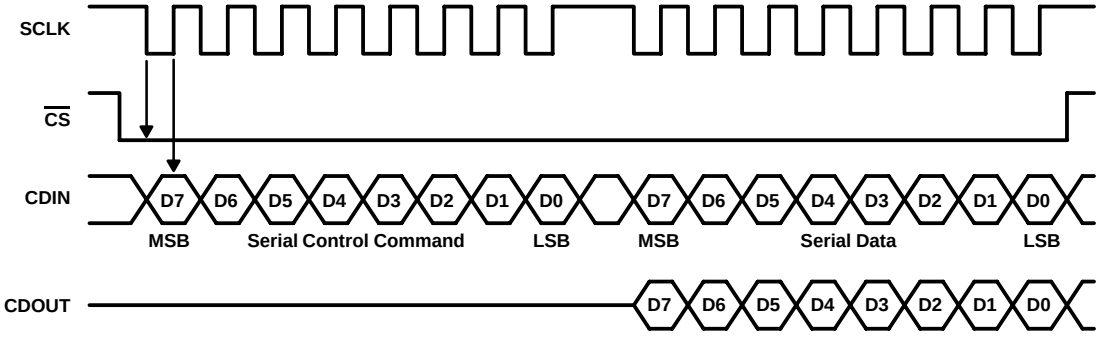


Figure 2–5. Serial Interface Timing

2.5.2 Serial Control Command Format

The serial control command format is shown below.

D7	D6	D5	D4	D3	D2	D1	D0
WR	Unused			ADDR(3–0)			

The serial control command fields are defined as:

WR – Serial interface direction

When this bit is 1:

- The serial interface is in write mode.
- Serial data is sent control register specified in the serial control command

When this bit is 0:

- The serial interface is in read mode.
- The control register data is output to CDOUT according to the control register address.

ADDR(3–0) – Control register address specifies the TLC320AD80 register being accessed.

2.5.3 Power-Down/Reset

When the $\overline{\text{RESET}}$ terminal is held low, the TLC320AD80C is put in a power-down condition. During power down, the sigma-delta DACs are disabled to conserve power and the digital output drivers (ABCLK, ALRCLK, and CDOUT) are placed in a high-impedance state. When powered down, the analog audio outputs settle near V_{ref} (2.25 V).

There are two ways in which to initialize the TLC320AD80C.

- The TLC320AD80C begins reset and initialization on the rising edge of the $\overline{\text{RESET}}$ signal. A stable clock waveform having a frequency within the specified allowable frequency range (see Timing Requirements section) must be present at the master clock (MCLK1) input prior to the rising edge of the $\overline{\text{RESET}}$ signal for proper operation. In order to prevent the occurrence of audible pops or clicks from the TLC320AD80C, the $\overline{\text{RESET}}$ terminal must be kept low 500 ms after the power supplies have settled. This provides adequate time for the 2.25-V based line outputs to charge the large output capacitors on the analog audio outputs while minimizing any audible pops.
- Set bit D0 of control register 02h to 1.

To maximize the initialization cycle accuracy, the TLC320AD80C should not be continually polled. This initialization cycle takes about 500 ms to complete following the rising edge of $\overline{\text{RESET}}$.

The power-down mode can also be selected by setting bit D0 of control register 02h to 1. In this software controlled power-down mode the sigma-delta DACs, the monaural decoder, and the audio input amplifiers are all disabled to conserve power. The external audio outputs (EXT OUTR, EXT OUTL) are muted to hold the output voltage at V_{ref}. Since muting the external audio output can cause an audible click, a zero crossing mute should be performed prior to initiating a software power-down.

2.6 Software Interface

Control of the TLC320AD80 is accomplished by means of the SPI serial interface and the control registers described in Appendix A.

3 Specifications

3.1 Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, AV_{DD} (see Note 1) . . . . . –0.3 V to 6 V
Supply voltage range, DV_{DD} (see Note 2) . . . . . –0.3 V to 6 V
Analog input voltage . . . . . –0.3 V to AV_{DD} + 0.3 V
Digital input voltage . . . . . –0.3 V to DV_{DD} + 0.3 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values for maximum ratings are with respect to AGND.
2. Voltage values for maximum ratings are with respect to DGND.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNITS
Analog supply voltage, AV_{DD} (see Note 3)	4.75	5	5.25	V
Digital supply voltage, DV_{DD}	4.75	5	5.25	V
Operating free-air temperature, T_A	0		70	°C
Storage temperature, T_{stg}	–65		150	°C

NOTE 3: Voltages at analog inputs and outputs and V_{CC} are with respect to the AGND terminal.

3.2.1 Static Digital Specifications, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V + 5%

	TEST CONDITIONS	MIN	NOM	MAX	UNITS
High-level input voltage, V_{IH}				2	V
Low-level input voltage, V_{IL}		0.8			V
High-level output voltage, V_{OH}	I_O = –1 mA	2.4		DV_{DD}	V
Low-level output voltage, V_{OL}	I_O = 4 mA			0.4	V
Input leakage current		–10		10	µA
Output leakage current		–10		10	µA
Leakage current, digital I/O terminals	Input mode	–10		10	µA

3.2.2 Power Supplies, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V + 5%

	TEST CONDITIONS	MIN	NOM	MAX	UNITS
Power supply current (see Note 4)	Normal		52	90	mA
	Power-down mode		19		mA
Power supply rejection	1 kHz		40		dB
	1 MHz		30		dB

NOTE 4: Power supply current rating for line outputs driving 10-kΩ load.

3.3 Electrical Characteristics

3.3.1 Analog Audio Channel Performance, T_A = 25 °C, AV_{DD} = DV_{DD} = 5 V ± 5%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Full-scale input voltage		All analog audio inputs	2.66	2.8	2.94	V_{PP}
Common mode input voltage		All analog audio inputs	2.1	2.25	2.4	V
Input impedance	Resistance	All analog audio inputs	20			kΩ
	Capacitance	All analog audio inputs		15		pF
3-dB Bandwidth		All analog audio inputs except the TV BASEBAND P or TV BASEBAND M inputs	20			kHz
Signal-to-noise ratio (SNR)		A-weighted, referenced to 0-dB f_S, All analog audio inputs except the TV BASEBAND P or TV BASEBAND M inputs	80	85		dB
Total harmonic distortion (THD)		A–weighted, referenced to 0-dB f_S			0.02%	
Frequency response		20 Hz to 20 kHz	–0.8		0.2	dB
Deviation from linear phase		20 Hz to 20 kHz		±1.5		degrees

3.3.2 Volume Control and Output Drivers Performance, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V ± 5%

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNITS
Volume control		Range	Total continuous control range		68		dB
		Step resolution	Differential error	0.5	1	1.5	dB
		Volume integral error	Deviation from ideal volume setting		±2		dB
		Gain tracking	Left and right channel gain matching		±1		dB
		Mute attenuation	Relative to volume setting of 0 dB	–80	–90		dB
Full-scale output voltage			All analog audio outputs, maximum volume	2.66	2.8	2.94	V_{PP}
Common mode output voltage			All analog audio outputs	2.1	2.25	2.4	V
Output resistance (open loop)			All analog audio outputs		300		Ω
Output drive capability		Ouput load resistance	Short circuit protected, AUDIO RIGHT, AUDIO LEFT, MUX OUT	600			Ω
			Short circuit protected, AUDIO MONO, EXT OUTR, EXT OUTL	10			kΩ
		Ouput load capacitance	Short circuit protected, AUDIO RIGHT, AUDIO LEFT			300	pF
			Short circuit protected, AUDIO MONO, EXT OUTR, EXT OUTL, MUX OUT			100	pF
V_{ref}	Output reference voltage			2.1	2.25	2.4	V
	Output reference current				100		µA
	Audio channel separation (relative to 0 dB)	EXT OUTL, EXT OUTR			80		dB
		AUDIO LEFT, AUDIO RIGHT			80		dB

3.3.3 Monaural Decoder Performance, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V ± 5%, f_S = 32 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
3-dB Bandwidth		TV BASEBAND P or TV BASEBAND M inputs only, MCLK = 256 x 32 kHz or 384 x 32 kHz		14		kHz
Signal-to-noise ratio (SNR)		A-weighted, referenced to –3 dB, f_S = 50 Hz to 14 kHz		54		dB
Total harmonic distortion (THD)		A-weighted, referenced to –3 dB, f_S = 50 Hz to 14 kHz		50		dB
BTSC filter	–3-dB Passband	TV baseband input filter referenced to 0 dB	14			kHz
	Passband ripple			±0.5		dB
	Stopband		15.73425			kHz
	Stopband rejection		–44	–50		dB

3.3.4 Wideband Multiplexer Performance, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V ± 5%

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
3-dB Bandwidth	MUX IN1 or MUX IN2 inputs	90			kHz
Signal-to-noise ratio (SNR)	Unweighted, referenced to 0 dB, f_S = 50 Hz to 47 kHz	70	85		dB
Total harmonic distortion (THD)	Unweighted, referenced to 0 dB, f_S = 50 Hz to 47 kHz			0.1%	
Frequency response	50 Hz to 47 kHz		±0.35		dB
Deviation from linear phase	50 Hz to 47 kHz		±2		degrees

3.3.5 PCM Audio Channel Performance, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V ± 5%, f_S = 48 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DAC resolution (see Note 5)			16			Bits
Signal-to-noise ratio (SNR) (see Note 5)		A-weighted, referenced to –3 dB, f_S	76	82		dB
Total harmonic distortion (THD) (see Note 5)		A-weighted, referenced to –3 dB, f_S		0.02%		
Total harmonic distortion + noise (THD+N) (see Note 5)		A-weighted, referenced to –3 dB, f_S	–70	–74		dB
Total harmonic distortion + noise (THD+N) without de-emphasis		A-weighted, referenced to –3 dB, f_S	62	66		dB
Signal-to-intermodulation distortion				–74		dB
Frequency response		0 to 0.4 f_S	–0.5		0.5	dB
Deviation from linear phase		0 to 0.4 f_S		±1.4		degrees
Crosstalk isolation			–72	–78		dB
Audible out of band energy		0.55 f_S to 22 kHz		–60		dB
Total out of band energy		0.55 f_S to 3 MHz		–45		dB
De-emphasis, 50/15 µs	Pole location	f_S = 32, 44.1, and 48 kHz only		3.18		kHz
	Zero location	f_S = 32, 44.1, and 48 kHz only		10.6		kHz
	Attenuation	f_S = 32, 44.1, and 48 kHz only, 20 log (15/50)		–10.5		dB

NOTE 5: Measurements are performed with de-emphasis enabled.

3.3.6 DAC Interpolation Filter, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V ± 5%, f_S = 48 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Passband	f_S = Audio sample rate	0		0.4 f_S	kHz
Passband ripple				±0.1	dB
Transition band		0.4 f_S		0.6 f_S	kHz
Stopband		>0.6 f_S			kHz
Stopband attenuation		74			dB
Group delay			30/f_S		sec
Group delay variation versus frequency			0.1/f_S		sec

3.4 Timing Requirements, T_A = 25 °C, AV_{DD} = DV_{DD} = 5 V ± 5%, f_s = 48 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
	Input frequency, MCLK1, MCLK2		4.096		18.432	MHz
f_s	Audio sample rate		8		48	kHz
t_{su1}	Setup time, PCM data	Relative to the rising edge of BCLK			60	ns
t_{h1}	Hold time, PCM data	Relative to the rising edge of BCLK			0	ns
t_{su2}	Setup time, LRCLK	Relative to the rising edge of BCLK			60	ns
t_{h2}	Hold time, LRCLK	Relative to the rising edge of BCLK			0	ns

3.4.1 Serial PCM Data Port (see Figures 3–1 and 3–2)

PARAMETER		MIN	TYP	MAX	UNITS
$t_{c(BCLK)}$	Cycle time, BCLK			60	ns
$t_{r(BCLK)}$	Rise time, BCLK			0	ns
$t_{f(BCLK)}$	Fall time, BCLK			0	ns
$t_{su(LRCLK)}$	Setup time, LRCLK↓ before BCLK↑			0	ns
$t_{h(LRCLK)}$	Hold time, LRCLK↑ after BCLK↑			0	ns
$t_{su(SDATA)}$	Setup time, SDATA before BCLK↑			0	ns
$t_{h(SDATA)}$	Hold time, SDATA after BCLK↑			0	ns
$t_{d(SDATA)}$	Delay time, SDATA valid after BCLK↓			0	ns
$t_{wL(BCLK)}$	Pulse duration, BCLK low			60	ns
$t_{wH(BCLK)}$	Pulse duration, BCLK high			60	ns
$t_{wL(MCLK)}$	Pulse duration, MCLK low			60	ns
$t_{wH(MCLK)}$	Pulse duration, MCLK high			60	ns
$t_{r(MCLK)}$	Rise time, MCLK			0	ns
$t_{f(MCLK)}$	Fall time, MCLK			0	ns

3.4.2 Serial Control Interface, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V ± 5%, (see Figure 3–3)

DESCRIPTION		MIN	TYP	MAX	UNITS
f_{SCLK}	Input frequency, SCLK			3	MHz
$t_{c(SCLK)}$	Cycle time, SCLK	333			ns
$t_{wL(SCLK)}$	Pulse width, SCLK low	100			ns
$t_{wH(SCLK)}$	Pulse width, SCLK high	100			ns
$t_{su(CS)}$	Setup time, $\overline{CS}$↓ before SCLK↓	150			ns
$t_{h(CS)}$	Hold time, $\overline{CS}$↑ after SCLK↑	150			ns
$t_{su(CDIN)}$	Setup time, CDIN before SCLK↑	50			ns
$t_{h(CDIN)}$	Hold time, CDIN after SCLK↑	50			ns
$t_{d(CDOUT)}$	Delay time, CDOUT after SCLK↓			30	ns
$t_{h(CDOUT)}$	Hold time, CDOUT after SCLK↓		5		ns
$t_{r(SCLK)}$	Rise time, SCLK			100	ns
$t_{f(SCLK)}$	Fall time, SCLK			100	ns

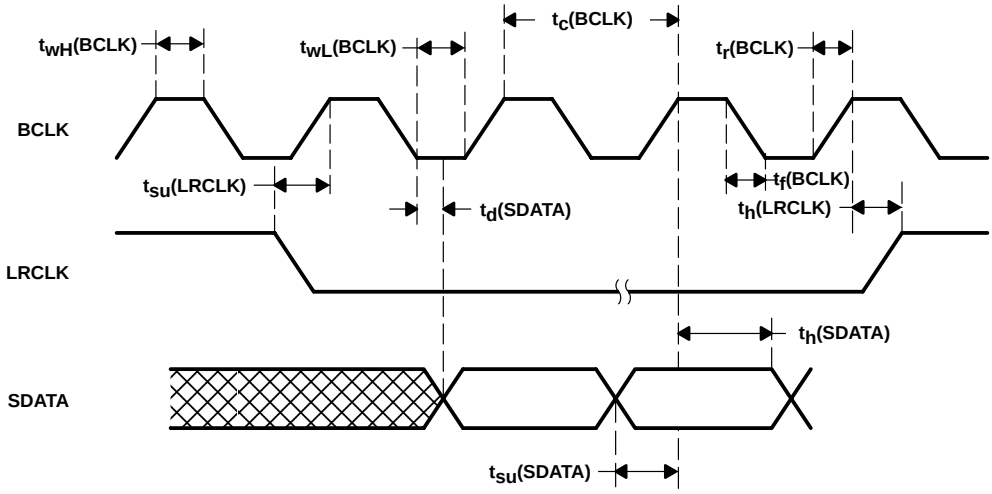


Figure 3–1. Serial Port Timing

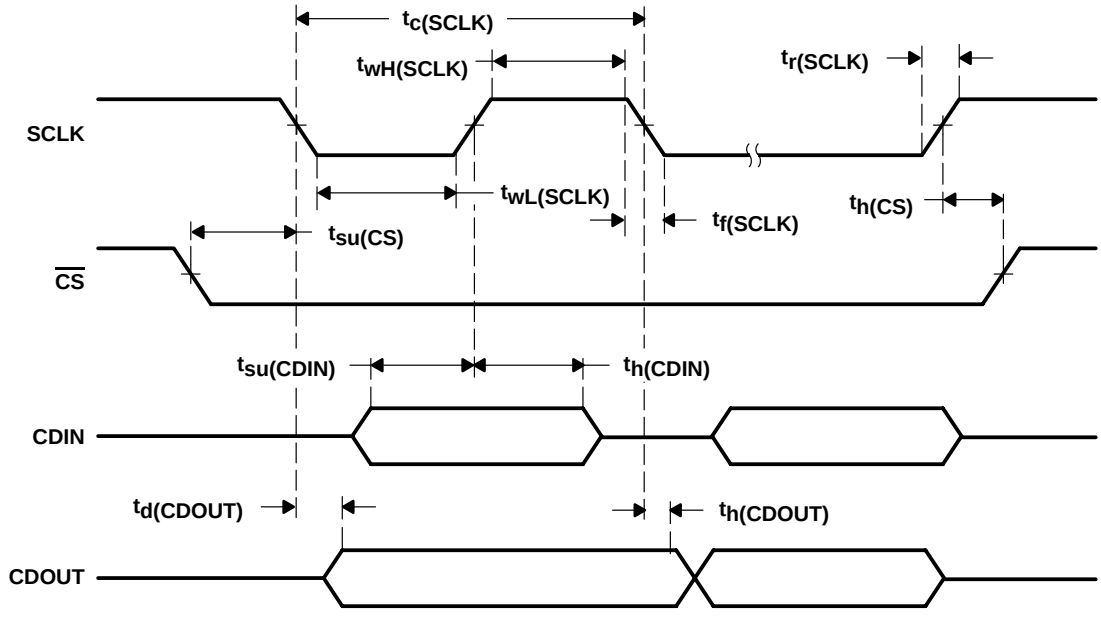


Figure 3–2. SPI Serial Control Port Timing

4 Application Information

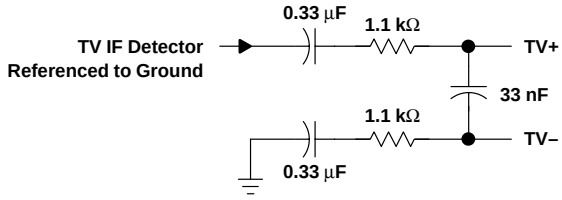


Figure 4–1. De-Emphasis 75 μs Low-Pass Filter at 2.12 kHz

Table 4–1. Digital Interface Capacitive Loading, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V ± 5%, f_S = 48 kHz

TERMINAL NAME	TERMINAL NO.	I/O	TYPICAL CAPACITIVE LOAD
SDATA	44	I	5 pF
BCLK	1	I	5 pF
LRCLK	2	I	5 pF
ASDATA	3	I	5 pF
ABCLK	4	I	5 pF
ABCLK	40	I	5 pF
ALRCLK	5	I	5 pF
ALRCLK	50	I	5 pF
MCLK	41	I	5 pF
AMCLK	40	I	5 pF
CDOUT	39	O	5 pF
CDIN	38	I	5 pF
SCLK	37	I	5 pF
$\overline{CS}$	36	I	TBD
$\overline{RESET}$	33	I	TBD

NOTE 1: ALRCLK and ABCLK are programmable as either inputs or outputs.

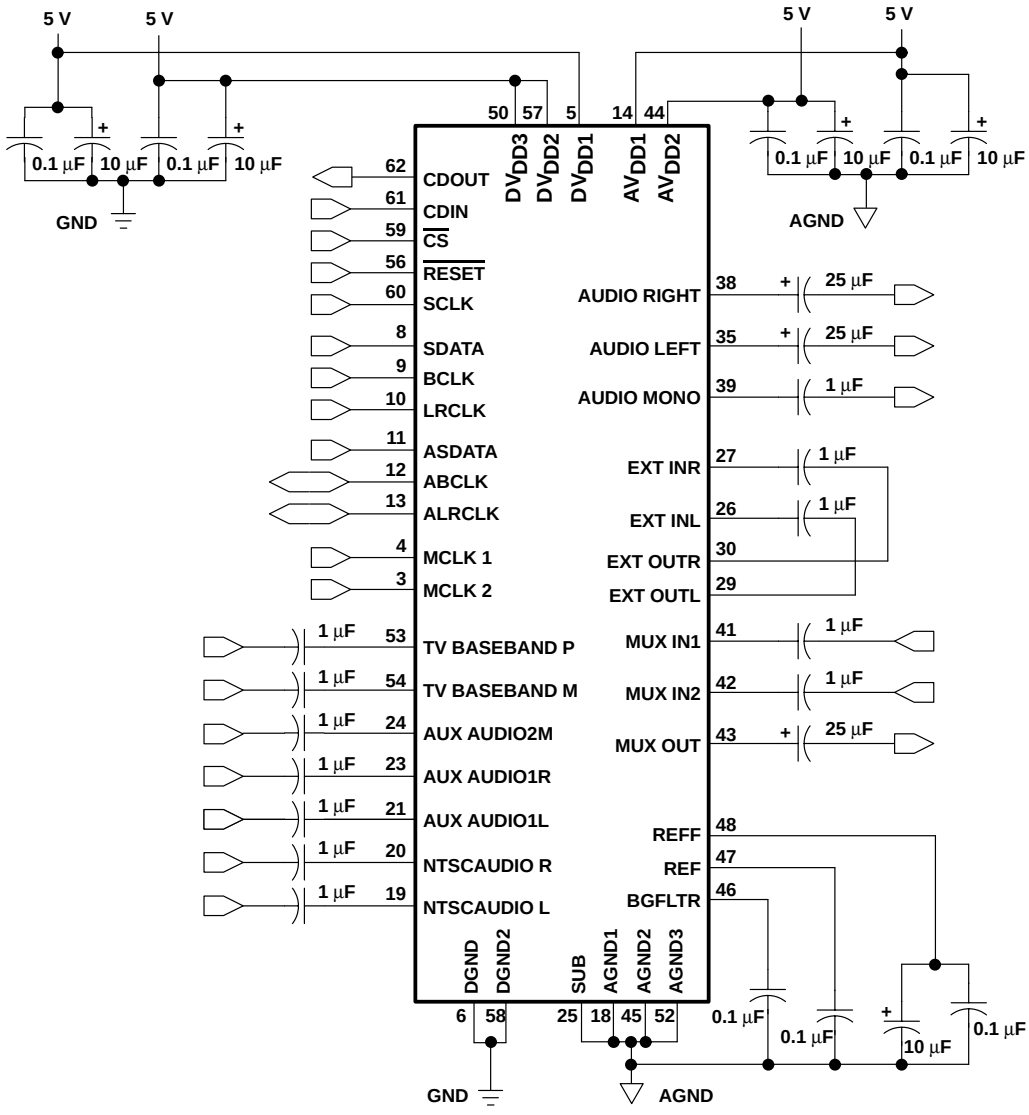
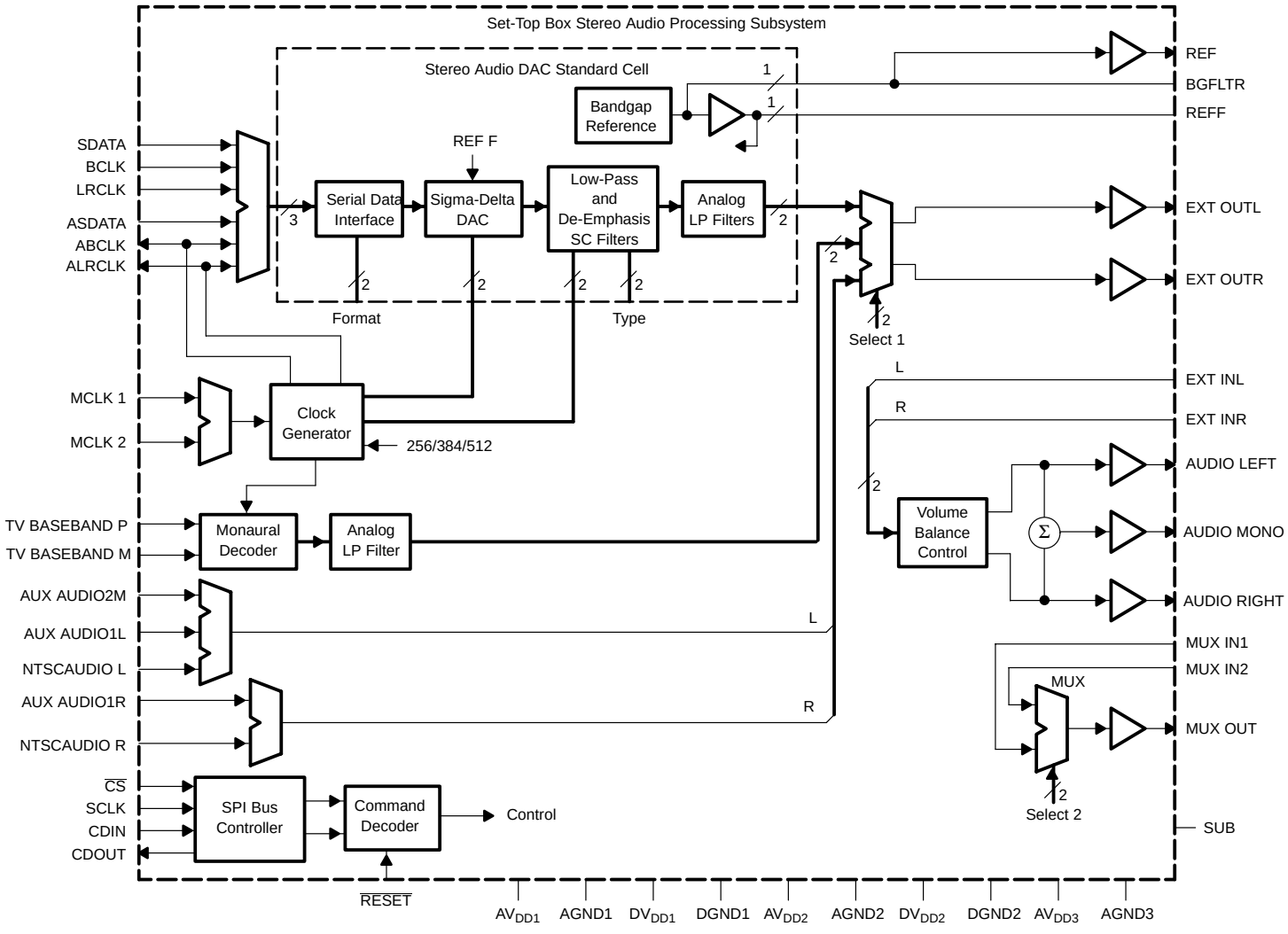


Figure 4–2. Application Schematic

NOTE: If the TLC320AD80 is to be used in applications where high voltage may be present, as with TV monitors or sets, it is recommended to add either external diodes (1N5347A) or transient suppressors (Motorola SA5. 0A) from any input and/or output terminals (that connect directly to external TV monitors or sets) to the circuit board ground.

4.1 Schematic



Appendix A
Register Set

Control of the TLC320AD80 is accomplished by means of the SPI serial interface and the control registers described in this section.

There are five control registers used to control the various functions of the device: volume control, multiplexer selections, serial interface, modes of operation, etc.

Table A–1. Serial PCM Data Format Control Register (Control Register 00h)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION	
0	0	–	–	–	–	–	–	Serial PCM data format	Philips I^2S protocol
0	1	–	–	–	–	–	–		Right justified
1	0	–	–	–	–	–	–		Left justified
1	1	–	–	–	–	–	–		Left justified DSP (inverted BCLK)
–	–	0	–	–	–	–	–	Serial PCM data precision	16 bits
–	–	1	–	–	–	–	–		18 bits
–	–	–	0	0	–	–	–	MCLK rate	256 x LRCLK (22.05 kHz ≤ LRCLK ≤ 48 kHz)
–	–	–	0	1	–	–	–		384 x LRCLK (22.05 kHz ≤ LRCLK ≤ 48 kHz)
–	–	–	1	0	–	–	–		512 x LRCLK (8 kHz ≤ LRCLK ≤ 16 kHz)
–	–	–	1	1	–	–	–	Reserved	
–	–	–	–	–	0	0	–	Bit clock (BCLK) rate	64 x LRCLK
–	–	–	–	–	0	1	–		48 x LRCLK (384x mode only)
–	–	–	–	–	1	0	–		32 x LRCLK (16-bit mode only)
–	–	–	–	–	1	1	–	Reserved	
–	–	–	–	–	–	–	x	Reserved	

The default value at reset is 00h.

Table A–2. Source Selection Control Register (Control Register 01h)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION	
0	0	0	0	–	–	–	–	Main audio input port select	NTSC AUDIO (stereo)
0	0	0	1	–	–	–	–		NTSC AUDIO (mono)
0	0	1	0	–	–	–	–		AUX AUDIO1 (stereo)
0	0	1	1	–	–	–	–		AUX AUDIO1 (mono)
0	1	0	0	–	–	–	–		Reserved
0	1	0	1	–	–	–	–		AUX AUDIO2 (mono)
0	1	1	0	–	–	–	–		Reserved
0	1	1	1	–	–	–	–		TV aural baseband multiplex (mono)
1	0	0	0	–	–	–	–		Main serial PCM data (slave mode)
1	0	0	1	–	–	–	–		Reserved
1	0	1	0	–	–	–	–		Aux serial PCM data (slave mode)
1	0	1	1	–	–	–	–		Aux serial PCM data (master mode) (see Note 1)
1	1	x	x	–	–	–	–		Reserved
–	–	–	–	0	–	–	–	Master clock input port select	MCLK 1
–	–	–	–	1	–	–	–		MCLK 2
–	–	–	–	–	0	–	–	Wideband mux input port select	MUX IN1
–	–	–	–	–	1	–	–		MUX IN2
–	–	–	–	–	–	0	–	Capacitor precharge mode	Disabled
–	–	–	–	–	–	1	–		Enabled
–	–	–	–	–	–	–	0	Audio input port mute	Enabled
–	–	–	–	–	–	–	1		Disabled

The default value at reset is 00h.

NOTE 1: All serial PCM data formats except DSP.

Table A–3. Control Register 02h

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION	
0	0	–	–	–	–	–	–	De-emphasis mode	50/15 µs (LRCLK = 48 kHz)
0	1	–	–	–	–	–	–		50/15 µs (LRCLK = 44.1 kHz)
1	0	–	–	–	–	–	–		50/15 µs (LRCLK = 32 kHz)
1	1	–	–	–	–	–	–		None
–	–	0	–	–	–	–	–	Wideband mux output mute	Enabled
–	–	1	–	–	–	–	–		Disabled
–	–	–	0	–	–	–	–	Volume/mute gating enabler	Zero crossing or time out
–	–	–	1	–	–	–	–		Zero crossing only
–	–	–	–	x	–	–	–	Reserved	
–	–	–	–	–	x	–	–	Reserved	
–	–	–	–	–	–	0	–	Reset	Normal mode
–	–	–	–	–	–	1	–		Clear DAC digital filter
–	–	–	–	–	–	–	0	Power down with ext out mute	Device enabled
–	–	–	–	–	–	–	1		Device powered down

The default value at reset is 00h.

Table A–4. Left Volume Control Register (Control Register 03h)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION	
0	–	–	–	–	–	–	–	Volume control mode	Ganged left/right control on left
1	–	–	–	–	–	–	–		Independent left/right control
–	0	0	0	0	0	0	0	Left volume control	–90 dB (mute)
–	0	0	0	0	0	0	1		–62 dB
–	0	0	0	0	0	1	0		–61 dB
–	0	1	1	1	1	1	0		–1 dB
–	0	1	1	1	1	1	1		0 dB
–	1	0	0	0	0	0	0		1 dB
–	1	0	0	0	1	0	1		6 dB
–	1	0	0	0	1	1	x	Reserved	
–	1	1	1	1	x	x	x	Reserved	

The default value at reset is 00h.

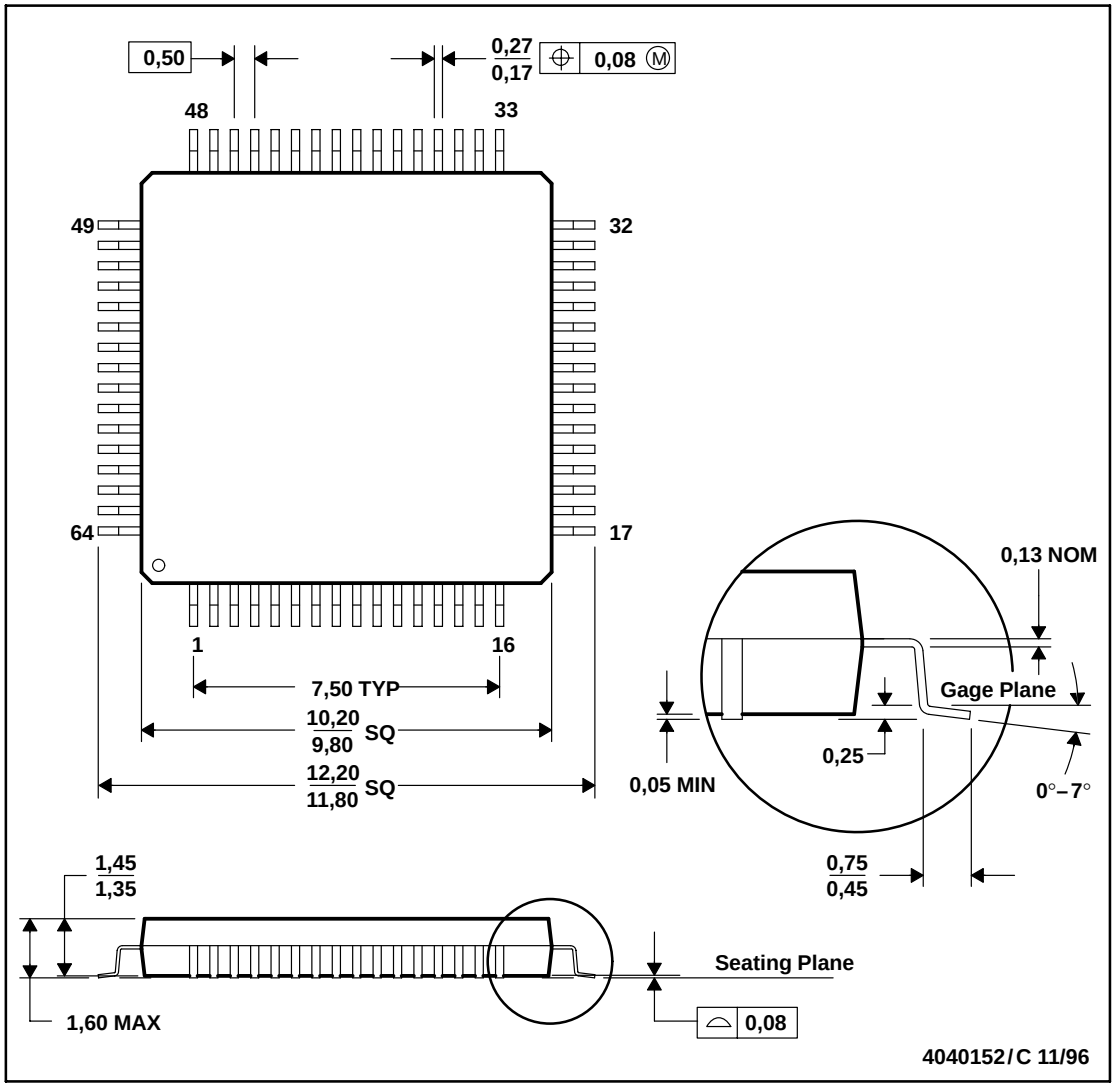
Table A–5. Right Volume Control Register (Control Register 04h)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION	
x	–	–	–	–	–	–	–	Reserved	
–	0	0	0	0	0	0	0	Right volume control	–90 dB (mute)
–	0	0	0	0	0	0	1		–62 dB
–	0	0	0	0	0	1	0		–61 dB
–	0	1	1	1	1	1	0		–1 dB
–	0	1	1	1	1	1	1		0 dB
–	1	0	0	0	0	0	0		1 dB
–	1	0	0	0	1	0	1		6 dB
–	1	0	0	0	1	1	x	Reserved	
–	1	1	1	1	x	x	x	Reserved	

The default value at reset is 00h.

Appendix B
Mechanical Data

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.